

World's Worst Video Card

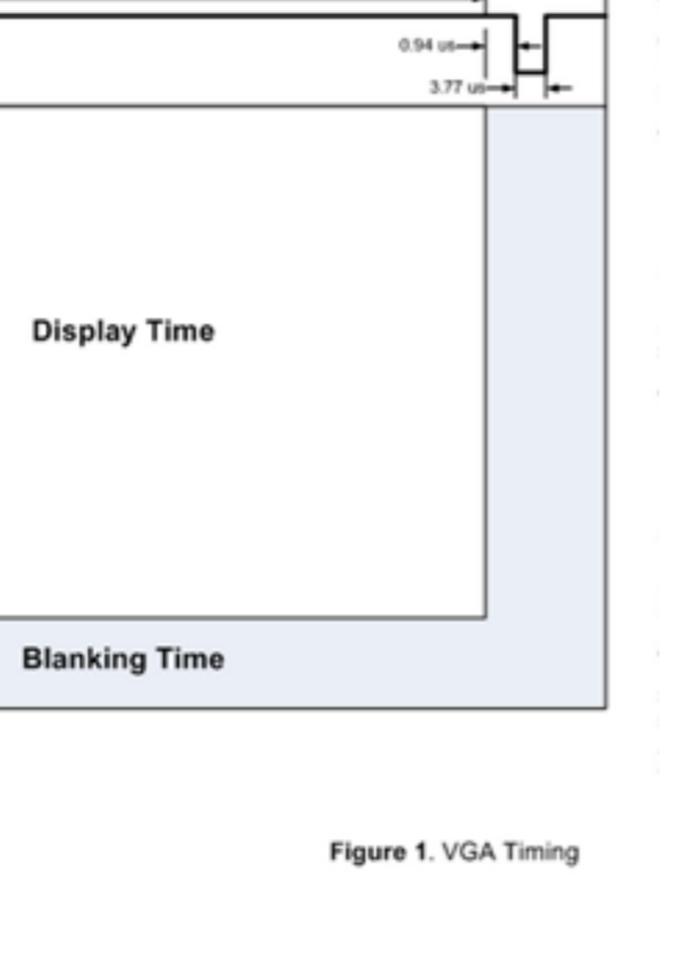
Simple facts:

- In the past monitors displayed information through a VGA interface

- It looks like this:



VGA cable



VGA Port

There are 15 pins in a standard VGA cable, and we are focusing on 5 specific signals: Red, Green, Blue (RGB), horizontal sync, and vertical sync.

There is a time, order of pixels in which they are printed on the screen. Including margins from top, bottom, left, and right giving an electron beam time before it paints the next scan line of pixels.

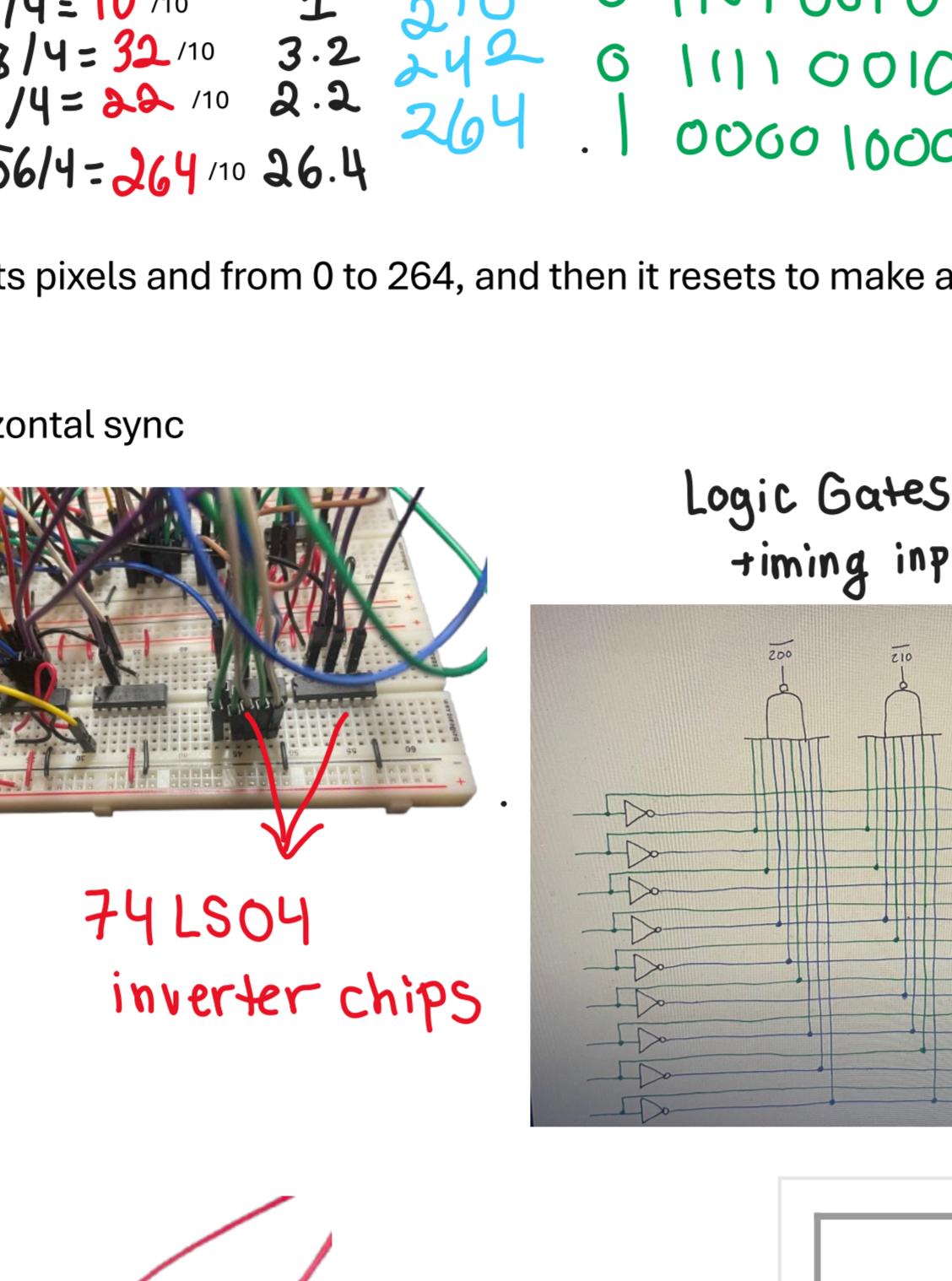


Figure 1: VGA Timing

These timings need to be correct in order to get the image that we want on the screen or monitor.

General Timing: Pixel Freq: 10 Mhz clock

- Screen Refresh Rate: 60 Hz

Vertical refresh: 37.87 kHz

	Pixels	Time [μs]
scanning part:	800/4 = 200	2.0
- visible area:	200	2.00
- Front porch:	40/4 = 10	1.0
- Sync pulse:	128/4 = 32	3.2
- Back porch:	88/4 = 22	2.2
- Whole line:	1056/4 = 264	26.4

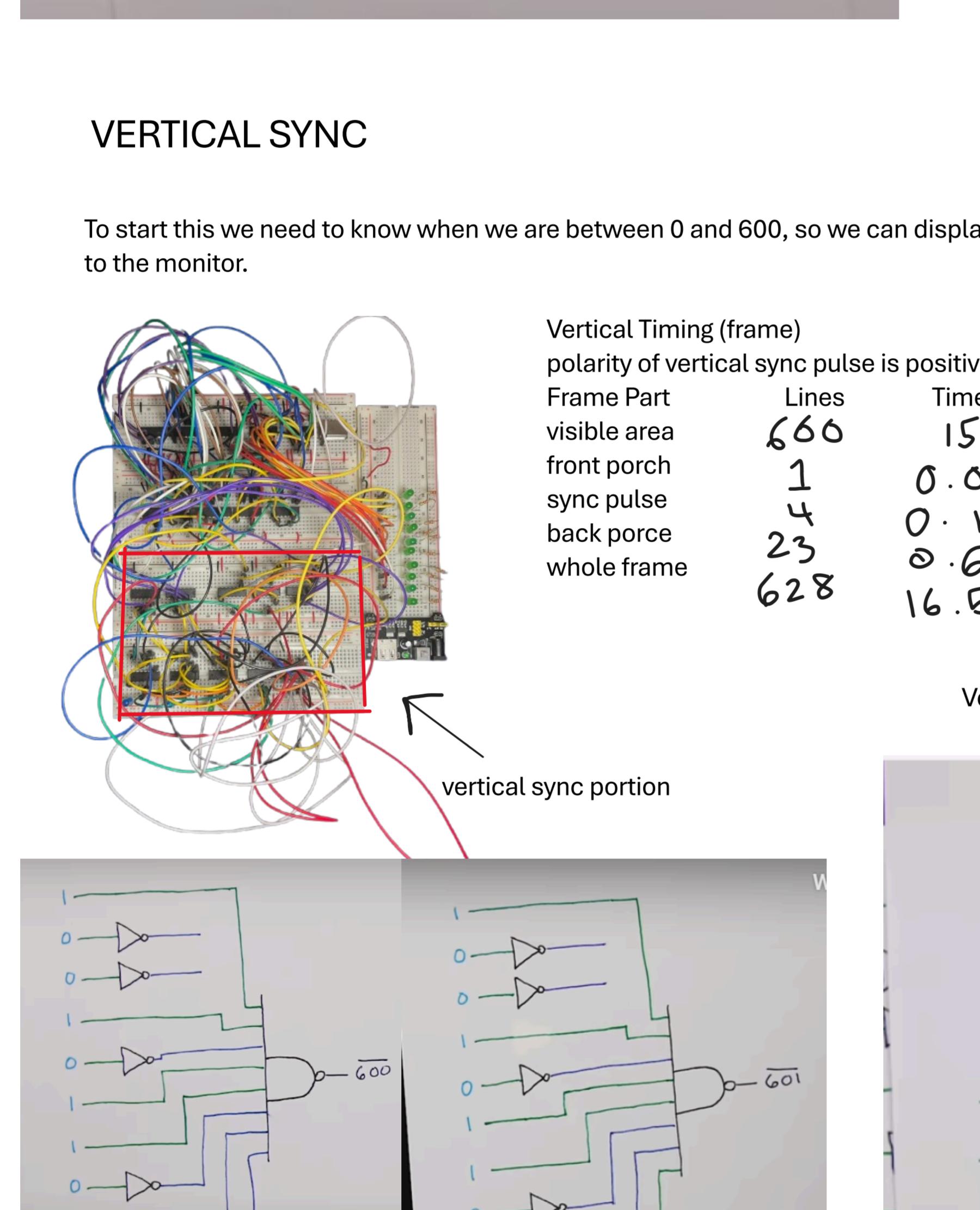
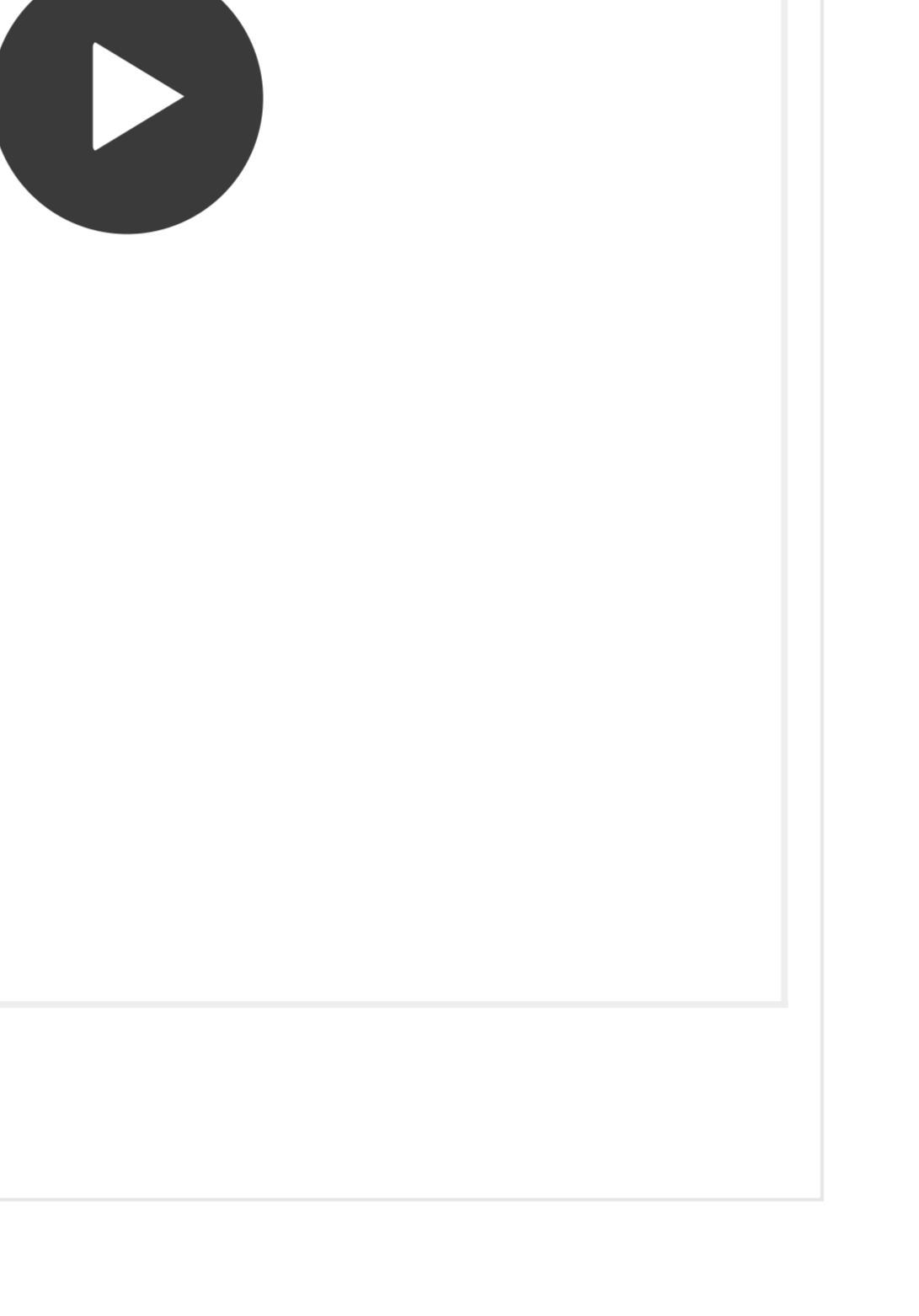
Build a circuit that counts pixels from 0 to 264, and then it resets to make a horizontal scanline.

close up view of the horizontal sync



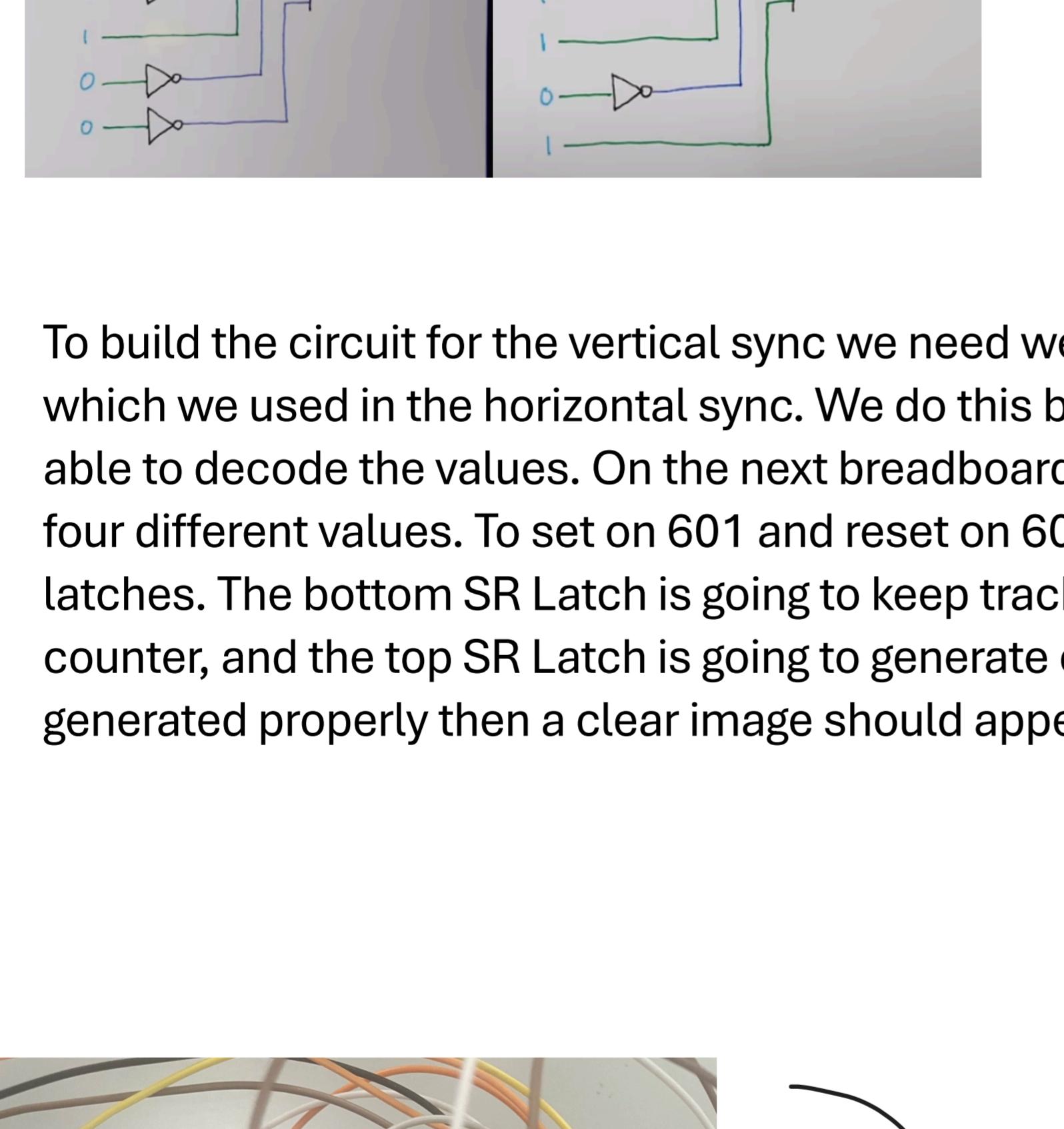
74LS04 inverter chips

Logic Gates and Horizontal timing inputs



IMG_2504
vimeo.com

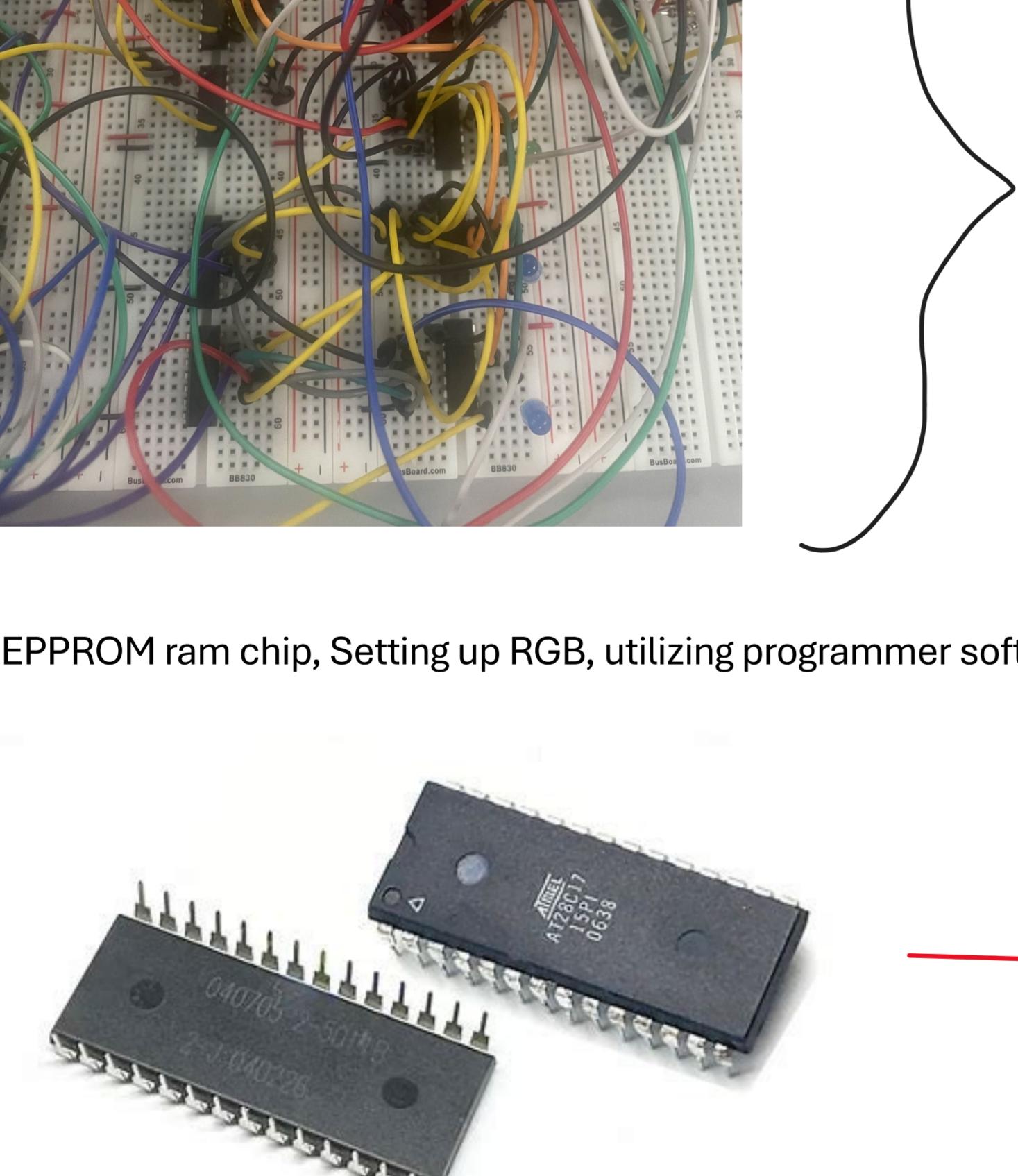
SR LATCH: Inverted SR-LATCH



We have a pulse to get to four points. At 0 on the horizontal line, we reset back to 0 every 264 and set the latch. At 200 we reset it; output Q is high during pixels and low during blanking. For HSYNC, at 210 we set the latch, at 242 we reset it; Q shows if HSYNC is active. For the SR Latch I used two NAND gates of 74LS00 chips which have 4 NAND gates on it.

VERTICAL SYNC

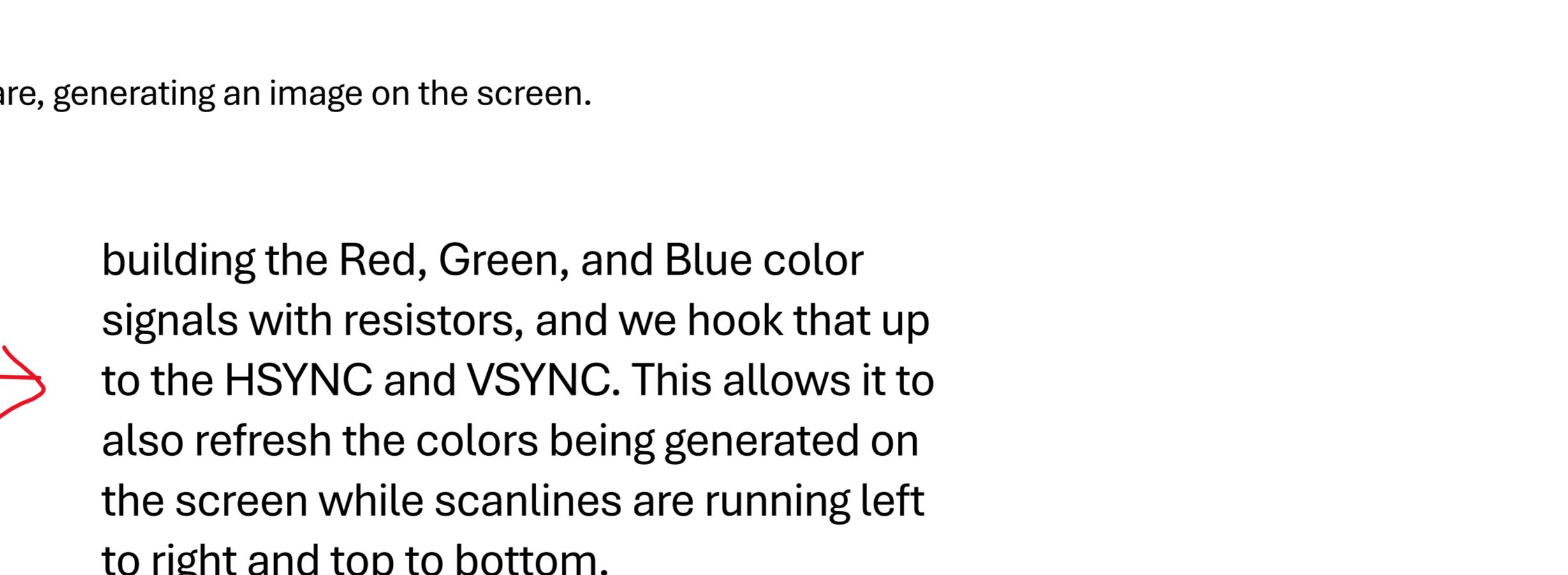
To start this we need to know when we are between 0 and 600, so we can display stuff. Also, we need to know when we are between 601 and 605 so we can output the vertical sync signal to the monitor.



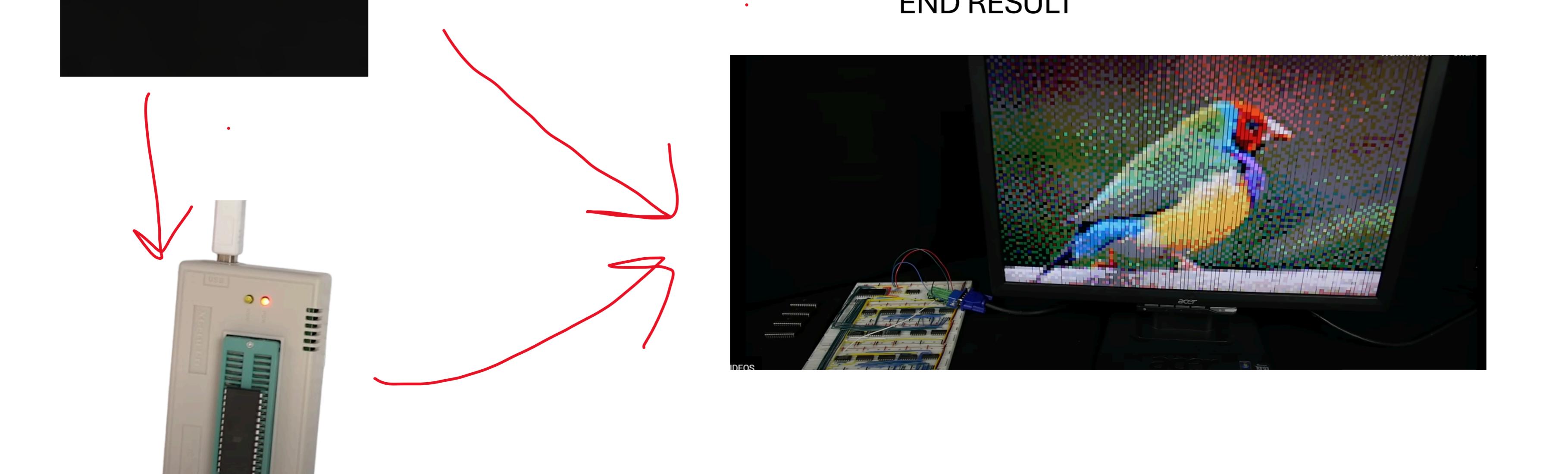
Vertical Timing (frame) polarity of vertical sync pulse is positive

Frame Part	Lines	Time [ms]	Value
visible area	600	15.84	0 10 0101 1000
front porch	1	0.024	000 10 0101 1001
sync pulse	4	0.1056	001 10 0101 1101
back porch	23	0.6072	005 10 0101 0100
whole frame	628	16.6792	028 10 0111 0100

Vertical Sync Input and Output Logic Diagram



To build the circuit for the vertical sync we need to count to 628 with 10 bits instead of 9 bits, which we used in the horizontal sync. We do this by using 3 74LS160 chips (12 bits) and inverters to be able to decode the values. On the next breadboard we can add the four NAND gates used to decode the four different values. To set on 601 and reset on 605 we will add a quad NAND gate and build our two SR latches. The bottom SR Latch is going to keep track of when we are displaying our image and resets the counter, and the top SR Latch is going to generate our vertical sync pulse. If all of these timings are generated properly then a clear image should appear on the screen.



EPPROM ram chip, Setting up RGB, utilizing programmer software, generating an image on the screen.



building the Red, Green, and Blue color signals with resistors, and we hook that up to the HSYNC and VSYNC. This allows it to also refresh the colors being generated on the screen while scanlines are running left to right and top to bottom.

Programmer Software



END RESULT

