

EEE 133 Key concepts and Equations

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1 Diode Models and Circuits

1.1 History of Electronics

1. 1904: John Fleming invented vacuum tubes. First time electron flow is controlled in non-conducting medium
 - (a) if the cathode is heated, some electrons can escape
 - (b) if a voltage is applied (+) on anode (–) on cathode, there will be current
2. 1906: the grid was added to control the current between the anode and cathode
 - (a) vacuum tubes allowed the development of amplifiers, transmitters, receivers, signal processor
3. 1946: the ENIAC computer was completed. it could execute 5000 additions per second
4. 1947: invention of transistor by Shockley, Bardeen, Brattain at the Bell Labs
 - (a) they were point-contact transistors
5. 1948: Schockley invented the BJT. the BJT is monolithic (containted in a single semiconductor crystal)
6. 1958: the first Integrated Circuits (IC) was invented by Jack Kilby of Texas Instruments (non-monolithic)
7. 1959: the first monolithic IC was developed by Robert Noyce at Fairchild Semiconduction
 - (a) uses silicon instead of germanium
 - (b) 2 interconnected BJT transistor
 - (c) SiO_2 insulator, Al interconnection
 - (d) planar IC, 0.06 in diameter
8. Bipolar ICs with BJT devices domidated until early 80s
 - (a) S/M/L Scale Integration : 10, 100, 1000 transistors
9. 1959: MOS ICs started in the 60s after the MOS transistor was developoed at Bell Labs
 - (a) easier to fabricate than bipolar
 - (b) uses less power
 - (c) can fit more transistor in the same silicon area
 - (d) slower than bipolar IC
 - (e) less robust than bipolar IC

10. MOS ICs

- (a) early 70s: MOS technology improved in speed and reliability
- (b) first microprocessor: Intel 4004 (1971)
- (c) emergence of VLSI (>10000 transistors)
- (d) microprocessors evolved into microcontrollers (MCUs) and system on a chip (SOCs)

11. Moore's Law: the transistor density would double every two years

1.2 Piecewise Linear Diode Models

1. 1st Approximation: (when $v_s \gg V_T$)

- (a) Open when $v_D < 0$
- (b) Short when $v_D \geq 0$

2. 2nd Approximation (when above condition not satisfied):

- (a) Open when $v_D < V_T$
- (b) Voltage of V_T when $v_D \geq V_T$

3. 3rd Approximation (2nd with resistor R in series)

- (a) Open when $v_D < V_T$
- (b) Voltage of V_T in series with resistance R when $v_D \geq V_T$

4. To determine diode state:

- (a) Assume it is conducting
- (b) Check direction of current
- (c) If current is from anode to cathode, the assumption is correct and equivalent circuit is valid
- (d) Otherwise, diode should be open

5. Another method:

- (a) Replace diode with open circuit
- (b) Determine the voltage across the diode terminals (+) on anode, (−) on cathode
- (c) If $v_D < \text{the needed threshold}$, assumption is correct
- (d) Otherwise, diode should be replaced with the appropriate model

1.3 Practical Diode Circuits

1. Half Wave Rectifier

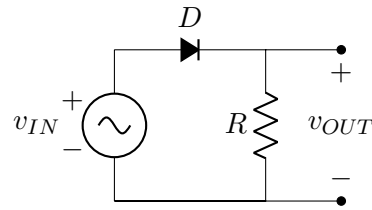


Figure 1: Half Wave Rectifier

(a) When diode is IDEAL:

$$v_{OUT} = \begin{cases} 0, & v_{IN} < 0 \\ v_{IN} & v_{IN} \geq 0 \end{cases}$$

(b) When diode has constant voltage model:

$$v_{OUT} = \begin{cases} 0, & v_{IN} < V_T \\ v_{IN} - V_T & v_{IN} \geq V_T \end{cases}$$

2. Full Wave Rectifier ($v_1 = v_2$)

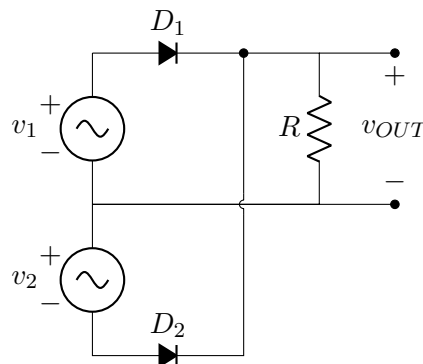


Figure 2: Full Wave Rectifier

(a) When diode is IDEAL:

$$v_{OUT} = |v_{IN}|$$

(b) When diode has constant voltage model:

$$v_{OUT} = \begin{cases} v_1 - V_T, & v_1 > V_T \\ -v_2 - V_T, & v_2 < -V_T \\ 0 & \text{otherwise} \end{cases}$$

(c) This requires a transformer with center-tapped secondary ($n_1 : n_2 = 1 : 2$)

3. Full Wave Bridge Rectifier

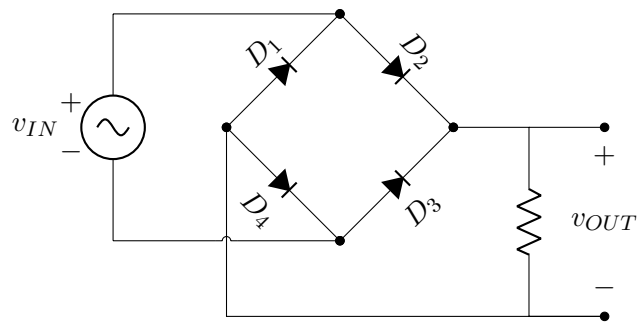


Figure 3: Full Wave Bridge Rectifier

(a) When diode is IDEAL:

$$v_{OUT} = |v_{IN}|$$

(b) When diode has constant voltage model:

$$v_{OUT} = \begin{cases} v_1 - 2V_T, & v_1 > 2V_T \\ -v_2 - 2V_T, & v_2 < -2V_T \\ 0 & \text{otherwise} \end{cases}$$

4. Positive Clipper

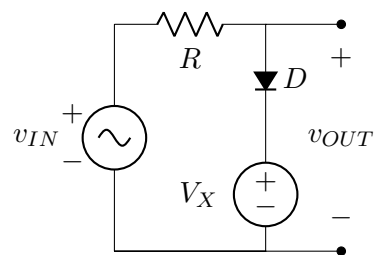


Figure 4: Positive Clipper

$$(a) v_{OUT} = \begin{cases} V_X + V_T, & v_{IN} - V_X > V_T \\ v_{IN}, & v_{IN} - V_X < V_T \end{cases}$$

5. Negative Clipper

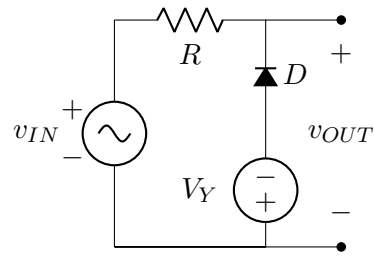


Figure 5: Negative Clipper

$$(a) v_{OUT} = \begin{cases} -(V_Y + V_T), & -V_Y - v_{IN} > V_T \\ v_{IN}, & -V_Y - v_{IN} < V_T \end{cases}$$

6. The positive and negative clippers can be combined

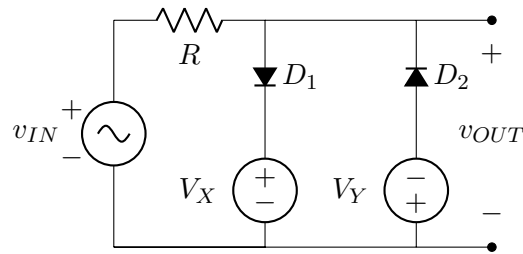


Figure 6: Positive and Negative Clipper

$$(a) v_{OUT} = \begin{cases} V_X + V_T, & v_{IN} - V_X > V_T \\ -(V_Y + V_T), & -V_Y - v_{IN} > V_T \\ v_{IN}, & \text{otherwise} \end{cases}$$

7. Peak Detector

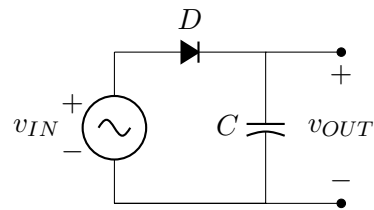


Figure 7: Peak Detector

(a) Let the time t_1 be the first time the input reaches its maximum value V_P and t_0 be the time to reach V_T

(b) When diode is IDEAL:

$$v_{OUT} = \begin{cases} v_{IN}, & t < t_1 \\ V_P, & t \geq t_1 \end{cases}$$

(c) When diode has constant voltage model:

$$v_{OUT} = \begin{cases} 0, & 0 \leq t < t_0 \\ v_{IN} - V_T, & t_0 \leq t < t_1 \\ V_P - V_T & t_1 \leq t \end{cases}$$

8. Peak Detector with Load Resistor (Ideal Diode)

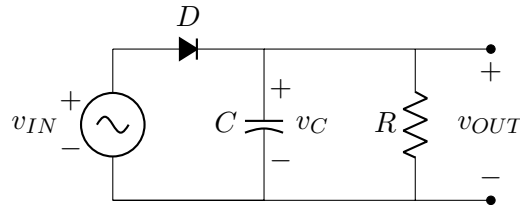


Figure 8: Peak Detector with load resistor

(a) Let the time t_1 be the first time the input reaches its maximum value V_P and the period be T . When the capacitor voltage decays, let time t_2 be when $v_C = v_{IN}$ again

$$(b) v_{OUT} = \begin{cases} v_{IN}, & t < t_1 \\ V_P \exp\left(-\frac{t - t_1}{RC}\right), & t_1 \leq t < t_2 \\ v_{IN}, & t_2 \leq t < t_1 + T \\ V_P \exp\left(-\frac{t - (t_1 + T)}{RC}\right), & t_1 + T \leq t < t_2 + T \\ \vdots & \end{cases}$$

9. Negative Clamper (ideal diode)

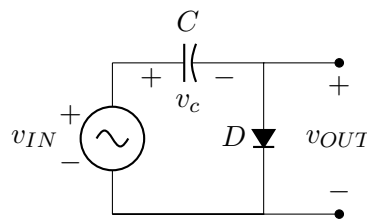


Figure 9: Negative Clamper

(a) Let the time t_1 be the first time the input reaches its maximum value V_P

(b) This is similar to the peak detector, only that $v_{OUT} = v_{IN} - v_C$ where v_C follows the characteristic of the peak detector

$$(c) v_C = \begin{cases} v_{IN}, & t < t_1 \\ V_P, & t_1 \leq t \end{cases}$$

$$(d) v_{OUT} = \begin{cases} 0, & t < t_1 \\ v_{IN} - V_P, & t \geq t_1 \end{cases}$$

10. Positive Clamper (ideal diode)

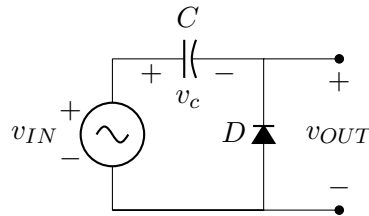


Figure 10: Positive Clamper

(a) Let the period be T

$$(b) v_C = \begin{cases} 0, & 0 \leq t < T/2 \\ v_{IN}, & T/2 \leq t < 3T/4 \\ -V_P, & 3T/4 \leq t \end{cases}$$

$$(c) v_{OUT} = \begin{cases} v_{IN}, & 0 \leq t < T/2 \\ 0, & T/2 \leq t < 3T/4 \\ v_{IN} + V_P, & 3T/4 \leq t \end{cases}$$

1.4 Exponential Diode Model

1. Shockley's Diode Equation

$$i_D = I_S \left[\exp \left(\frac{v_D}{\eta V_T} \right) - 1 \right] \quad (1)$$

(a) v_D : diode voltage with positive at anode

(b) i_D : diode current from anode to cathode

(c) I_S : reverse saturation current due to minority carriers. $10^{-15} \text{A} < I_S < 10^{-9} \text{A}$

(d) η : ideality factor, $1 < \eta < 2$; close to 1 for well fabricated diodes

(e) V_T : thermal voltage, $V_T = \frac{kT_K}{e} \approx \frac{T_K}{11600}$

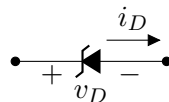
2. for typical operating voltages (forward biased): $\exp \left(\frac{v_D}{\eta V_T} \right) \gg 1 \Rightarrow i_D \approx I_S \exp \left(\frac{v_D}{\eta V_T} \right)$

3. for typical reverse bias voltages, $\exp \left(\frac{v_D}{\eta V_T} \right) \ll 1 \Rightarrow i_D \approx -I_S$

1.5 Small Signal Model

1. $v_D = V_D + v_d$
2. $i_D = I_D + i_d$. I_D is calculated using large signal analysis
3. if the amplitude of v_d is very small, the diode characteristic equation is approximately a line with conductance $g_d = \frac{\partial i_D}{\partial v_D} = \frac{I_S}{\eta V_T} \exp\left(\frac{v_D}{\eta V_T}\right) \approx \frac{I_D}{\eta V_T} \implies r_d = \frac{\eta V_T}{I_D}$

1.6 Zener Diode



1. has 3 modes of operations:

Operation	Condition	Equivalent
Forward-biased	$v_D \leq V_T$	$v_D = -V_T$
Non-conducting	$-V_T < v_D < V_Z$	open circuit
Zener region	$v_D \geq V_Z$	$v_D = V_Z$

2 PN Junction and BJT Operation

2.1 Semiconductor Fundamentals

1. The Silicon (14) Atom:
 - (a) has 4 valence electrons
 - (b) the semiconductor lattice has bounded valence electrons at 0K
 - (c) energy bands: electrons can occupy discrete energy levels
 - (d) there is a **band gap** between the valence band and conduction band
 - (e) at higher temperatures, an electron can gain enough energy to break the bonds
 - (f) when an electron leaves a bond, it leaves a positively charged **hole**
2. Groups by electrical properties:
 - (a) insulators: huge band gap
 - (b) conductor: conduction band and valence overlap
 - (c) semiconductor: small band gap that can be easily reached
3. Semiconductors:
 - (a) narrow band gap
 - (b) has 2 groups:
 - i. intrinsic: just enough valence electrons to complete the matrix. either has group IV semiconductors (Si and Ge) or III-V compound (GaAs)
 - ii. extrinsic: produced by doping intrinsic semiconductors
 - A. N-type: dopants have excess electrons. energy level just below the conduction band
 - B. P-type: dopants have less electrons. energy level just above the valence
4. Fermi level: hypothetical energy level where there is 50% probability that the level is occupied by an electron at any given time
 - (a) intrinsic semiconductor: midway between E_C and E_V
 - (b) extrinsic semiconductor:
 - i. N-type: closer to E_C
 - ii. P-type: closer to E_V

2.2 Carrier Actions in Semiconductors

1. Charge Carriers: the electrons and holes. units in coulombs (C)
2. Intrinsic semiconductor: $n = p$ equal concentration of electrons and holes
3. N-type semiconductors:
 - (a) $n > p$
 - (b) majority charge carriers: electrons
 - (c) minority charge carriers: holes
4. P-type semiconductors:
 - (a) $p > n$

- (b) majority charge carriers: holes
- (c) minority charge carriers: electrons
- 5. Current: rate of movement of charge past a point or region. units in ampere (A). + is the direction of the hole/opposite the electron
- 6. Mobility: ability of charge carrier to move. $\mu_e > \mu_h$
- 7. Factors that affect mobility:
 - (a) Scattering - the random motion of charges. One mechanism is the *lattice scattering* when electrons bump with the vibrating lattice or other electrons and change directions
 - (b) another scattering mechanism is *impurity scattering* when dopant ions deflect charge carriers
 - (c) Temperature vs Scattering vs Mobility. At low temperatures, impurity scattering dominates (and with low mobility). at high temperatures, lattice scattering dominates (and low mobility). there is a temperature in the middle with maximum mobility. (like a parabolic log-log graph)
 - (d) Doping vs Scattering vs Mobility. more doping = more impurity scattering
 - (e) scattering has a net current of 0
- 8. There are 3 primary carrier actions:
 - (a) Generation and Recombination: generation = electron gains enough energy to break a covalent bond and leaves a hole. recombination = moving electron moves close to a hole and experience attractive force
 - (b) Diffusion: electrons move from higher concentration/temperature to lower concentration/temperature. + diffusion is parallel to positive charges. becomes 0 when there is uniform distribution of charge carriers
 - (c) Drift: caused by applied external voltage. modeled by a constant drift velocity $v_d = \mu E$ (directly related to the electric field with the mobility as constant)
 - i. $I_n = -Aqnv_{n\text{-drift}}$
 - ii. $I_p = Aqp v_{p\text{-drift}}$

2.2.1 PN Junction

- 1. PN Junction: formed when in a single silicon crystal, one region is doped with donor dopants (N-type) and the other with acceptor dopants (P-type). PN Junction is the boundary.
- 2. Depletion Region: happens at the boundary when the electrons diffuse and recombine with the holes at the P-type region. This results to a potential difference (and thus an electric field) across the depletion region (points from N to P)
 - (a) drift current of minority carriers are drifted by this electric field
- 3. There are 3 junction operations:
 - (a) Open-circuit (equilibrium condition):
 - i. the diffusion current I_D is limited by the built in voltage V_0 and equal to the drift current I_S
 - (b) Forward Bias (+ on the P-type)
 - i. the + potential pushes the holes in the P-type and the depletion region in the P-side decreases
 - ii. the - potential pushes the electrons in the N-type and the depletion region in this side also decreases
 - iii. the diffusion current I_D dominates, but the temperature dependent I_S remain the same

- iv. the net current $I = I_D - I_S$ in the direction from P to N
- v. when $V_F \geq V_o$, the depletion region disappears and $I \approx I_D$
- (c) Reverse Bias (+ on the N-type)
 - i. the + potential attracts the electrons in the N-type, the depletion region becomes larger
 - ii. the - potential attracts the holes in the P-type, the depletion region becomes larger
 - iii. the voltage V_o increases so I_D decreases
 - iv. net current $I = I_D - I_S$ from N to P
 - v. if I_D becomes very small, $I \approx -I_S$
- 4. The energy band diagram will align the Fermi levels, thus bending the E_C and E_V with the maximum deviation V_0
 - (a) at forward bias, V_0 decreases so the bending energy will also decrease and the Fermi level will not be aligned anymore (E_{FN} is higher)
 - (b) at reverse bias, V_0 increases so the bending energy will also increase and the Fermi level will not be aligned anymore (E_{FN} is lower)
- 5. The PN Junction implements a Diode. anode at P, cathode at N
 - (a) the Shockley Equation summarizes the 3 conditions for the PN Junction operations
 - (b) Diode resistivity:
 - i. at higher temperature, more electrons are freed and resistivity decreases
 - ii. higher doping density lowers the resistivity

3 BJTs as Amplifiers

3.1 DC Characteristics and Operating Modes

Mode of Operation	EB Junction	CB Junction
Cut-off	Reverse-biased	Reverse-biased
Active	Forward-biased	Reverse-biased
Saturation	Forward-biased	Forward-biased
Reverse Active	Forward-biased	Reverse-biased

1. Cutoff Mode Relationships:

$$(a) I_B = I_C = I_E = 0$$

2. Active Mode Relationships:

$$(a) I_B = \frac{I_S}{\beta} \left[\exp \left(\frac{eV_{BE}}{kT} \right) - 1 \right] \left[1 + \frac{V_{CE}}{V_A} \right]$$

$$(b) I_C = \beta I_B = I_S \left[\exp \left(\frac{eV_{BE}}{kT} \right) - 1 \right] \left[1 + \frac{V_{CE}}{V_A} \right]$$

$$(c) I_E = \frac{1}{\alpha} I_C = (\beta + 1) I_B$$

$$(d) \alpha = \frac{\beta}{\beta + 1} \iff \beta = \frac{\alpha}{1 - \alpha}$$

(e) In most cases, $V_A \gg V_{CE}$ so the factor is approximately 1

(f) Model:

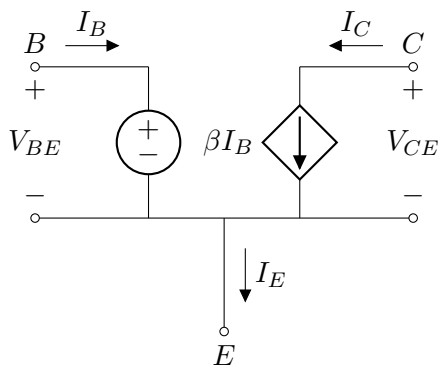


Figure 11: NPN Transistor Active Mode

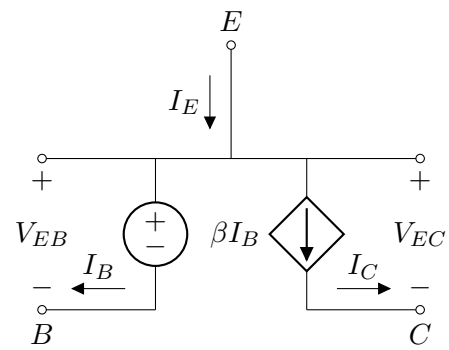


Figure 12: PNP Transistor Active Mode

3. Saturation Mode Relationships

$$(a) I_{C, sat} = \beta_{forced} I_B$$

$$(b) V_{BE} = 0.7 \text{ V}, V_{EB} = 0.7 \text{ V}$$

$$(c) V_{CE} = 0.3 \text{ V}, V_{EC} = 0.3 \text{ V edge of saturation}$$

$$(d) \text{ deep saturation is normally } 0.2 \text{ V}$$

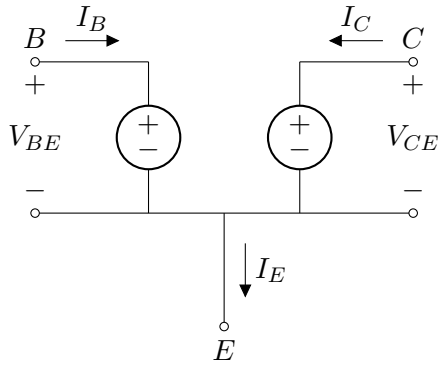


Figure 13: NPN Transistor Saturation Mode

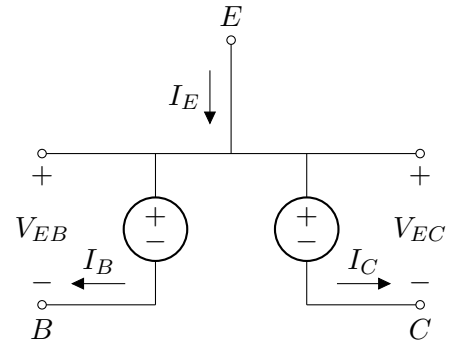


Figure 14: PNP Transistor Saturation

3.2 BJT Biasing Circuits

1. Q point: fixed characteristics of the transistor
 - (a) active region for amplifier
 - (b) cut-off/saturation for switches
2. Biasing: application of DC voltages to establish the operating point
3. Transistor Parameter variations on Temperature:
 - (a) leakage current: $I_{C0}(25^{\circ}C) = 1 \text{ nA}$. doubles every 6° rise
 - (b) $V_{BE}(25^{\circ}C) = 0.7 \text{ V}$. drops about $2.2 \text{ mV}/^{\circ}C$
 - (c) β doubles with an increase of $80^{\circ}C$

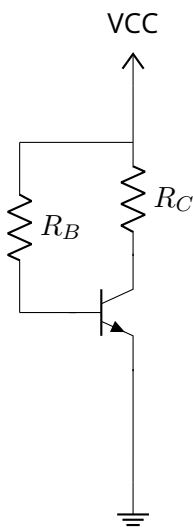


Figure 15: Fixed Bias Circuit

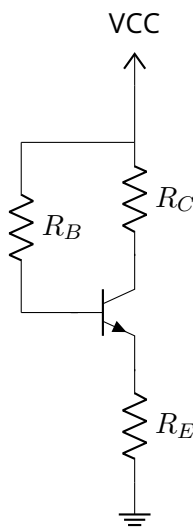


Figure 16: Emitter Stabilized

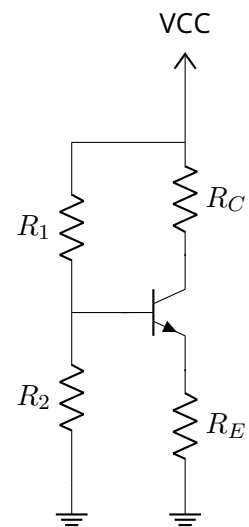


Figure 17: Voltage Divier Bias

3.3 BJT Amplifiers

1. General steps in circuit analysis:

- (a) In the DC part, treat the capacitors as open
- (b) The DC analysis calculates the Q point values
- (c) In the AC part, treat the capacitors and DC voltage sources as shorts

2. Common Emitter Amplifier:

- (a) Inverting amplifier with very huge gains

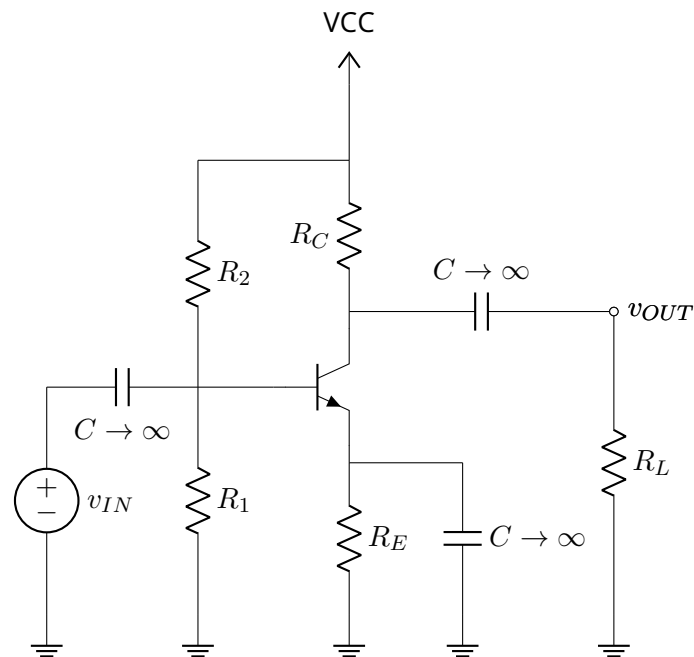
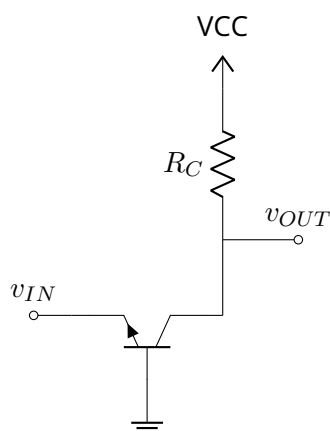


Figure 18: CE Amplifier

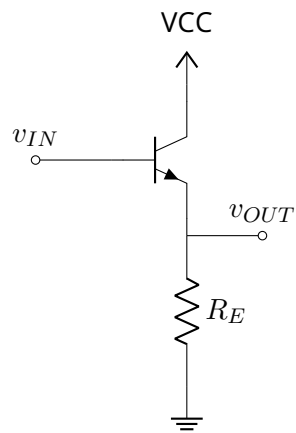
3. Common Base Amplifier:

- (a) has a sudden rise of gain in the vicinity of the V_{BE} threshold



4. Common Collector Amplifier:

- (a) has unity gain
- (b) is a voltage follower



4 MOSFETs as Amplifiers

4.1 MOSFET Fundamentals

1. FET: an electric field is applied normal to the surface (gate) of a semiconductor that modulates the conductance of the semiconductor
 - (a) NMOS: uses electrons as charge carriers
 - (b) PMOS: uses holes as charge carriers
2. The source and drain terminals are heavily doped (n for NMOS, p for PMOS)
 - (a) Enhancement Mode: default off
 - (b) Depletion Mode: default on
3. Threshold voltage: minimum V_{GS} for the MOSFET to conduct
4. Saturation Voltage: minimum V_{DS} that causes the channel of the transistor to pinch-off in the drain side due to widening depletion region in the drain bulk junction
5. MOSFET Regions of Operation:

Region of Operation	Conditions (NMOS)	Current I_D
Cut-off	$V_{GS} < V_{Th, n}$	$I_D = 0$
Linear	$V_{GS} \geq V_{Th, n}$ $V_{DS} < V_{GS} - V_{Th, n}$	$I_D = k_n \left(V_{GS} - V_{Th, n} - \frac{V_{DS}}{2} \right) V_{DS}$
Saturation	$V_{GS} \geq V_{Th, n}$ $V_{DS} \geq V_{GS} - V_{Th, n}$	$I_D = \frac{1}{2} k_n (V_{GS} - V_{Th, n})^2$
Region of Operation	Conditions (PMOS)	Current I_D
Cut-off	$V_{GS} < V_{Th, n}$	$I_D = 0$
Linear	$V_{SG} \geq V_{Th, p} $ $V_{SD} < V_{SG} - V_{Th, p}$	$I_D = -k_p \left(V_{SG} - V_{Th, p} - \frac{V_{SD}}{2} \right) V_{SD}$
Saturation	$V_{SG} \geq V_{Th, p}$ $V_{SD} \geq V_{SG} - V_{Th, p}$	$I_D = -\frac{1}{2} k_p (V_{SG} - V_{Th, p})^2$

4.2 MOSFET DC Characterization

1. Steps in solving MOSFET circuits:
 - (a) Identify the terminals
 - (b) Solve for voltage terminals
 - (c) Use the current equation to get I_D . assume saturation if region of operation is unknown

4.3 MOSFET Amplifier

1. Common Source Amplifier:

- (a) inverting amplifier
- (b) can have large gains

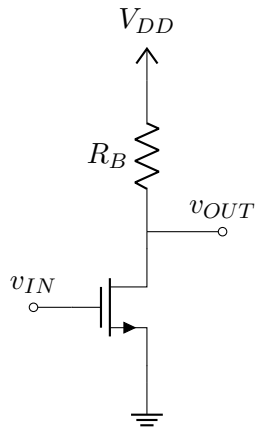


Figure 19: NMOS CS Amplifier

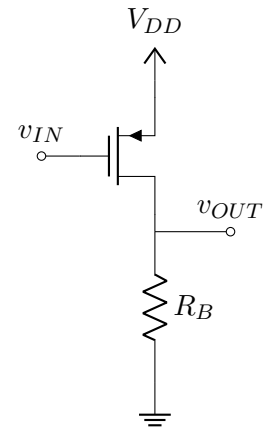


Figure 20: PMOS CS Amplifier

2. Common Drain Amplifier:

- (a) has a unity gain
- (b) non-inverting amplifier

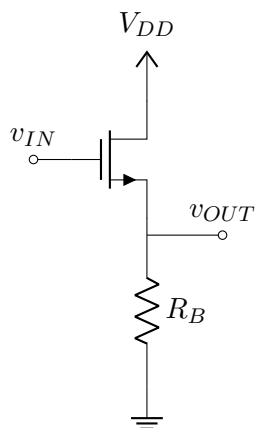


Figure 21: NMOS CD Amplifier

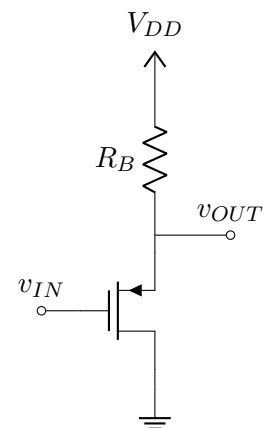


Figure 22: PMOS CD Amplifier

3. Common Gate Amplifier:

- (a) non-inverting amplifier
- (b) can have gain more than 1

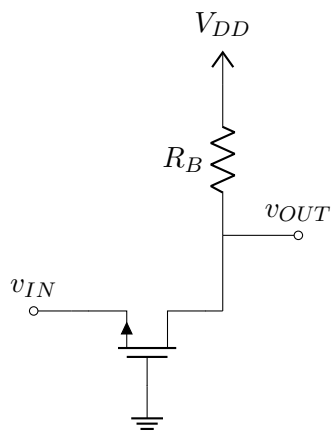


Figure 23: NMOS CG Amplifier

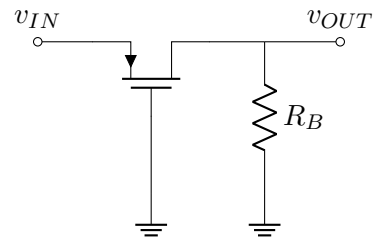


Figure 24: PMOS CG Amplifier

5 Small Signal Analysis of Transistor Amplifiers

5.1 Two Port Networks

1. one port serves as input, the other as output
2. Z parameters: impedance parameters. taken for open circuit of both ports

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{1,1} & Z_{1,2} \\ Z_{2,1} & Z_{2,2} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

3. Y parameters: admittance parameters. taken for short circuit of both ports

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{1,1} & Y_{1,2} \\ Y_{2,1} & Y_{2,2} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

4. h parameters: hybrid parameters. first column is short circuit of Port 2, second column is open circuit for Port 1

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{1,1} & h_{1,2} \\ h_{2,1} & h_{2,2} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

5. g parameters: inverse hybrid parameters. first column is open circuit of Port 2, second column is short circuit for Port 1

$$\begin{bmatrix} I_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} g_{1,1} & g_{1,2} \\ g_{2,1} & g_{2,2} \end{bmatrix} \begin{bmatrix} V_1 \\ I_2 \end{bmatrix}$$

6. Unilateral Hybrid π Network: only has 3 parameters

(a) R_i , R_o , A_v for Thevenin Equivalent

(b) R_i , R_o , G_m for Norton Equivalent

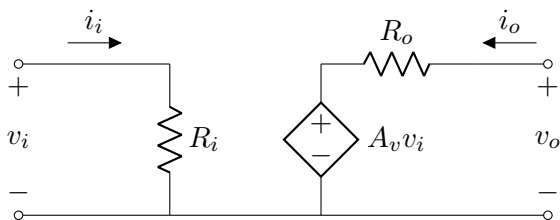


Figure 25: Thevenin Equivalent

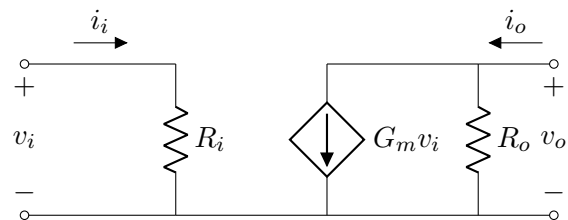


Figure 26: Norton Equivalent

Figure 27: Unilateral Hybrid π Network

5.2 Small Signal Model

Parameter	BJT	MOSFET
g_m Transconductance	$g_m = \frac{I_C}{V_T}$	$g_m = \frac{2I_D}{V_{GS} - V_{Th,n}} = \sqrt{2K_n I_D (1 + \lambda V_{DS})} \approx \sqrt{2K_n I_D}$
r_π Input Resistance	$r_\pi = \frac{\beta}{g_m} = \frac{\beta V_T}{I_C}$	$r_\pi = \infty$
r_o Output Resistance	$r_o = \frac{V_A + V_{CE}}{I_C} \approx \frac{V_A}{I_C}$	$\frac{1}{I_D} \left(\frac{1}{\lambda} + V_{DS} \right) \approx \frac{1}{\lambda I_D}$

1. the approximations above are from:

(a) $V_A \gg V_{CE}$

(b) $\lambda \ll \frac{1}{V_{DS}}$

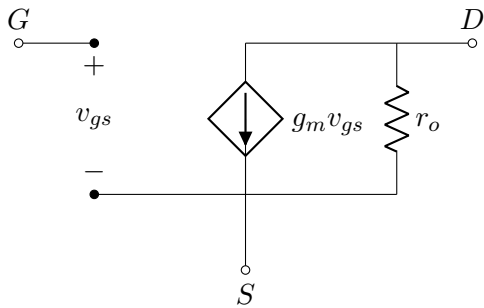


Figure 28: MOSFET Small Signal Model

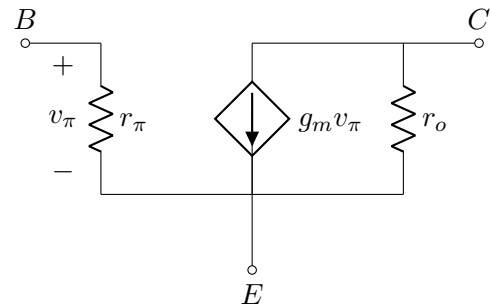


Figure 29: BJT Small Signal Model

5.3 Small Signal Analysis

1. Amplifier Parameters:

Voltage Gain	$A_v = \frac{v_o}{v_i}$
Open-loop Gain	$A_{vo} = \frac{v_o}{v_i} \Big _{R_L \rightarrow \infty}$
Input Resistance	$R_i = \frac{v_i}{i_i}$
Output Resistance of Amplifier	$R_o = \frac{v_o}{i_o} \Big _{v_i \rightarrow 0}$
Output Resistance of the circuit	$R_{out} = \frac{v_o}{i_o} \Big _{v_{sig} \rightarrow 0}$
Overall Gain	$A = \frac{R_i}{R_i + R_{sig}} A_v$

2. Design considerations:

(a) $R_i \gg R_{sig}$

(b) $R_o \ll R_L$

3. Solving Amplifier Circuits

- (a) Find Bias and Signal Circuits
- (b) Get the bias (Q point) values
 - i. capacitors are open
 - ii. large signal models
- (c) Get the signal parameters
 - i. capacitors are shorts
 - ii. independent sources are suppressed
 - iii. replace with small signal model
- (d) Terminal Resistance:
 - i. Consider that a voltage v_x and current i_x is supplied through the terminal. the terminal resistance is $\frac{v_x}{i_x}$

6 Amplifier Frequency Response