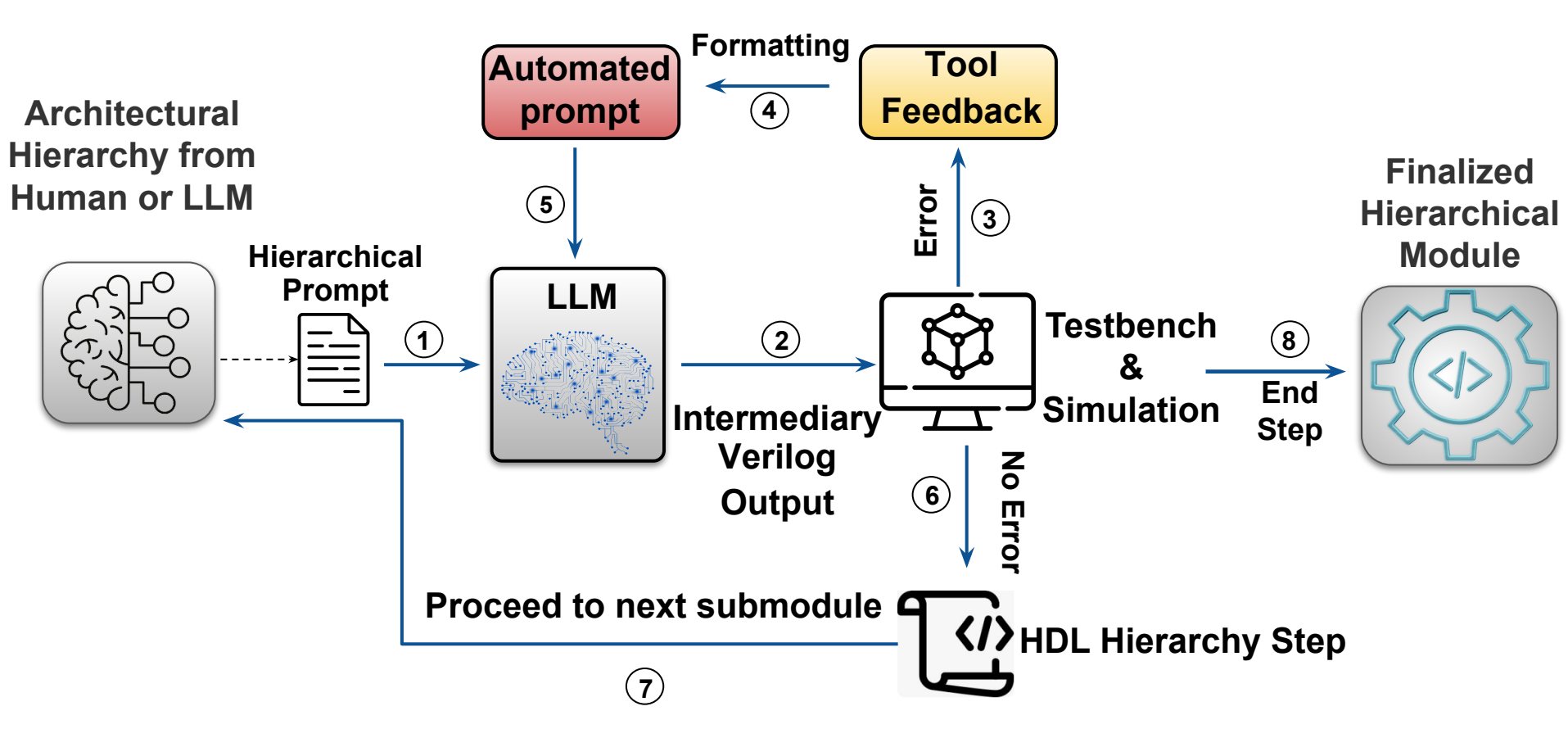
Automated prompt
Formatting
Tool Feedback
4
Architectural Hierarchy from Human or LLM
5
Error
3
Finalized Hierarchical Module
Hierarchical Prompt
1
LLM
2
Testbench & Simulation
8
End Step
Intermediary Verilog Output
6
No Error
Proceed to next submodule
HDL Hierarchy Step
7