# Improving Soft Error Reliability in Modern Processors

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**Advisor: Prof. Lieven Eeckhout**

**Doctoral Thesis Defense**

GHENT UNIVERSITY

FACULTY OF ENGINEERING AND ARCHITECTURE

# Reliability in Computer Science

The term reliability refers to the ability of a computer hardware or software component to consistently perform according to its specifications.

# What if the Reliability is Compromised?

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```
A problem has been detected and Windows has been shut down to prevent damage
to your computer.

The problem seems to be caused by the following file: kbdhid.sys

MANUALLY_INITIATED_CRASH

If this is the first time you've seen this stop error screen,
restart your computer. If this screen appears again, follow
these steps:

Check to make sure any new hardware or software is properly installed.
If this is a new installation, ask your hardware or software manufacturer
for any Windows updates you might need.

If problems continue, disable or remove any newly installed hardware
or software. Disable BIOS memory options such as caching or shadowing.
If you need to use safe mode to remove or disable components, restart
your computer, press F8 to select Advanced Startup Options, and then
select Safe Mode.

Technical Information:

*** STOP: 0x000000e2 (0x00000000, 0x00000000, 0x00000000, 0x00000000)

*** kbdhid.sys - Address 0x94efd1aa base at 0x94efb000 DateStamp 0x4a5bc705
```

# What if the Reliability is Compromised?

SARAH SCOLES SCIENCE 06.04.2018 07:00 AM

## Cosmic Ray Showers Crash Supercomputers. Here's What to Do About It

What happens when a national laboratory's supercomputers start glitching?

EMILY WAITE

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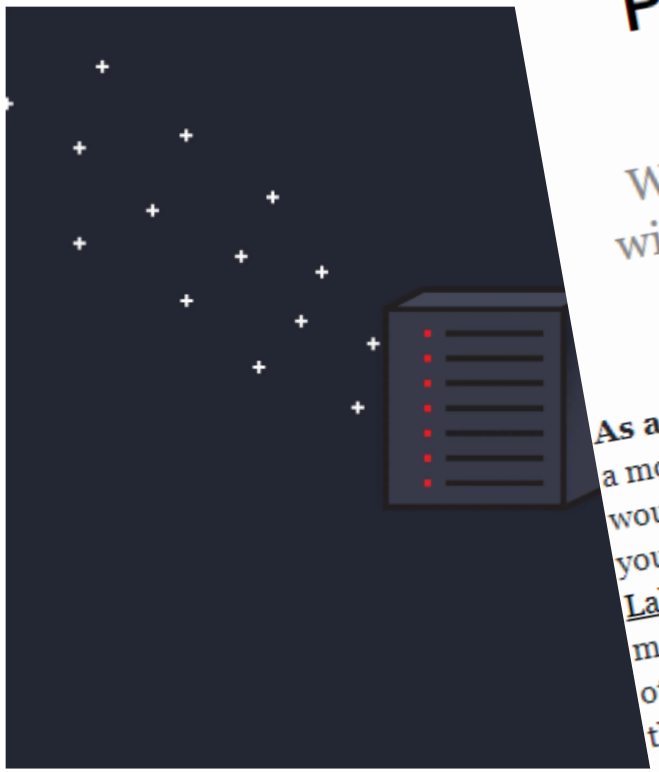


EMILY WAITE

## How To Kill A Supercomputer: Dirty Power, Cosmic Rays, and Bad Solder

Will future exascale supercomputers be able to withstand the steady onslaught of routine faults?

By Al Geist

**As a child**, were you ever afraid that a monster lurking in your bedroom would leap out of the dark and get you? My job at Oak Ridge National Laboratory is to worry about a similar monster, hiding in the steel cabinets of the supercomputers and threatening to crash the largest computing machines on the planet.

The monster is something

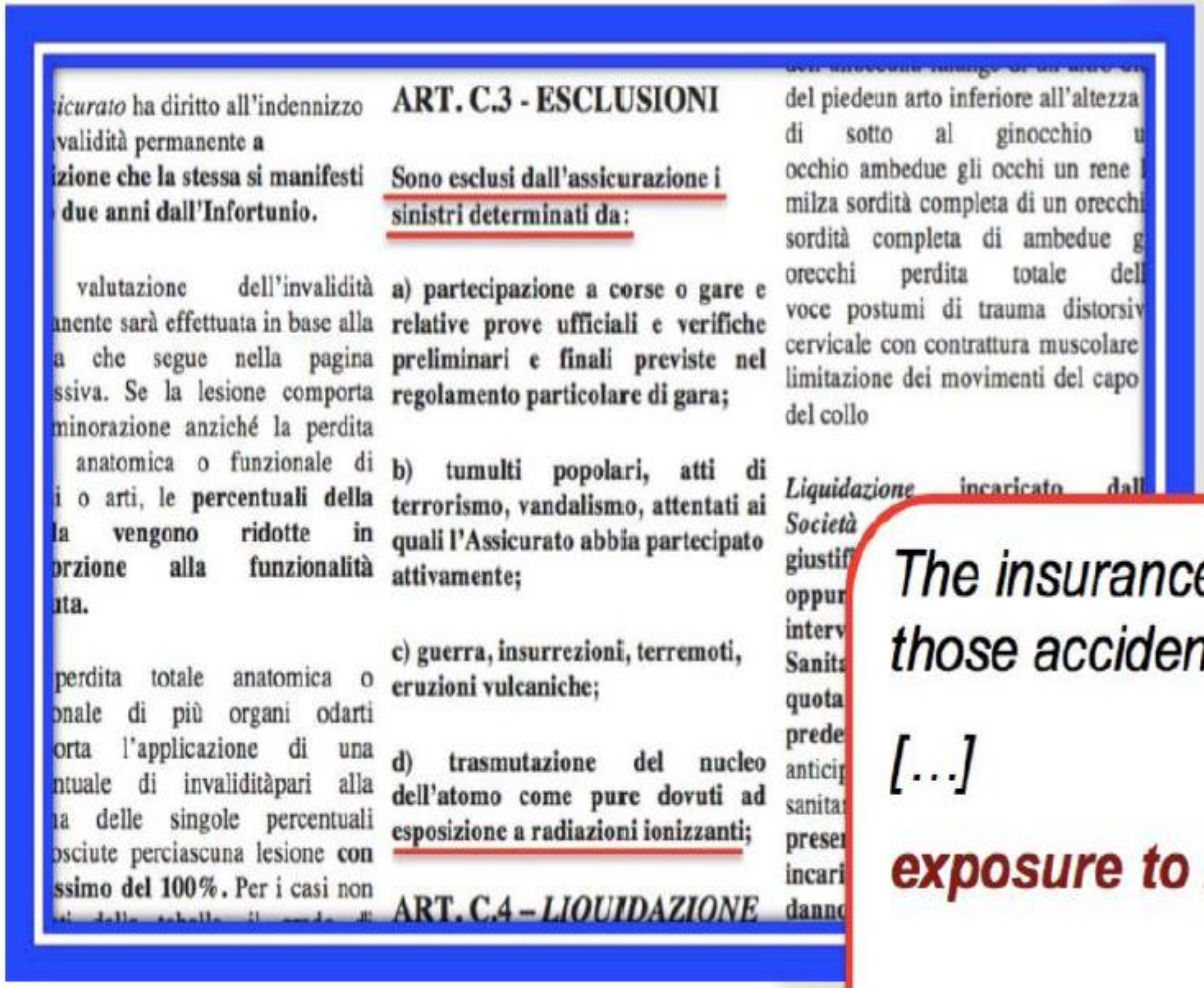
# What if the Reliability is Compromised?

## The Uber Crash Won't Be the Last Shocking Self-Driving Death

These systems will fail, and when the do, the result will look nothing like human-powered crashes.


KIEN HONG LE/BLOOMBERG/GETTY IMAGES

# Did you Read your Car Insurance Carefully?



*icurato* ha diritto all'indennizzo
validità permanente a
**izione che la stessa si manifesti**
**due anni dall'Infortunio.**

valutazione dell'invalidità
nente sarà effettuata in base alla
a che segue nella pagina
ssiva. Se la lesione comporta
minorazione anziché la perdita
anatomica o funzionale di
i o arti, le **percentuali della**
**la vengono ridotte in**
**orzione alla funzionalità**
**ita.**

perdita totale anatomica o
onale di più organi odarti
orta l'applicazione di una
ntuale di invalidità pari alla
a delle singole percentuali
osciute perciascuna lesione **con**
**ssimo del 100%.** Per i casi non

**ART. C.3 - ESCLUSIONI**

**Sono esclusi dall'assicurazione i sinistri determinati da:**

**a) partecipazione a corse o gare e relative prove ufficiali e verifiche preliminari e finali previste nel regolamento particolare di gara;**

**b) tumulti popolari, atti di terrorismo, vandalismo, attentati ai quali l'Assicurato abbia partecipato attivamente;**

**c) guerra, insurrezioni, terremoti, eruzioni vulcaniche;**

**d) trasmutazione del nucleo dell'atomo come pure dovuti ad esposizione a radiazioni ionizzanti;**

**ART. C.4 – *LIQUIDAZIONE***

del piedeun arto inferiore all'altezza
di sotto al ginocchio u
occhio ambedue gli occhi un rene
milza sordità completa di un orecchi
sordità completa di ambedue g
orecchi perdita totale dell
voce postumi di trauma distorsiv
cervicale con contrattura muscolare
limitazione dei movimenti del capo
del collo

***Liquidazione*** incaricato dall
***Società***
giustif
oppur
interv
Sanit
quota
prede
anticip
sanita
preser
incari
danno

*The insurance does not cover those accidents caused by:*

*[…]*

***exposure to ionizing radiation****

# Different Types of Computing Systems

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Consumer

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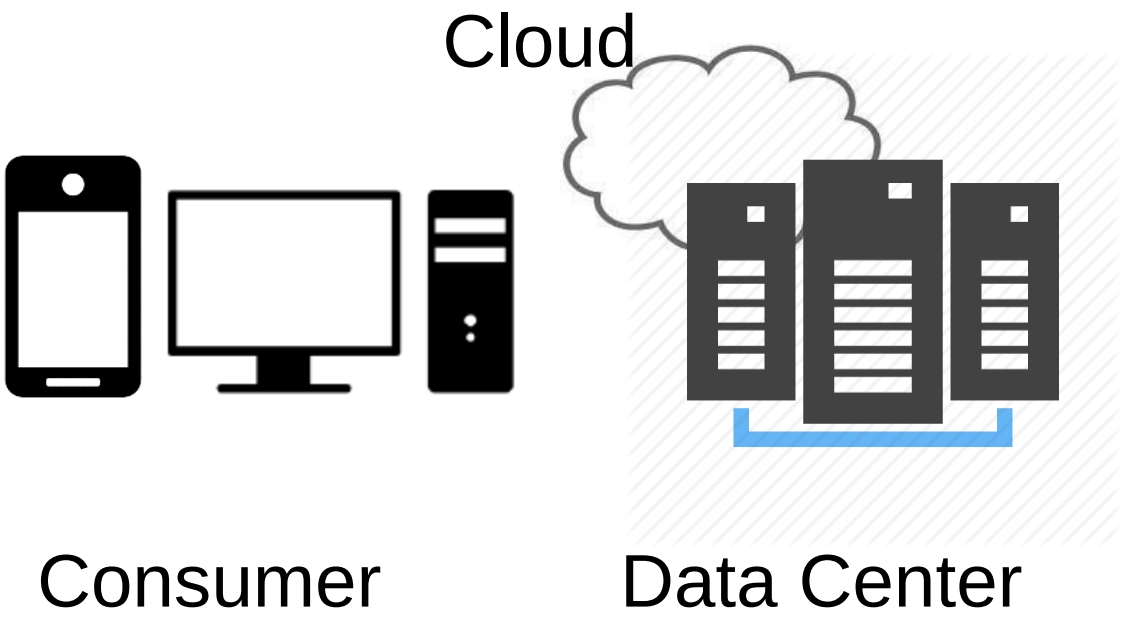

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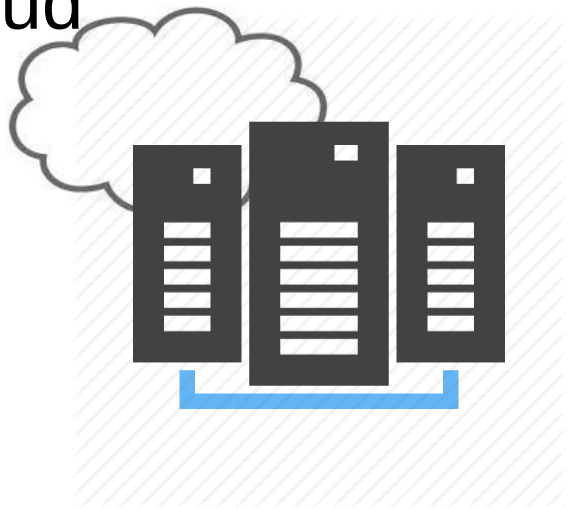


Data Center

Scientific Computing

# Different Types of Computing Systems

Consumer

Cloud

Data Center

Scientific Computing

Automotive

# Different Reliability Requirements

Consumer


Data Center

Scientific Computing

Automotive

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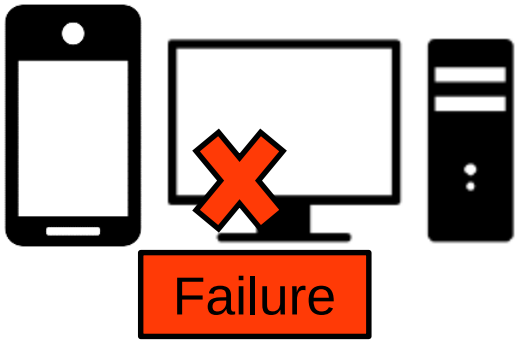
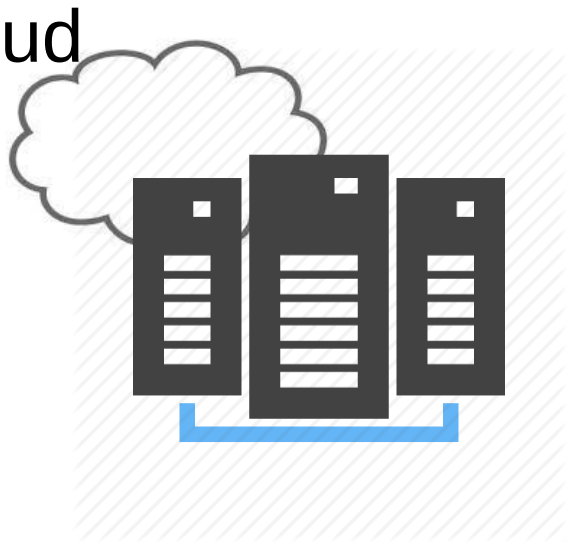



Consumer

**Less critical**

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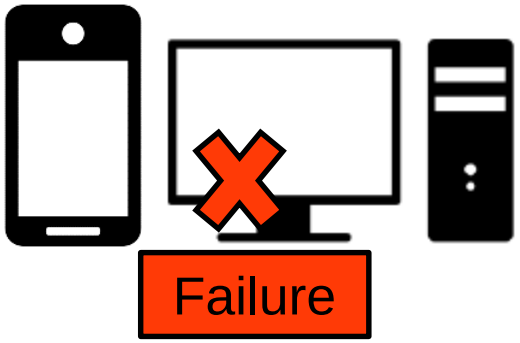


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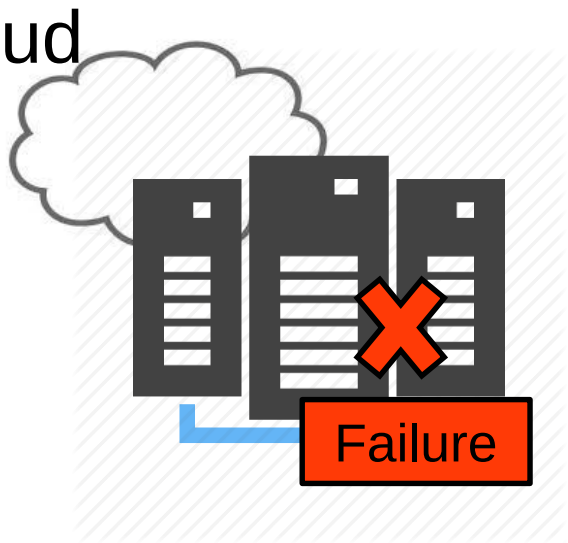


Data Center

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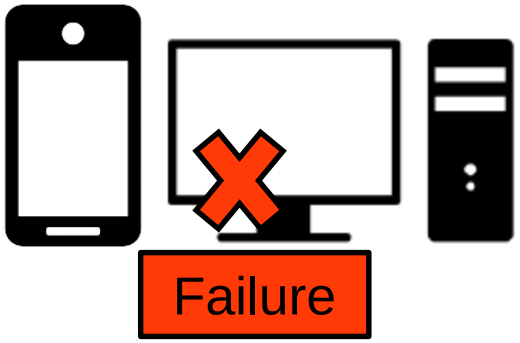


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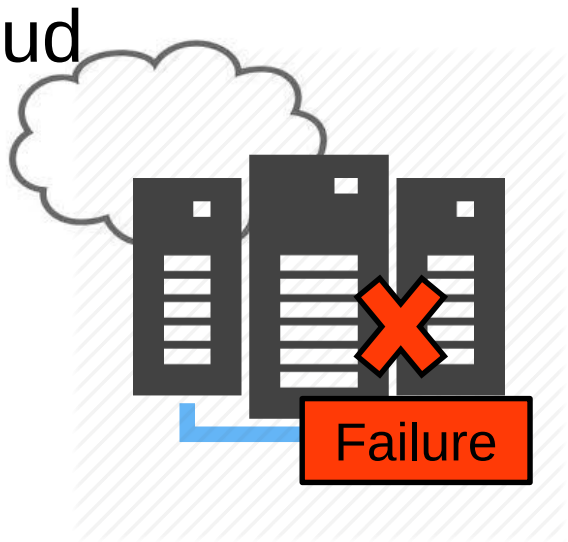


Data Center

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Scientific Computing

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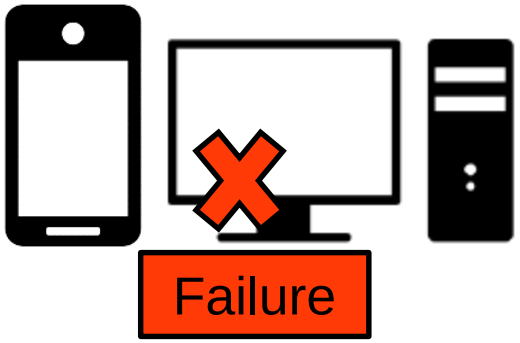


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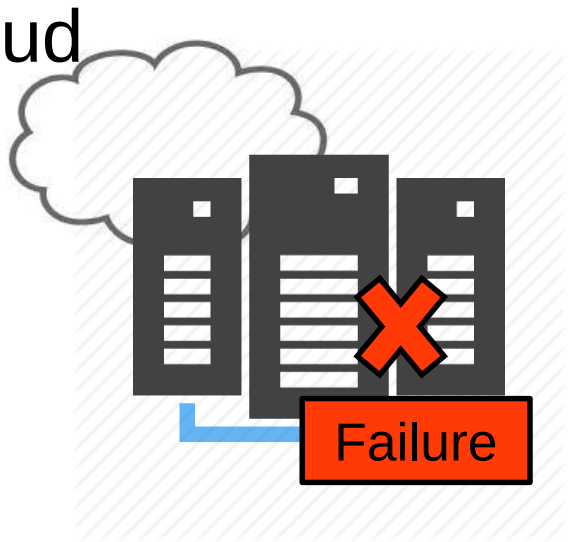



Data Center

**Critical**

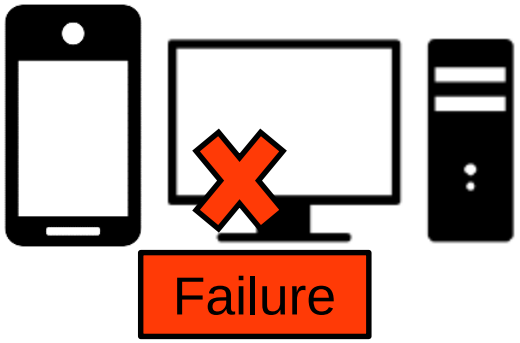

Scientific Computing

**More Critical**


Automotive

**Human life**

# Different Reliability Requirements

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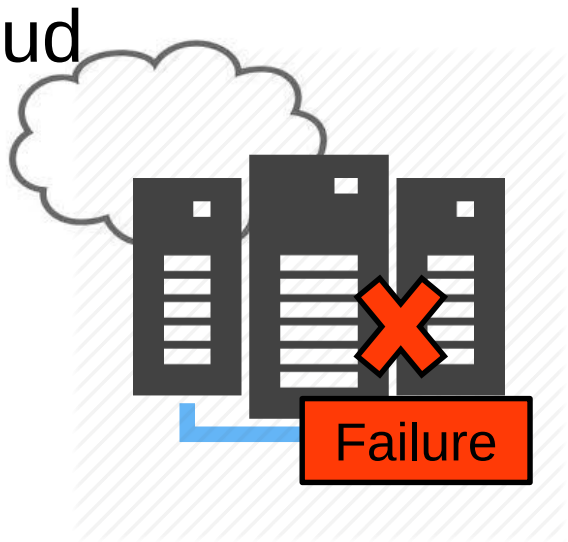


Data Center

**Critical**


Scientific Computing

**More Critical**


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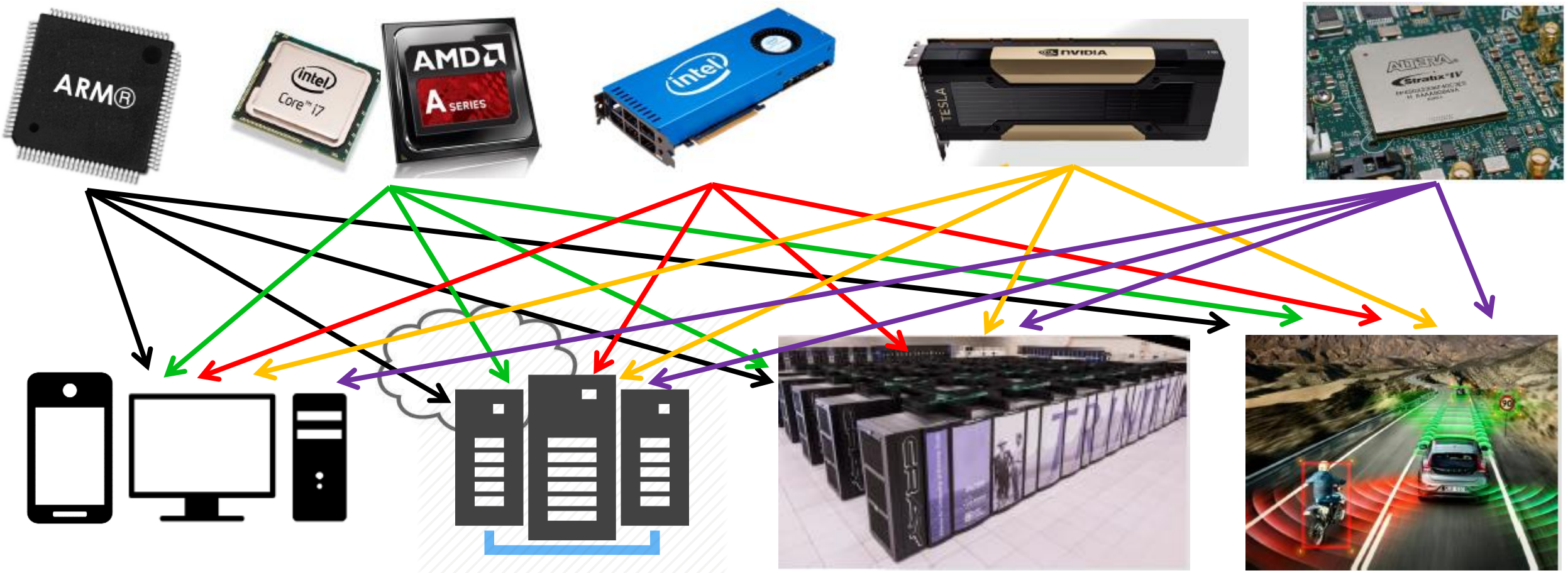
**Human life**

**Reliability Requirements**

# Different Devices Running These Systems

ARM CPU Coprocessor GPU FPGA/SoC




Consumer Data Center Scientific Computing Automotive

[Arijit Biswas, SELSE 2018]

# Two Key Components: Processor and Memory

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Processor

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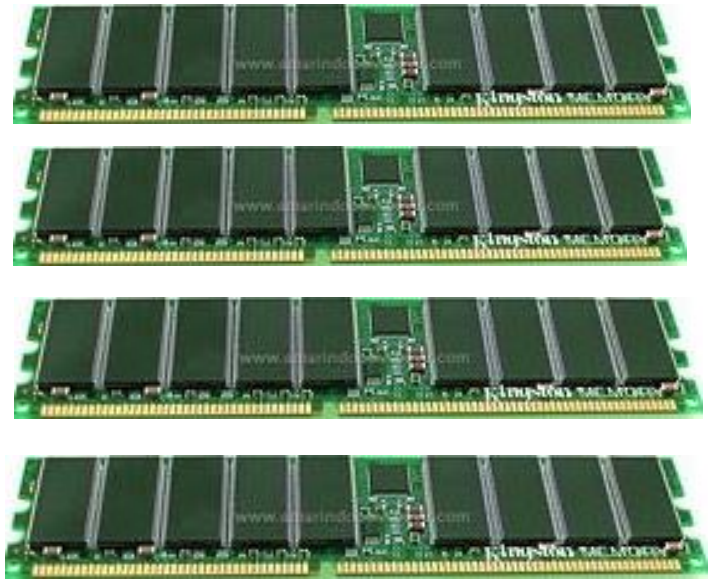
Memory

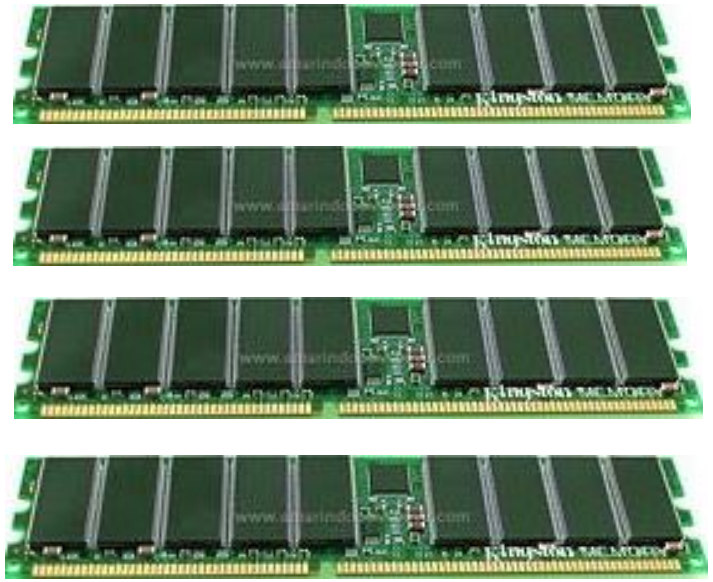


# Two Key Components: Processor and Memory

Processor


Read

Memory



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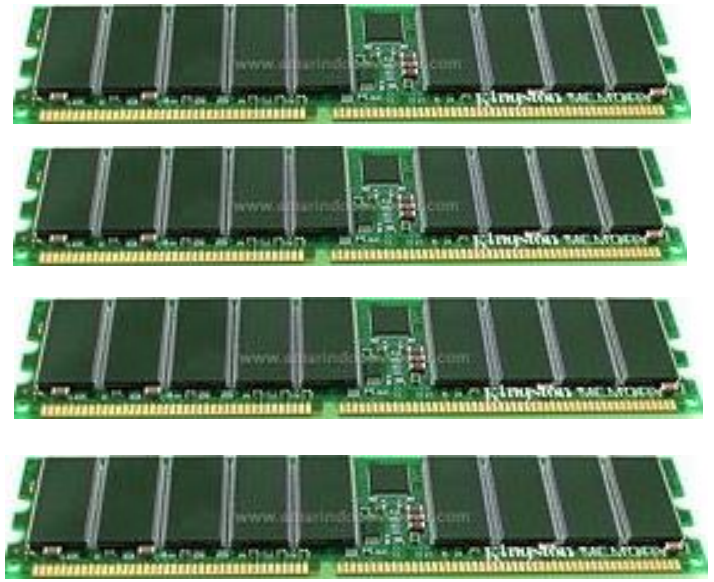
Processor


Compute

Read

Memory



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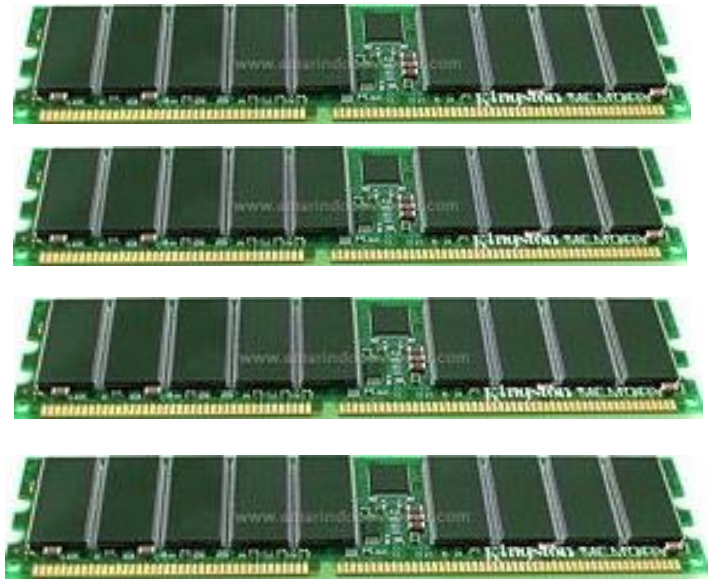
Compute

Read

Write

Memory



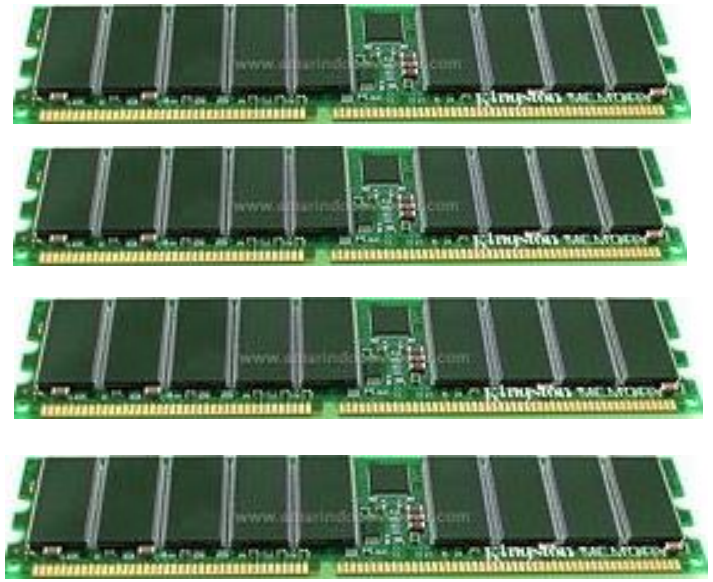
# Two Key Sources of Failures: Processor and Memory

Processor

Memory


Read

Write



Compute

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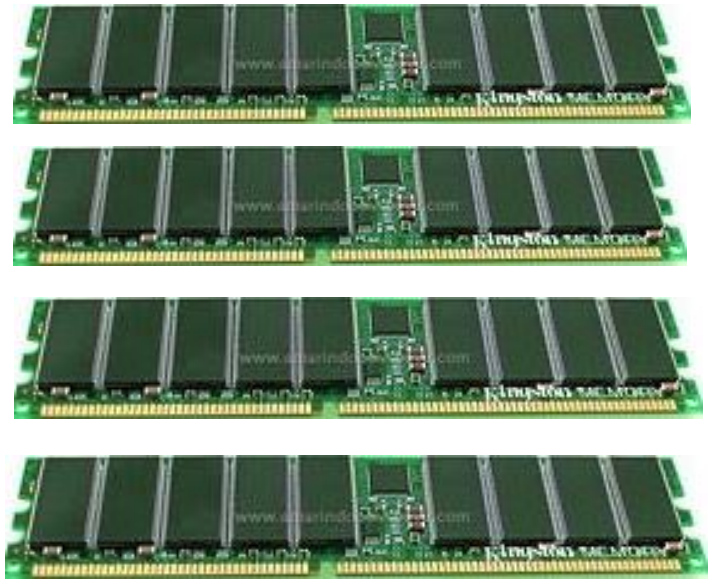

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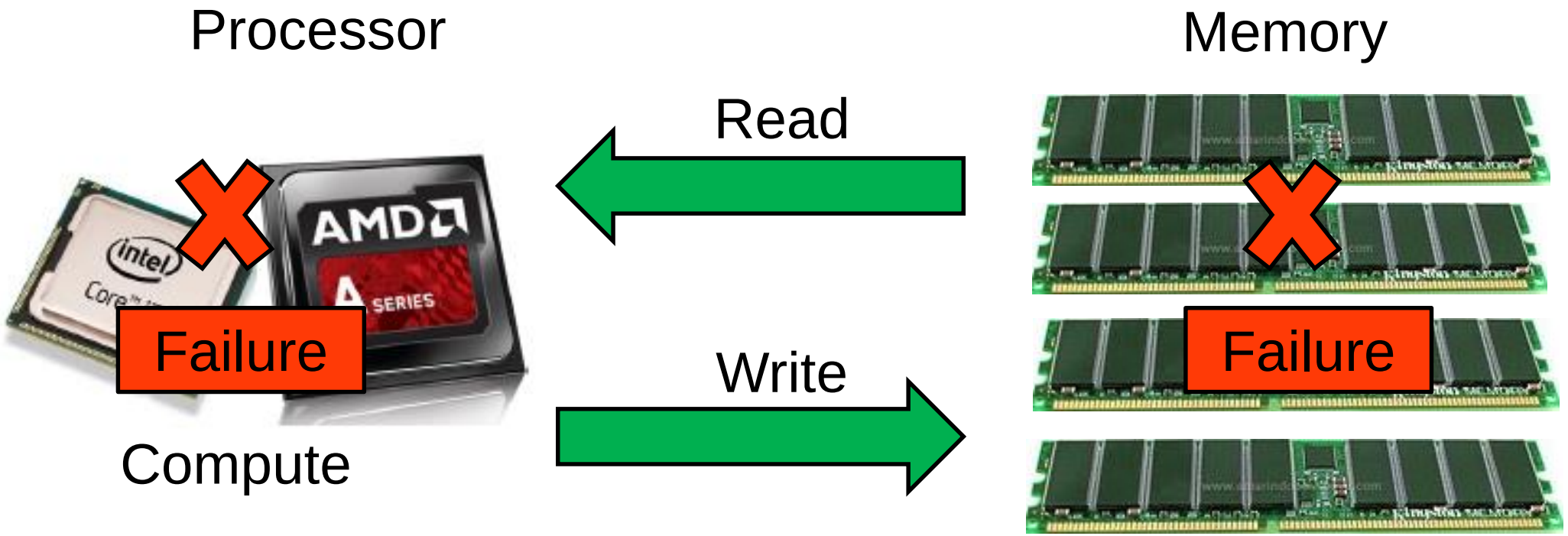

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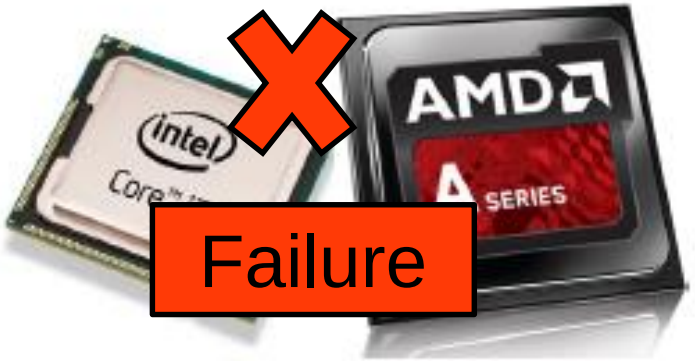
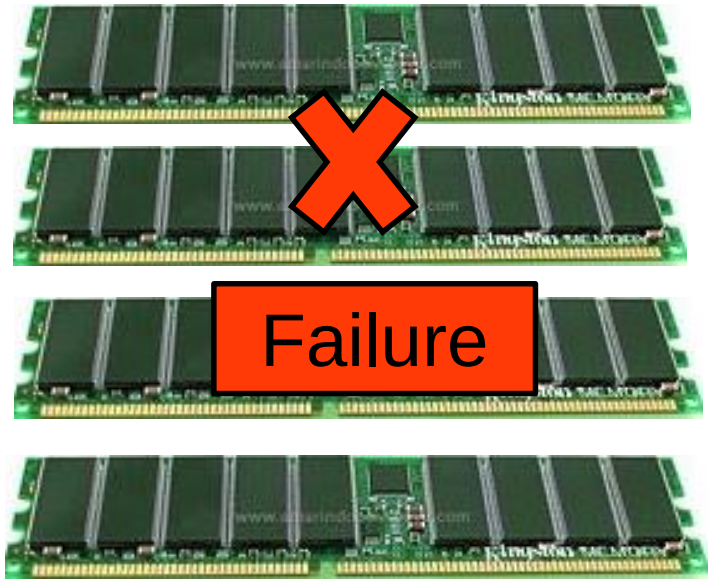



Compute

Read

Write

Memory




Error Correcting Code
(ECC)

# Processor Failures are a Result of Underlying Faults

Processor

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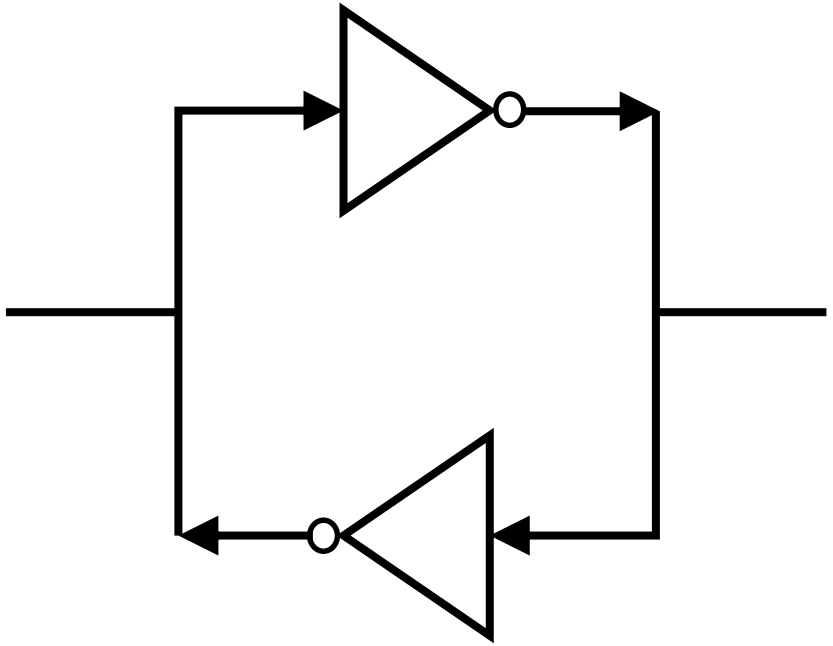

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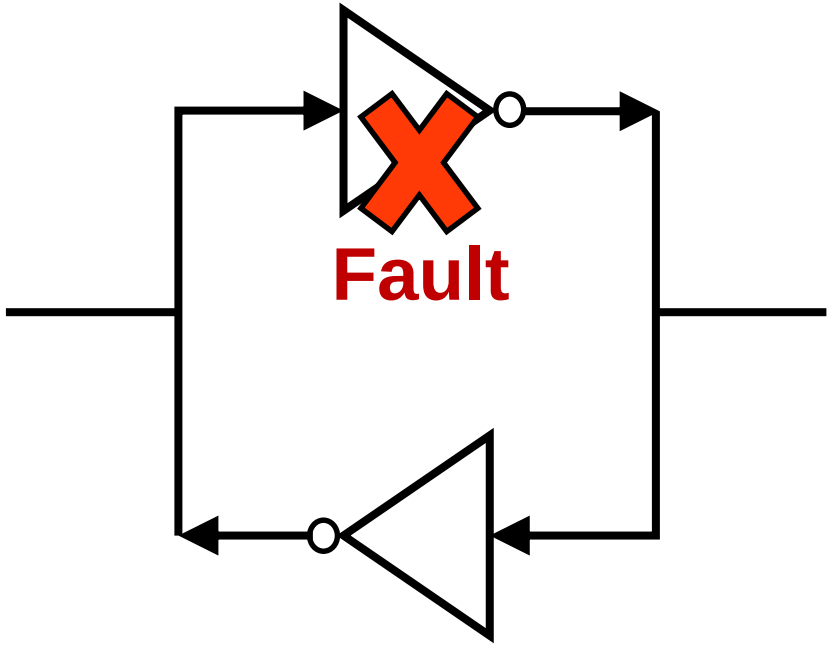


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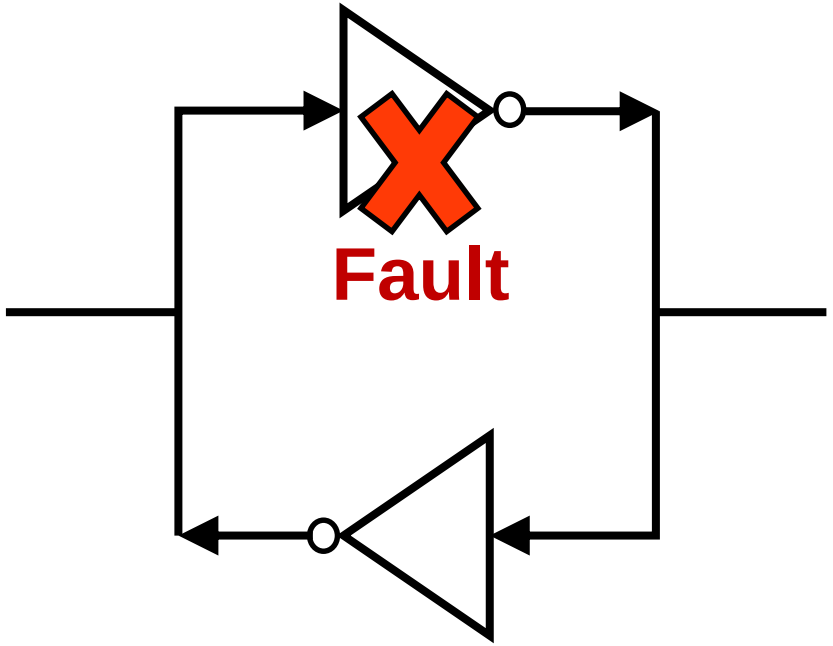


Processor


Example: non-functioning or defective transistor

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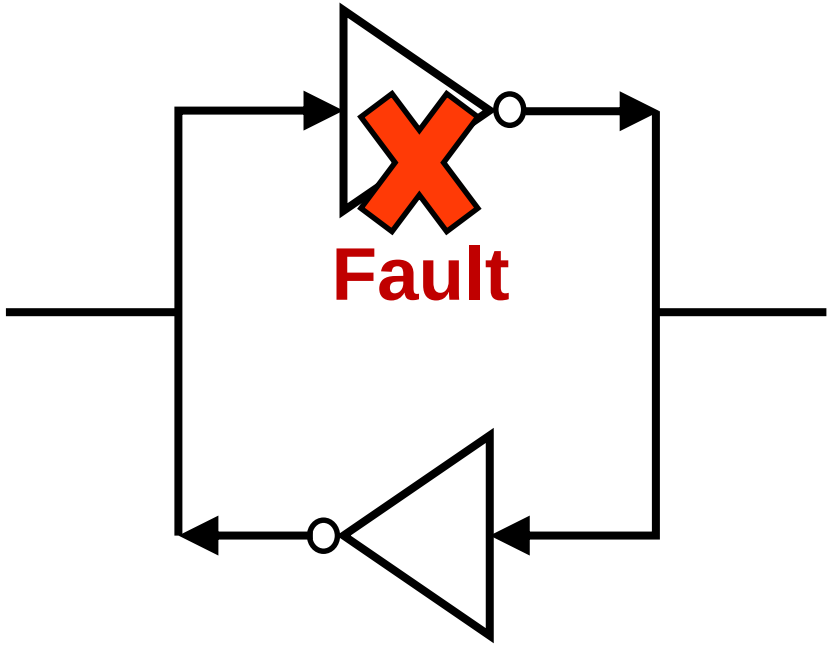


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3. Transient – random, temporary, non-reproducible
   -- Energy particle strikes or radiations

# What are Radiation-Induced Faults?

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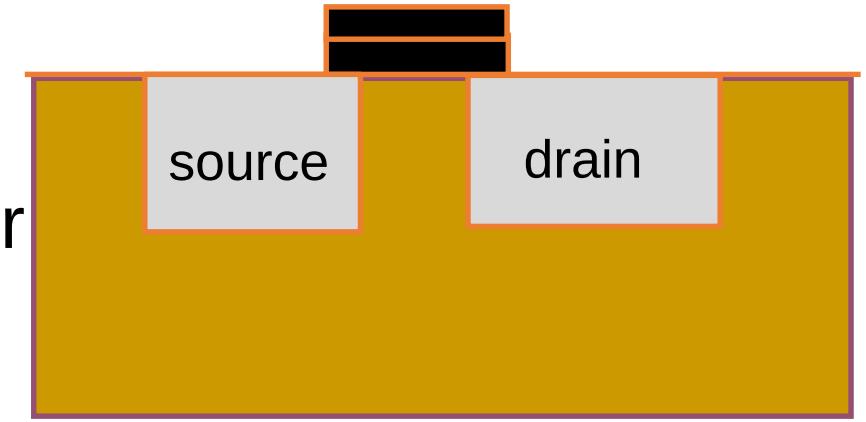
Transistor device*

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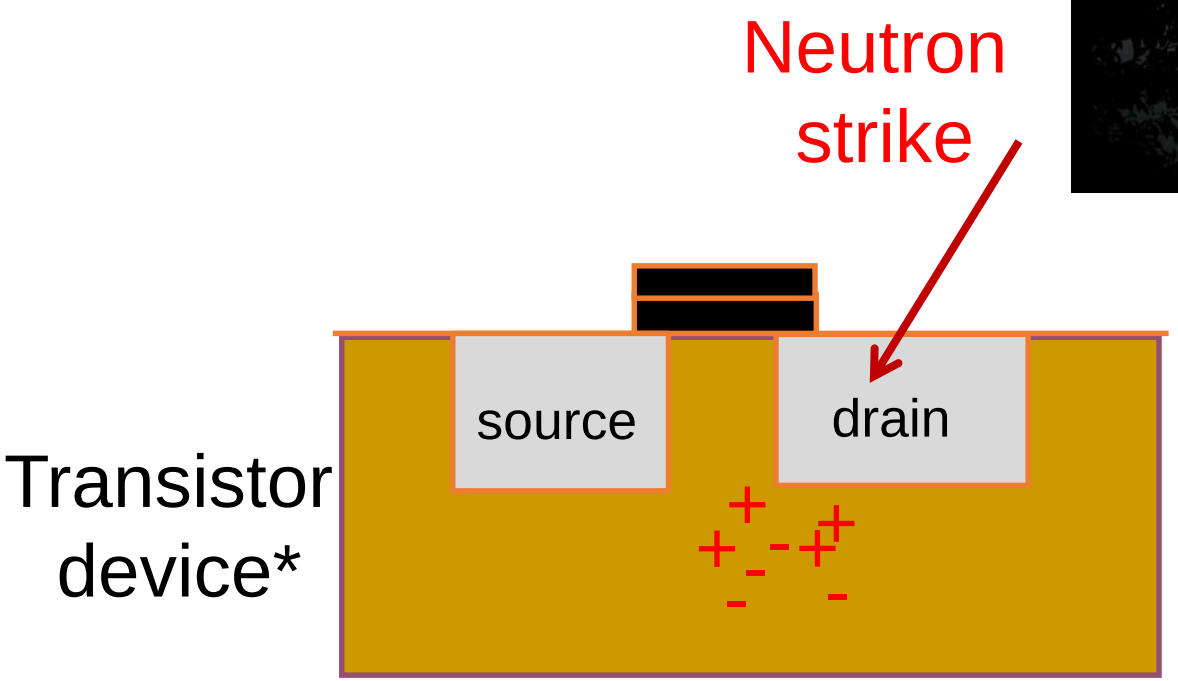


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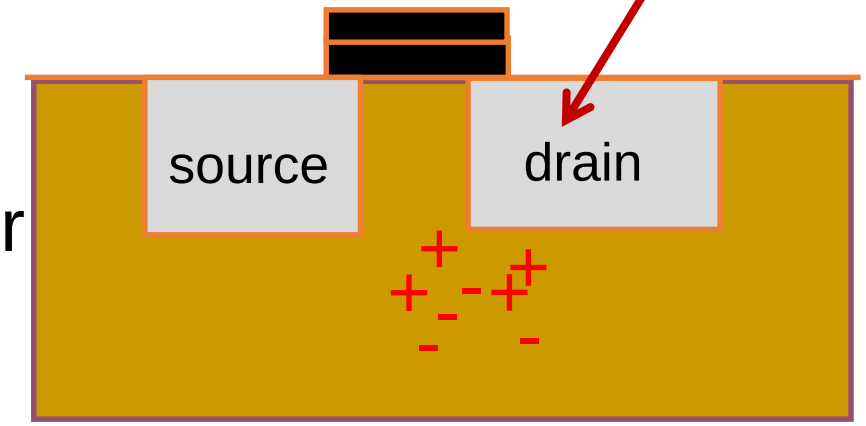


**Temporarily changes device state**

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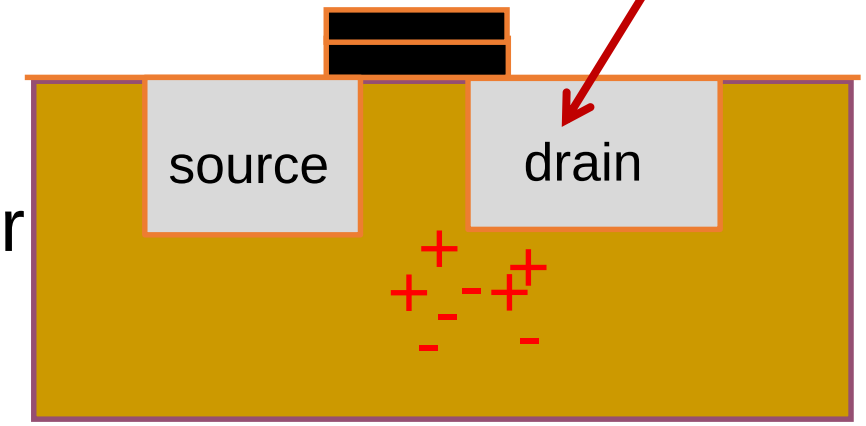
- Main source: neutrons from deep space

- Secondary source: alpha particles from packaging material

Neutron strike

Transistor device*

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# Faults → Errors → Failures

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Fault

# Faults → Errors → Failures

Fault

↓

Error

# Faults → Errors → Failures

Fault

↓

Error

↓

Failure

# Faults → Errors → Failures

Fault

Radiations

↓

Error

↓

Failure

# Faults → Errors → Failures

Fault

Radiations

Error

Soft error

Failure

# Faults → Errors → Failures

Fault

Radiations

↓

↓

Error

Soft error

↓

↓

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Failure

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Fault

↓

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↓

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↓

Soft error

↓

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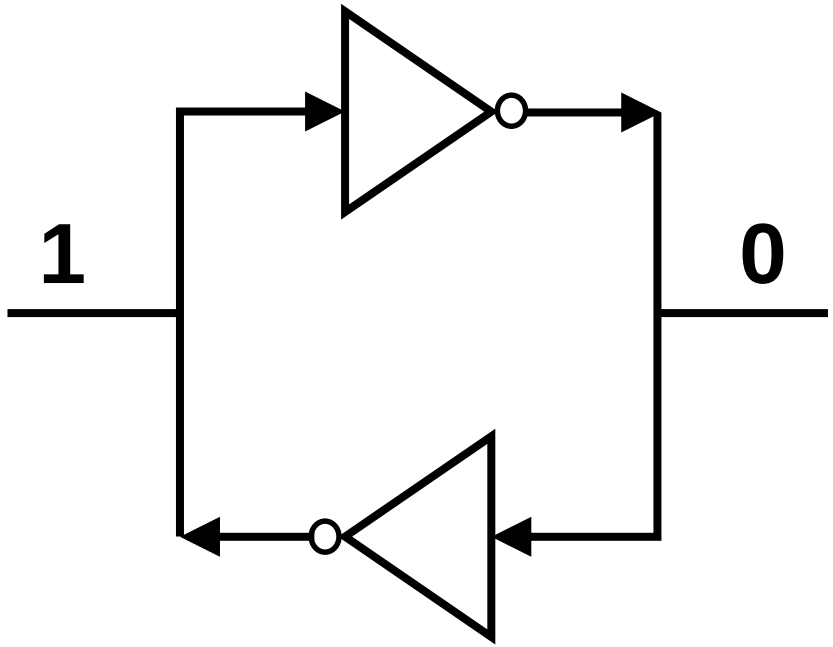

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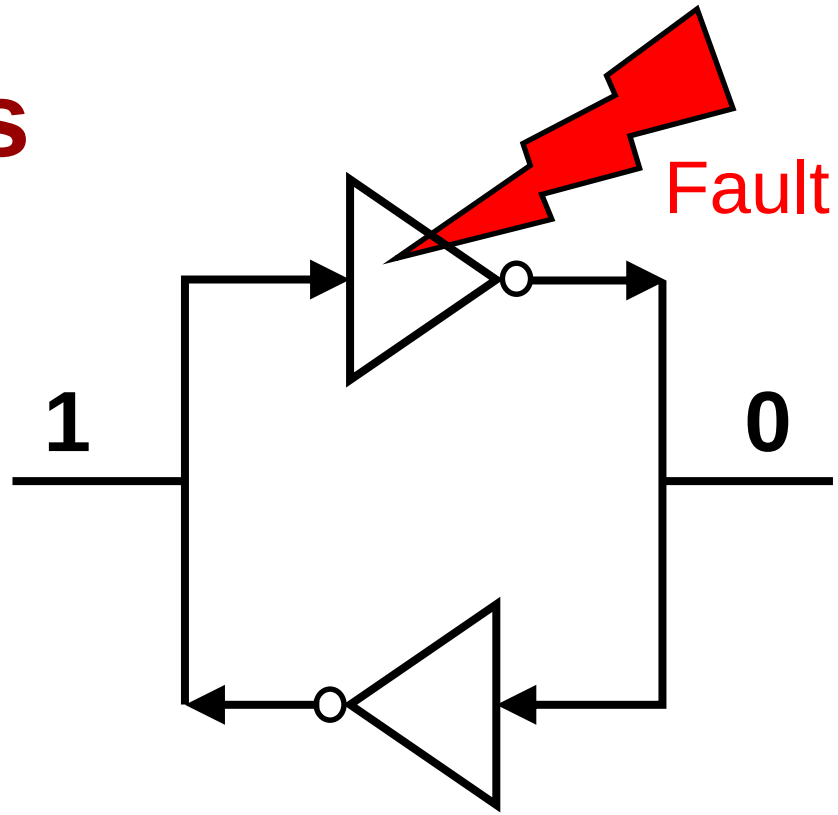

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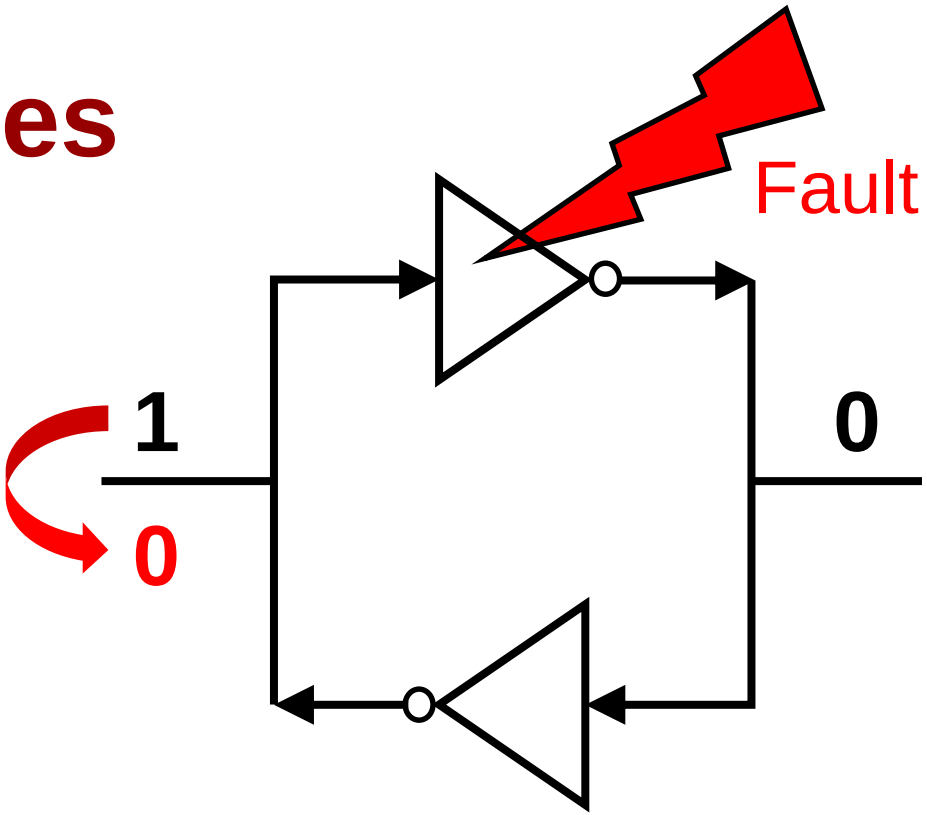

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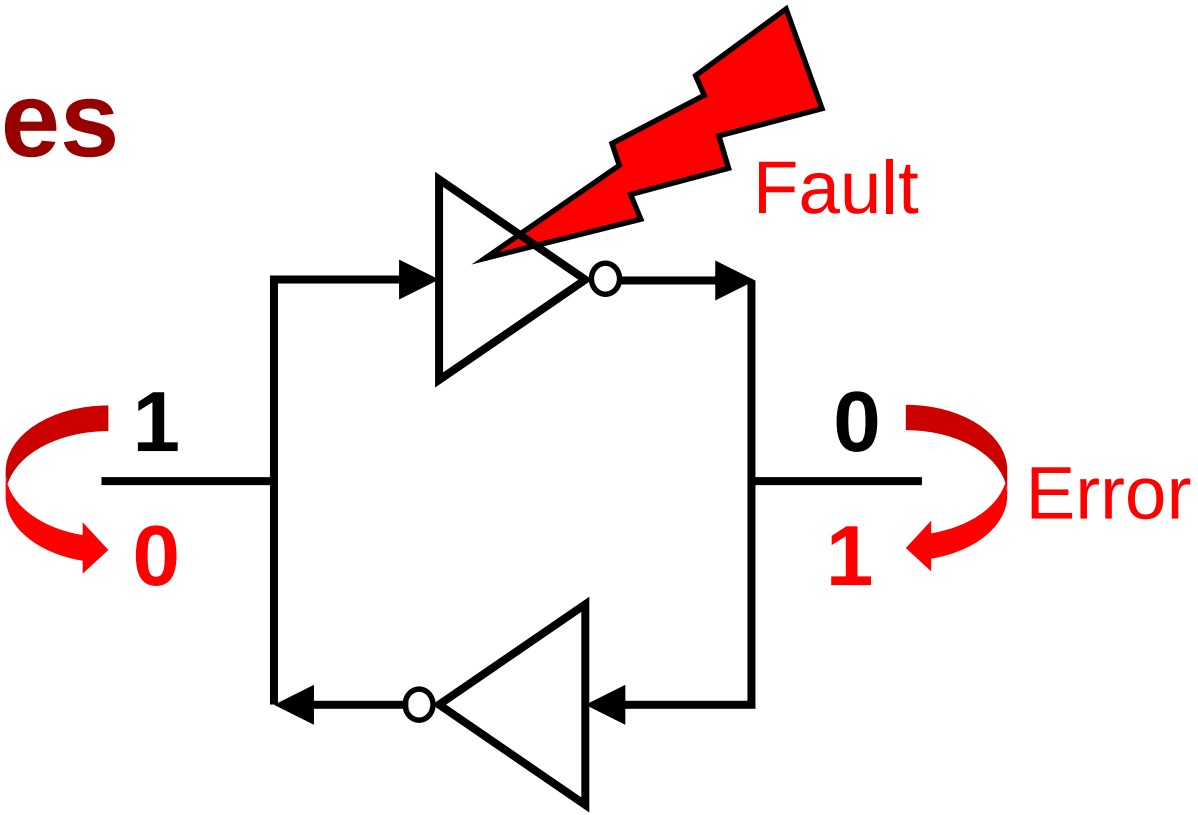

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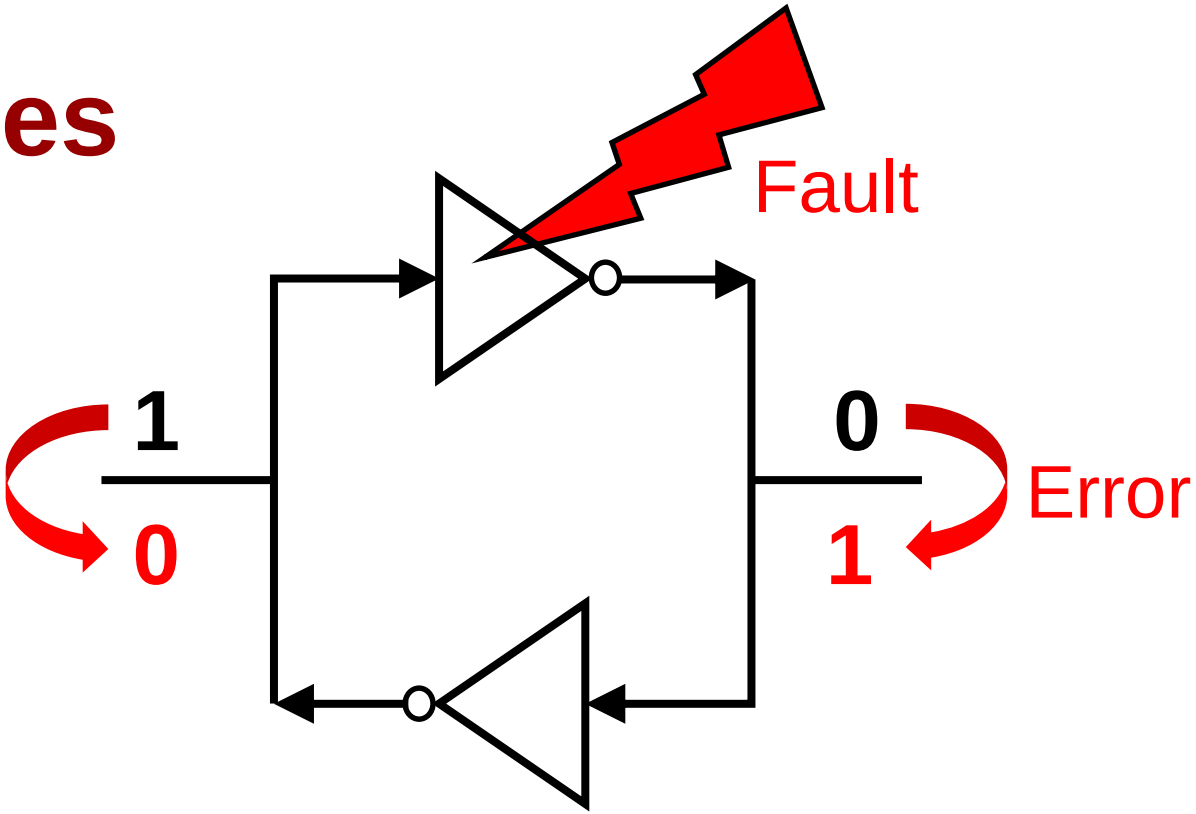


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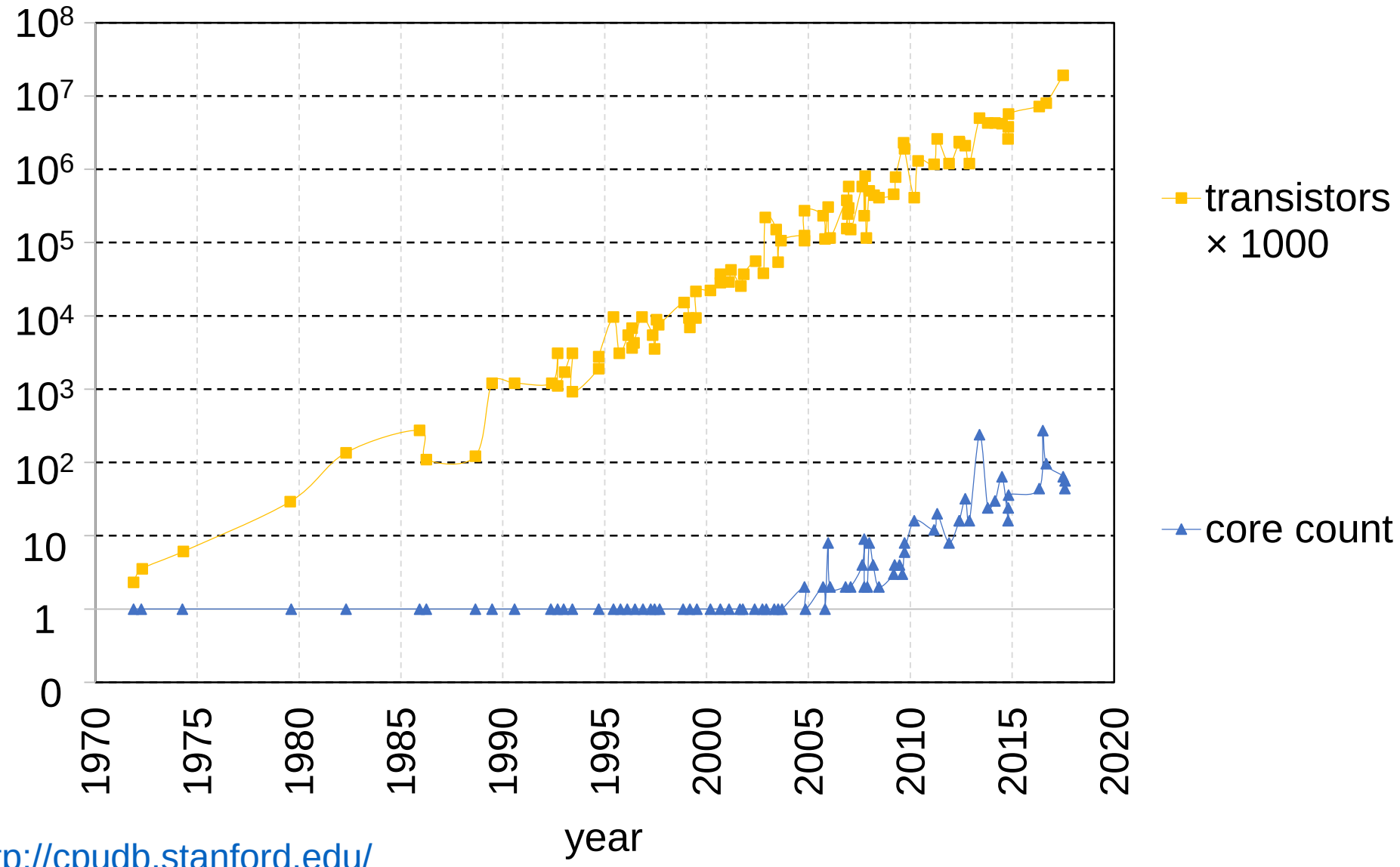
2. **Microarchitectural innovations** – pipelining, out-of-order execution, prefetching, branch prediction

# Consequences of Technology Scaling




http://cpudb.stanford.edu/

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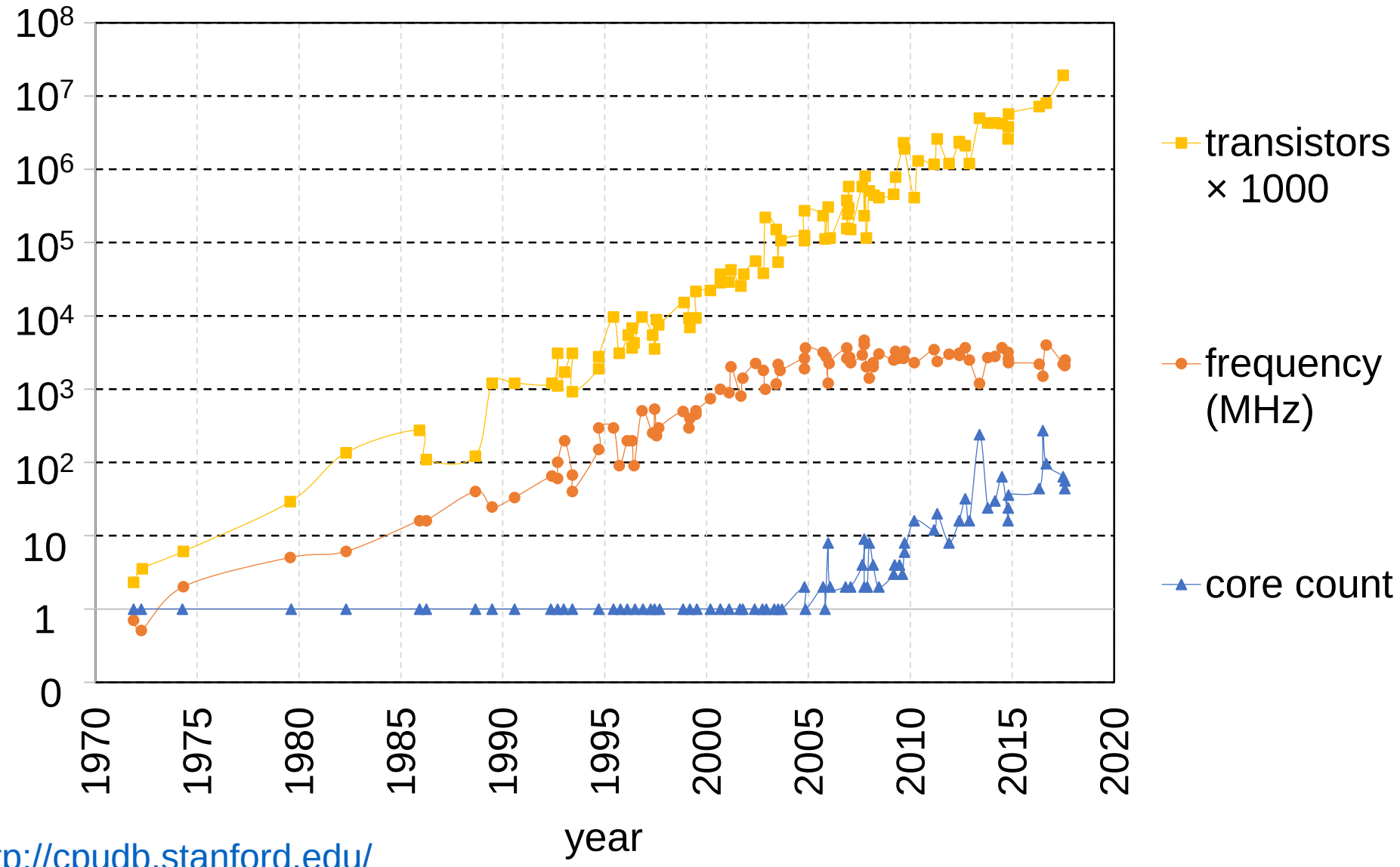


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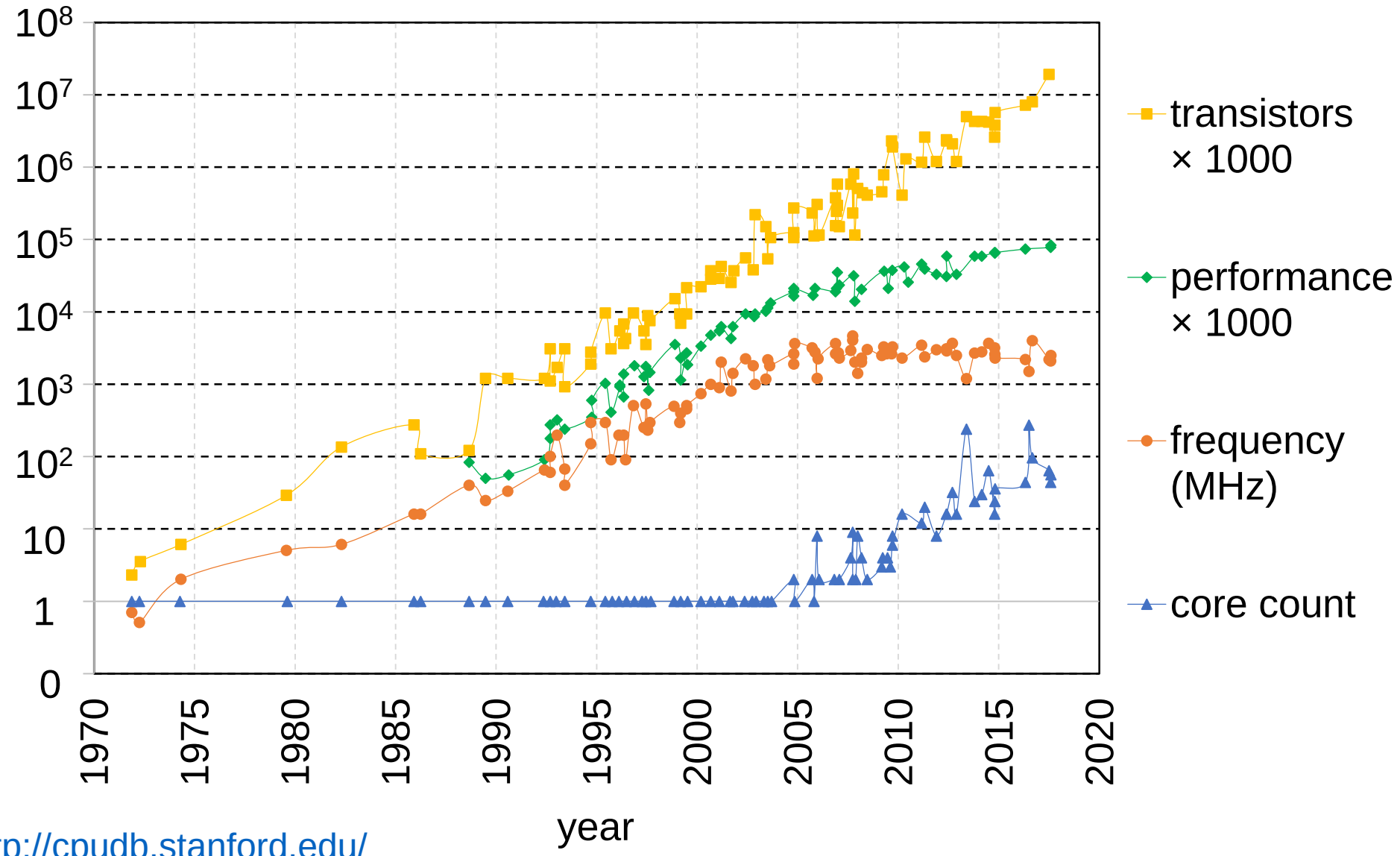


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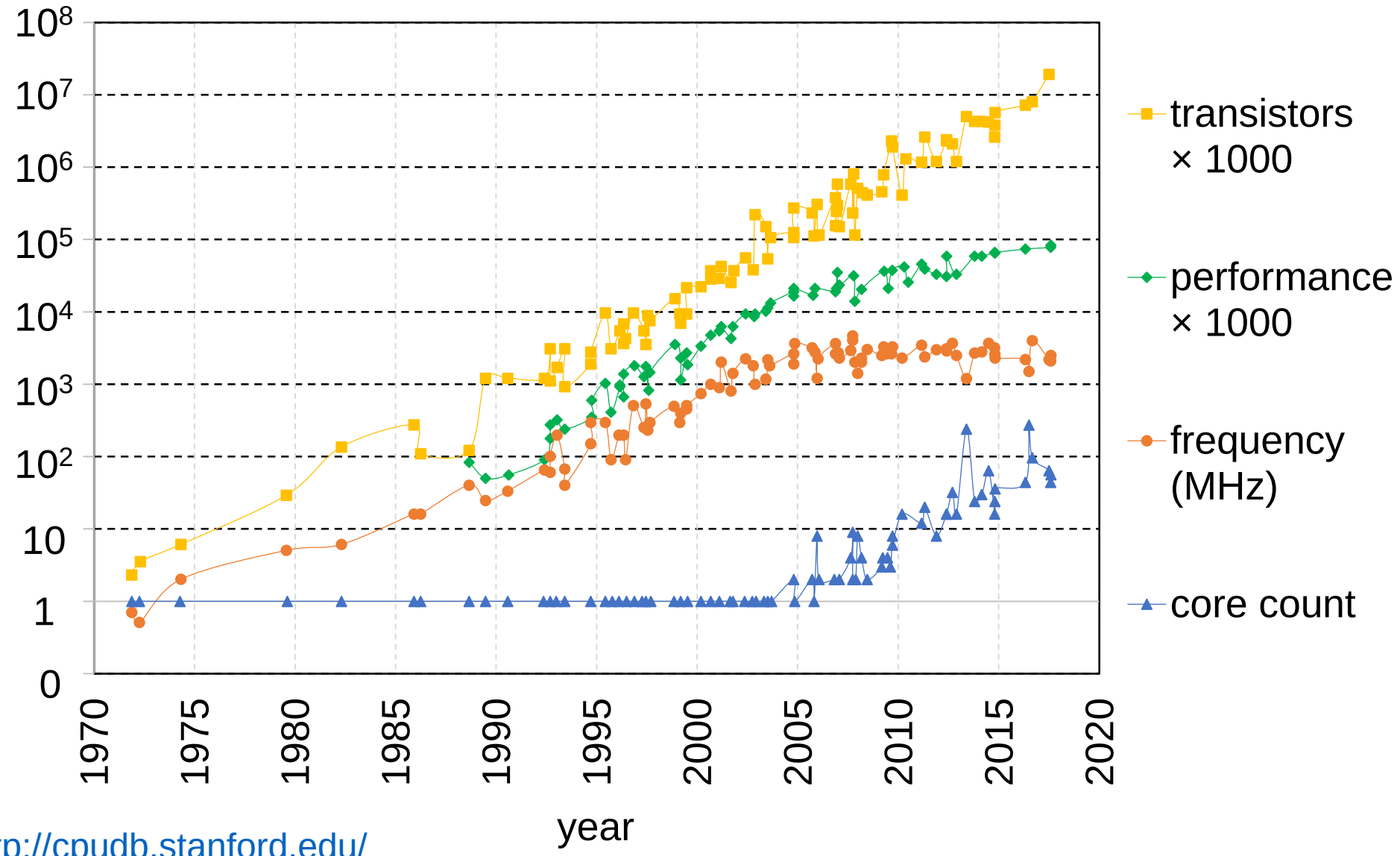


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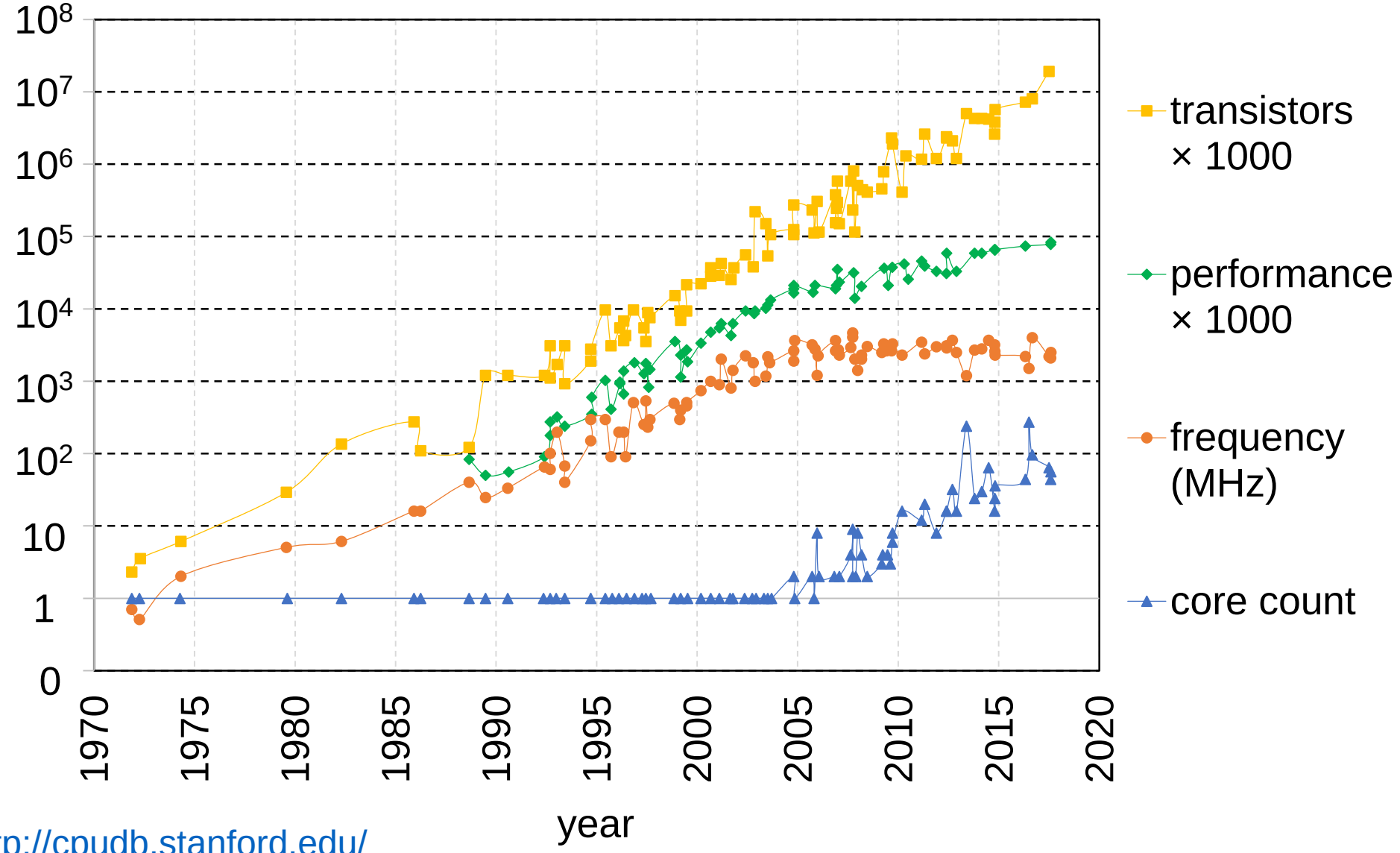


Size ↓ K

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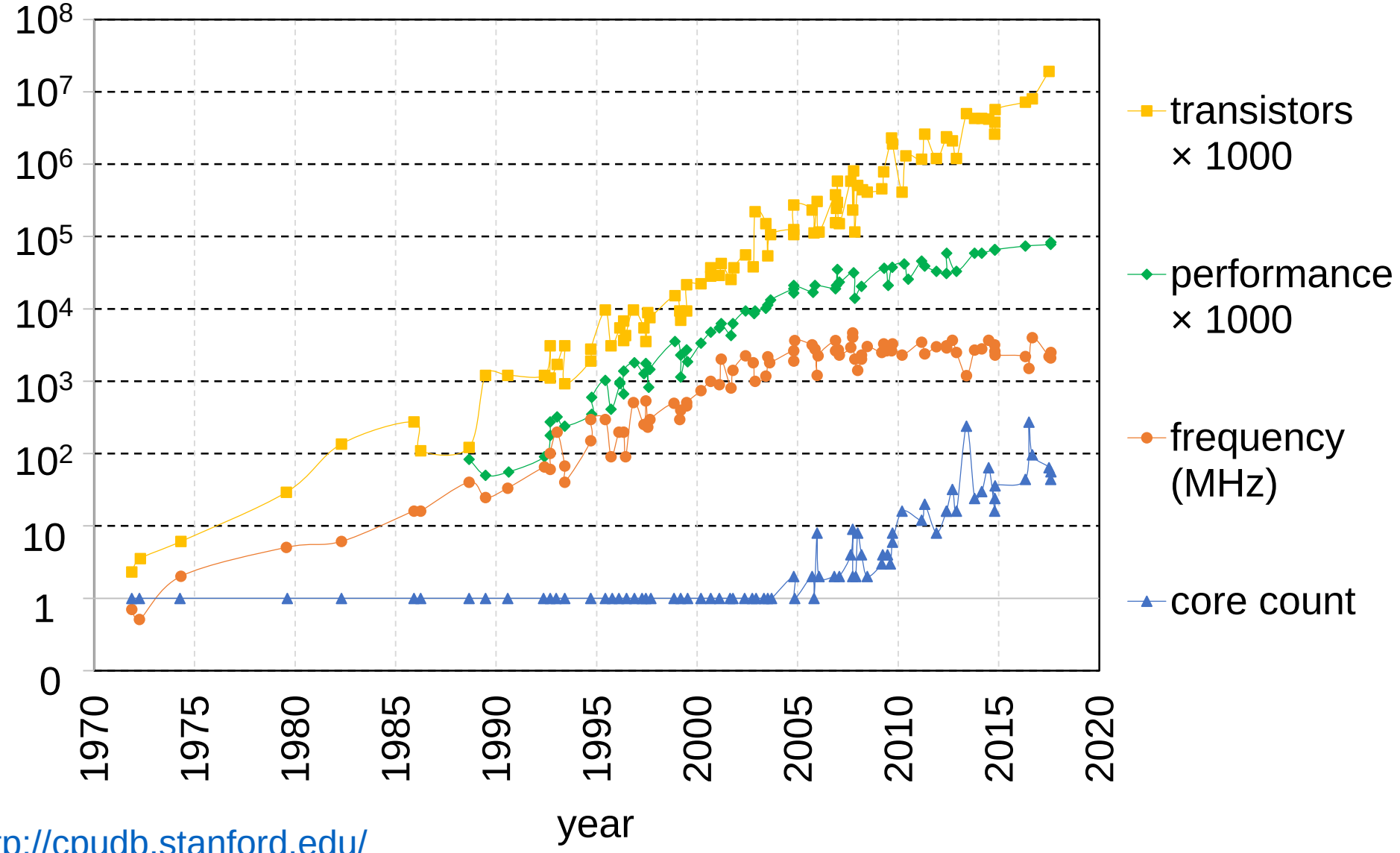


Size ↓ K

Circuit Delay ↓ K

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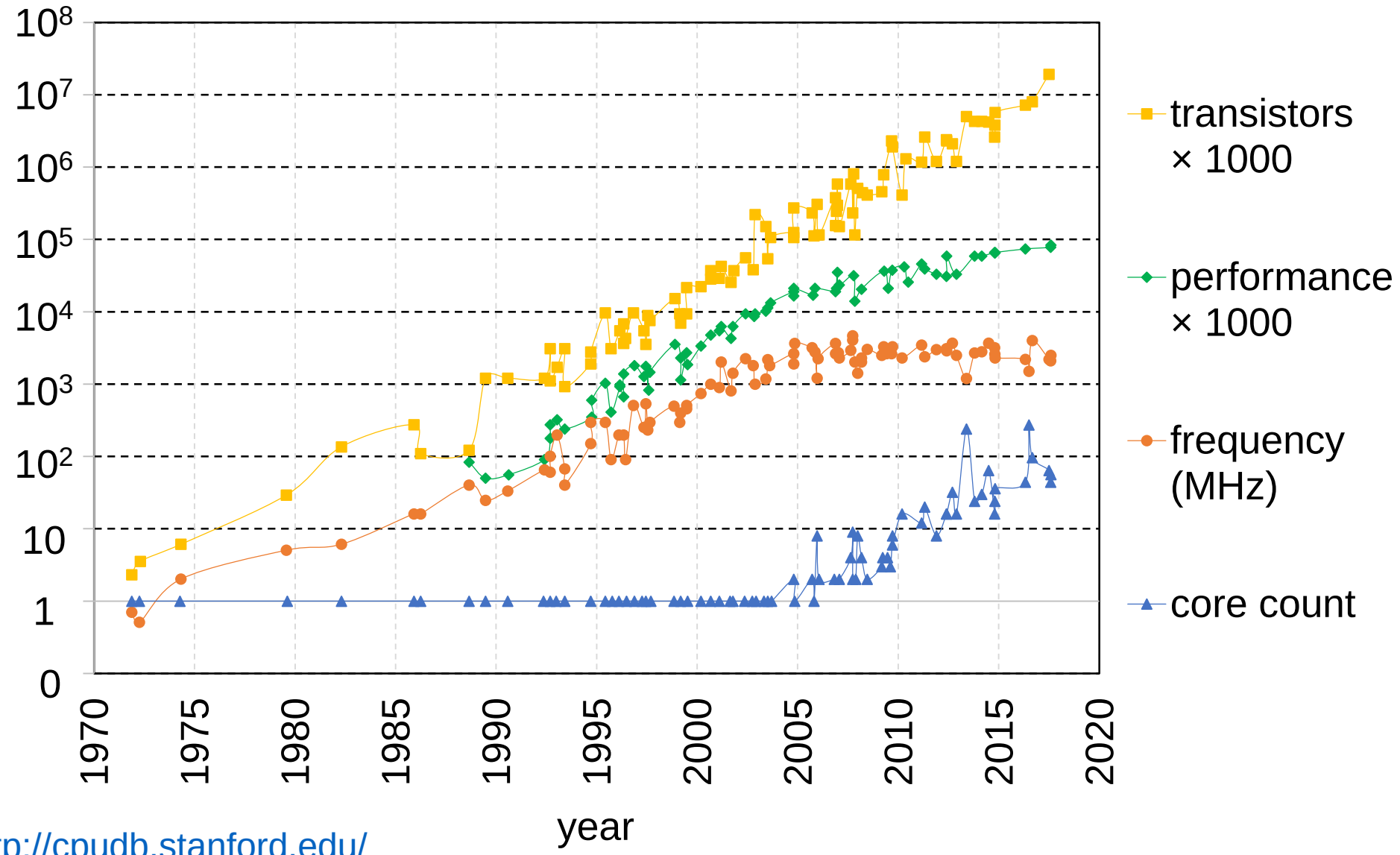


Size ↓ K

Circuit Delay ↓ K

Switching Charge ↓ K

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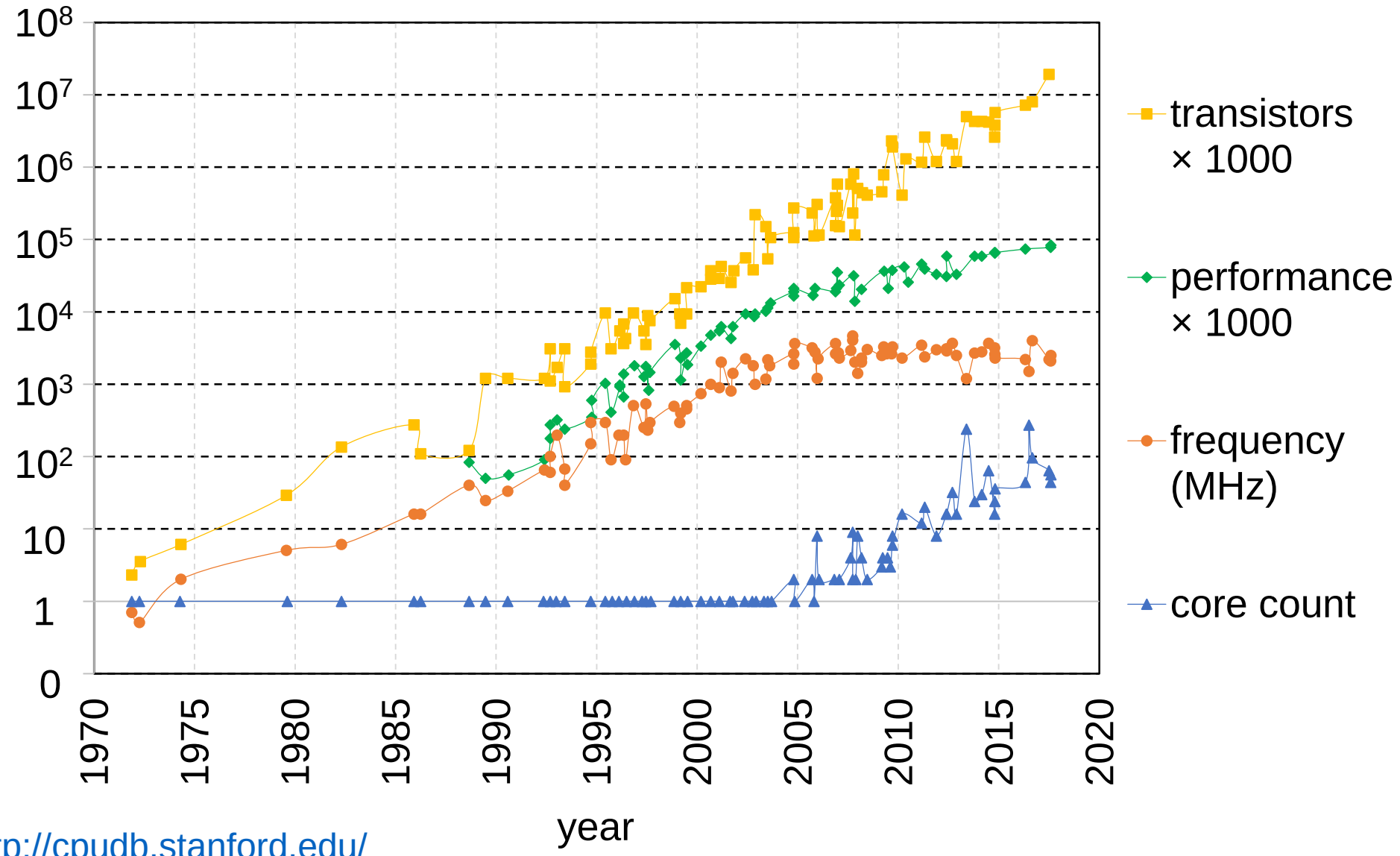


Size ↓ K

Circuit Delay ↓ K

Switching Charge ↓ K

Voltage ↓ K

http://cpudb.stanford.edu/

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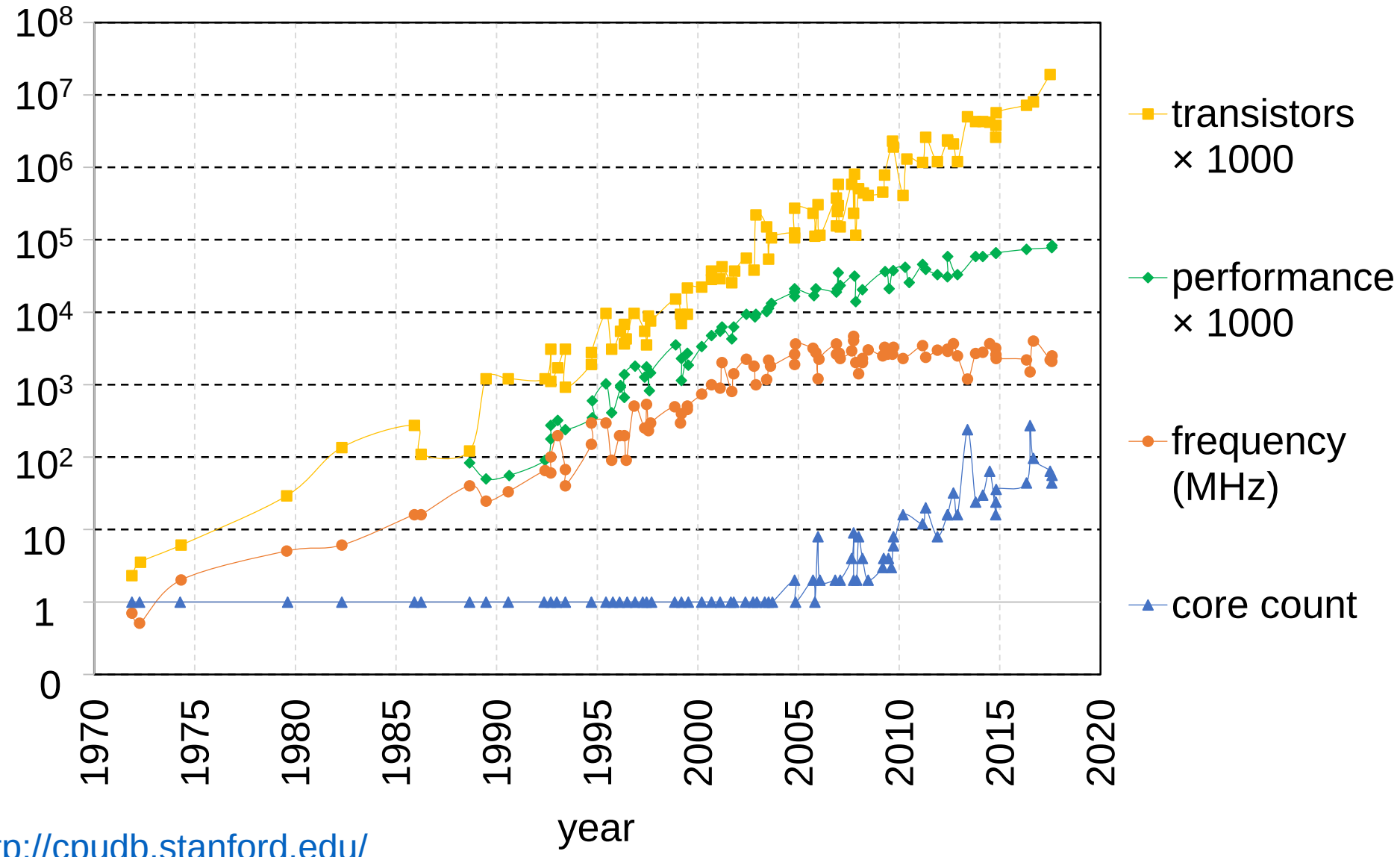


| | |
|---|---|
| Size | ↓ K |
| Circuit Delay | ↓ K |
| Switching Charge | ↓ K |
| Voltage | ↓ K |
| Area | ↓ $K^2$ |

http://cpudb.stanford.edu/

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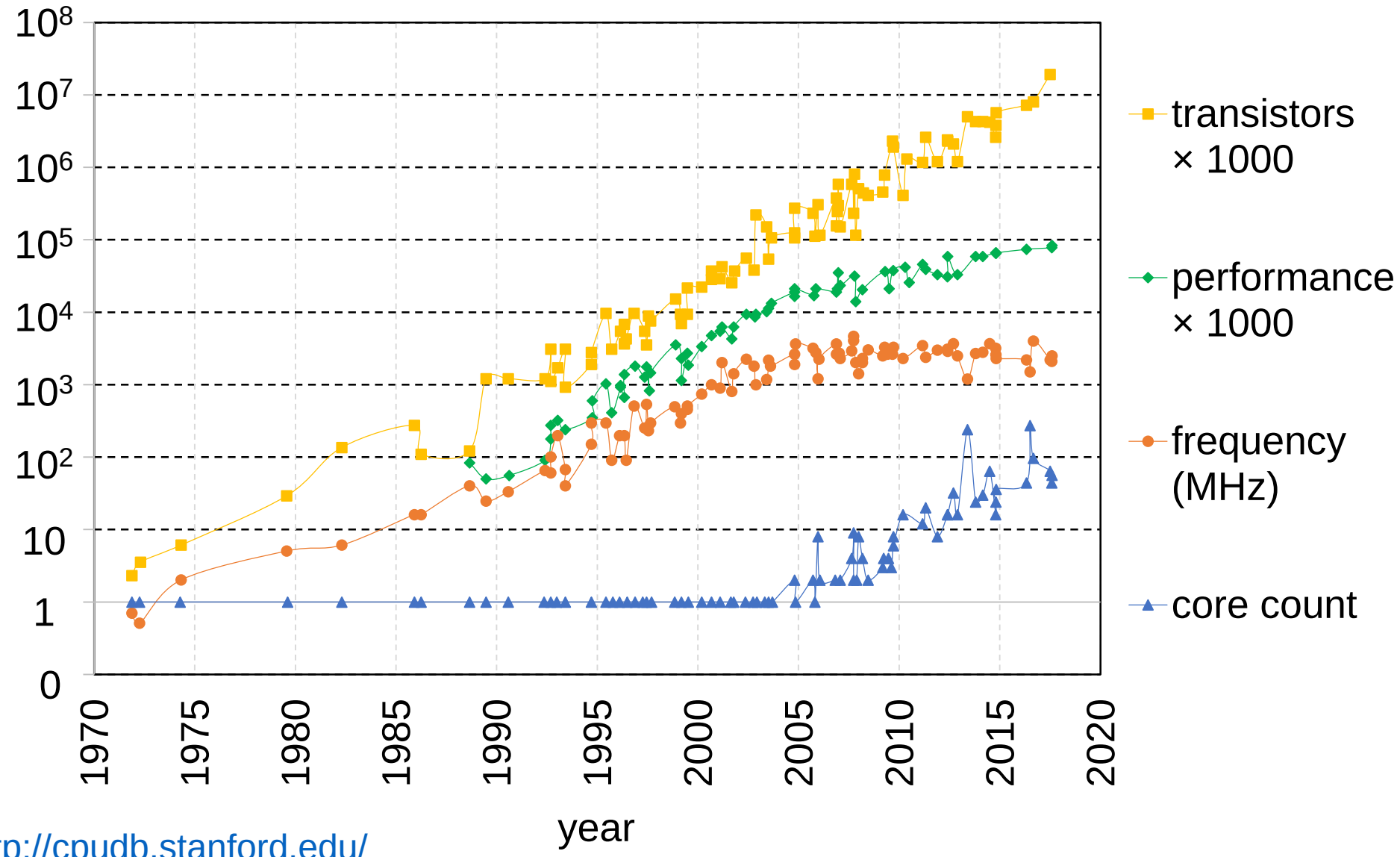


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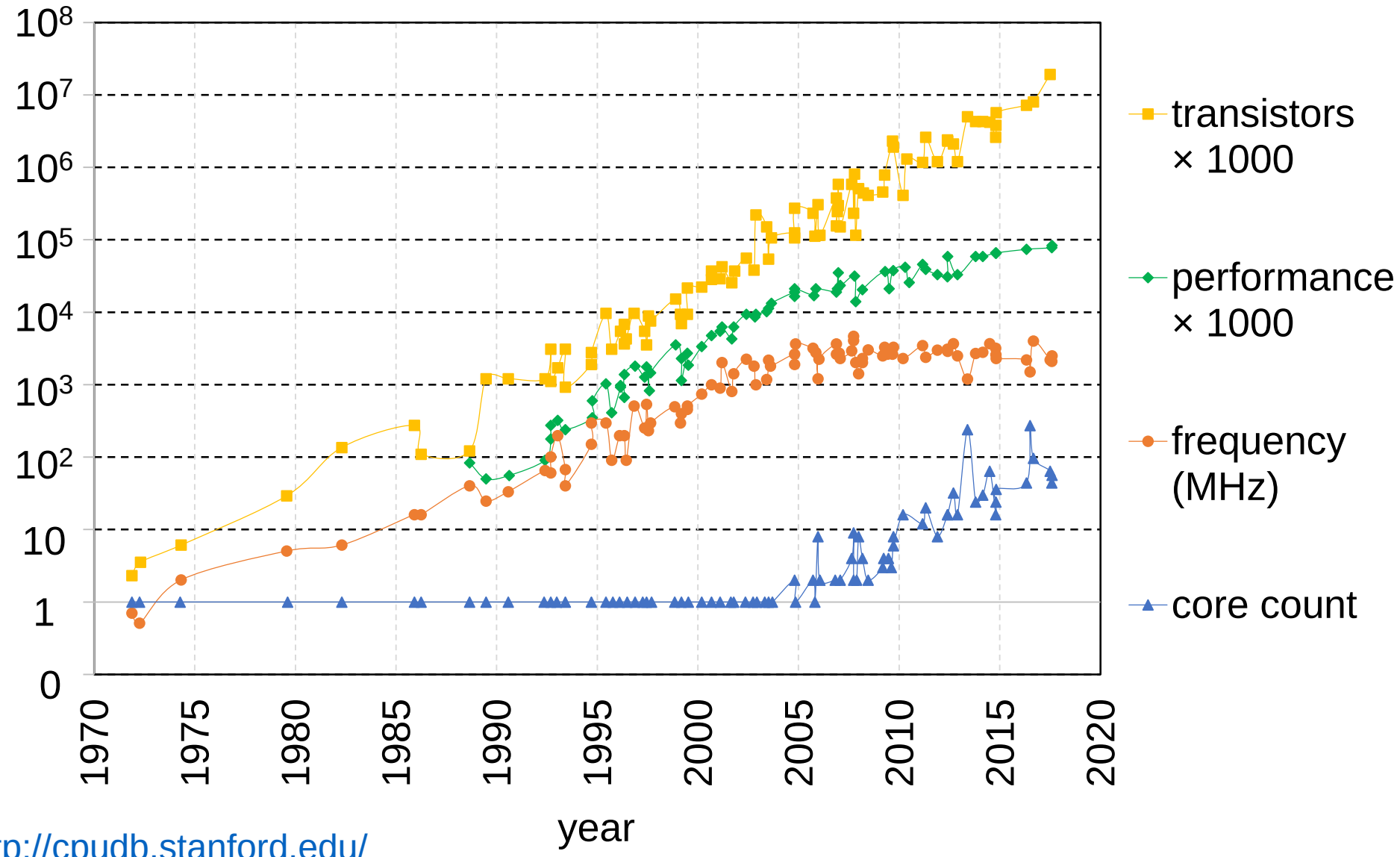


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| Power Density | |

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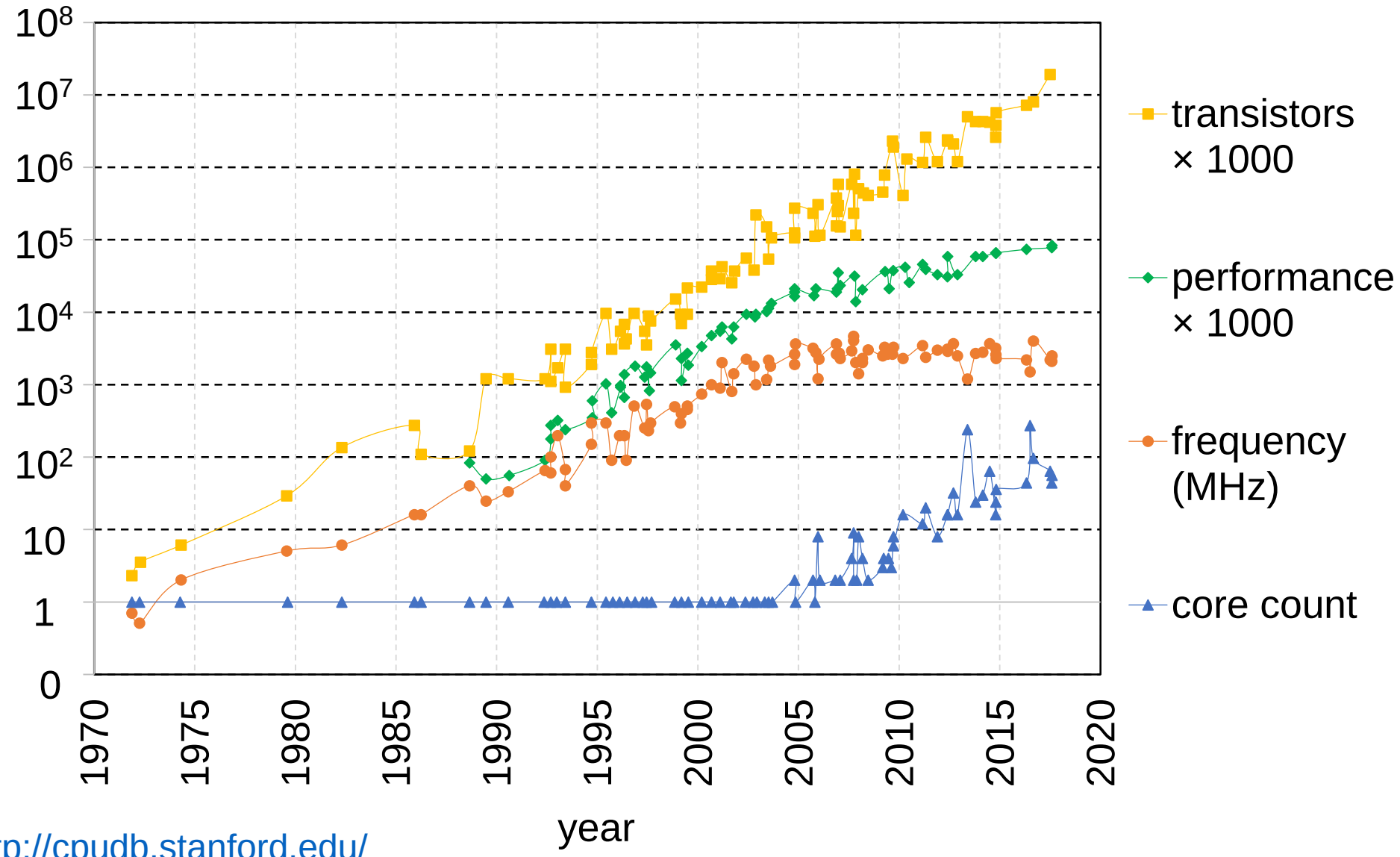


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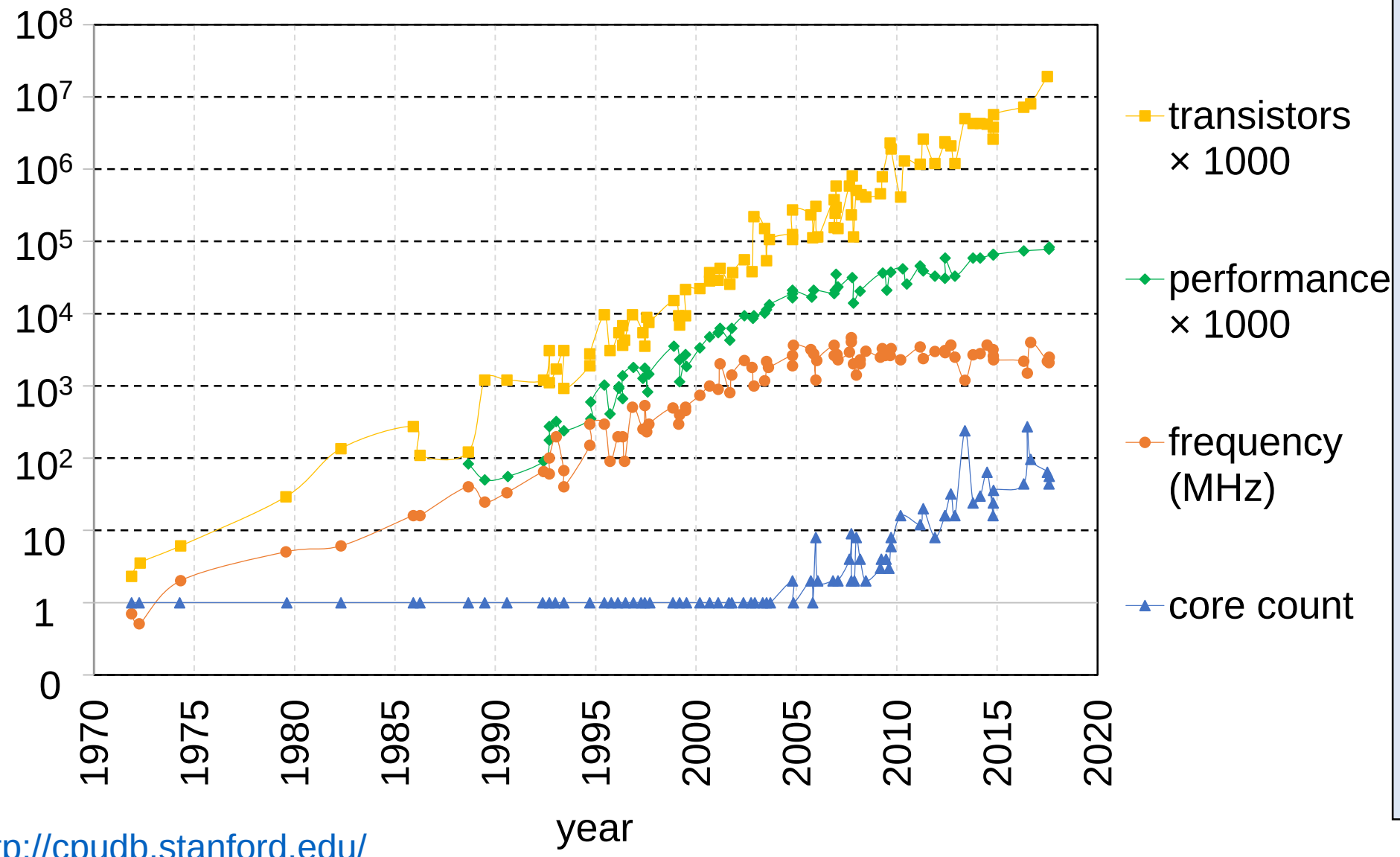


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## Dennard Scaling

| | |
|---|---|
| Size | ↓ K |
| Circuit Delay | ↓ K |
| Switching Charge | ↓ K |
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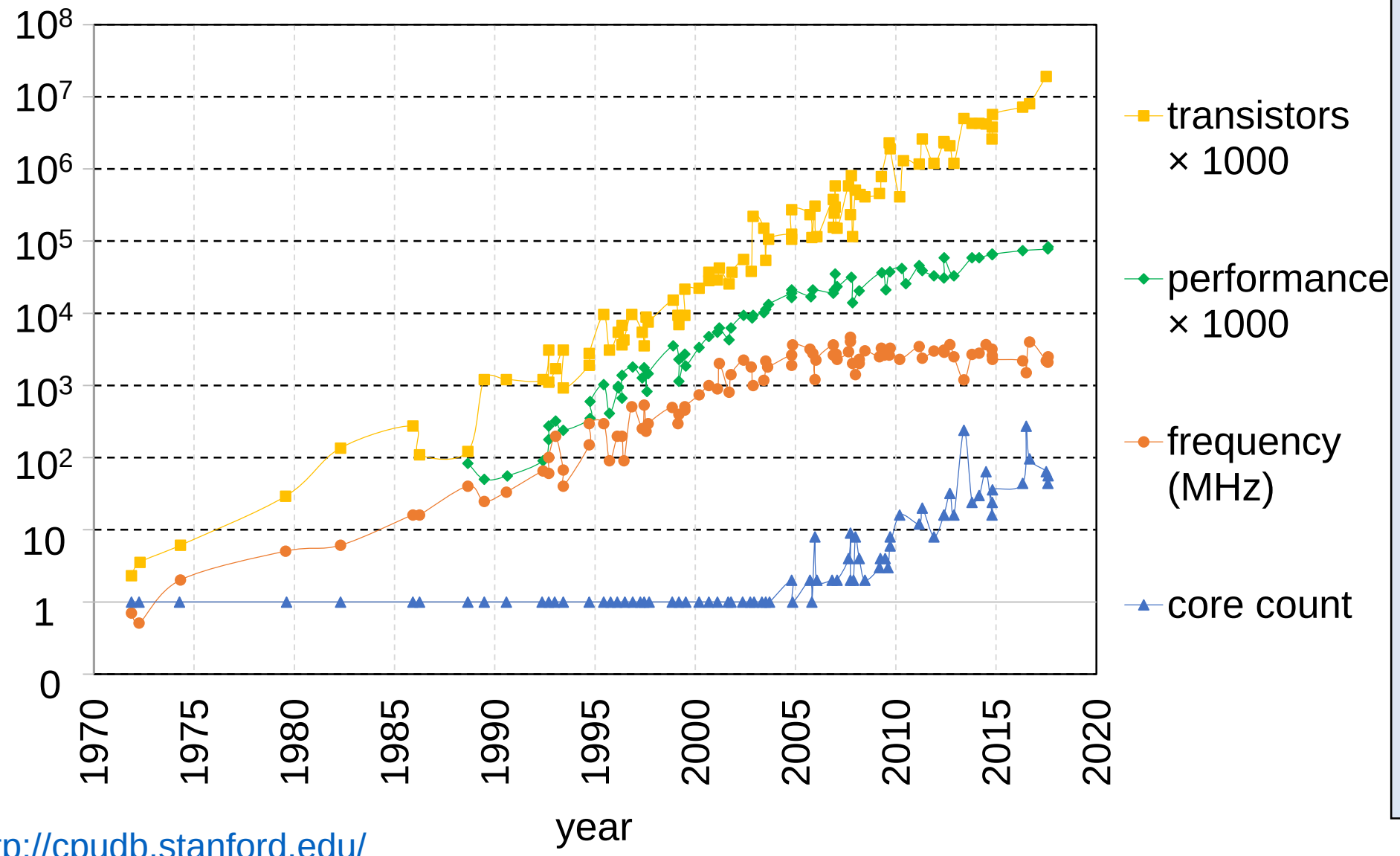


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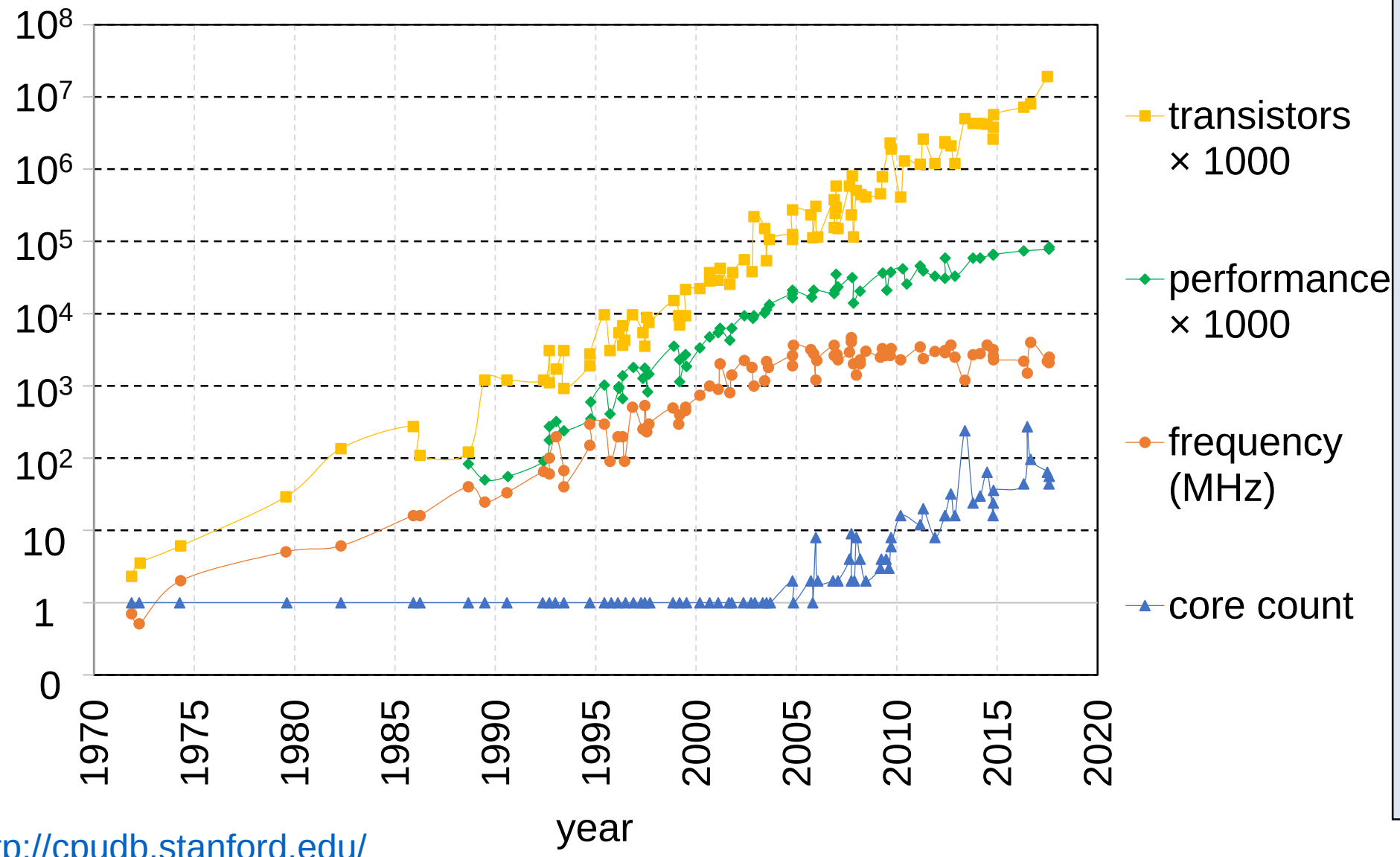


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| | |
|---|---|
| Size | ↓ K |
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| Switching Charge | ↓ K |
| Voltage | ✗ ↓ K |
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| Power | ↓ $K^2$ |
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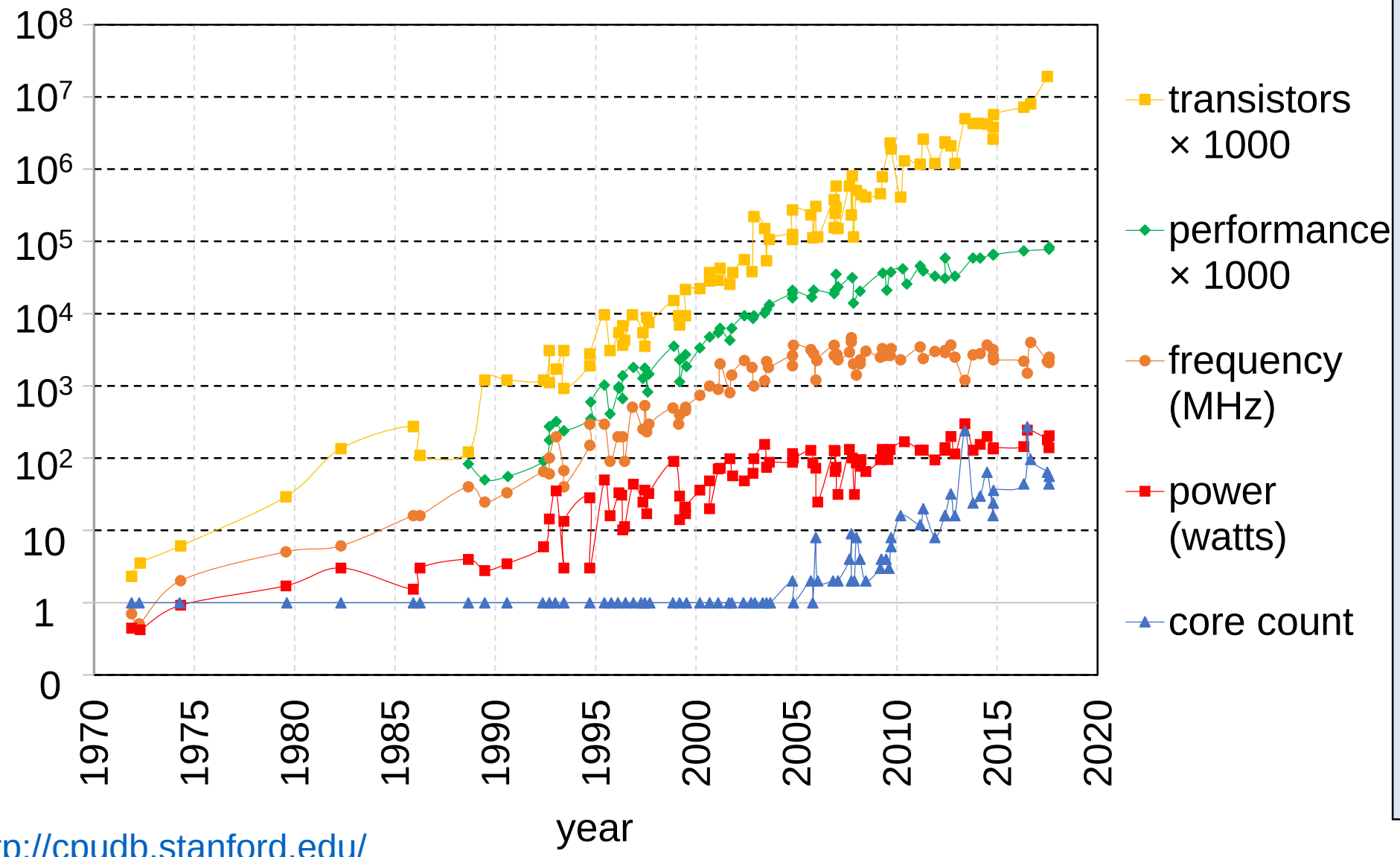


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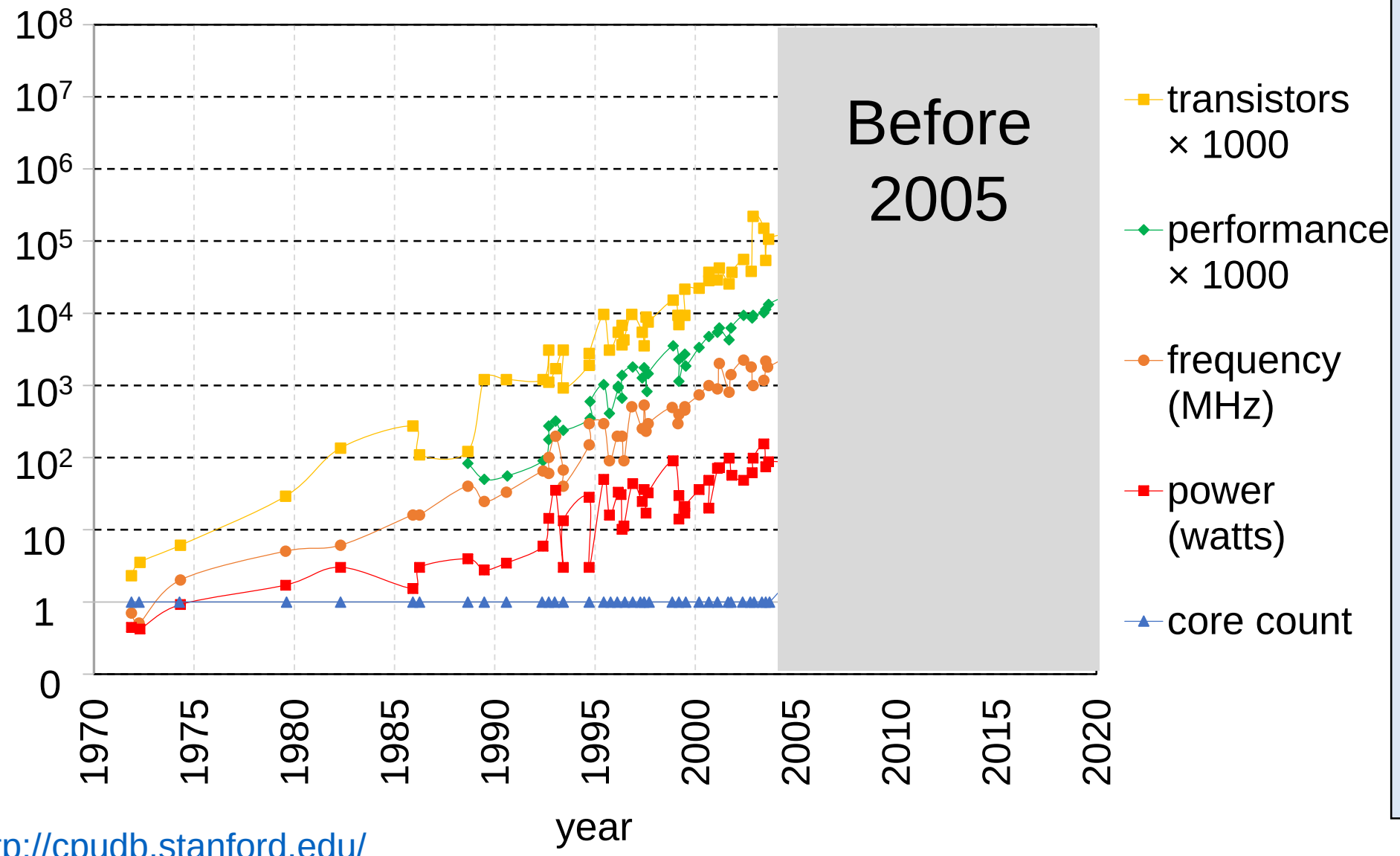


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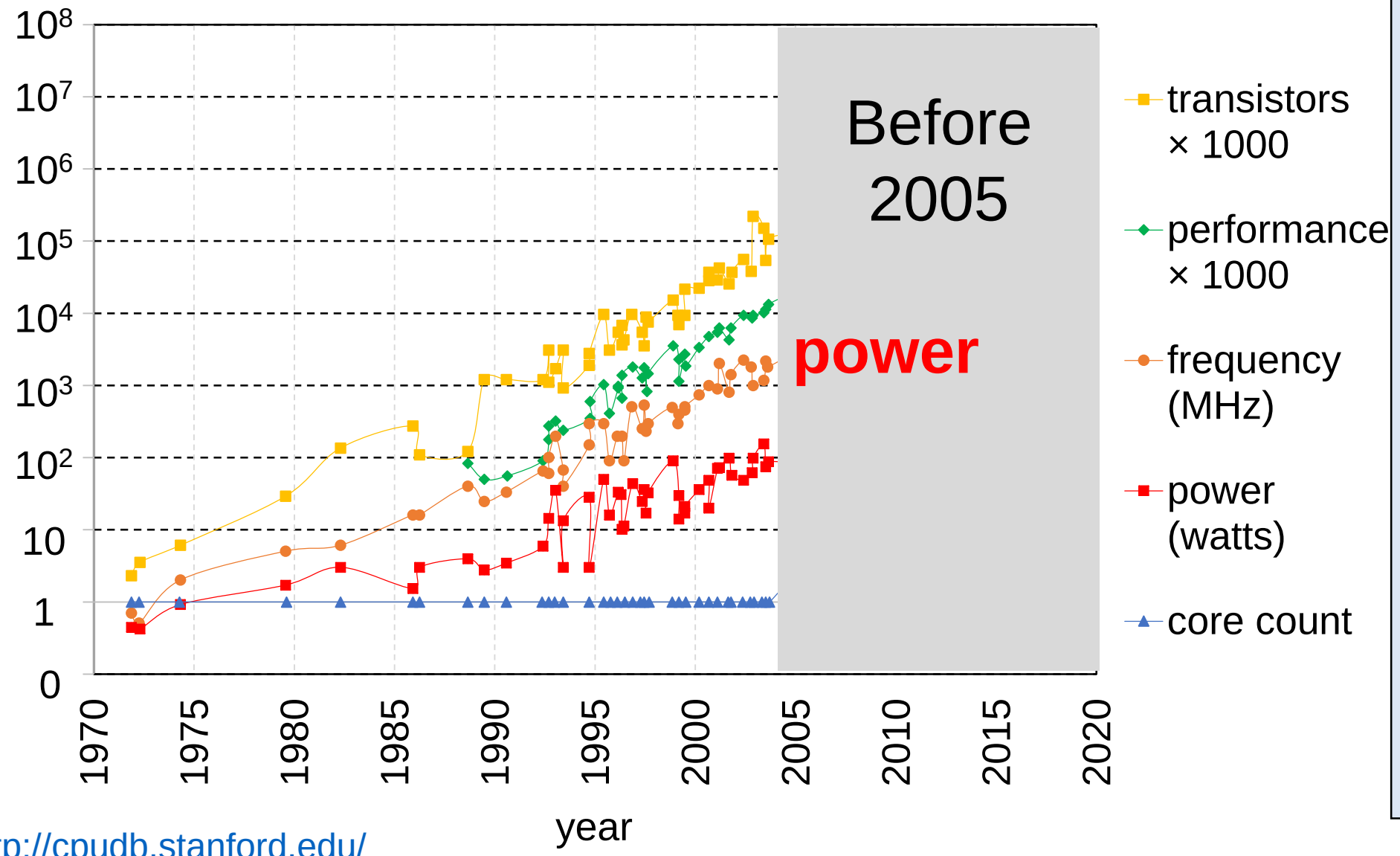


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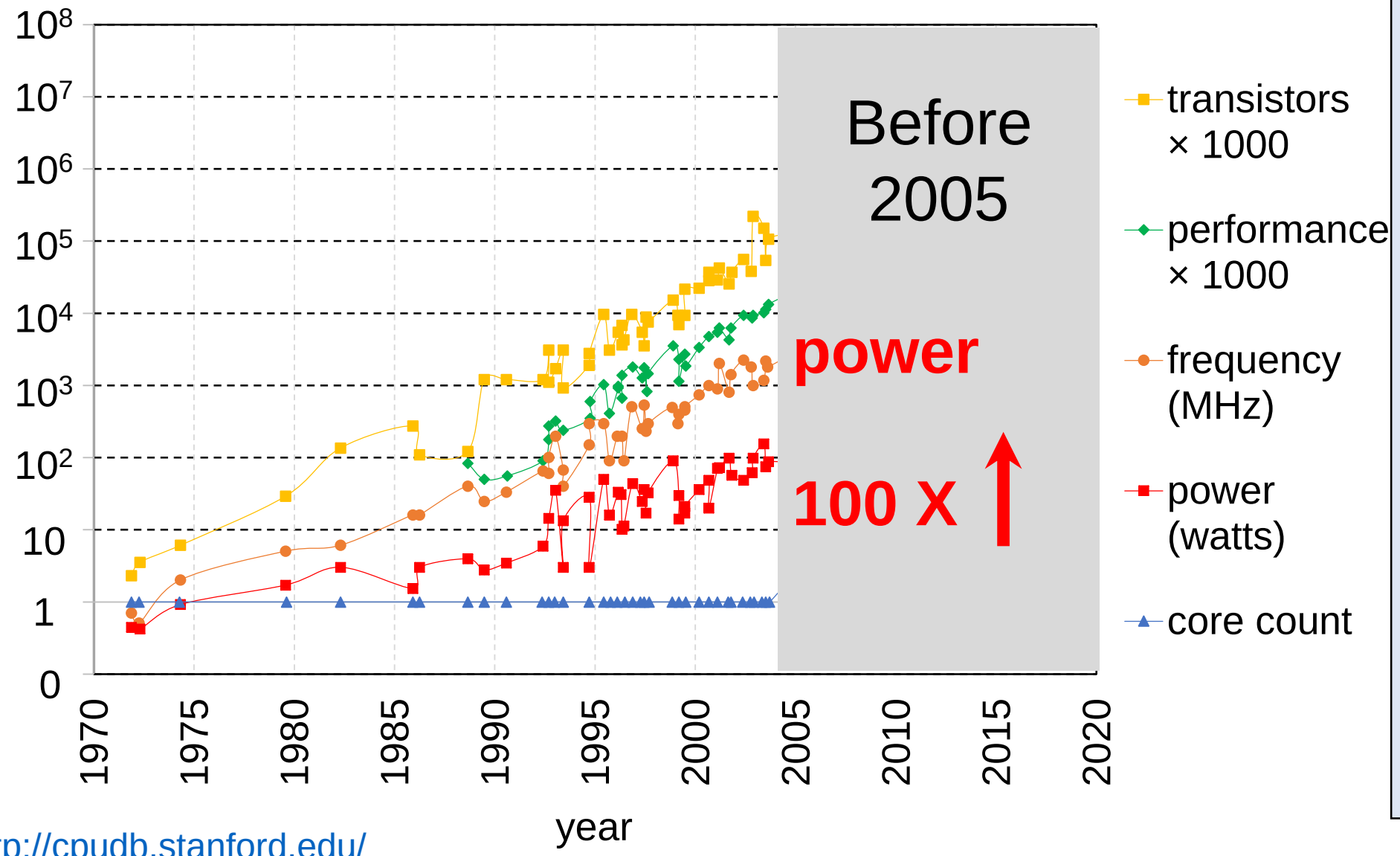


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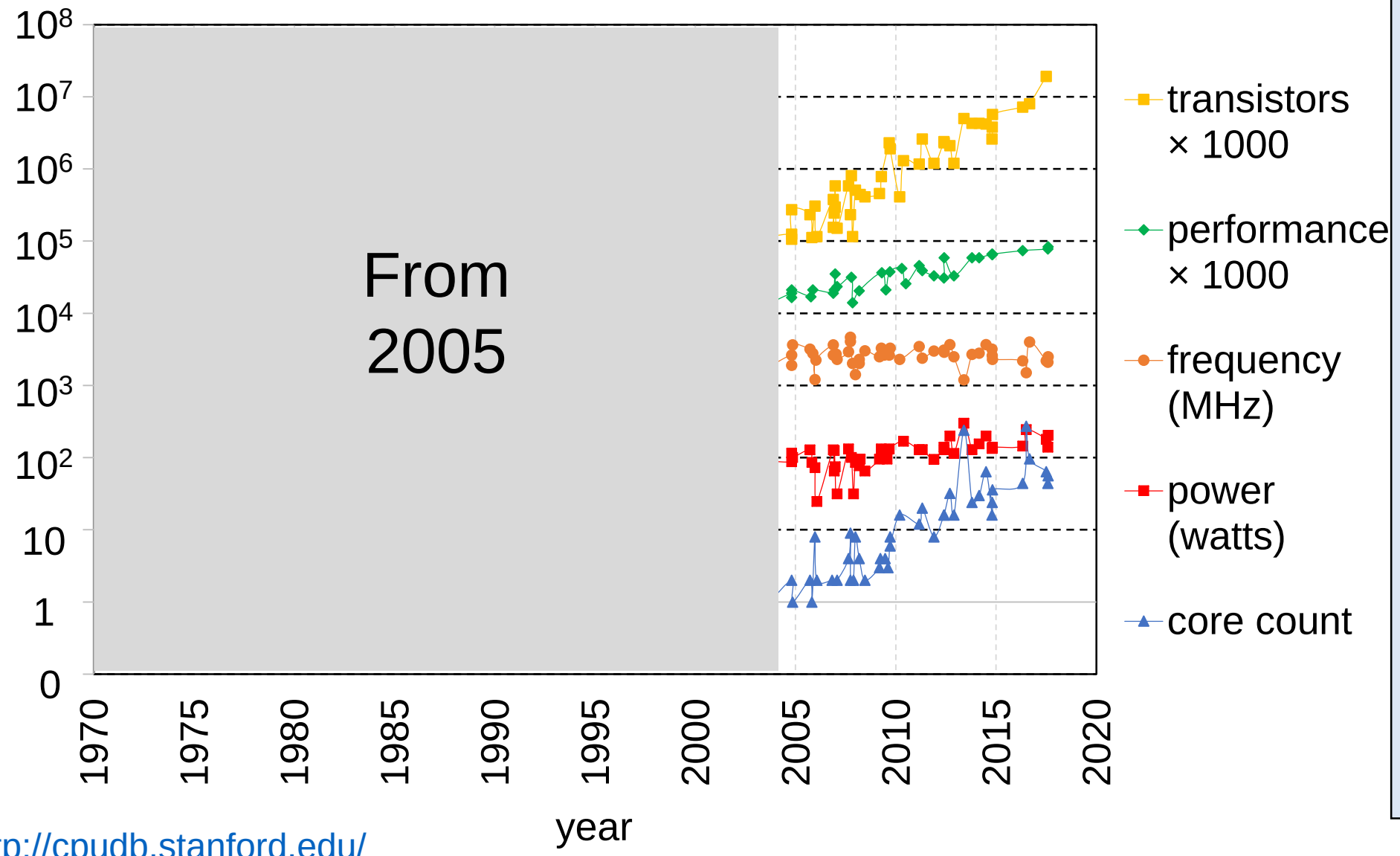


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# Consequences of Technology Scaling on Soft Error Reliability

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Smaller transistors → Reduced charge

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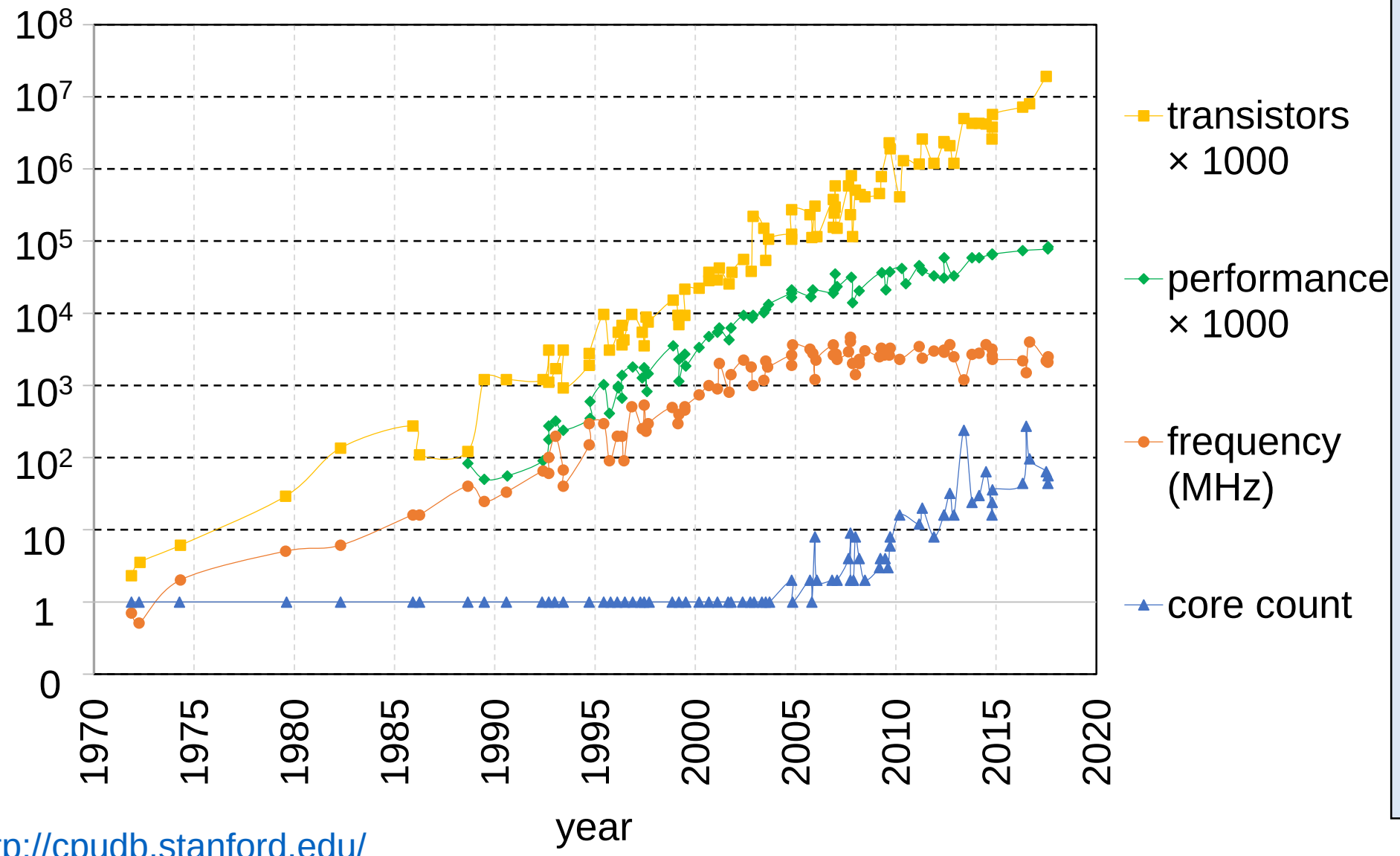


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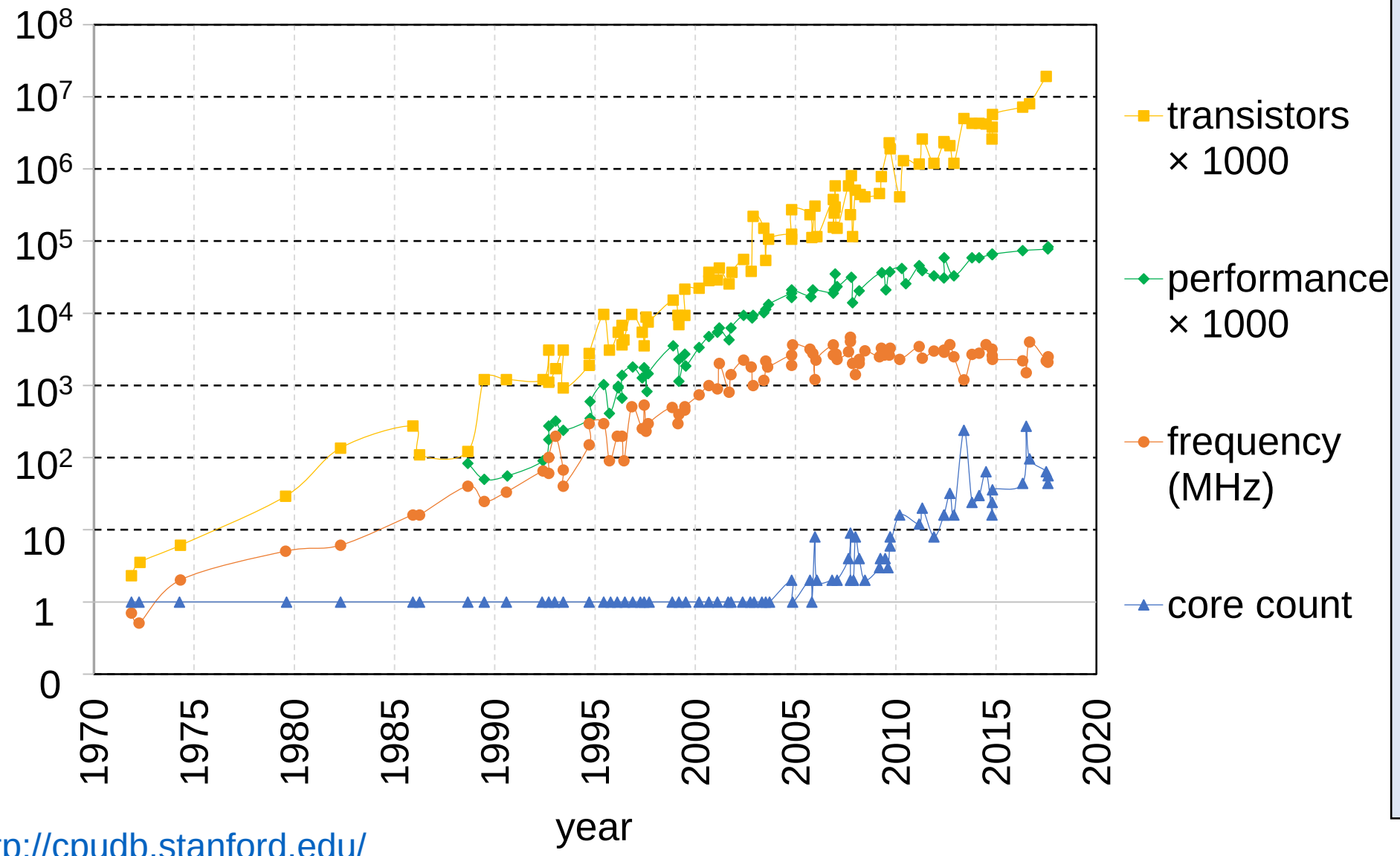


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Technology scaling

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Smaller transistors → Reduced charge

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Technology scaling → Increased rate of soft errors

# Modern Processors are Increasingly Vulnerable to Soft Errors

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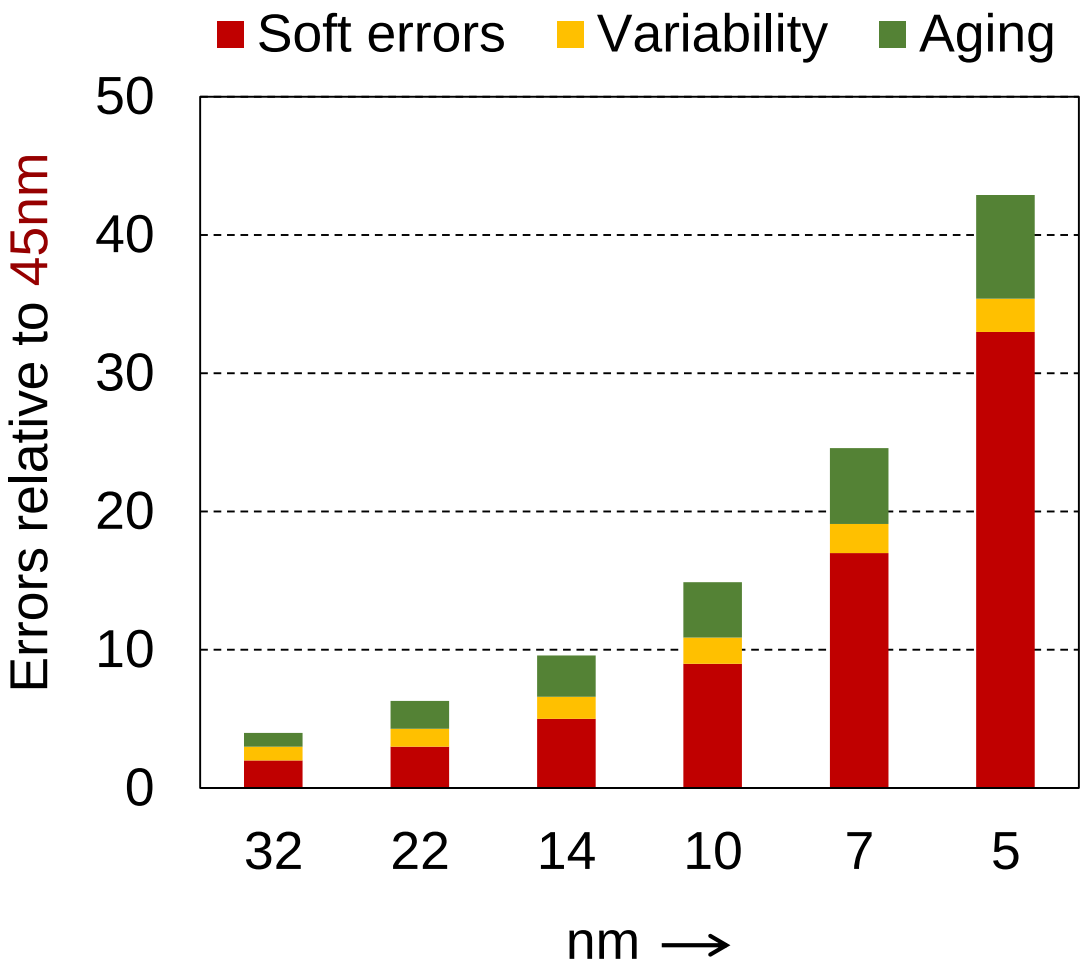


[Source: Inter-Agency Workshop on HPC Resilience at Extreme Scale, 2012]

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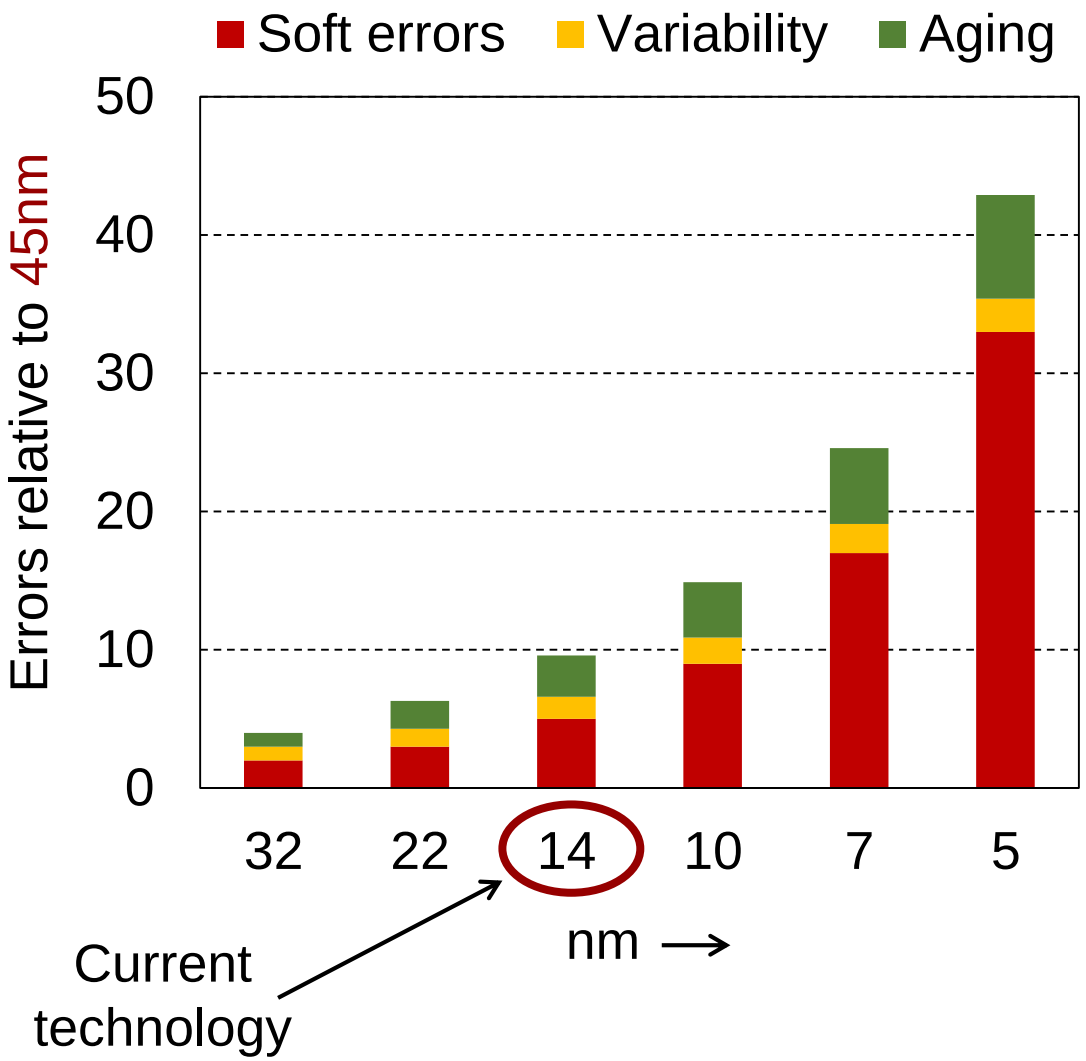


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# This Dissertation: Three New Contributions

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1. Exploiting core heterogeneity to improve reliability
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   [DSN 2020, Under review]

3. Precise Runahead Execution: Improving performance and evaluating reliability
   [CAL 2019, HPCA 2020]

# Contribution #1 [HPCA 2017, TC 2018]

# Exploiting Core Heterogeneity to Improve Reliability

# Benefits of Heterogeneous Multicores

- Multiple core types

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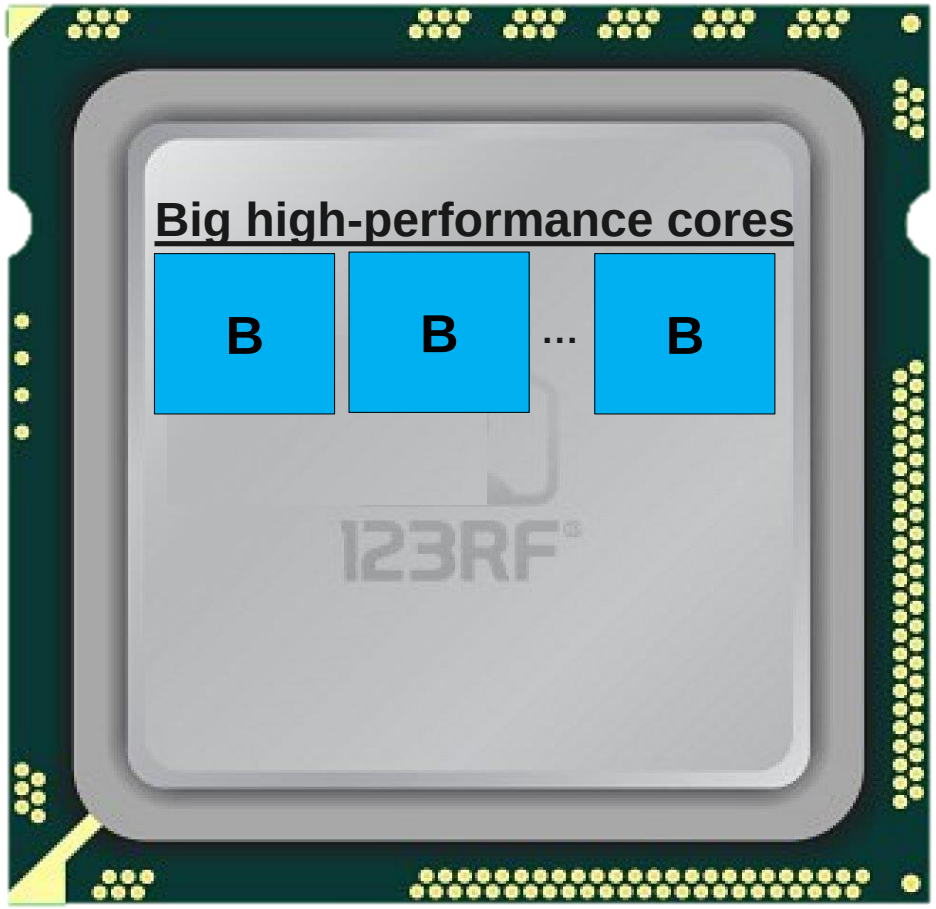

# Benefits of Heterogeneous Multicores

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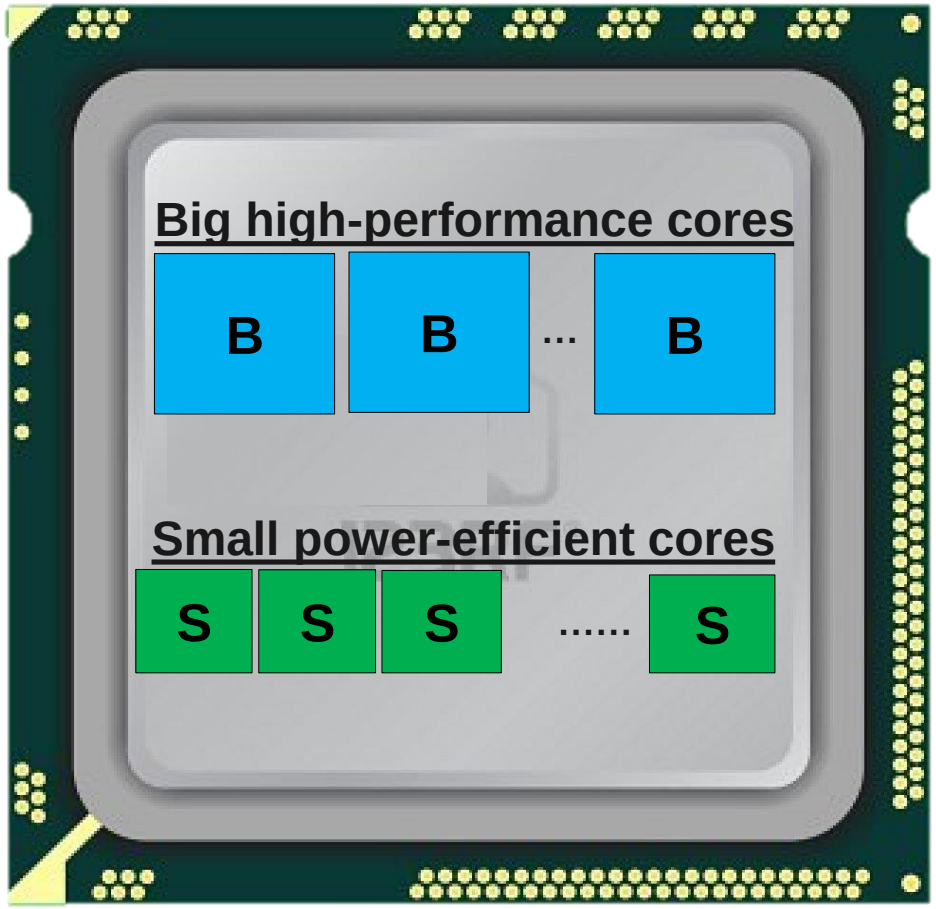
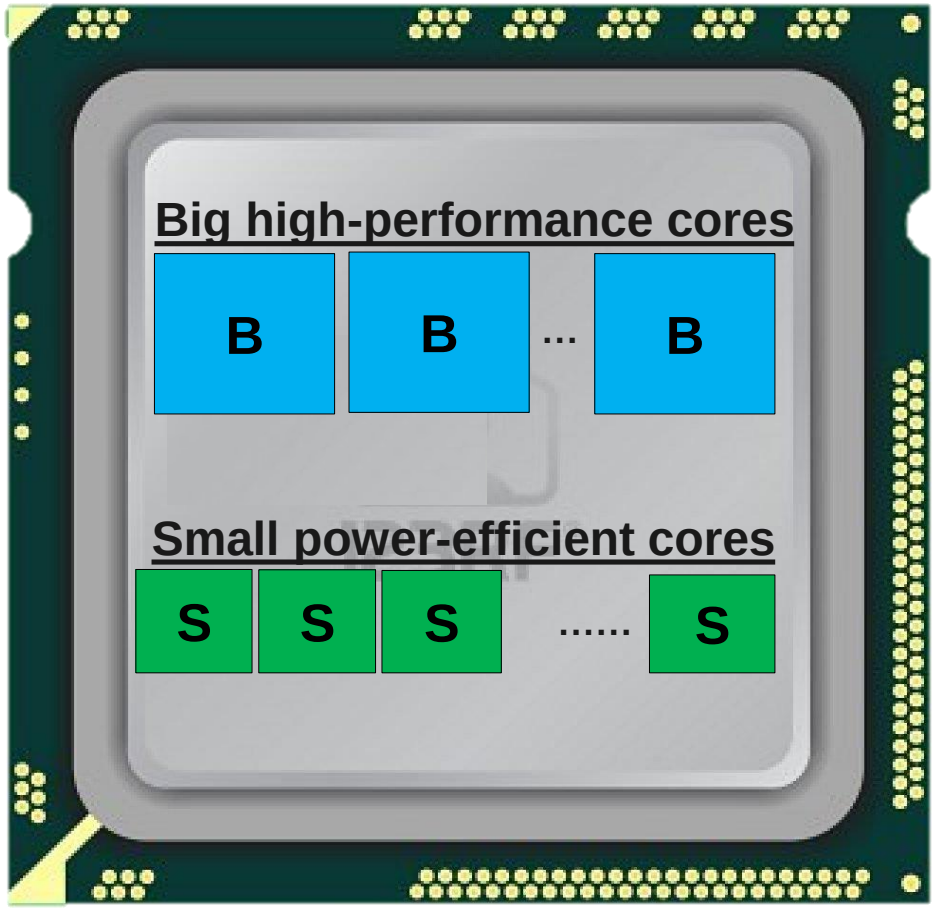


# Benefits of Heterogeneous Multicores

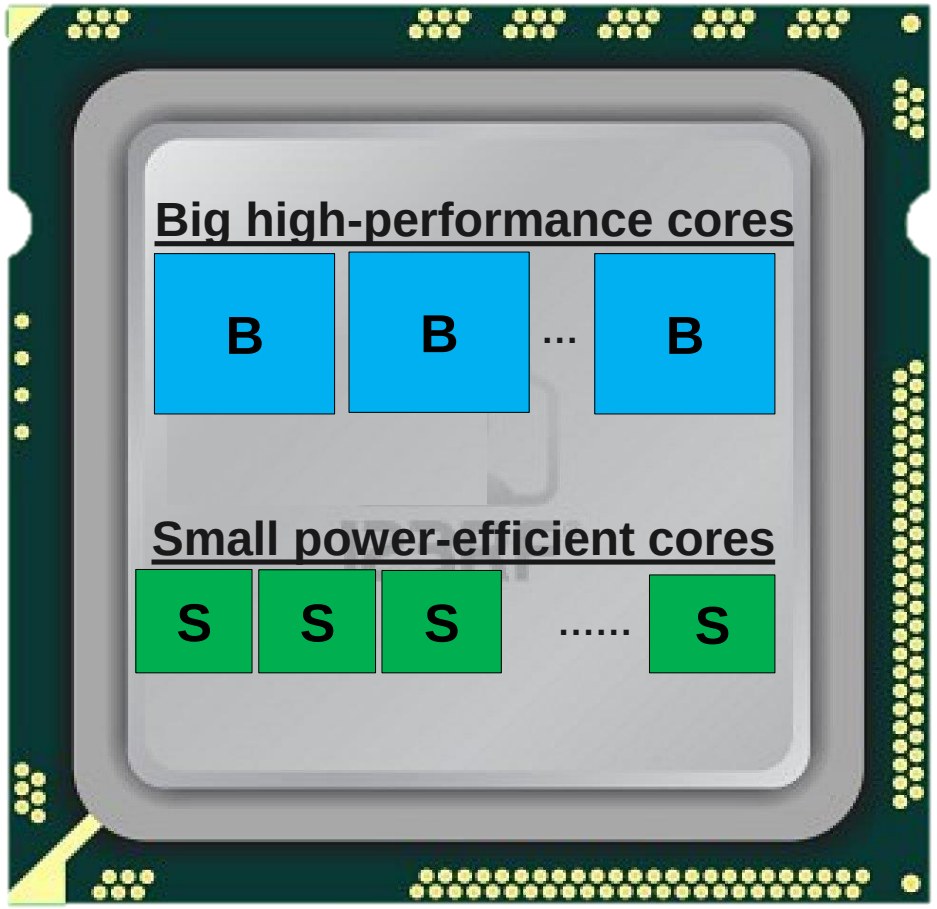
- Multiple core types
- Well-established power benefits*




*[Kumar et al. MICRO'03, ISCA'04]

# Benefits of Heterogeneous Multicores

- Multiple core types
- Well-established power benefits*
- Well-established scheduling techniques**




e.g. Big.LITTLE and Kal-El

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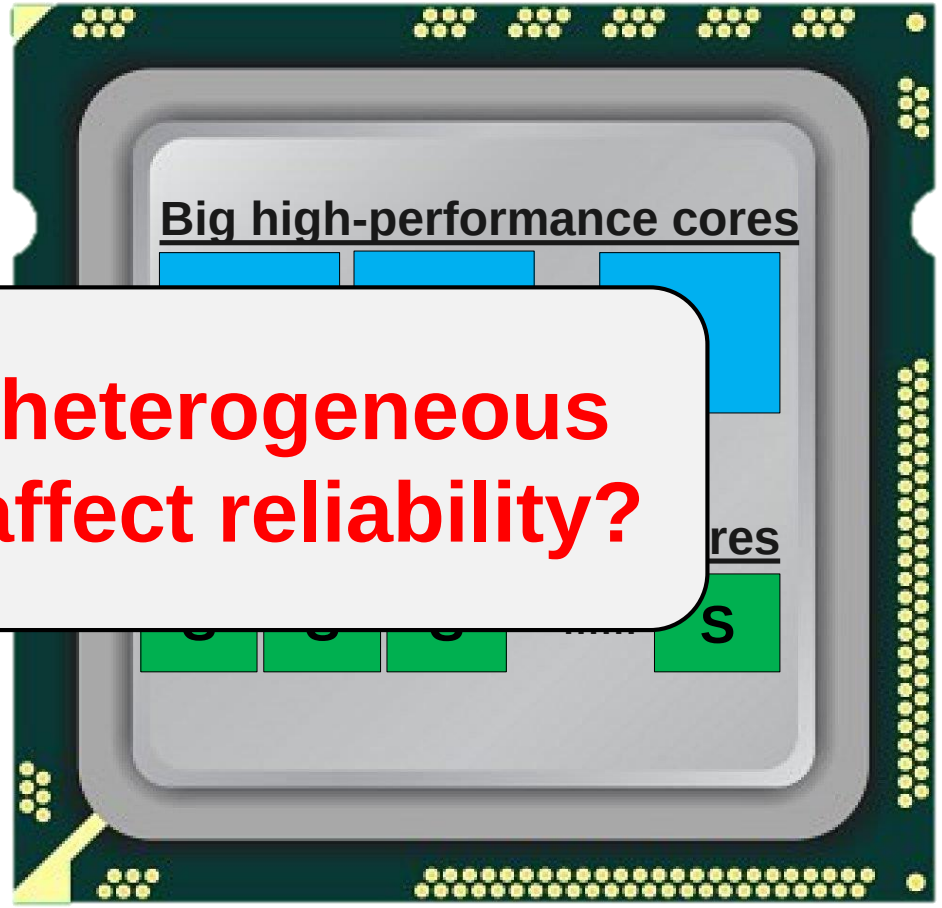


**No prior work → How heterogeneous chip-multiprocessors affect reliability?**

e.g. Big.LITTLE and Kal-El

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# ACE Analysis for Estimating Soft Errors

Processor bit

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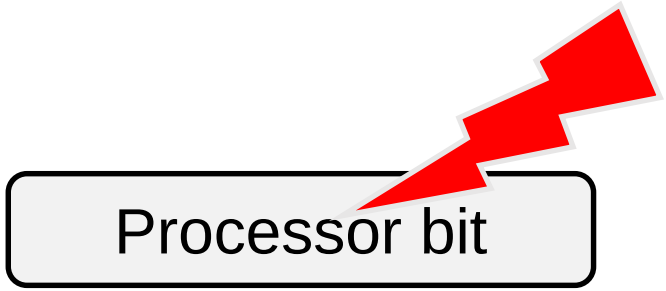

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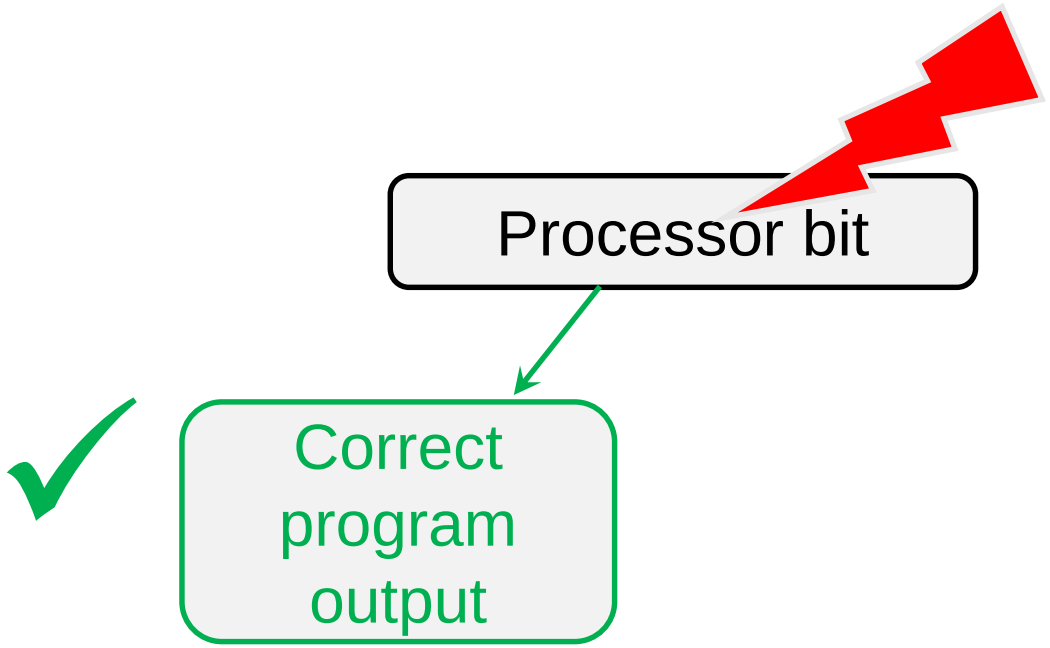

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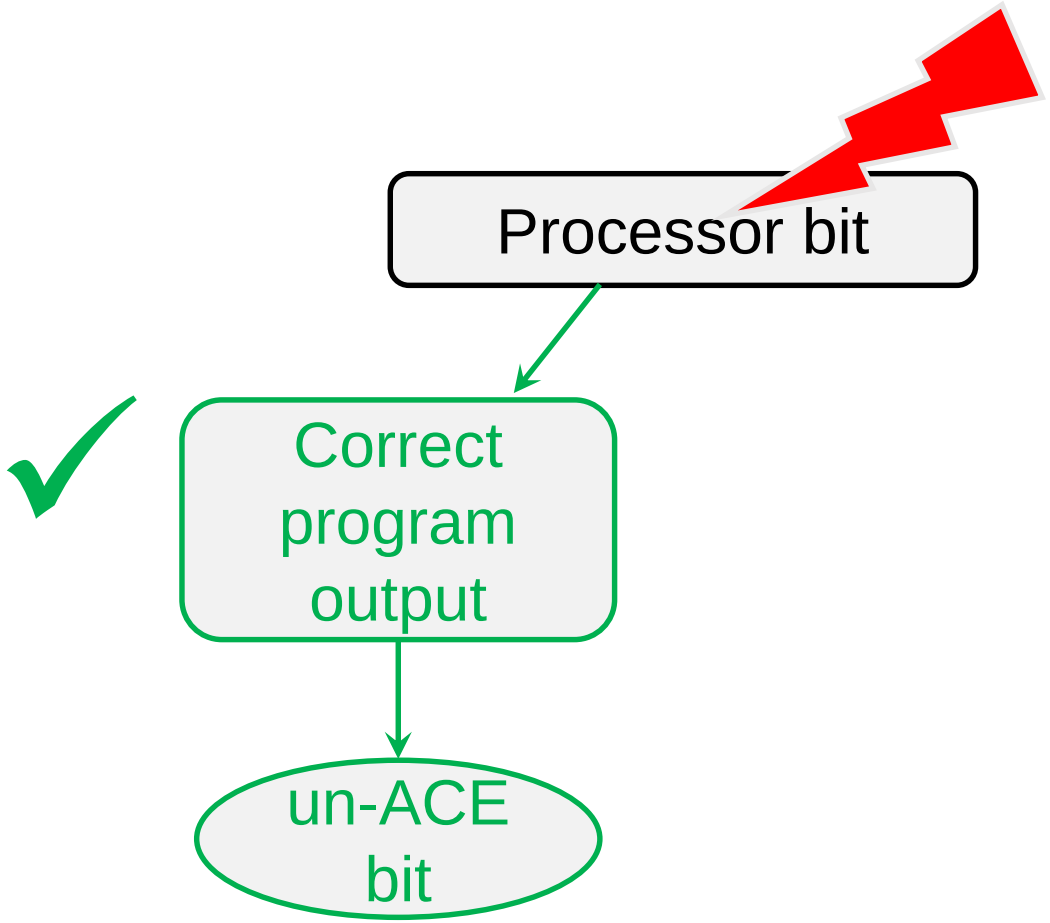


**ACE** →
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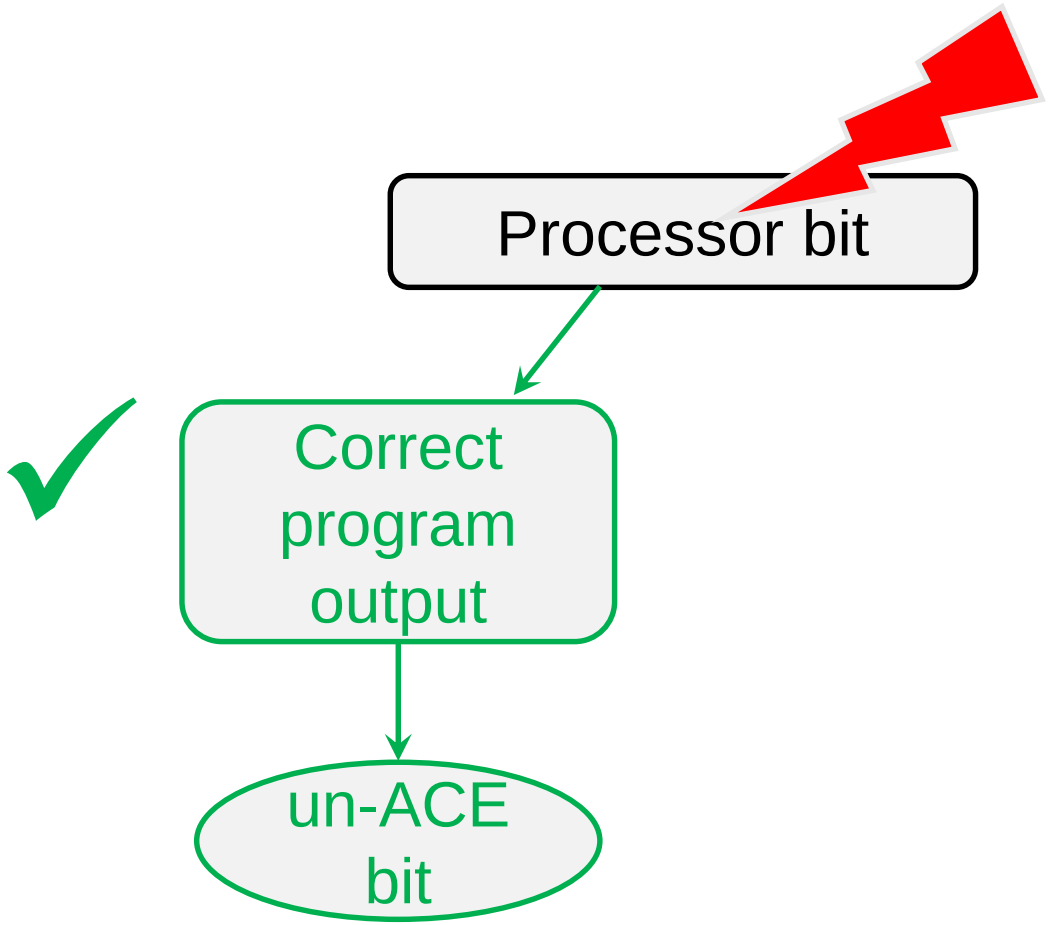


Branch predictor, wrong-path instructions

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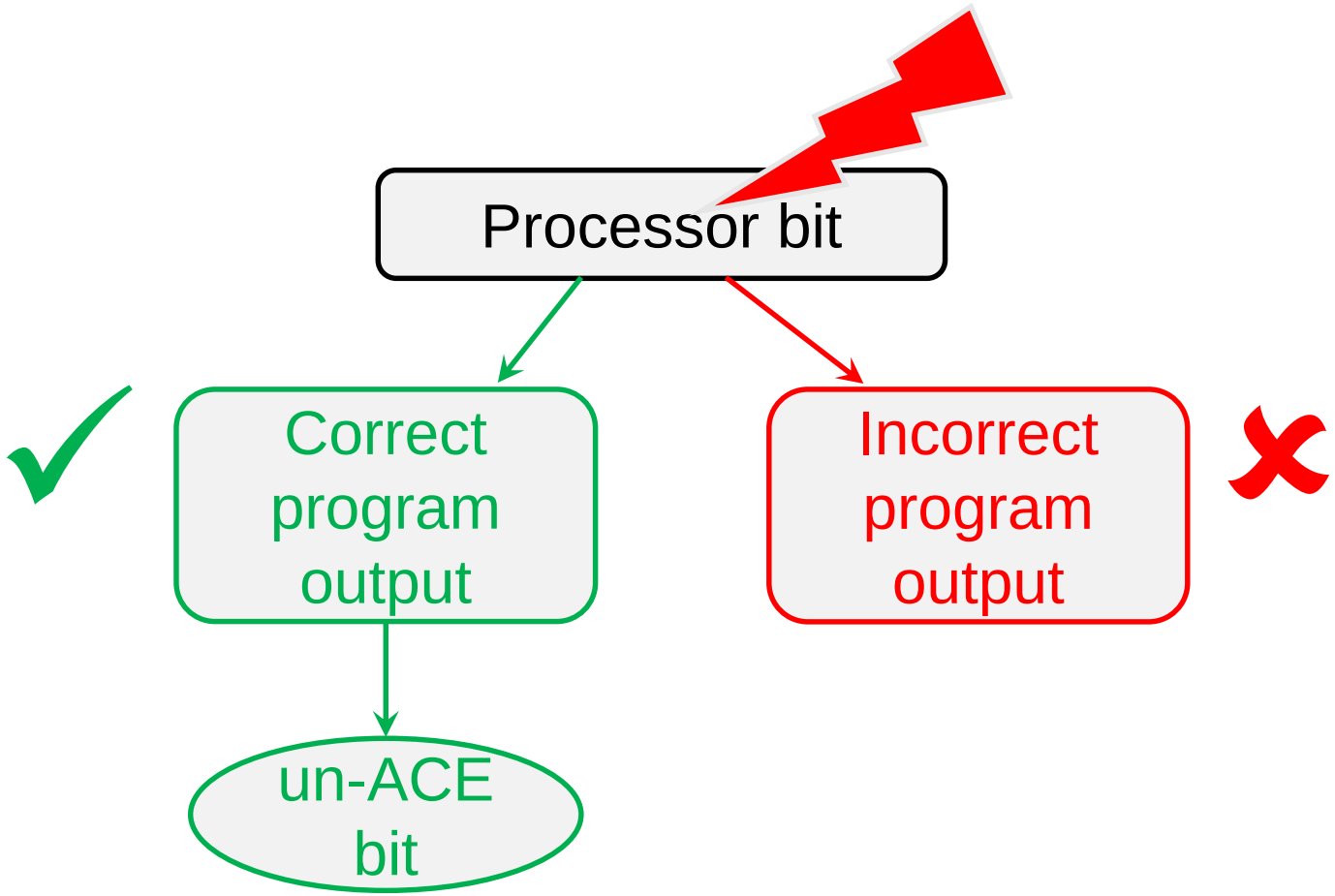


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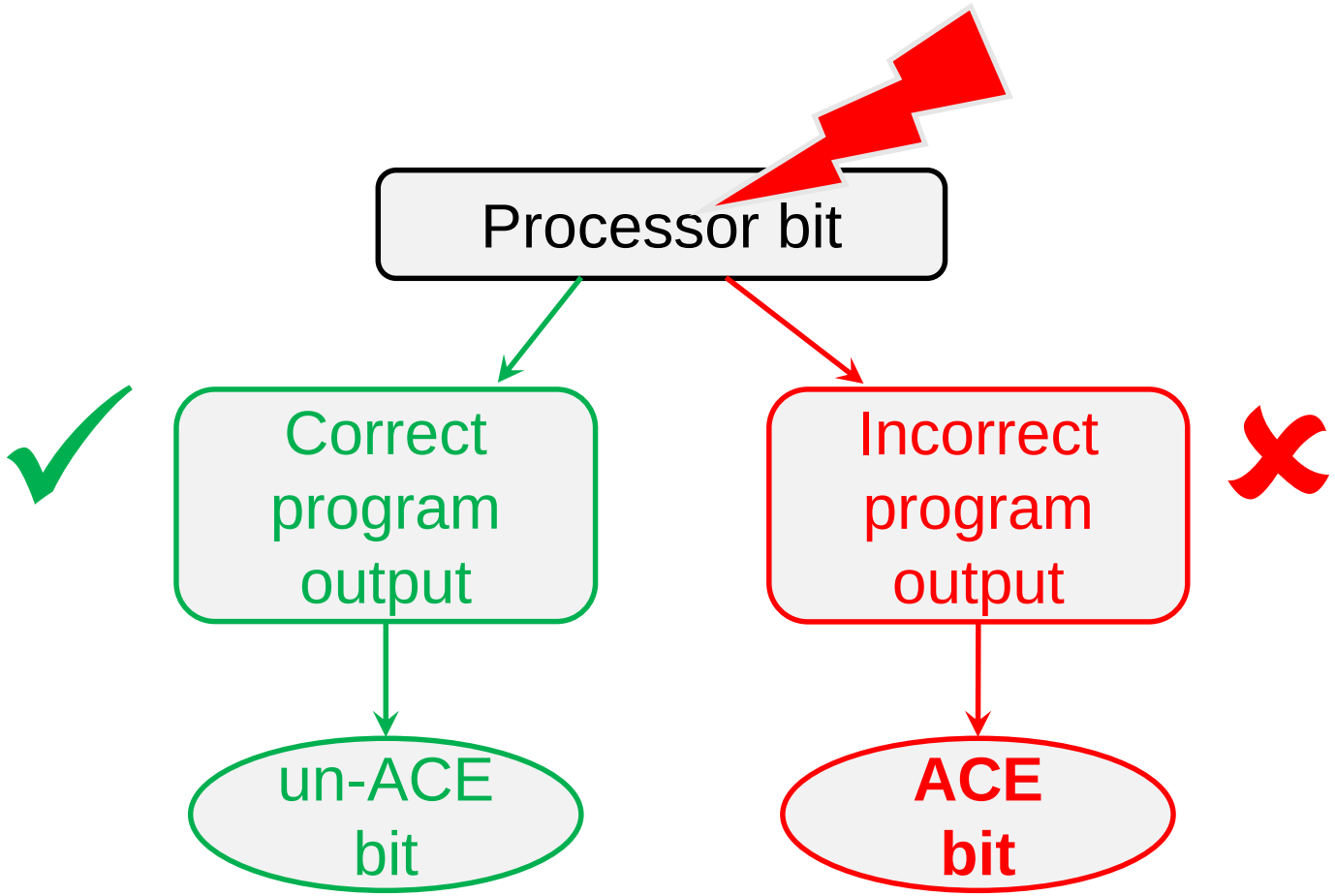


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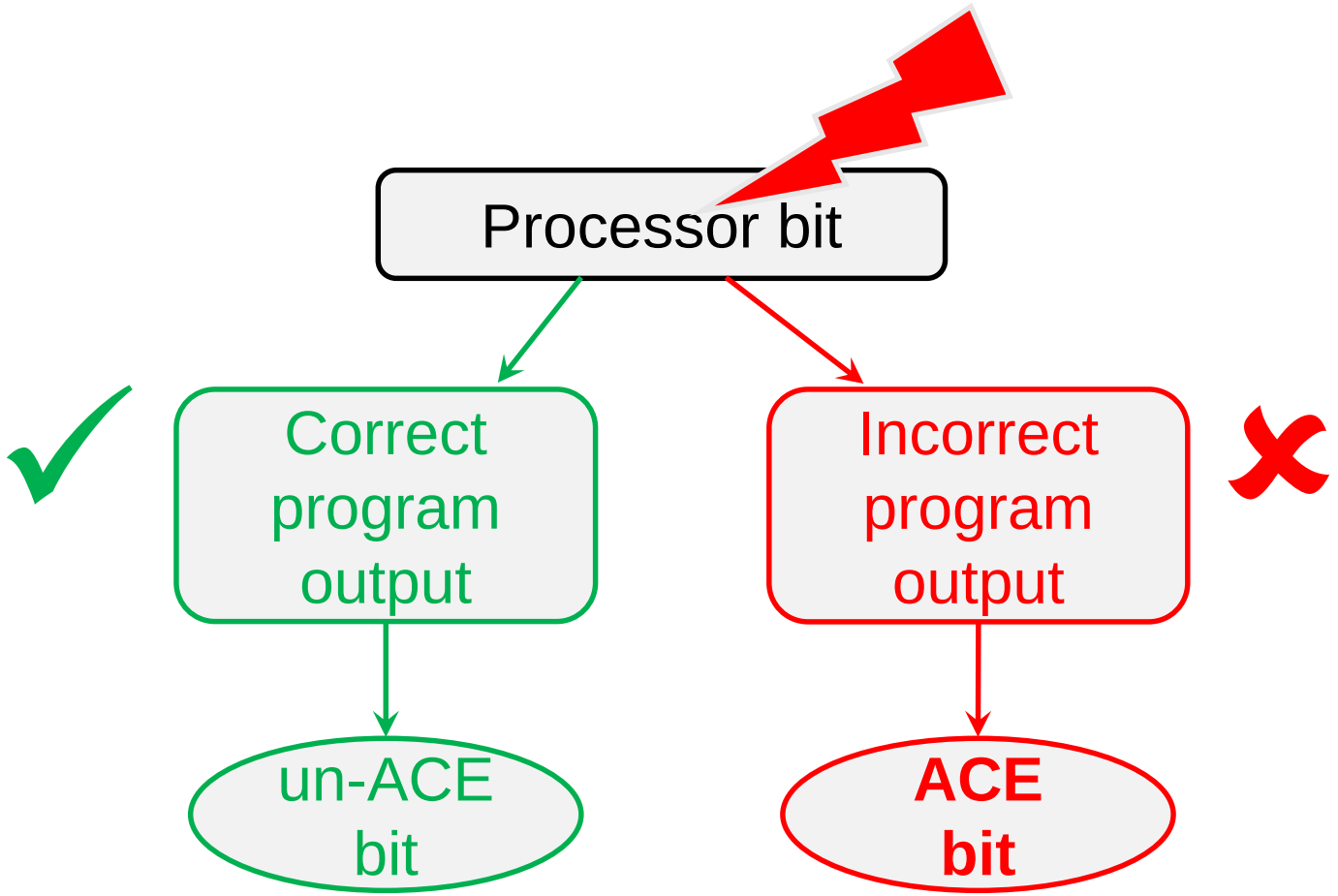


Branch predictor, wrong-path instructions

Program counter, correct-path instructions

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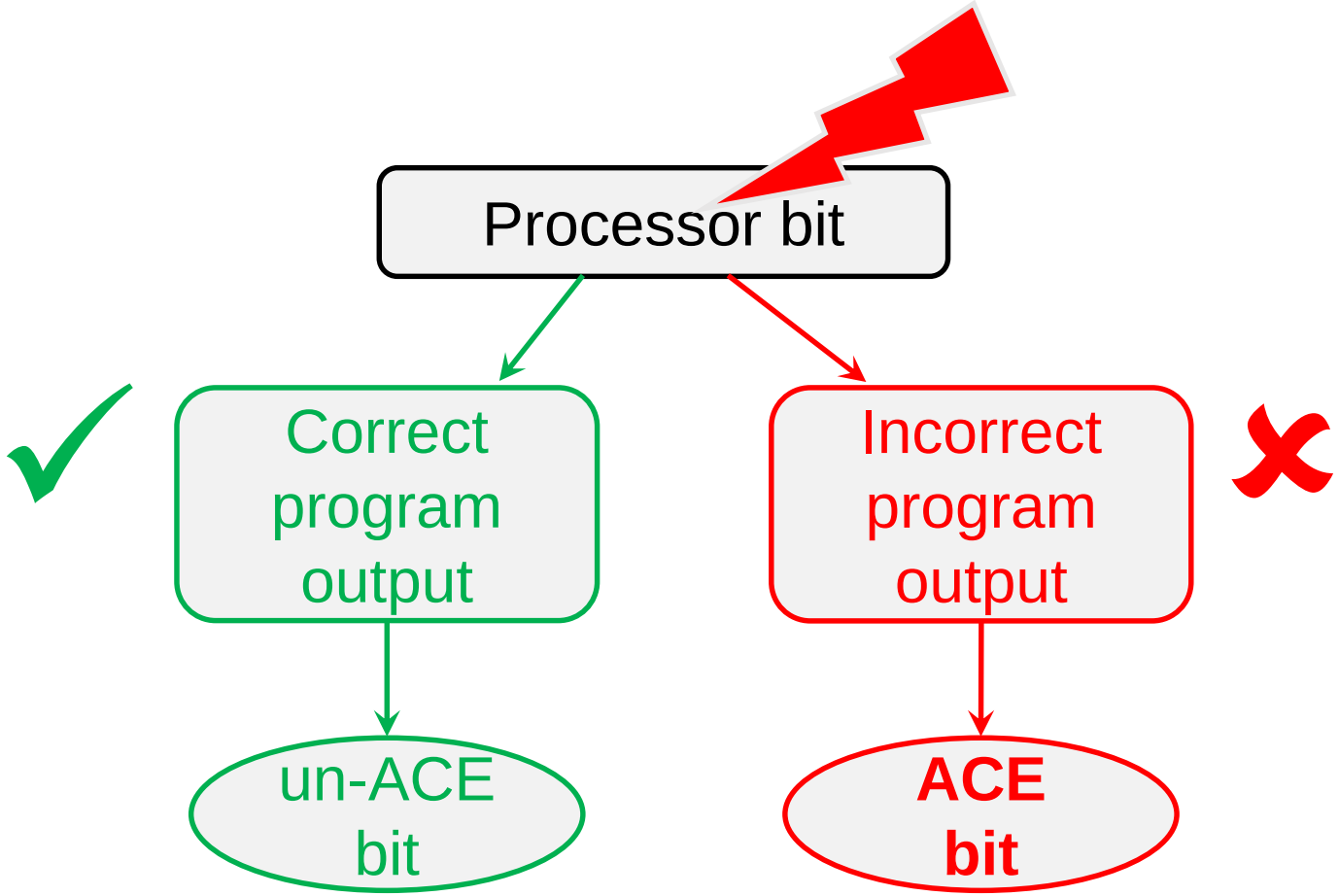


Branch predictor, wrong-path instructions

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**ACE** → **A**rchitecturally **C**orrect **E**xecution

**For correct program execution, all ACE bits must be correct**

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IFR = Probability of a soft error

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IFR = Probability of a soft error

For the same execution time

# ACE Analysis for Estimating Soft Errors

ACE Cycles = Total cycles a bit was ACE

ACE Bit Count (ABC) = Sum of ACE cycles for all committed instructions

Soft Error Rate (SER) = $\frac{\text{ABC}}{\text{Total cycles}} \times \text{IFR}$

IFR = Probability of a soft error

For the same execution time

ABC

SER

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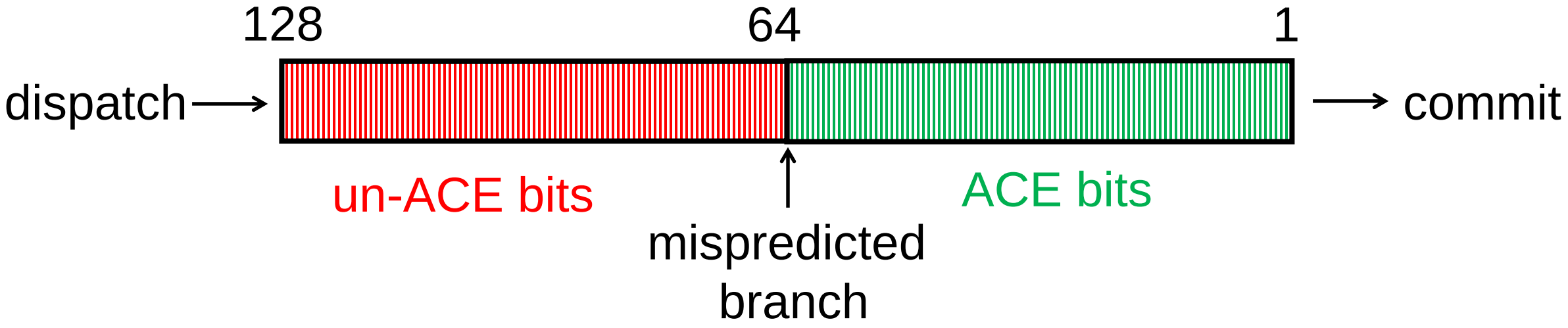

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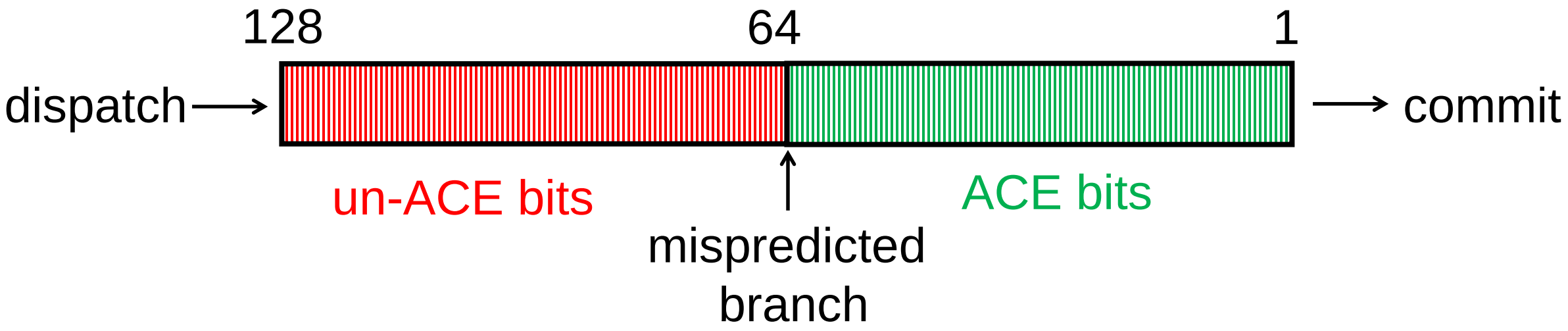


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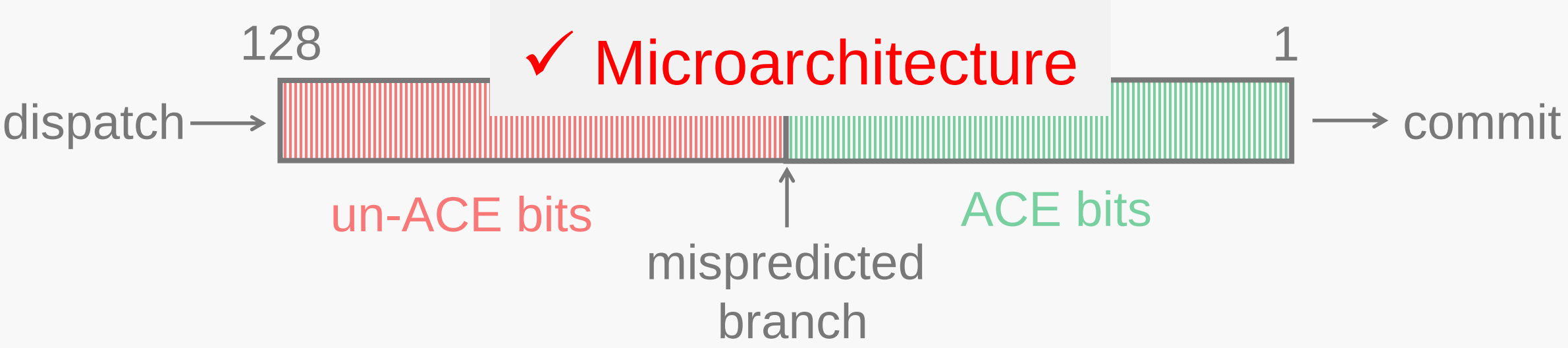


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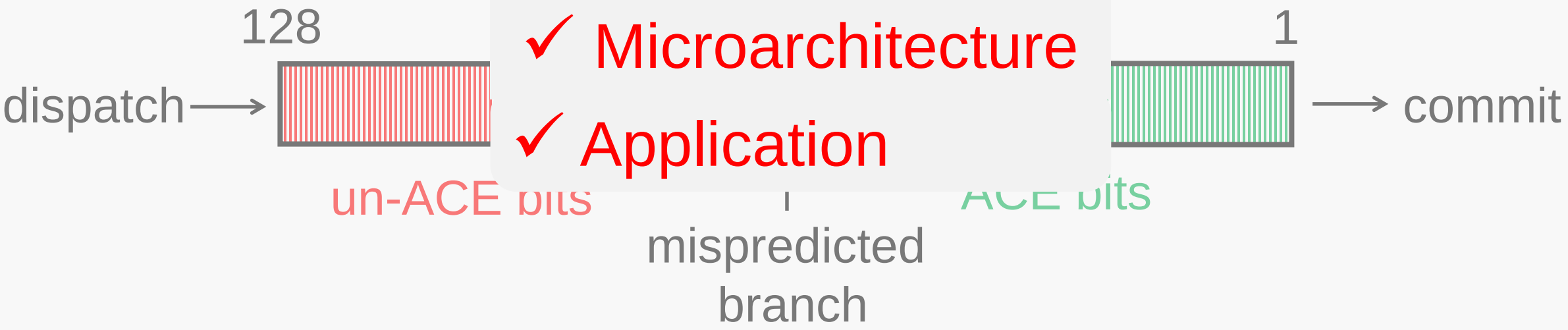


✓ Microarchitecture

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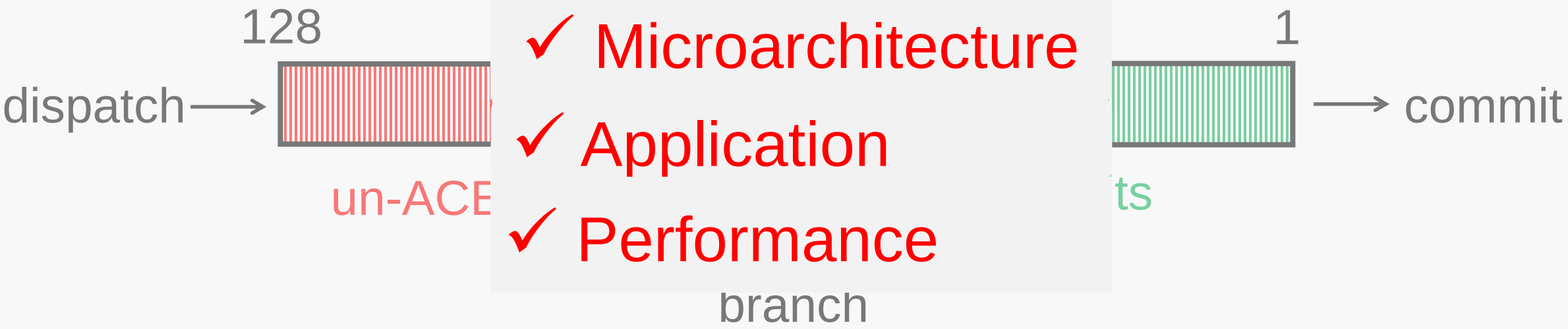


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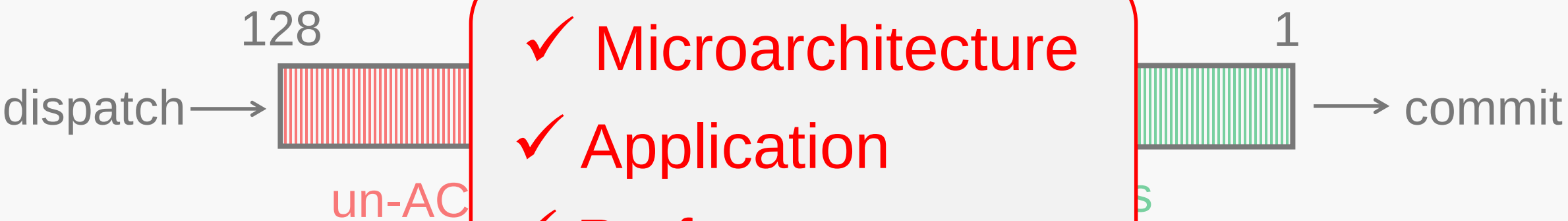


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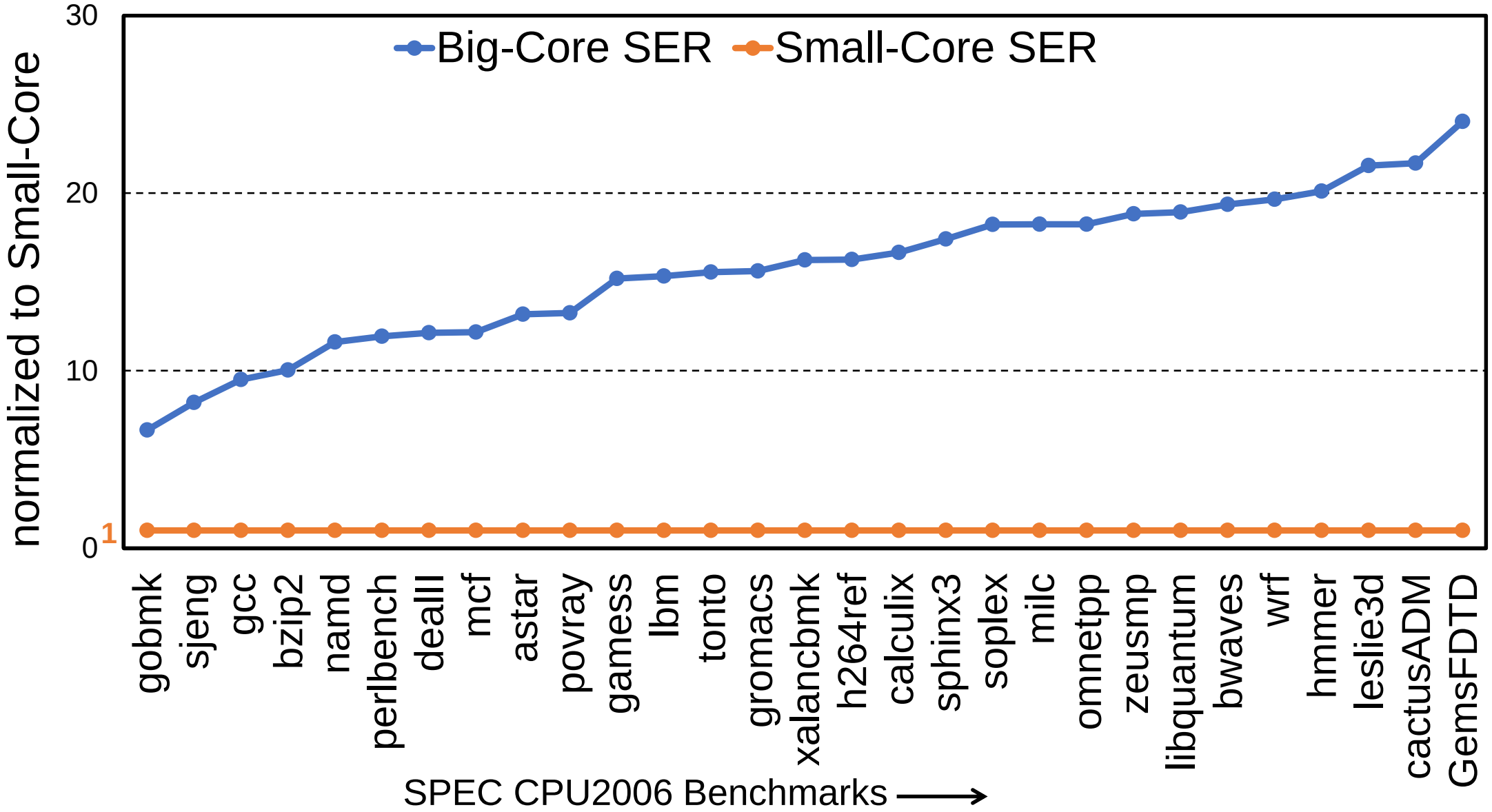
# Vulnerability vs. Core Type



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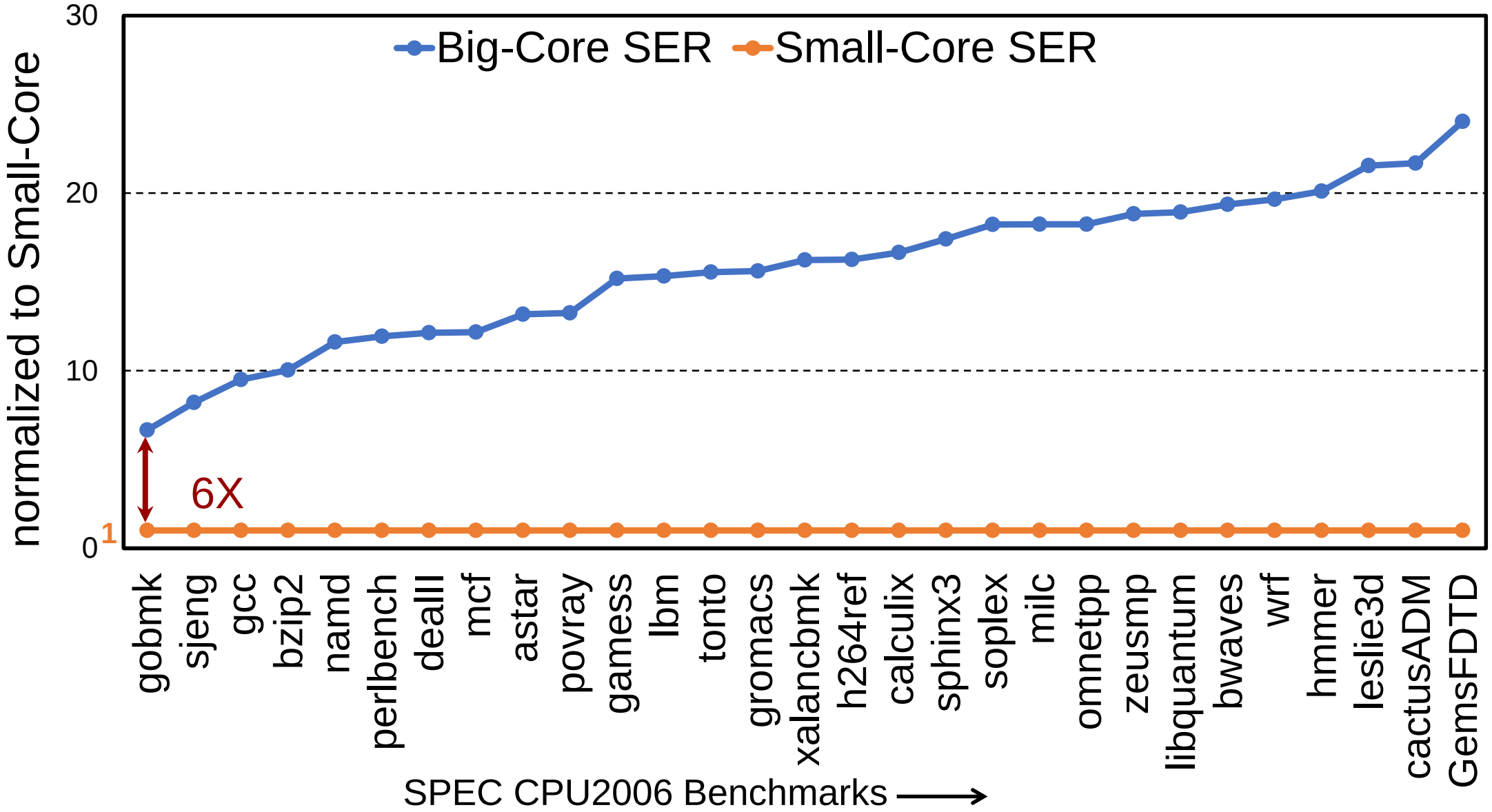

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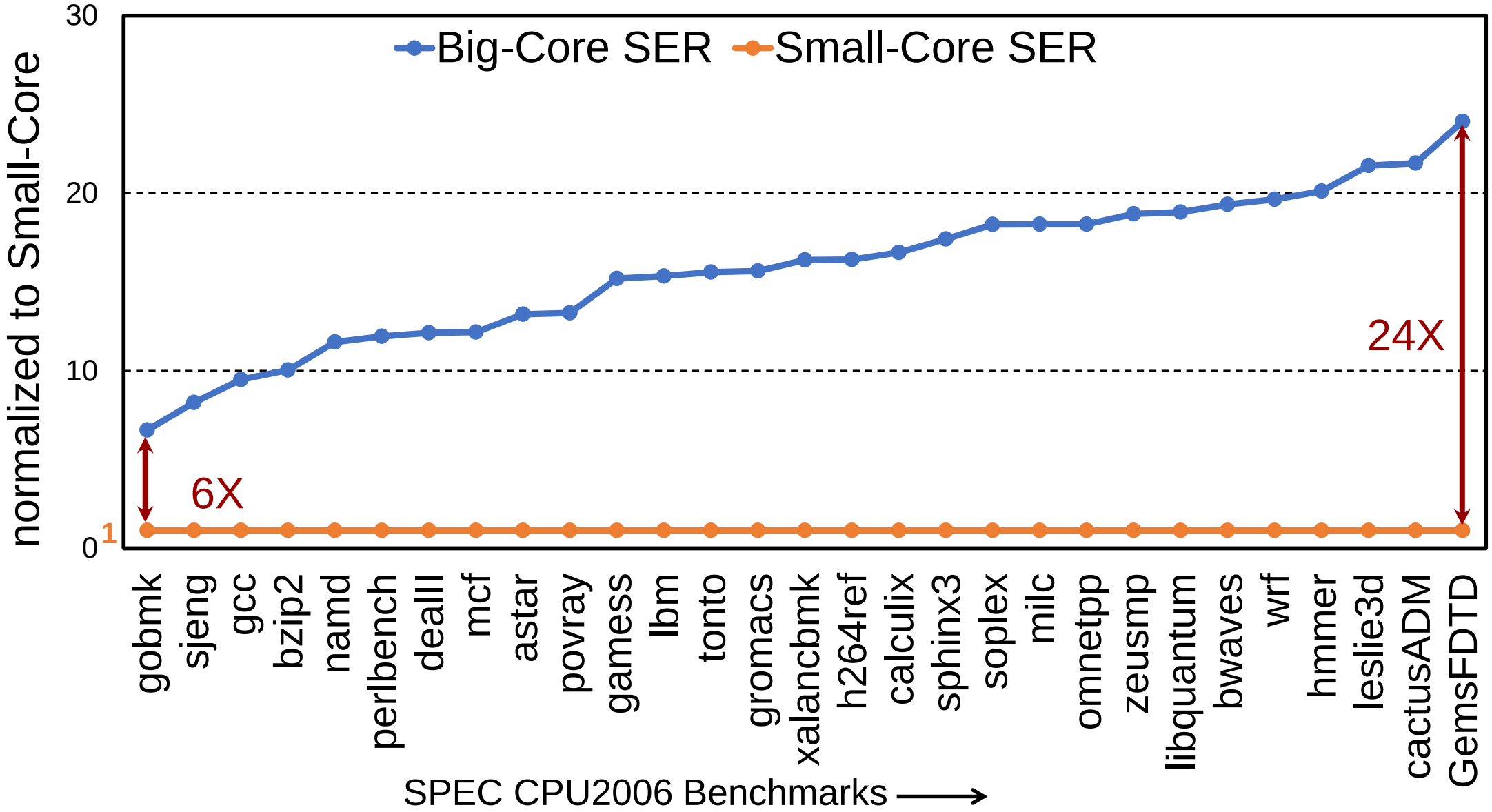

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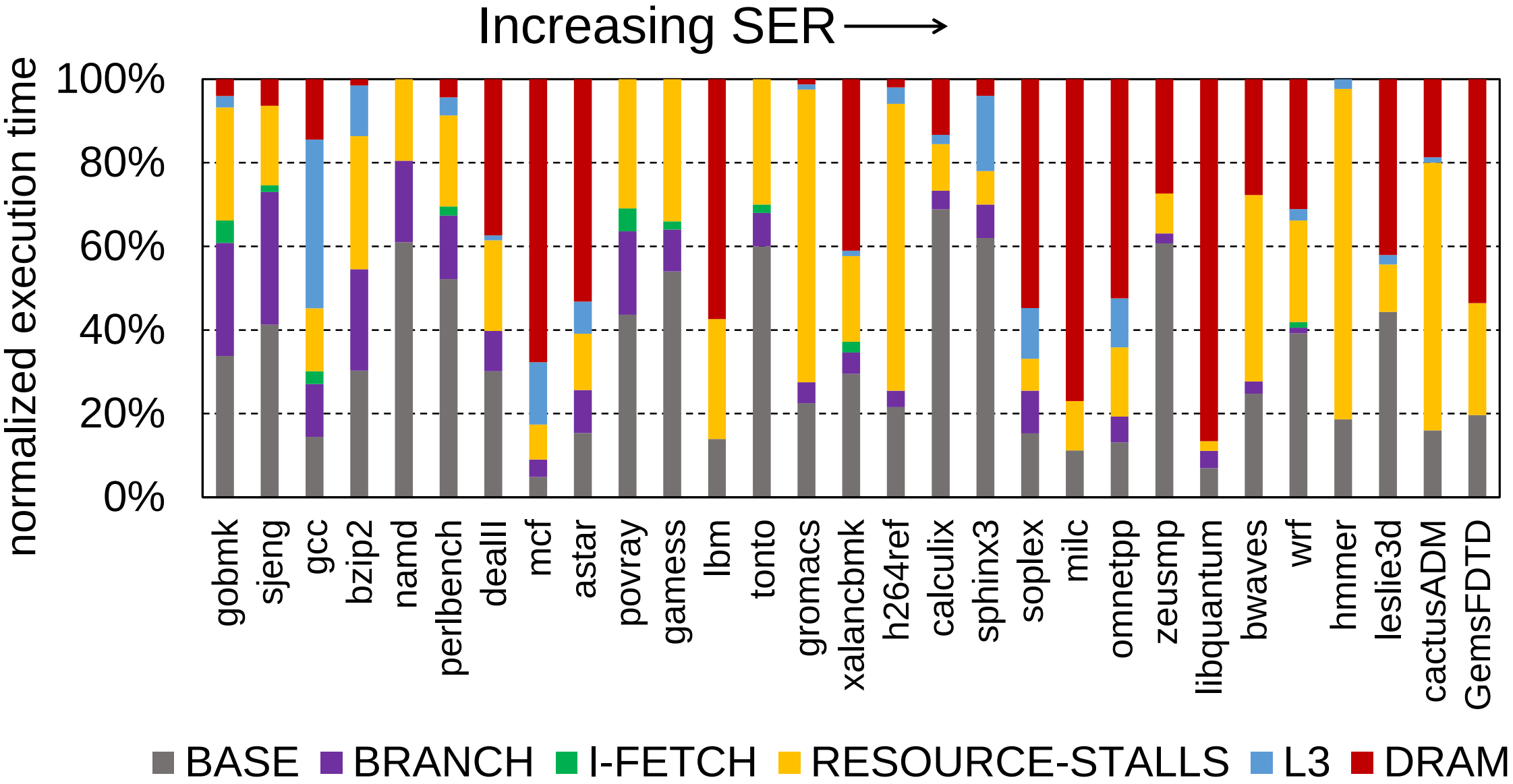

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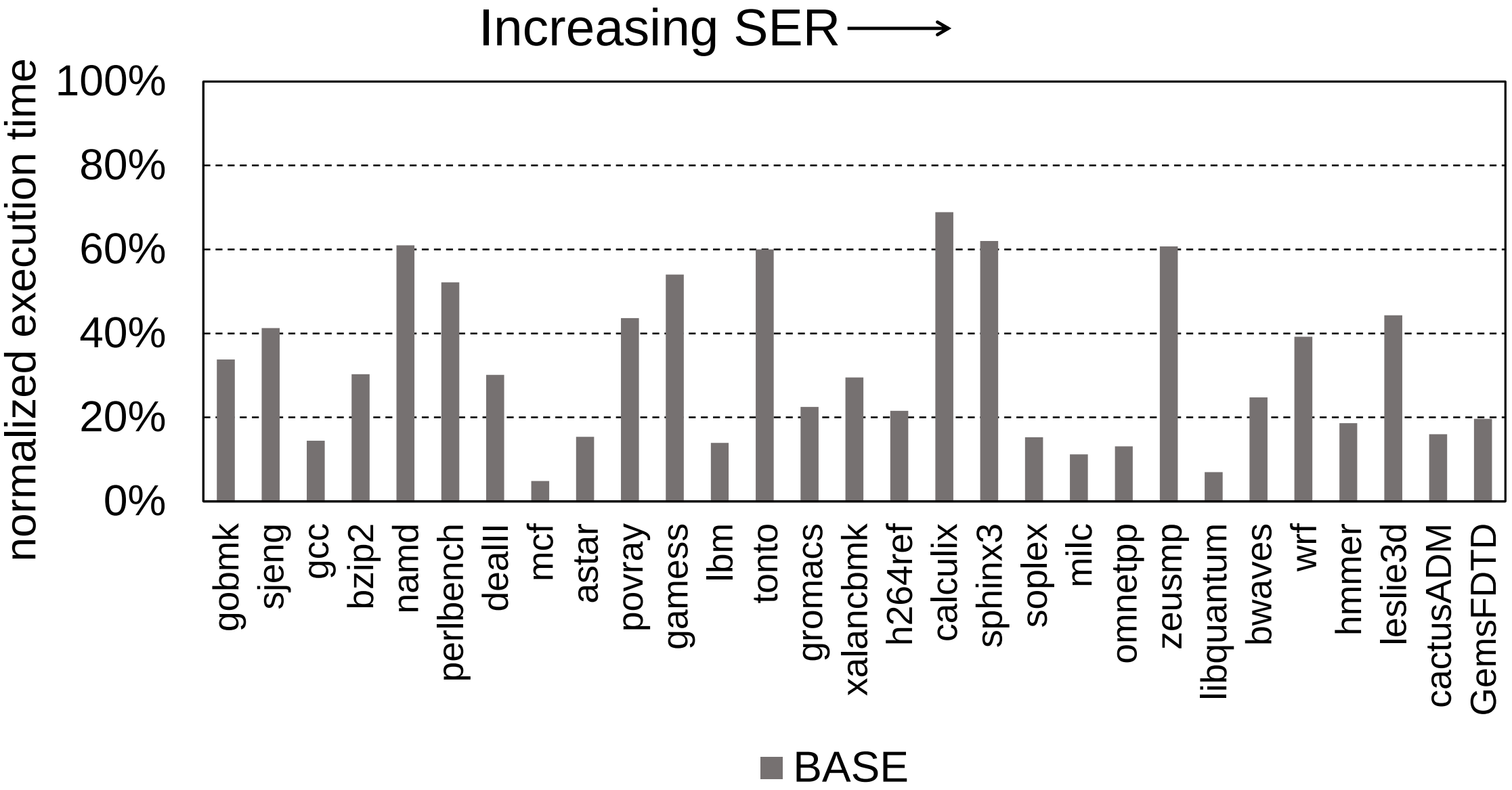

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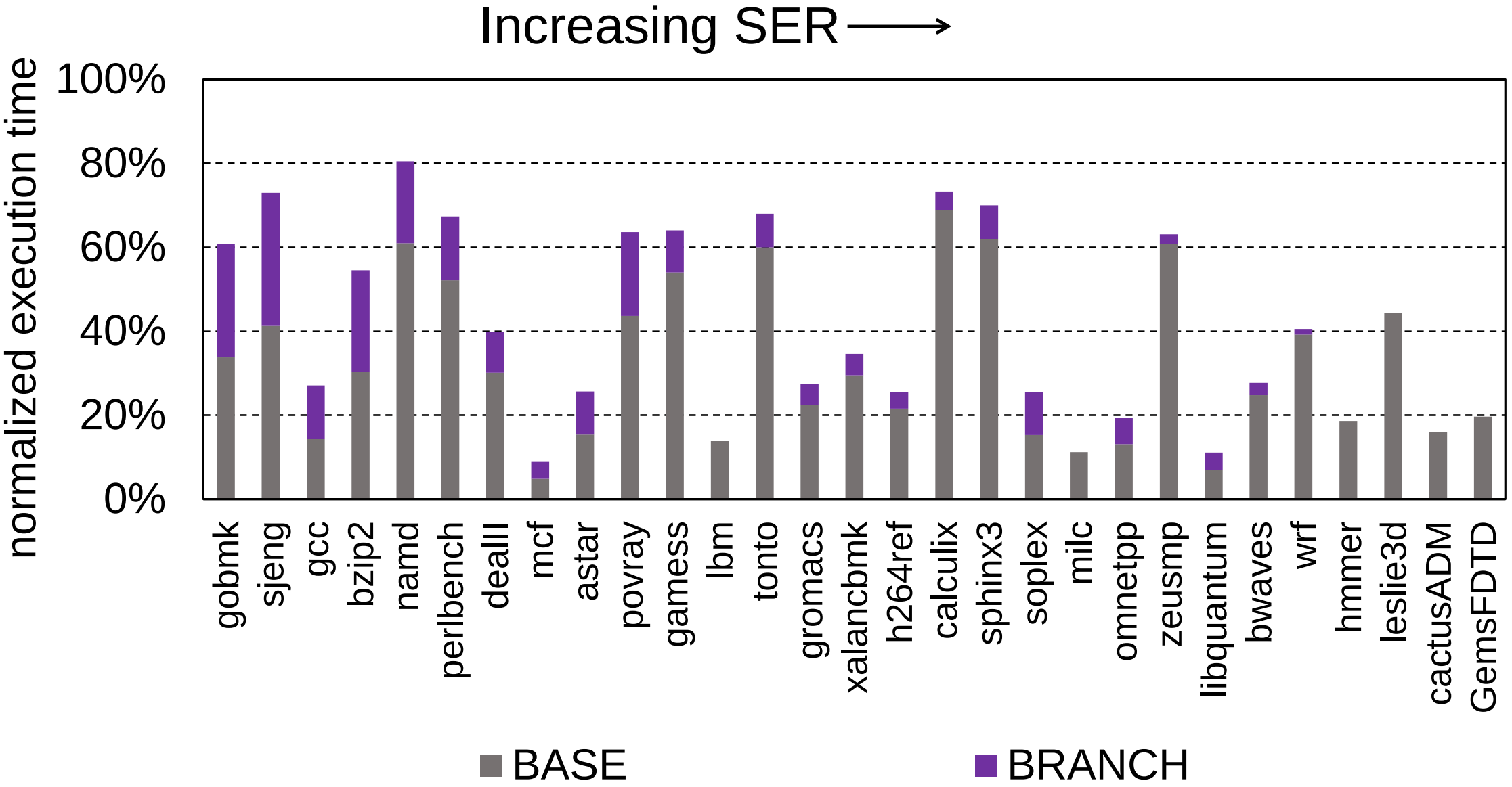

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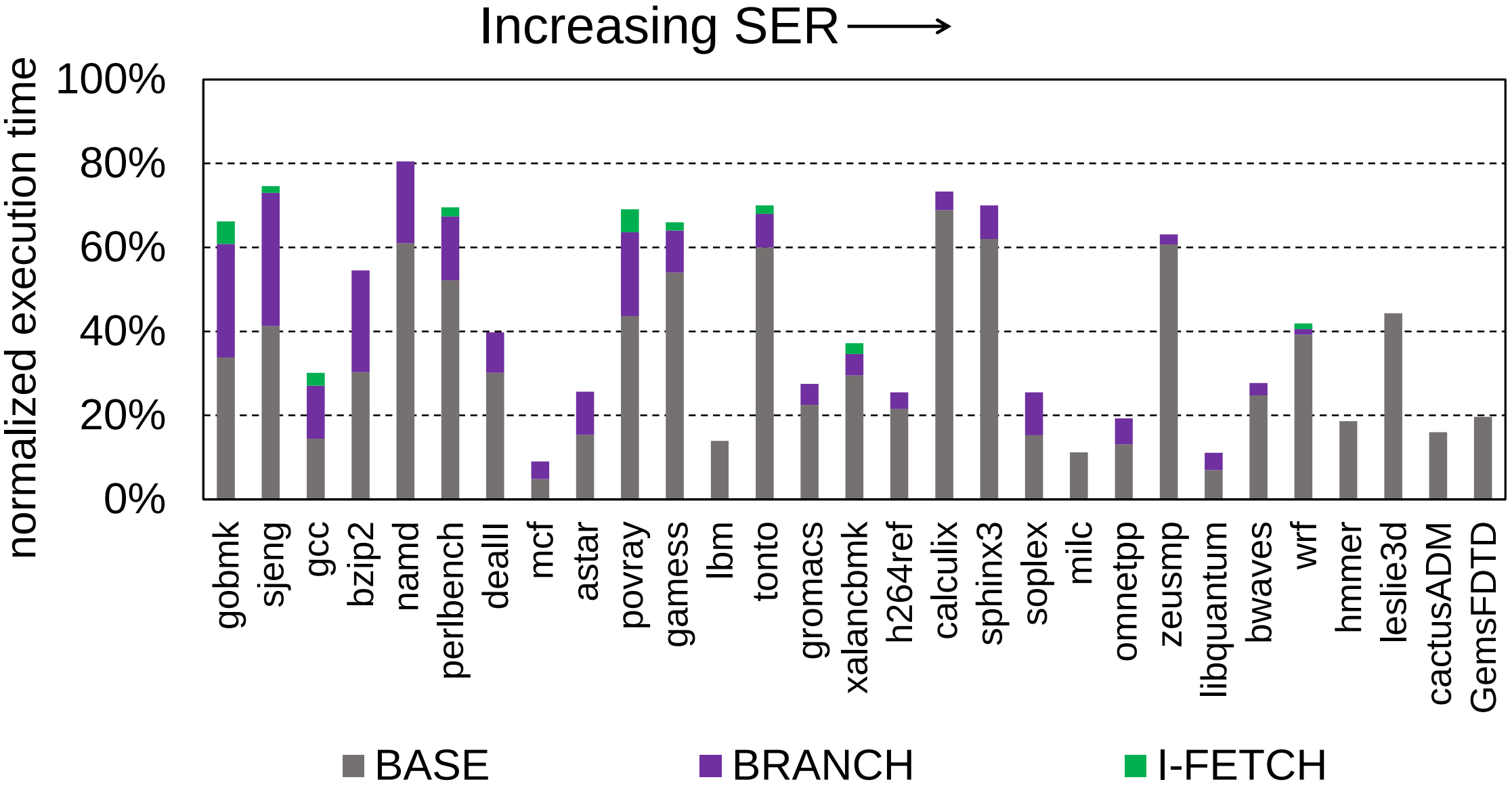

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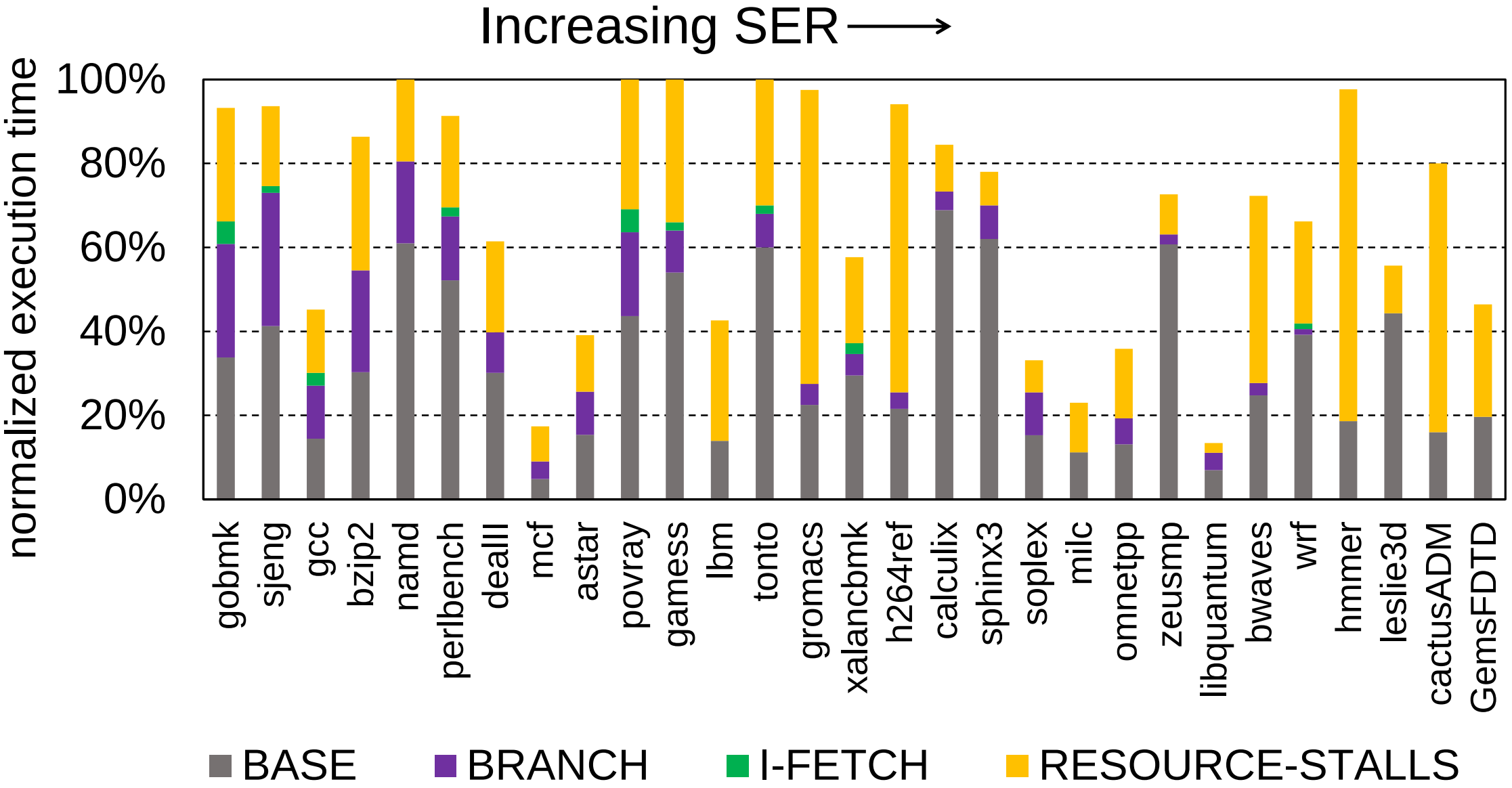

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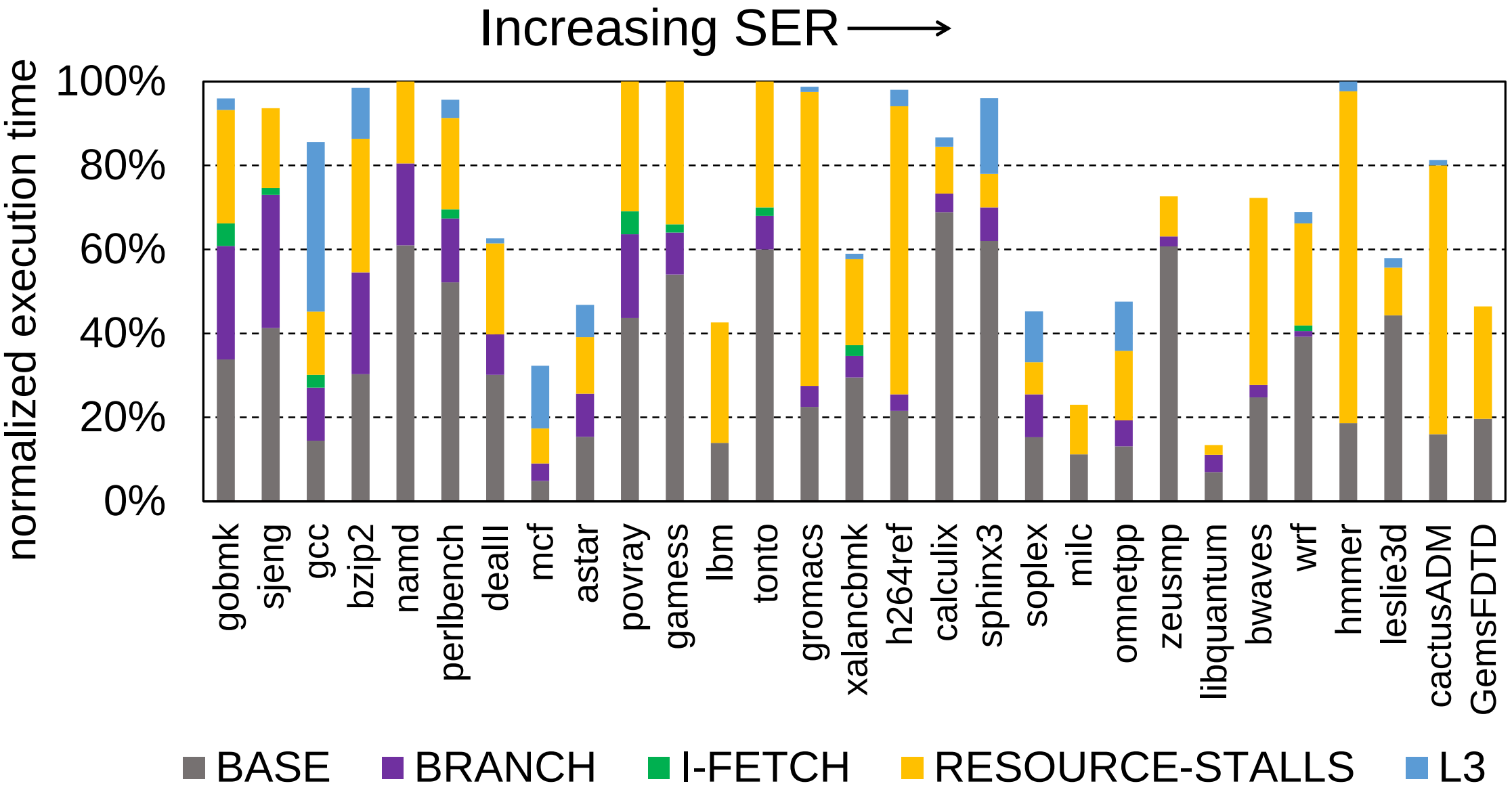

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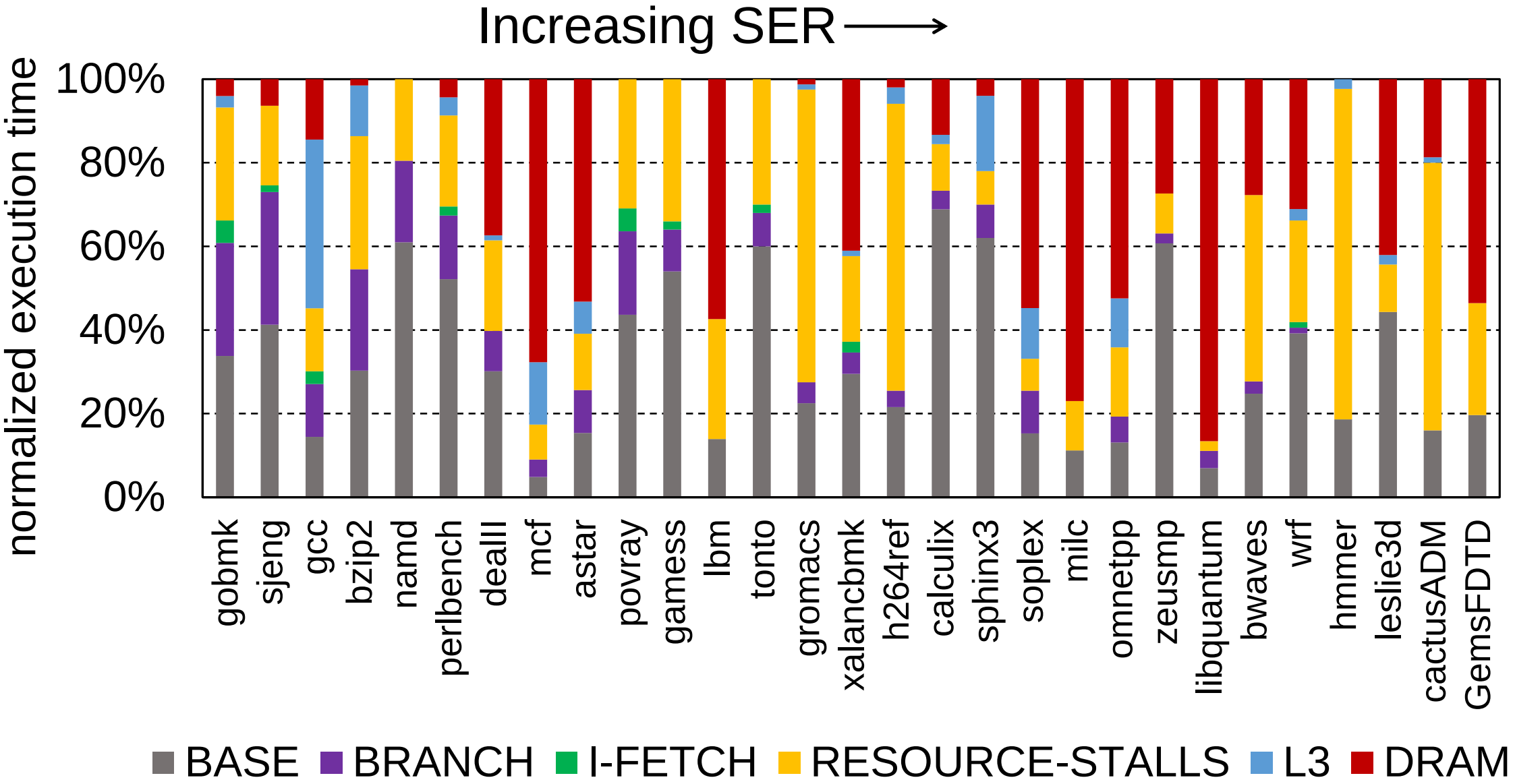
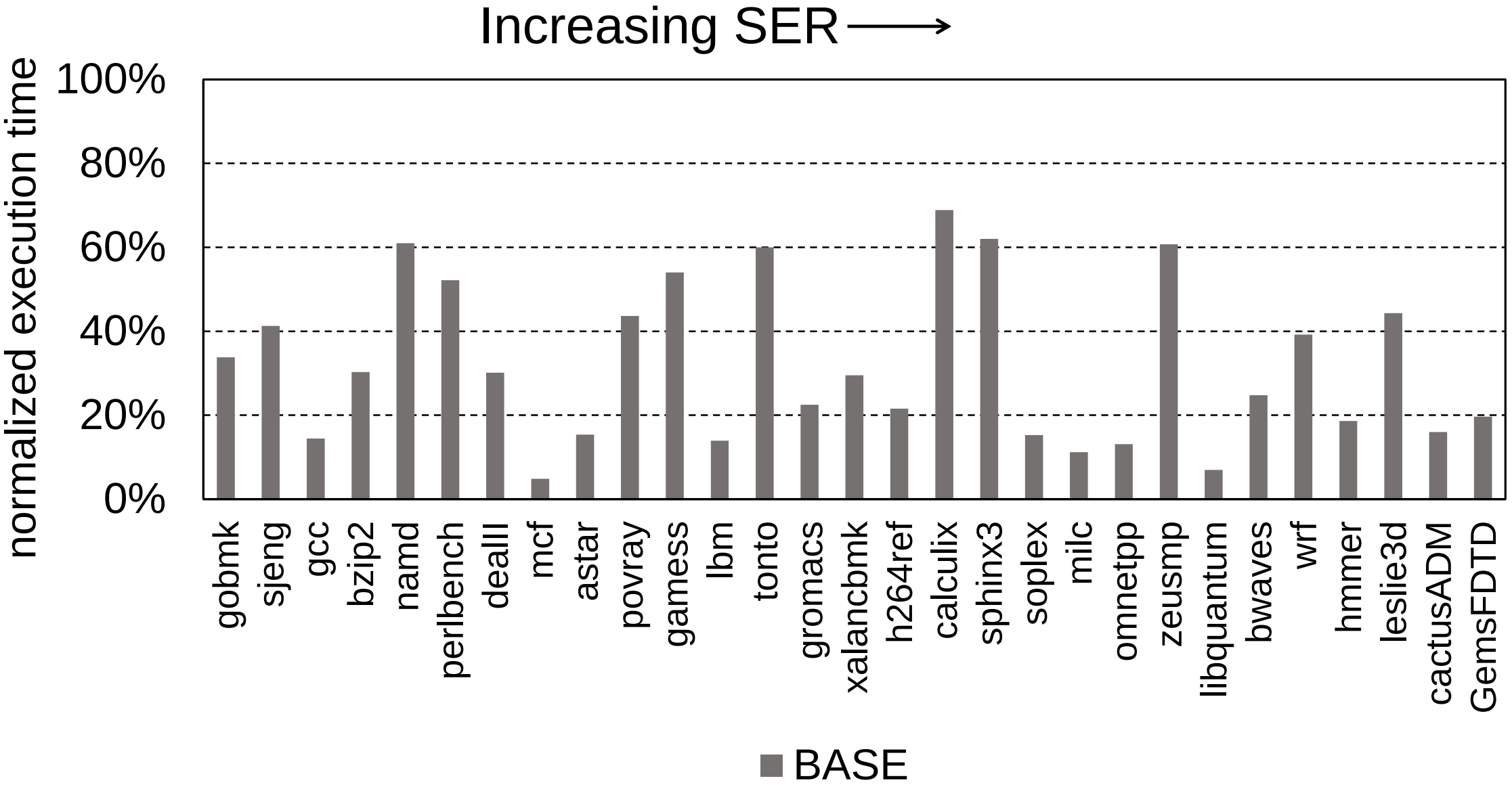
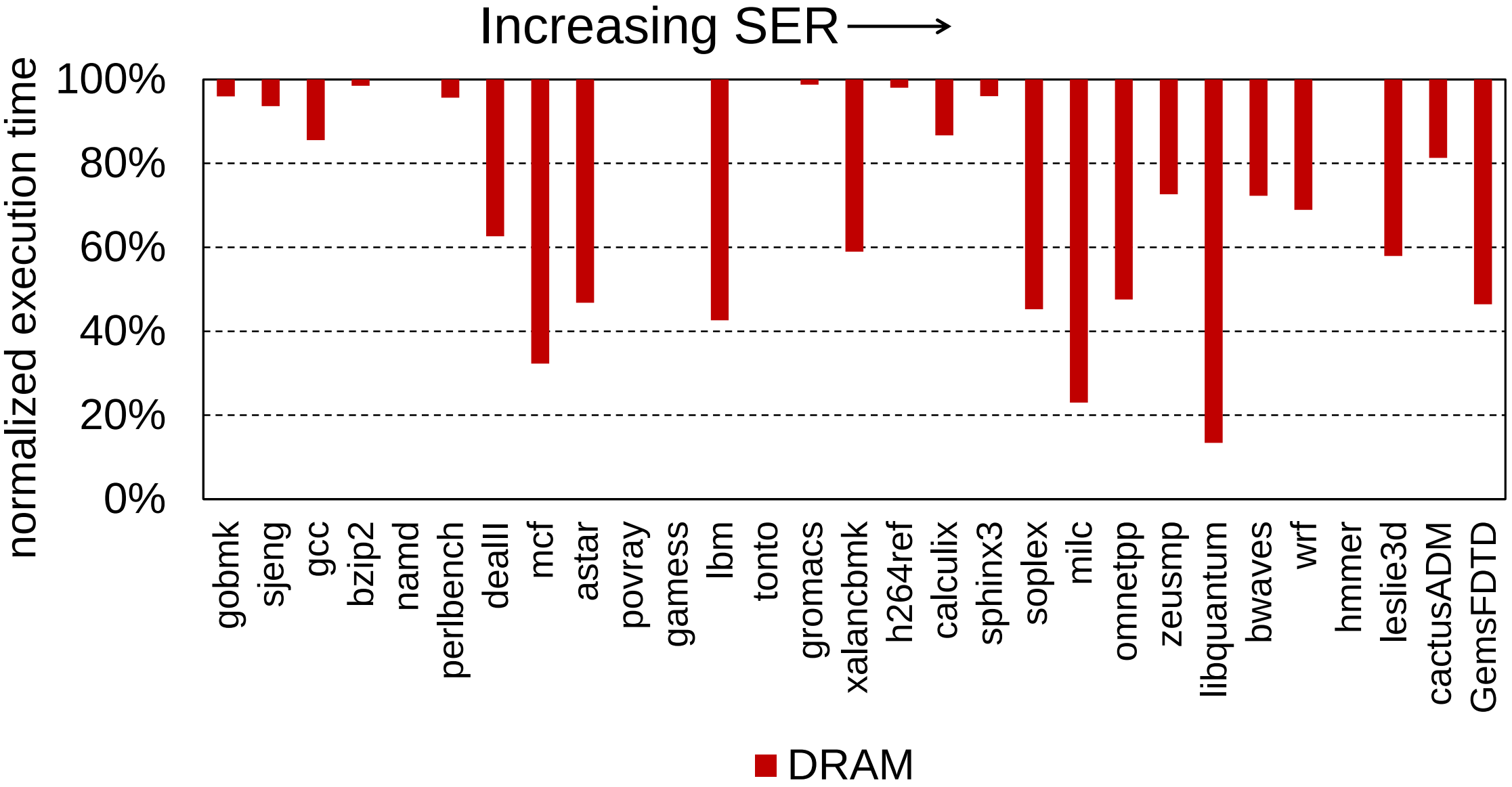


# Vulnerability vs. Compute-Intensity



# Vulnerability vs. Memory-Intensity



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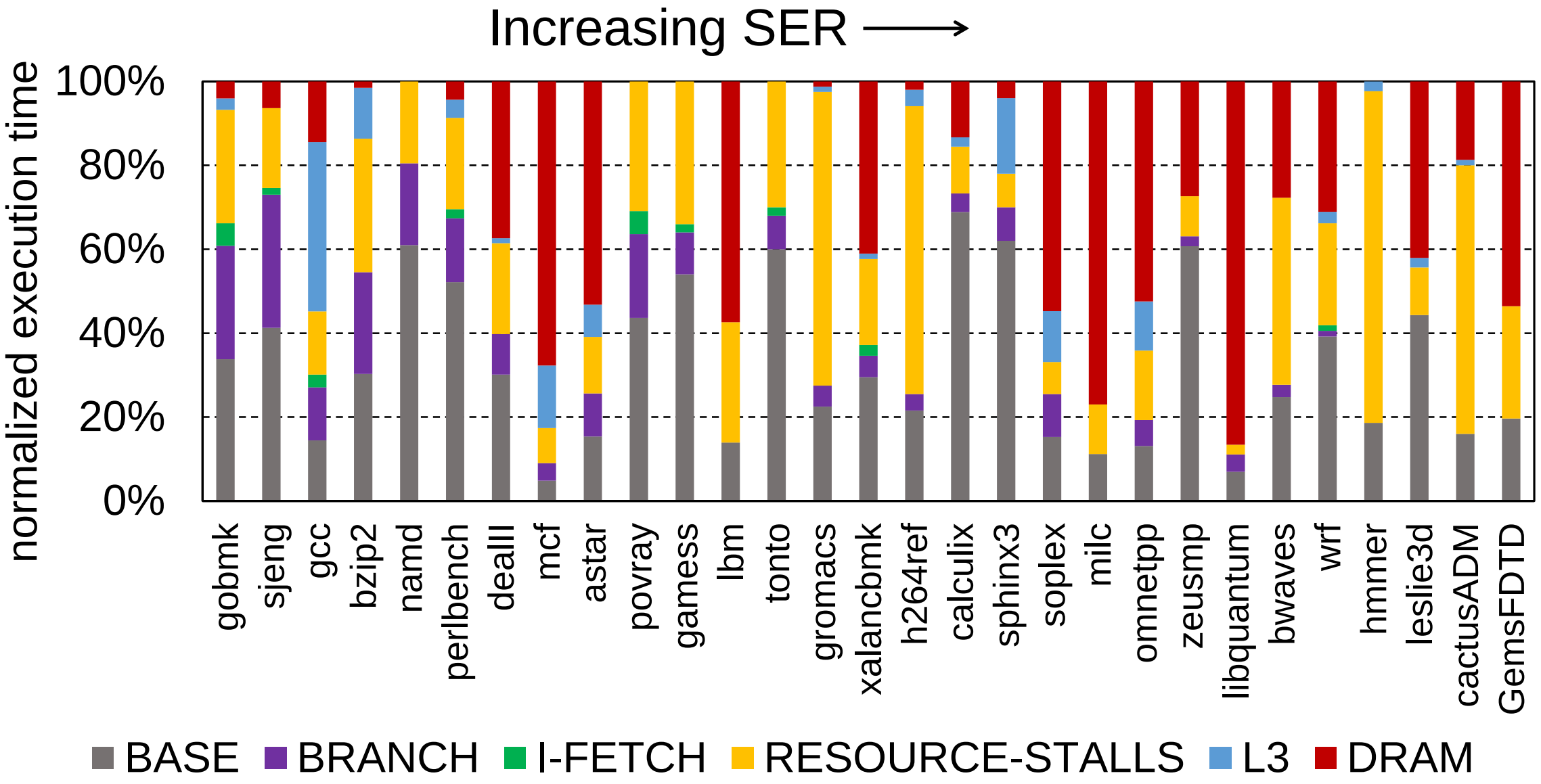

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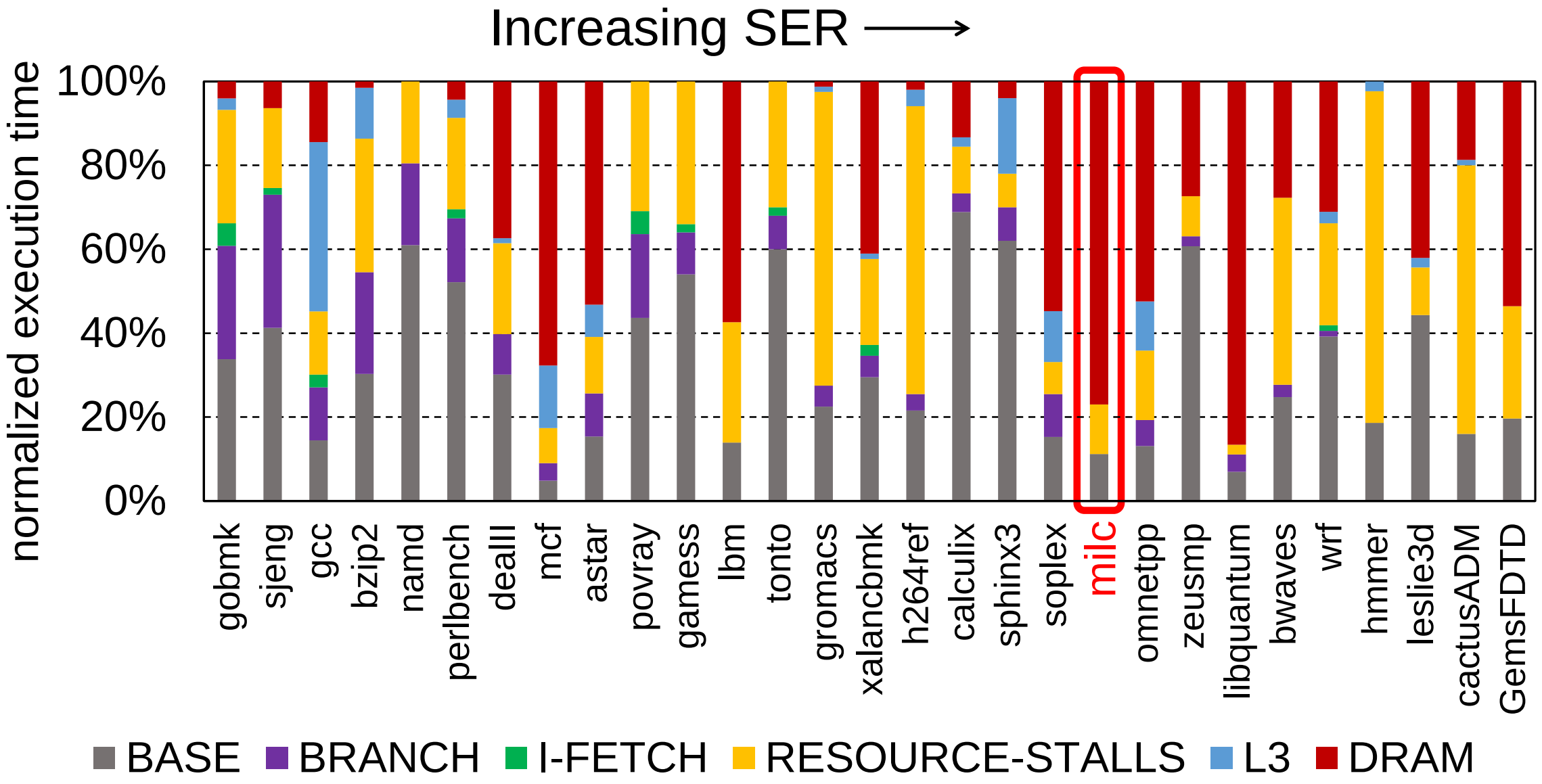

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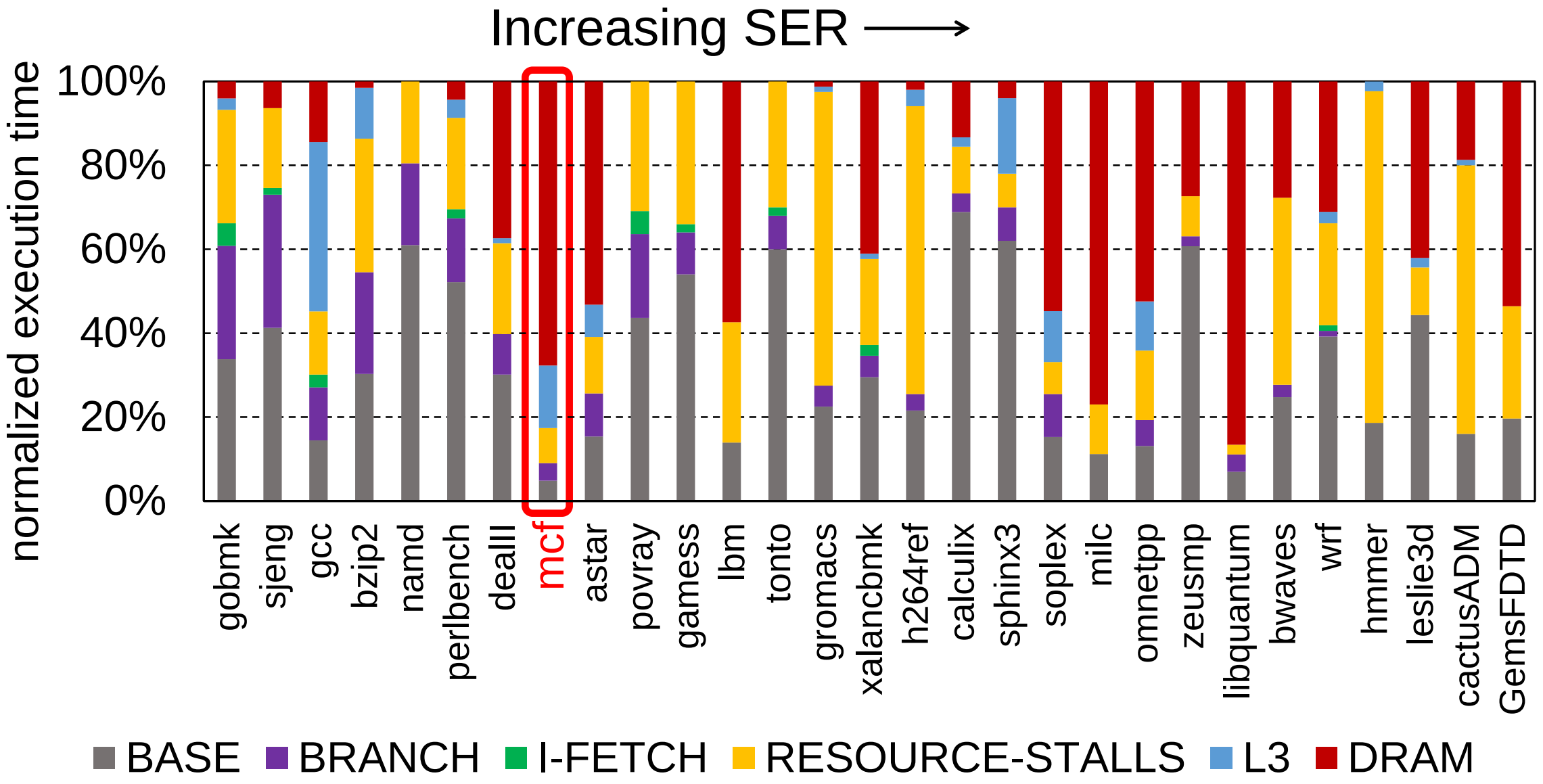

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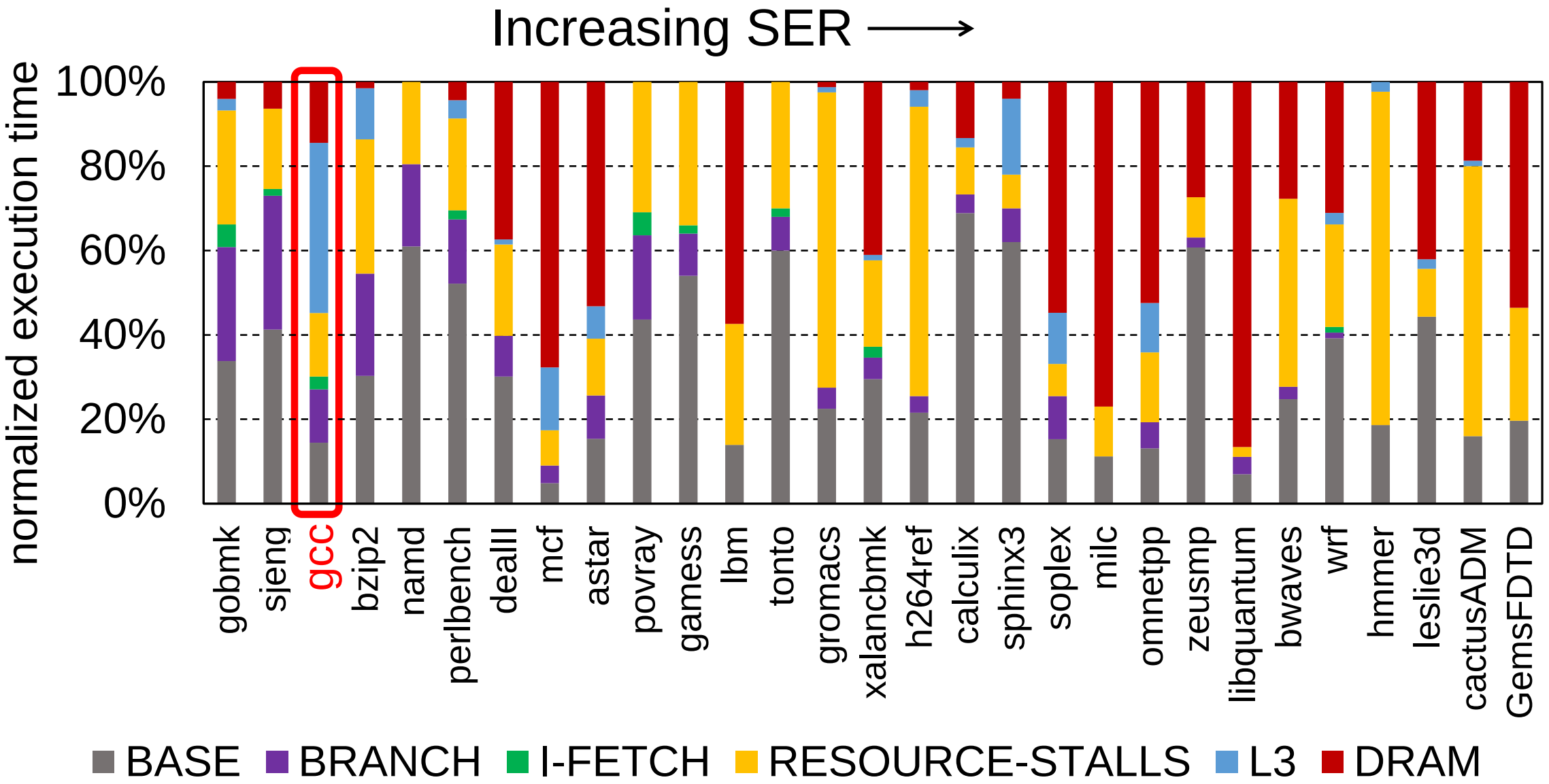

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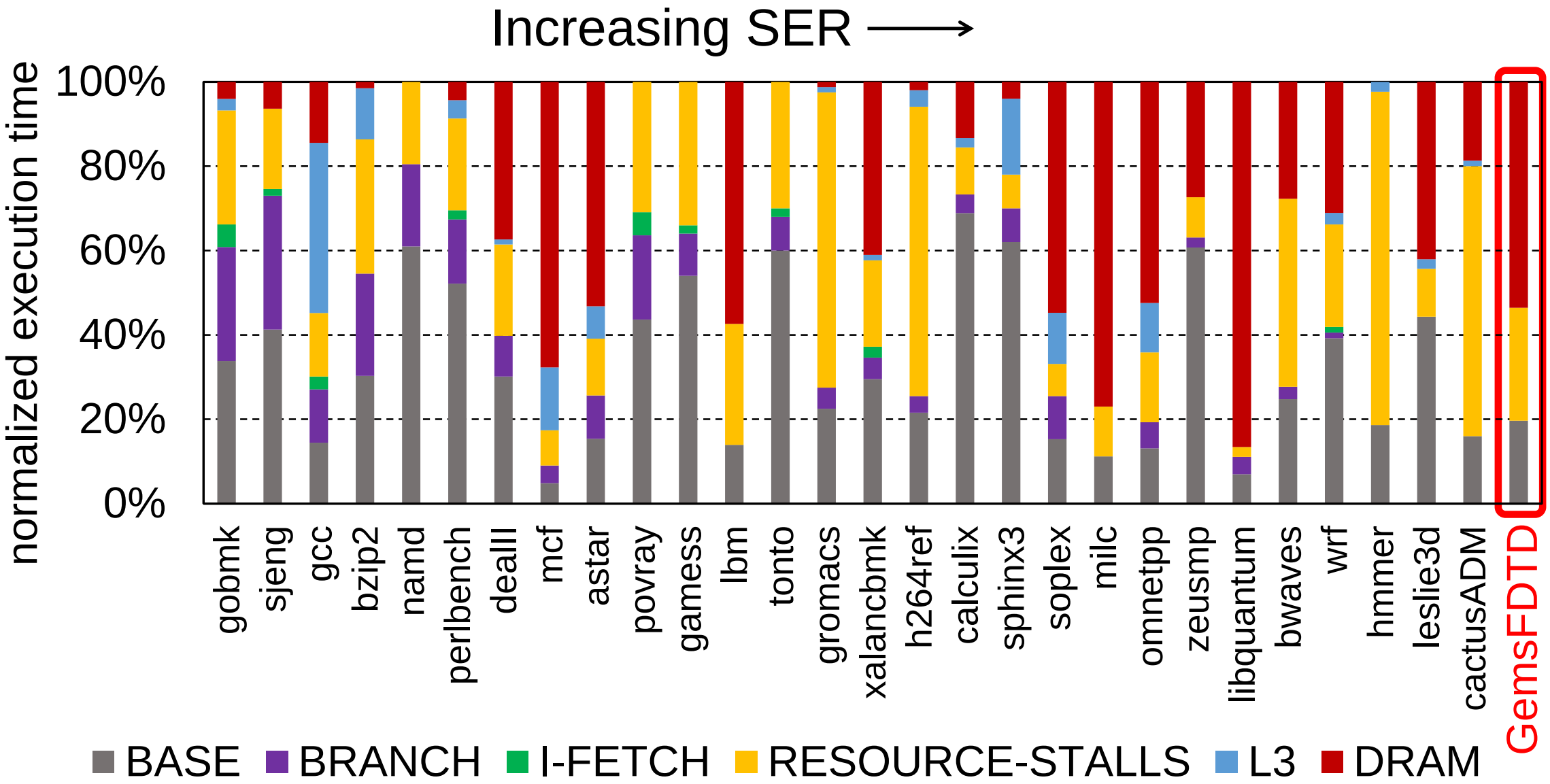

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**Reliability-Aware Scheduling**

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# Reliability Metric for Multiprogram Workloads

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**A** Time = 1

SER = 4

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As a 2-program workload on a CMP with two cores:

| | | |
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| | | + |
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Total SER = 5

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Solution

New metric: System Soft Error Rate (SSER)

# System Soft Error Rate (SSER) Correctly Accounts for the Slowdown

In isolation on one core:

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| | | | |
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As a 2-program workload on a CMP with two cores:

| | | | |
|---|---|---|---|
| A | Time = 1 | SER = 4 | 1 × 4 Weighted SER = 4 |
| | | + | |
| B | Time = 2 | SER = 1 | |

Total SER = 5

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SSER = 6

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Total SER = 5 ✗

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| | | + | + |
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Total SER = 5 ✗

SSER = 6 ✓

# Scheduling Algorithm

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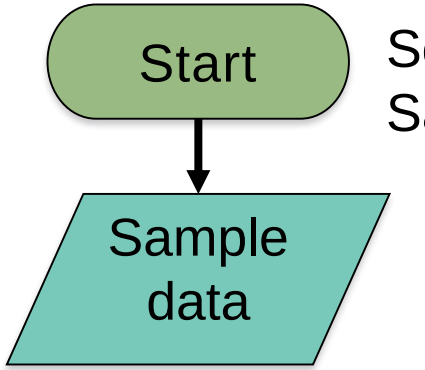


Scheduler quantum = 1ms
Sampling for 0.1ms

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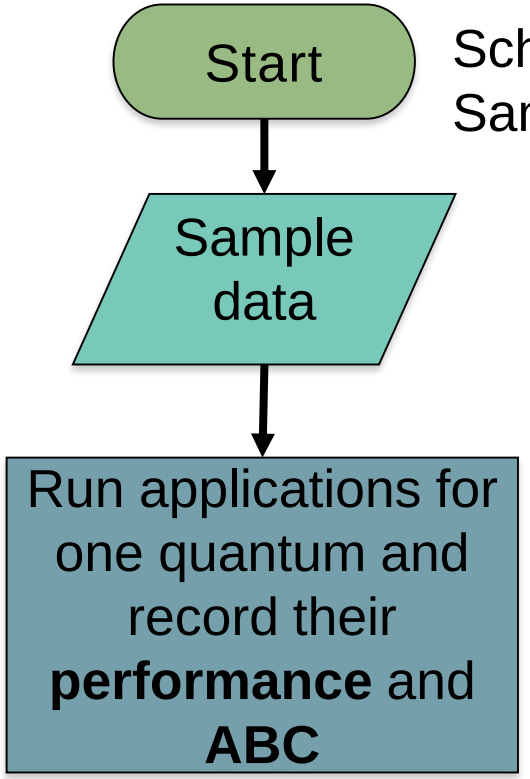


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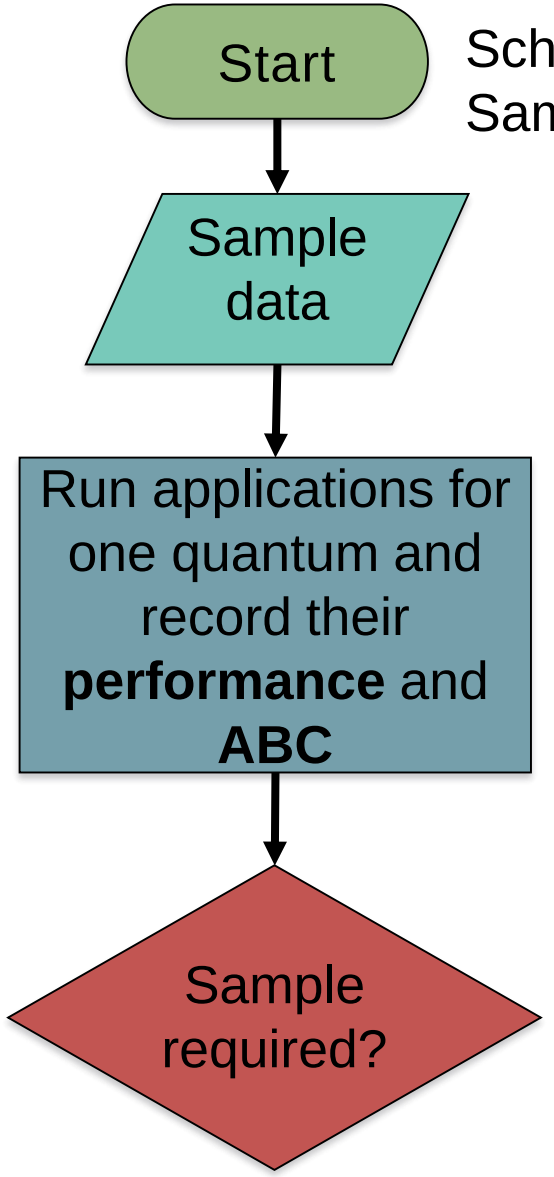


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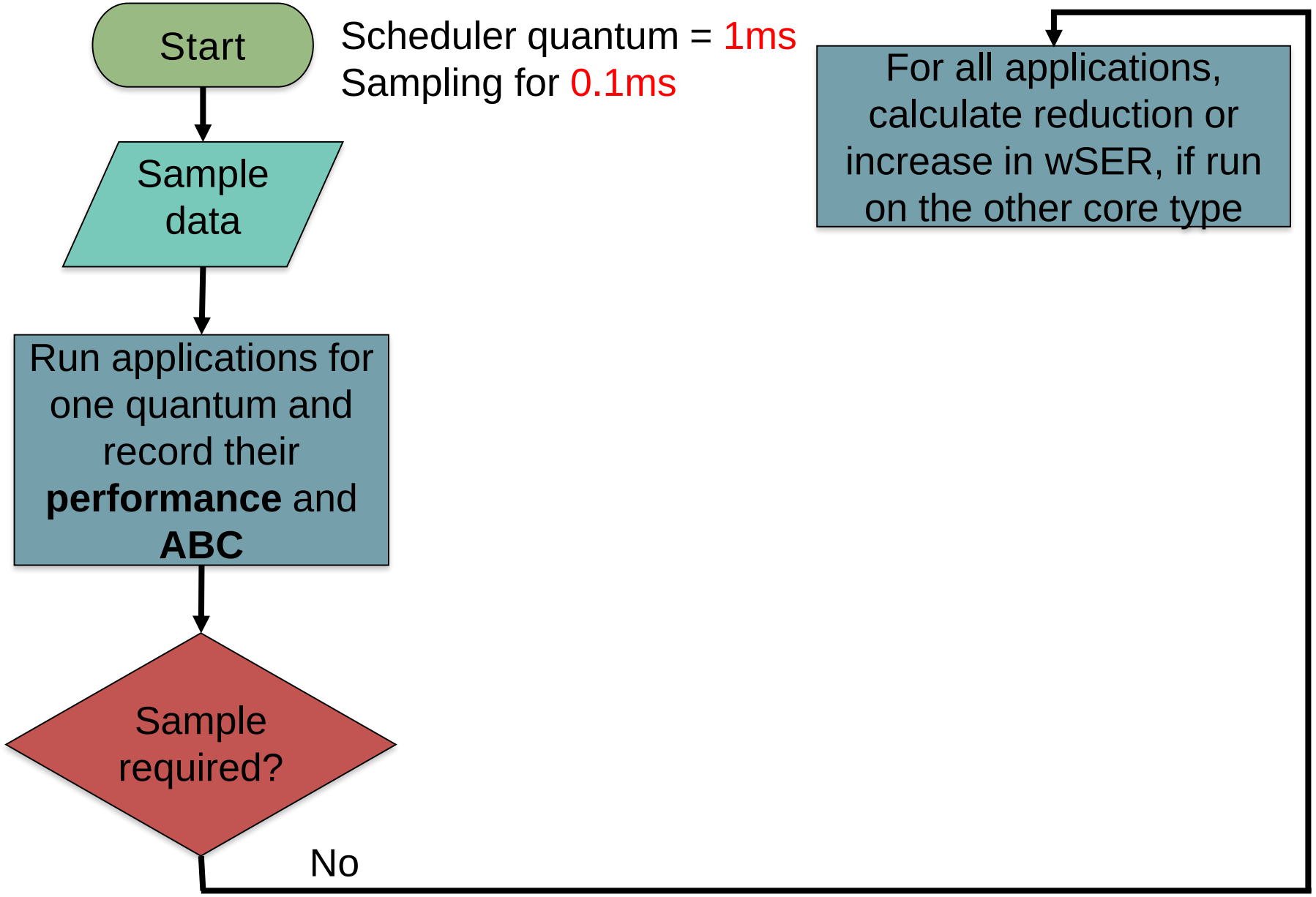

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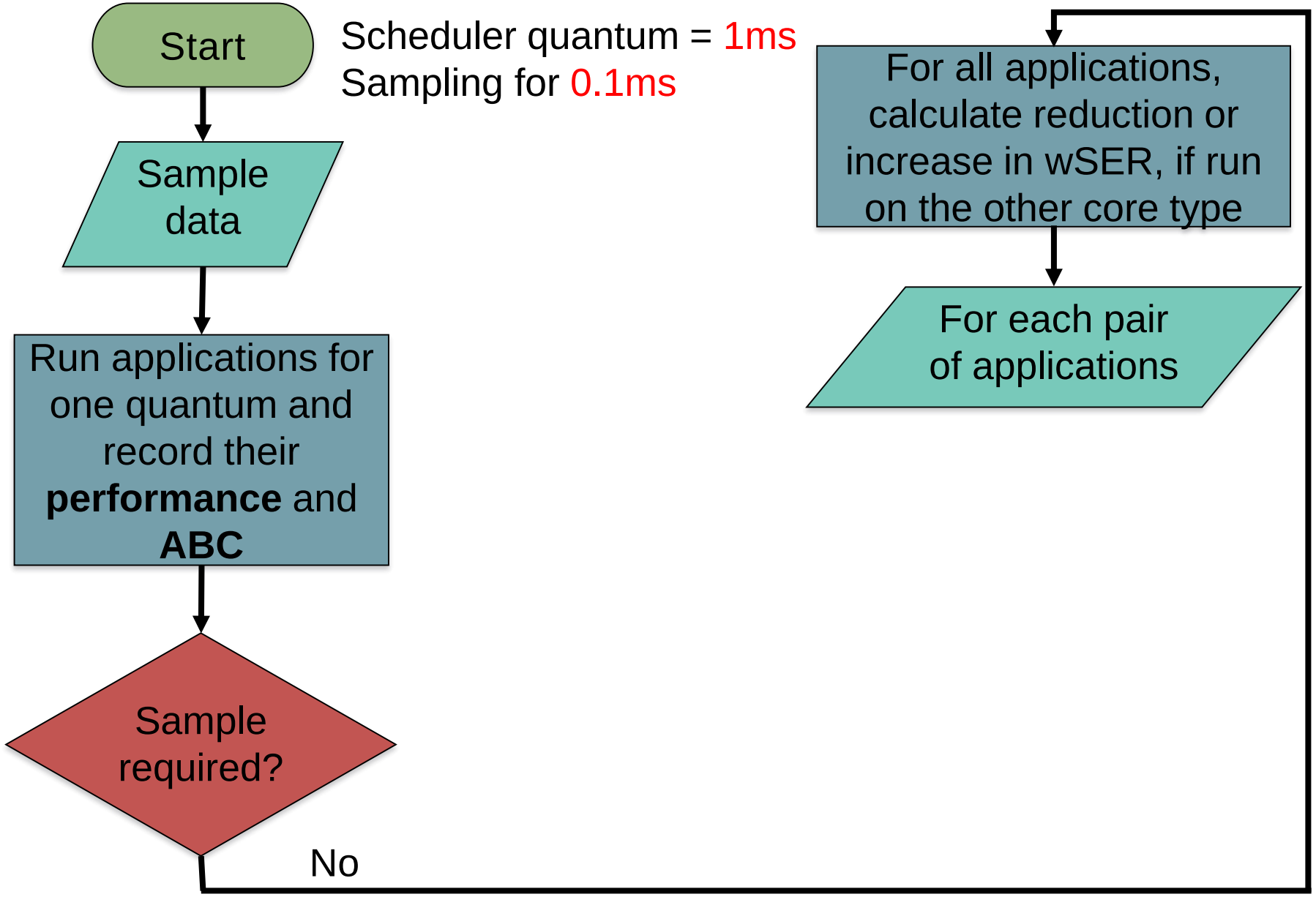

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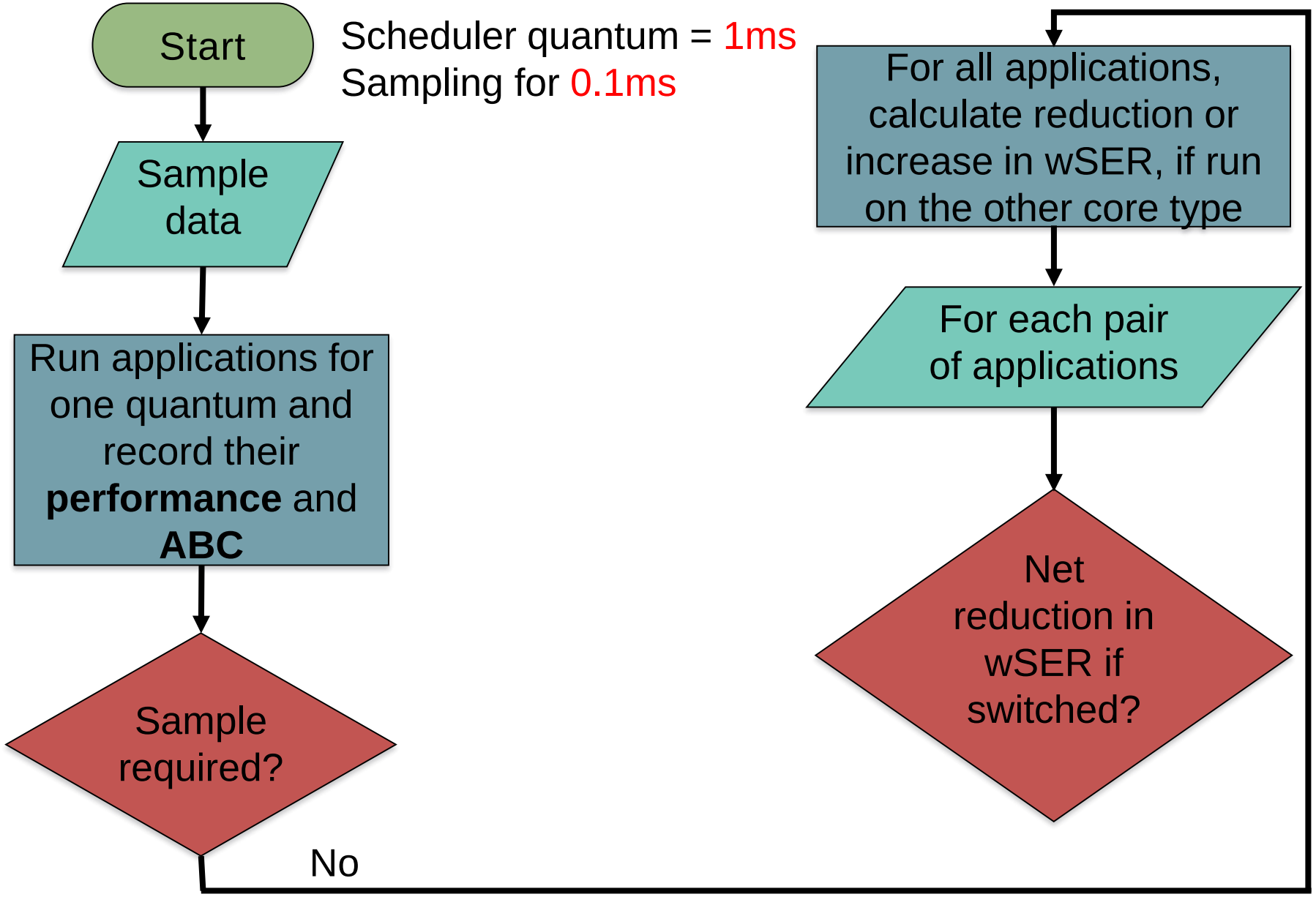

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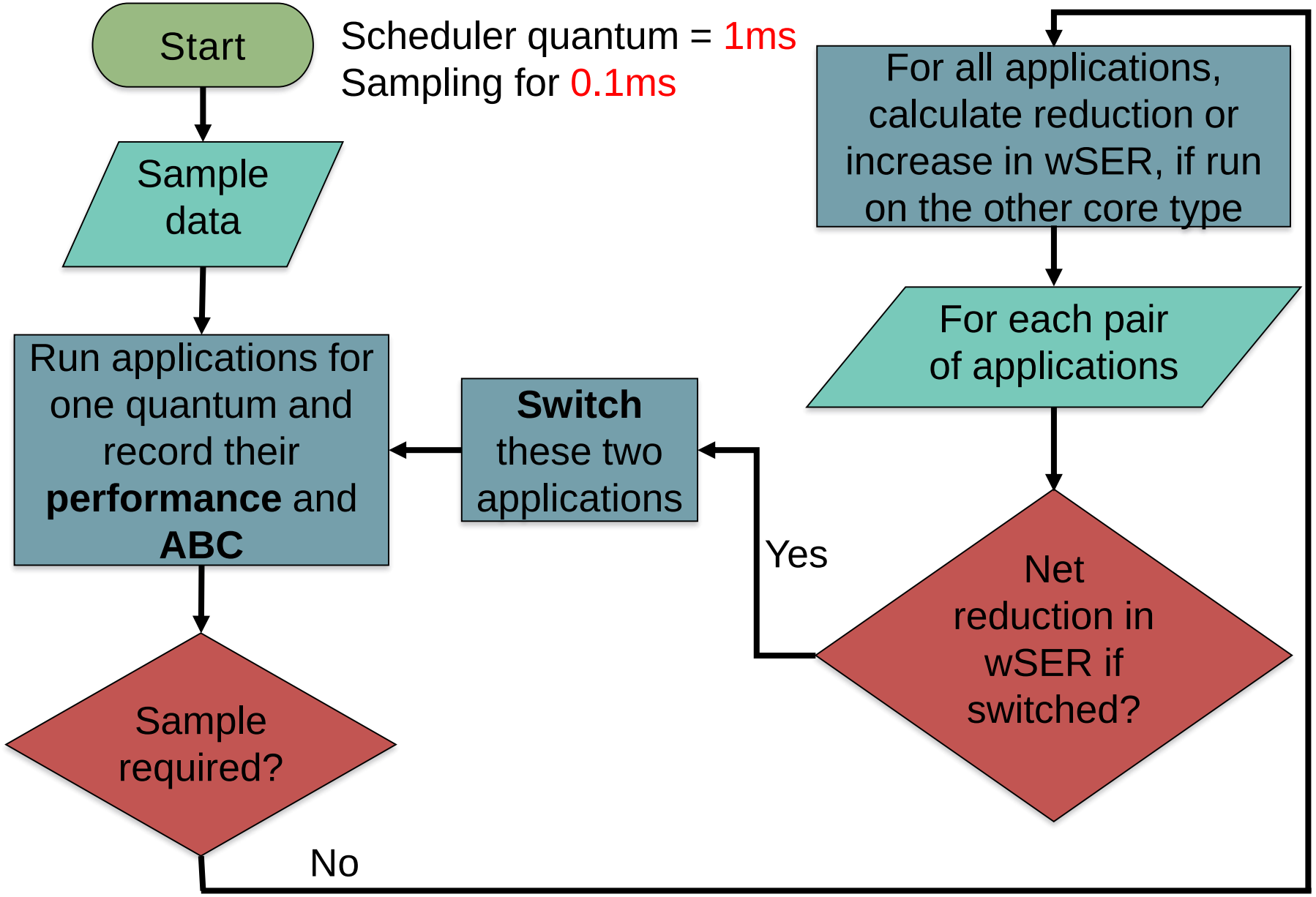

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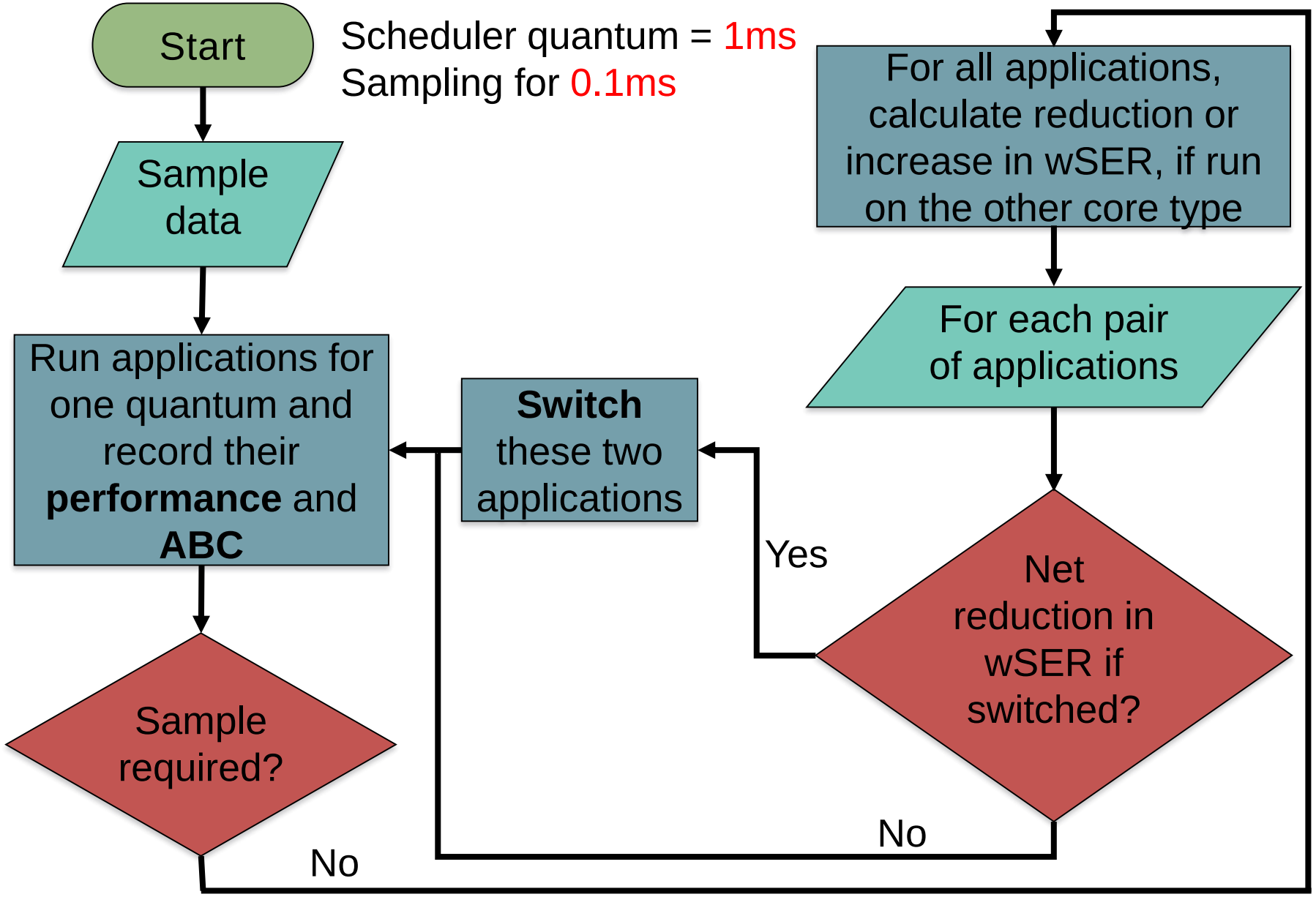

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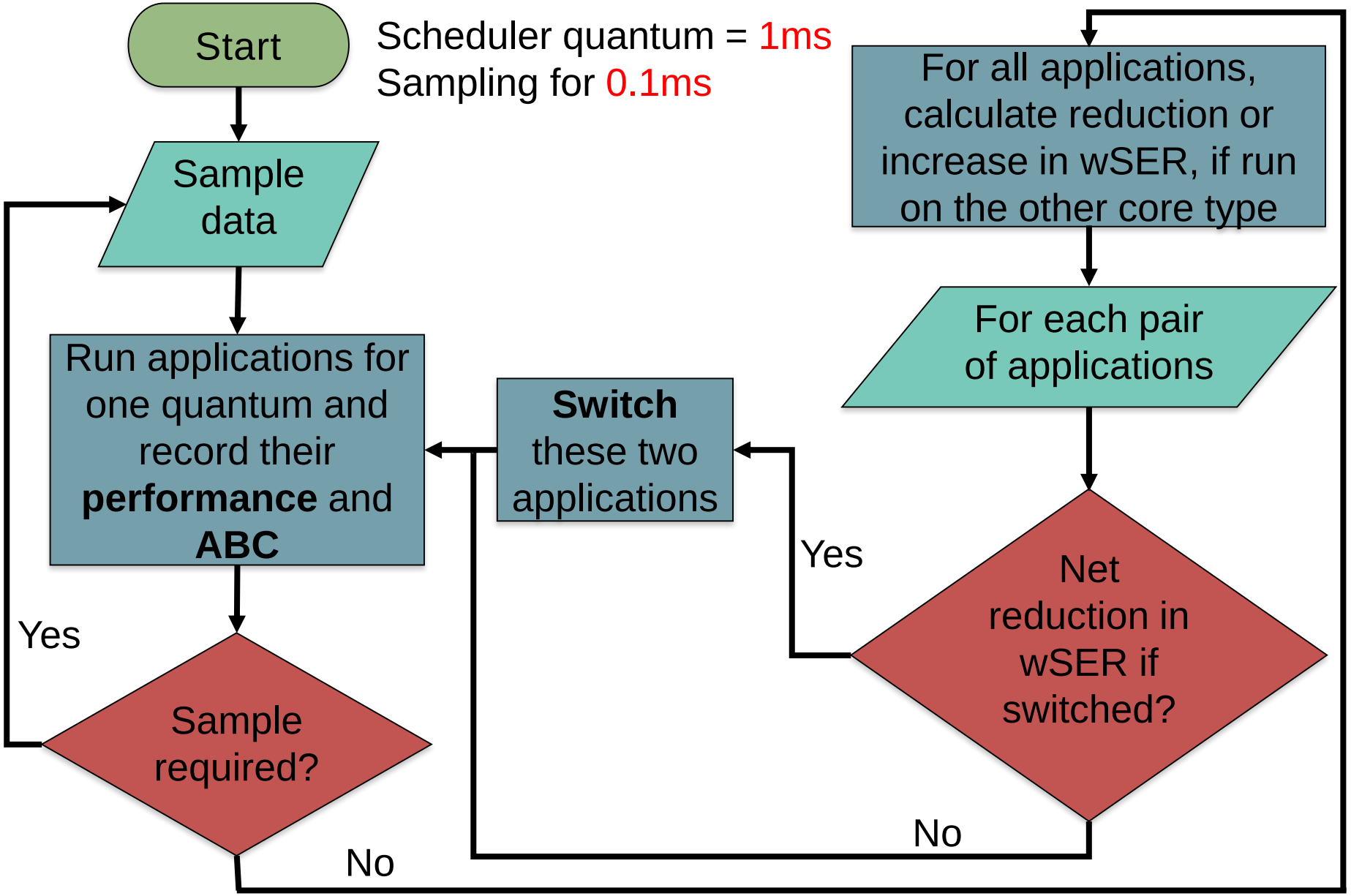

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Sniper 6.0

-- Augmented with ACE Bit Counters

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SPEC CPU2006

-- 1B instruction SimPoints

-- Based on big-core SER

- ✓ L→ Low SER
- ✓ M → Medium SER
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## 4-program workloads

-- 6 categories → HHHH, HHMM, HHLL, MMMM, MMLL, LLLL

# Experimental Setup

Sniper 6.0

-- Augmented with ACE Bit Counters

SPEC CPU2006

-- 1B instruction SimPoints

-- Based on big-core SER

4-program workloads

-- 6 categories → HHHH, HHMM, HHLL, MMMM, MMLL, LLLL

✓ L→ Low SER

✓ M → Medium SER

✓ H → High SER

HCMP → two big and two small cores (2B2S)

# Evaluation

Reliability-Optimized Scheduler

-- Optimizes SSER using our scheduling algorithm

# Evaluation

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-- Optimizes SSER using our scheduling algorithm

Performance-Optimized Scheduler

-- Optimizes System Throughput (STP)

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Reliability-Optimized Scheduler

-- Optimizes SSER using our scheduling algorithm

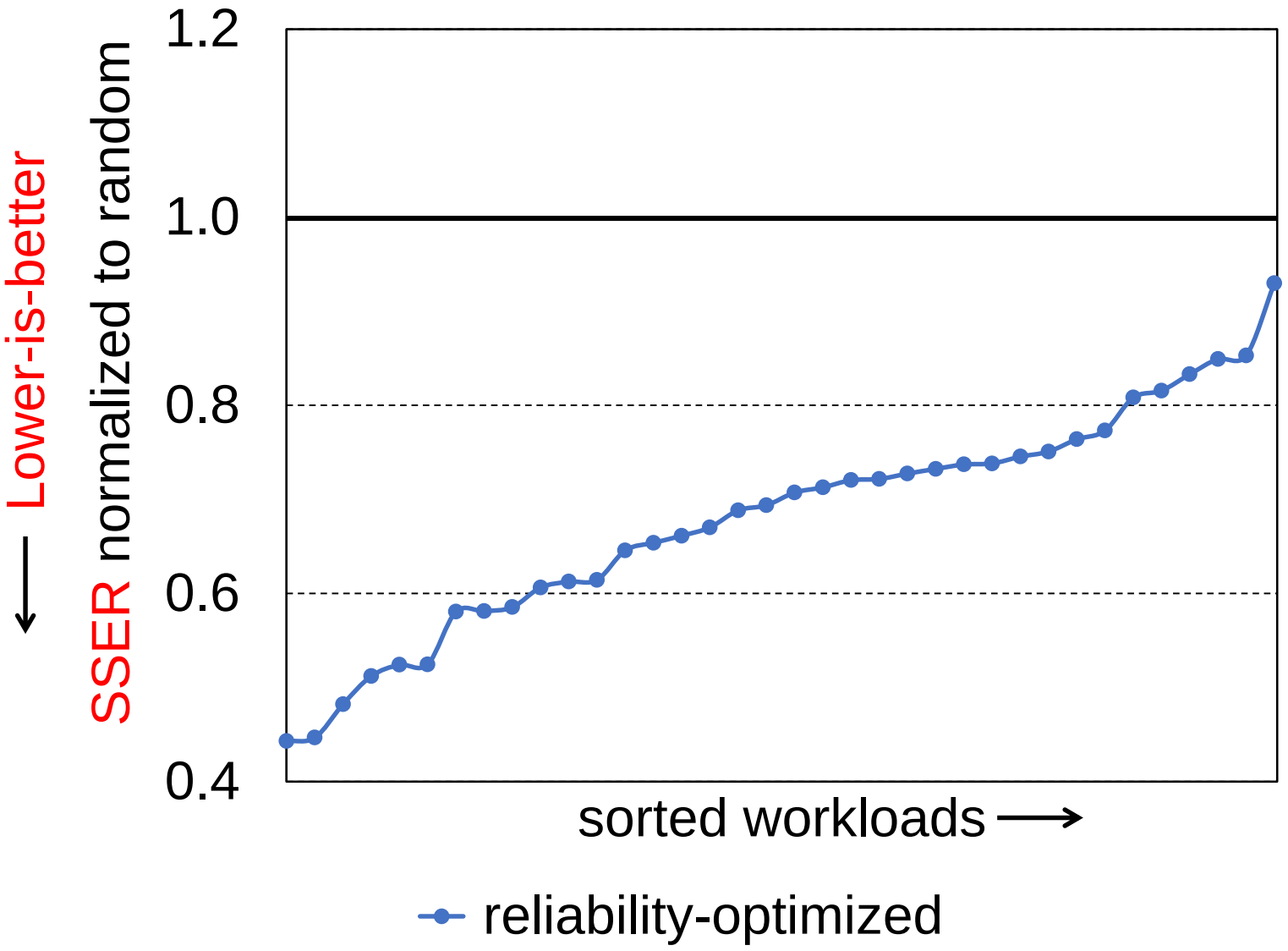
Performance-Optimized Scheduler

-- Optimizes System Throughput (STP)

Random Scheduler

-- Randomly selects applications to run on the big core(s)

# 2B2S Results – Reliability




Compared to random

Reliability-optimized
-- improves SSER by 32%

-- up to 55.6%

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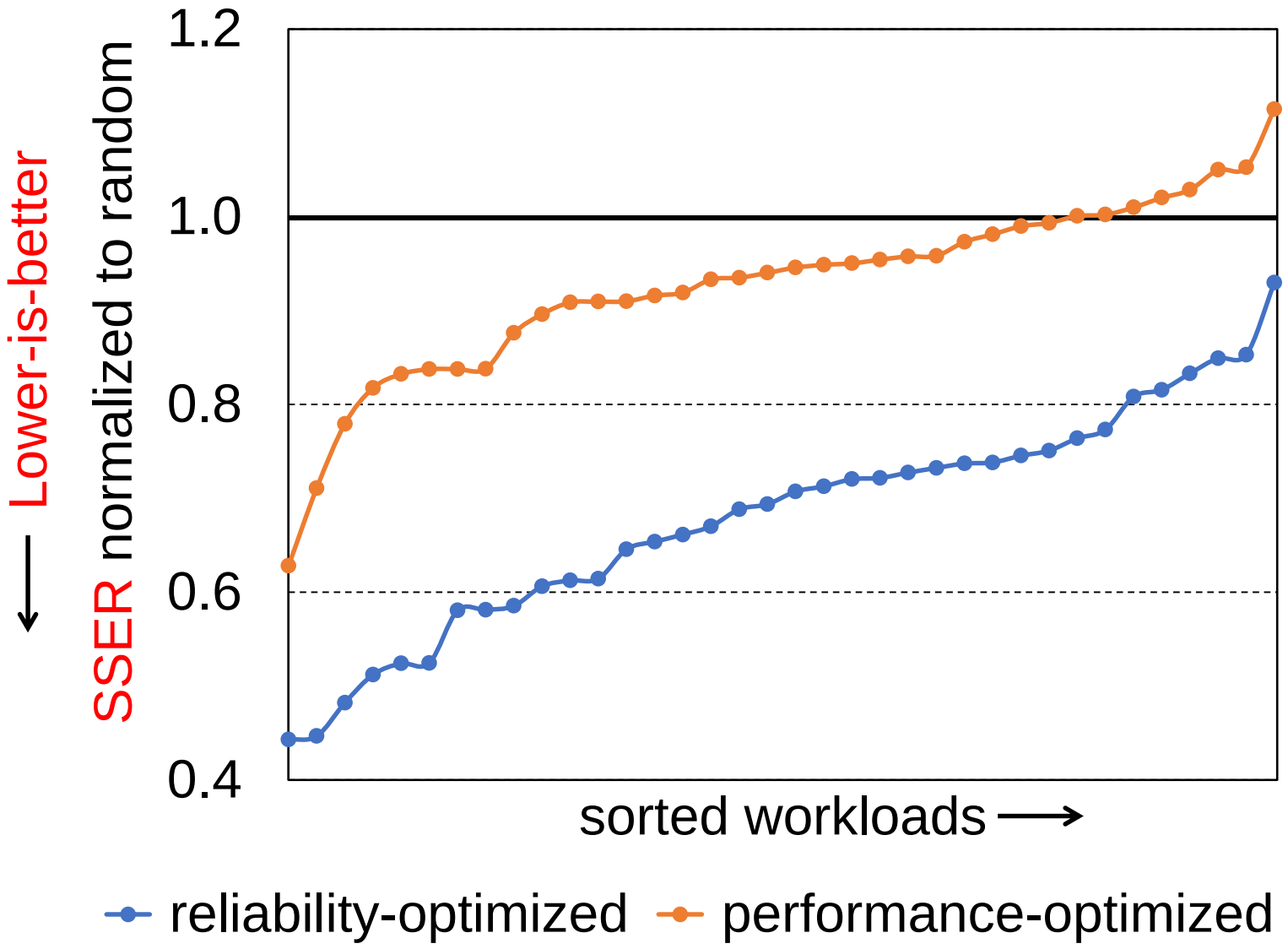


Compared to random

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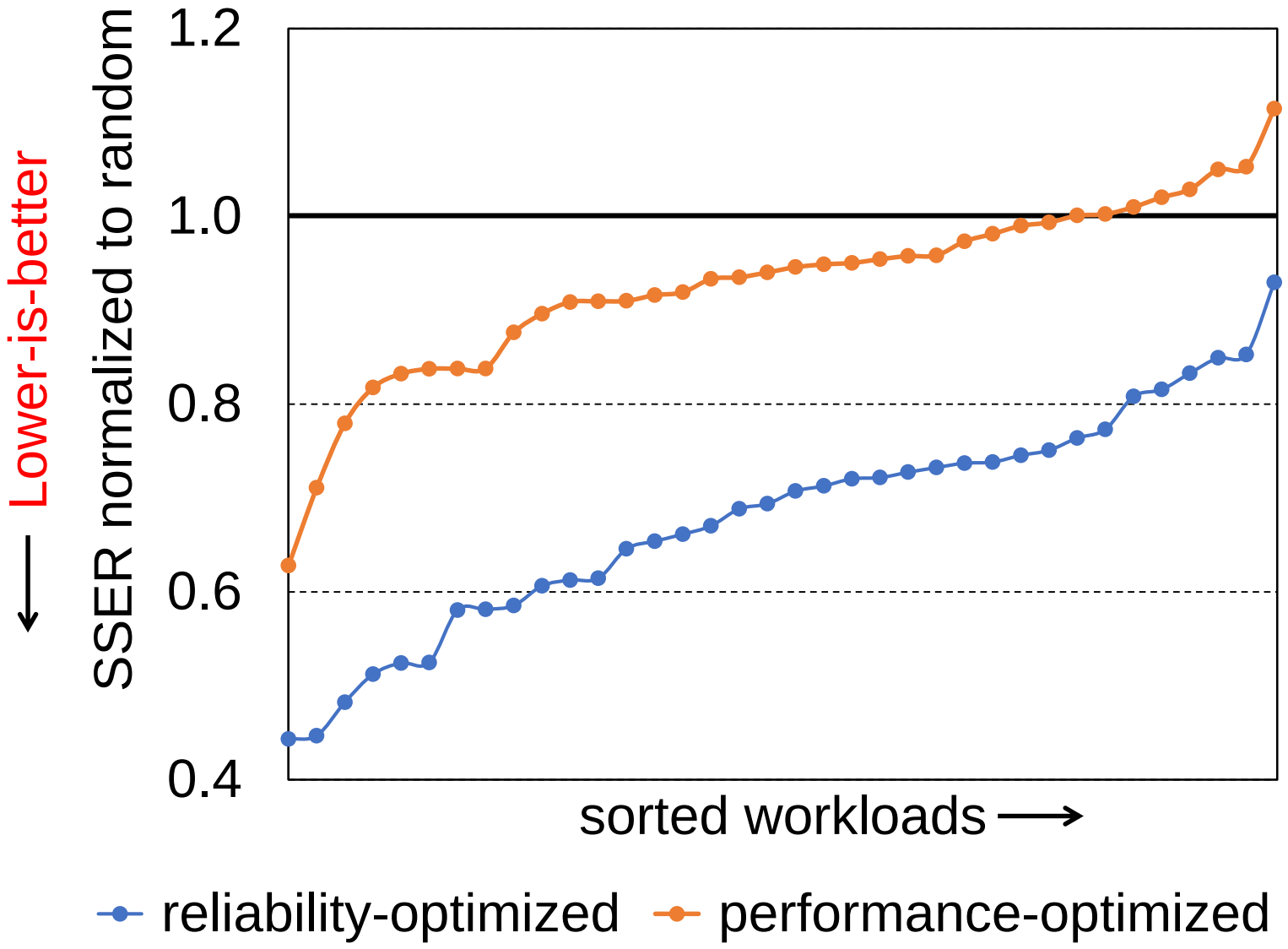
Performance-optimized
-- improves SSER by 7.3%

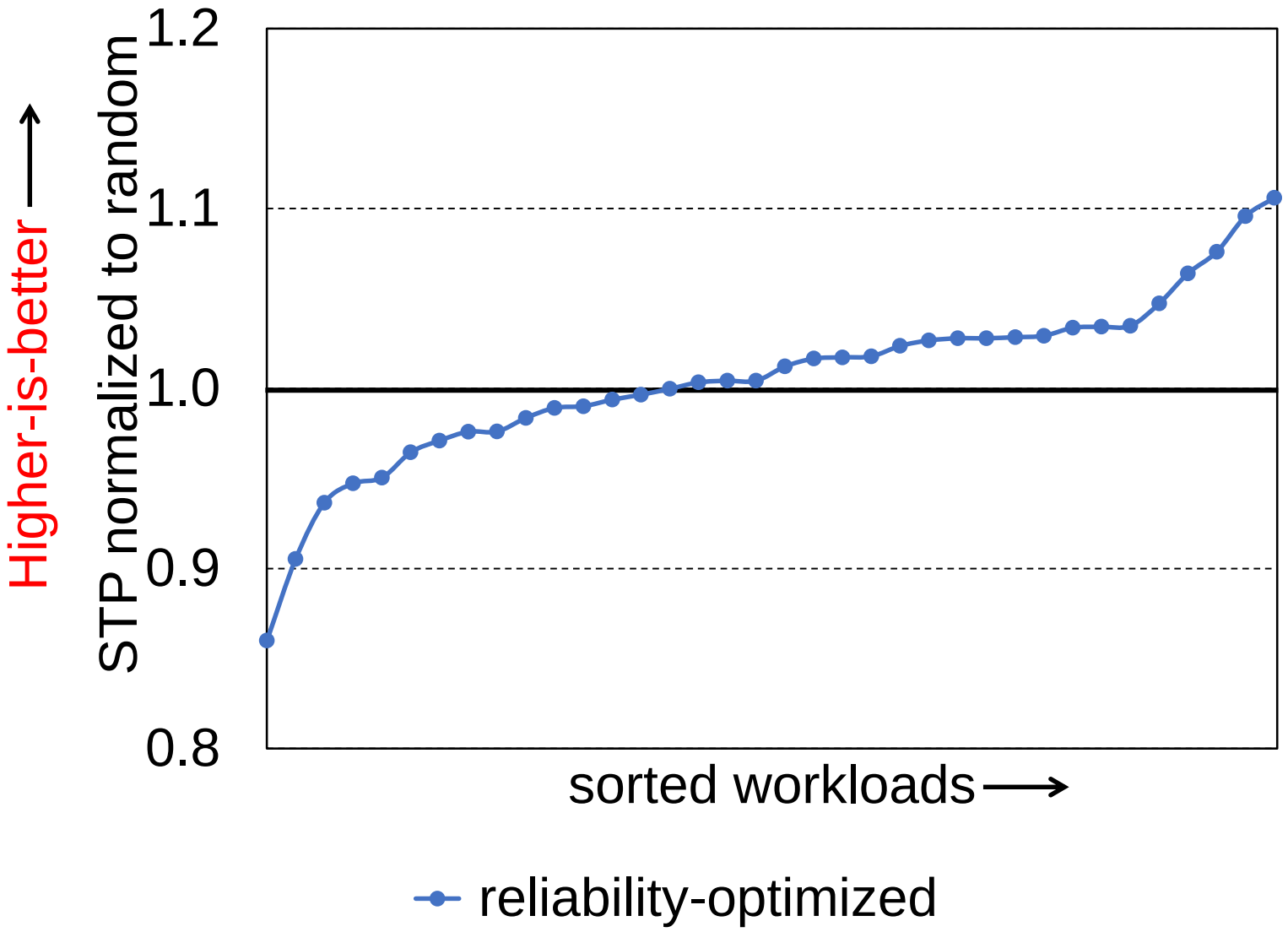
# 2B2S Results – Reliability




Compared to performance-optimized

Reliability-optimized
-- improves SSER by 25.4%
-- up to 60.2%

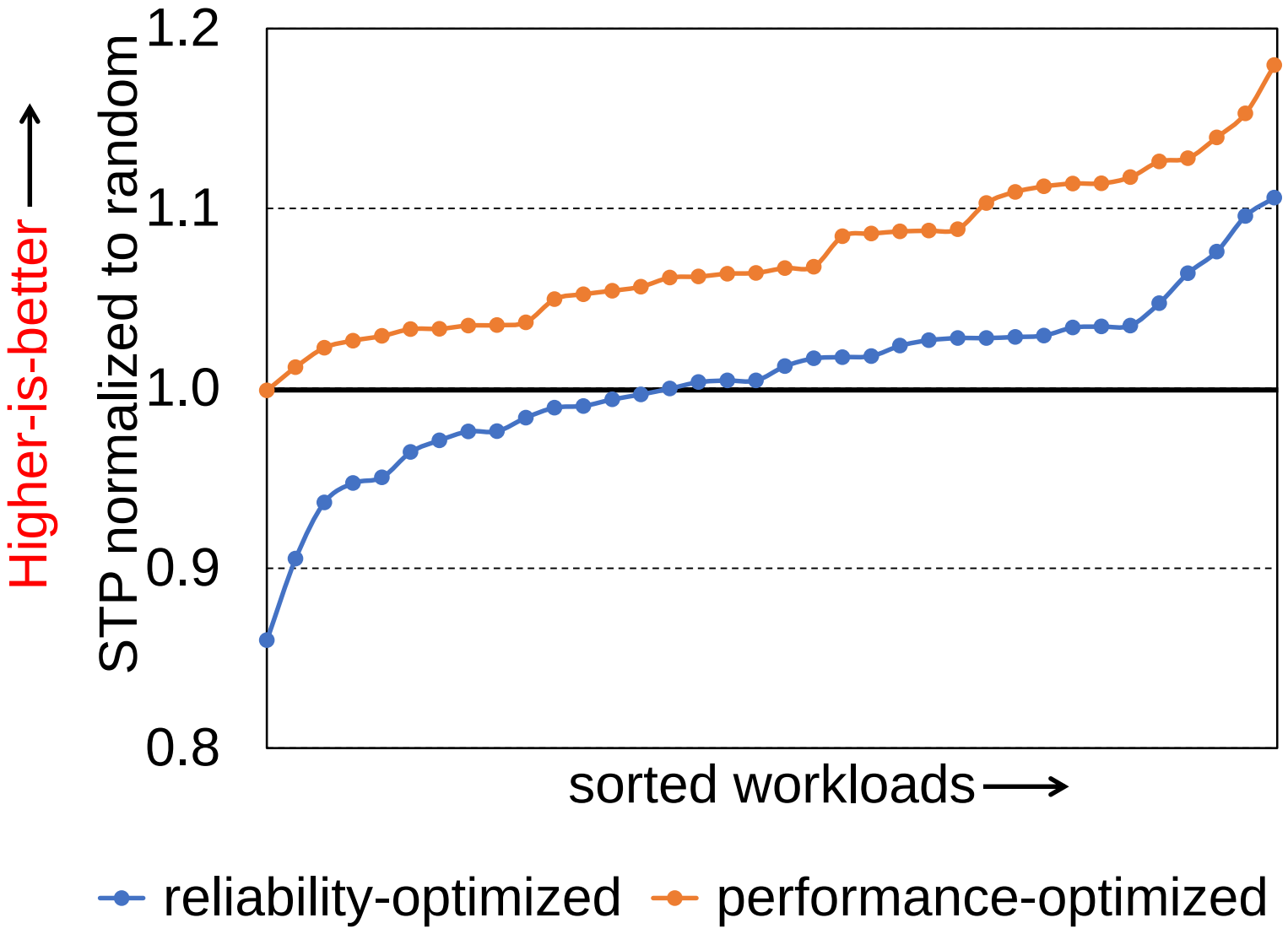
# 2B2S Results – Performance




Compared to random

Reliability-optimized
-- does not degrade STP

# 2B2S Results – Performance



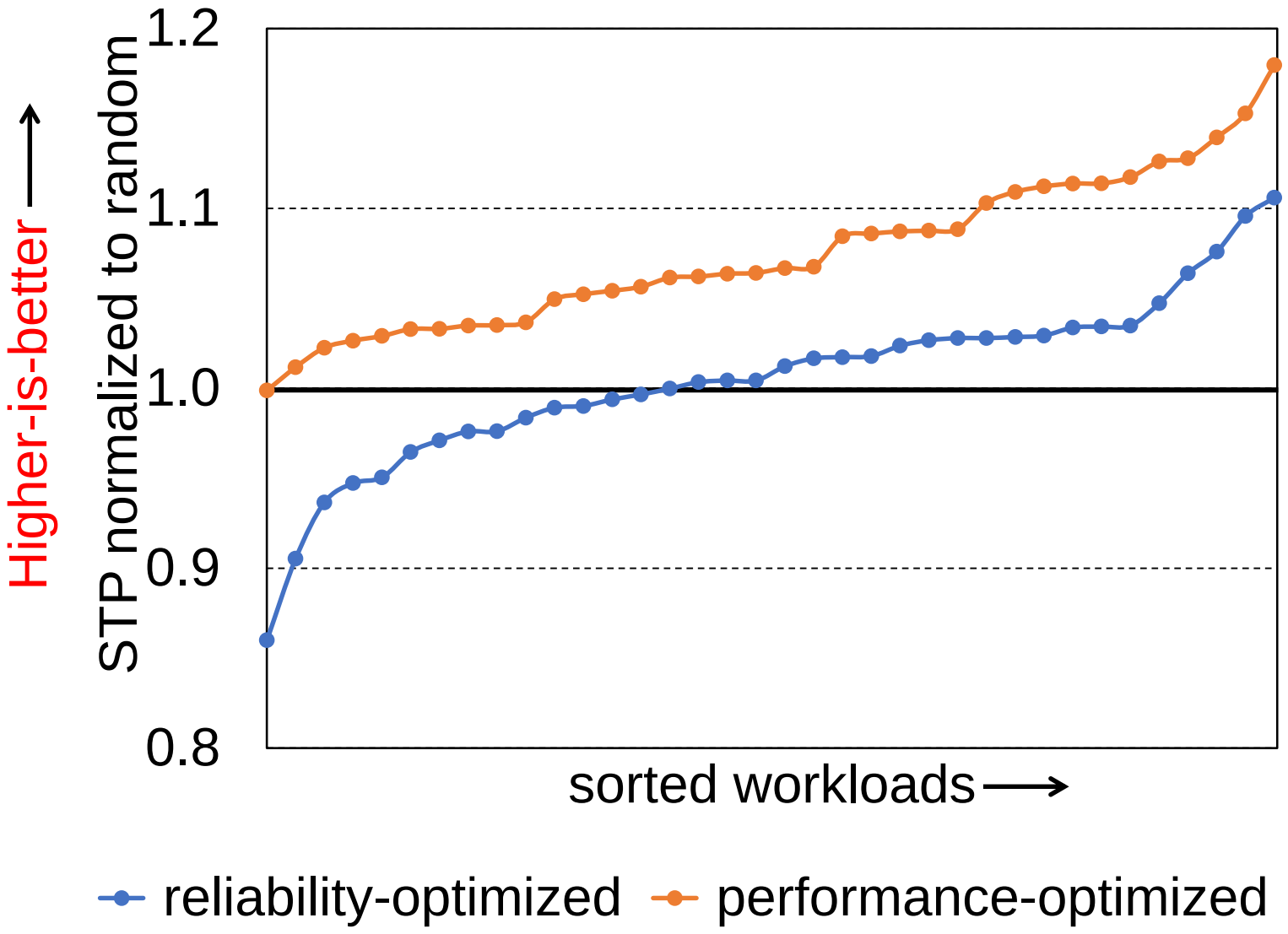

Compared to random

Reliability-optimized
-- does not degrade STP

Performance-optimized
-- improves STP by 6.3%

-- up to 18.7%

# 2B2S Results – Performance

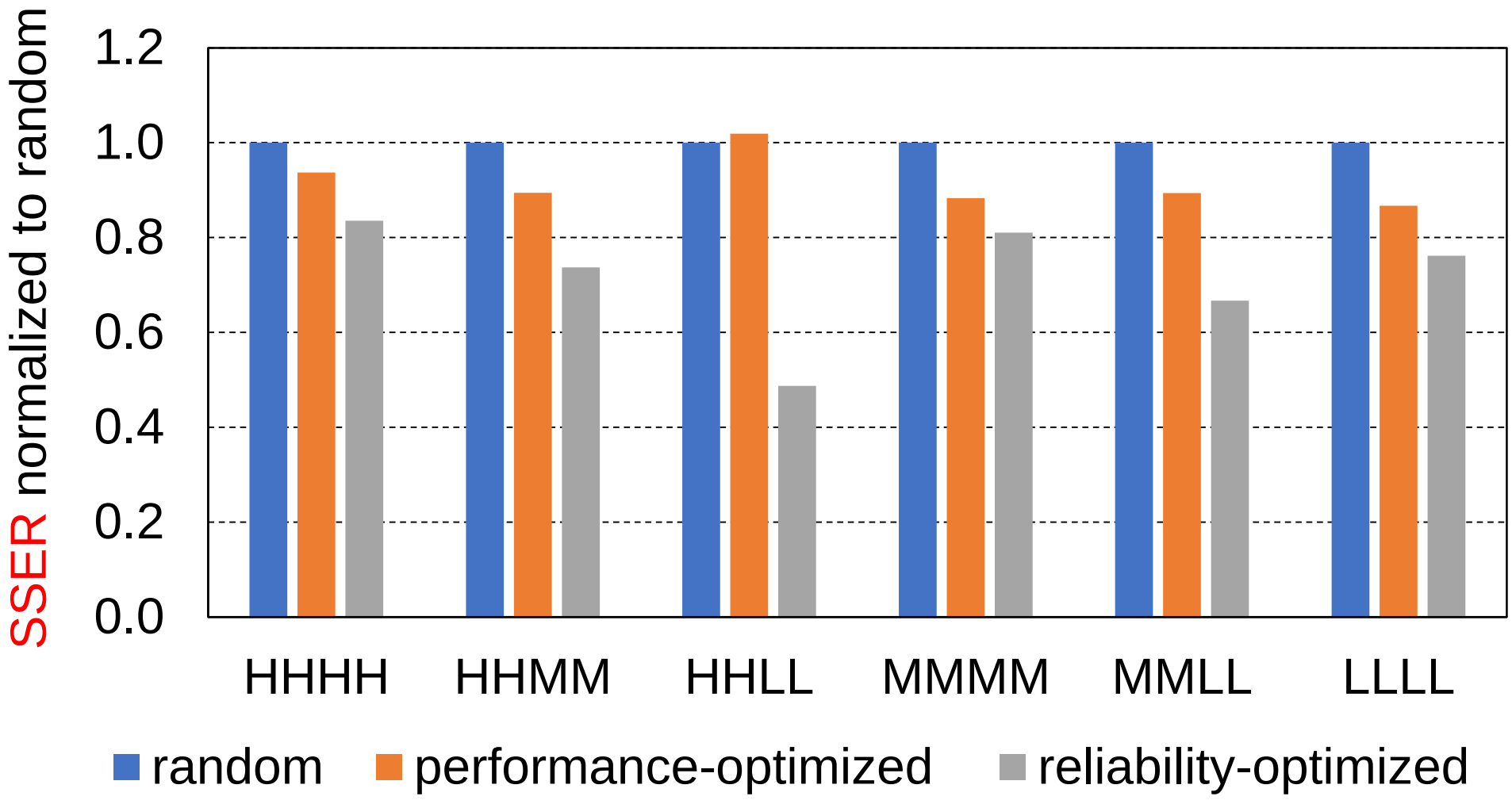



Compared to performance-optimized

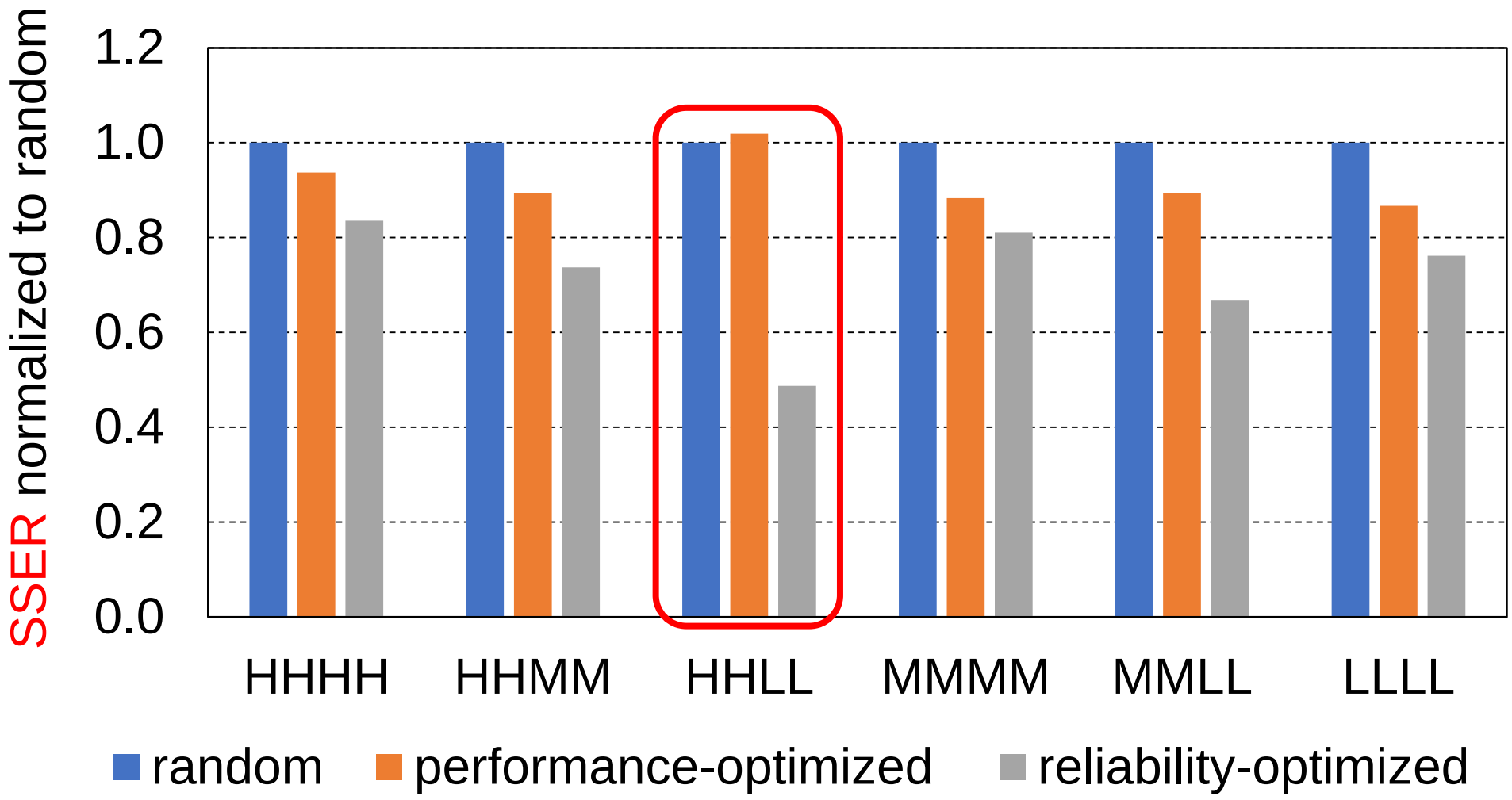
Reliability-optimized
-- degrades STP by 6.3%

-- up to 18.7%

# 2B2S Results – by Workload Category

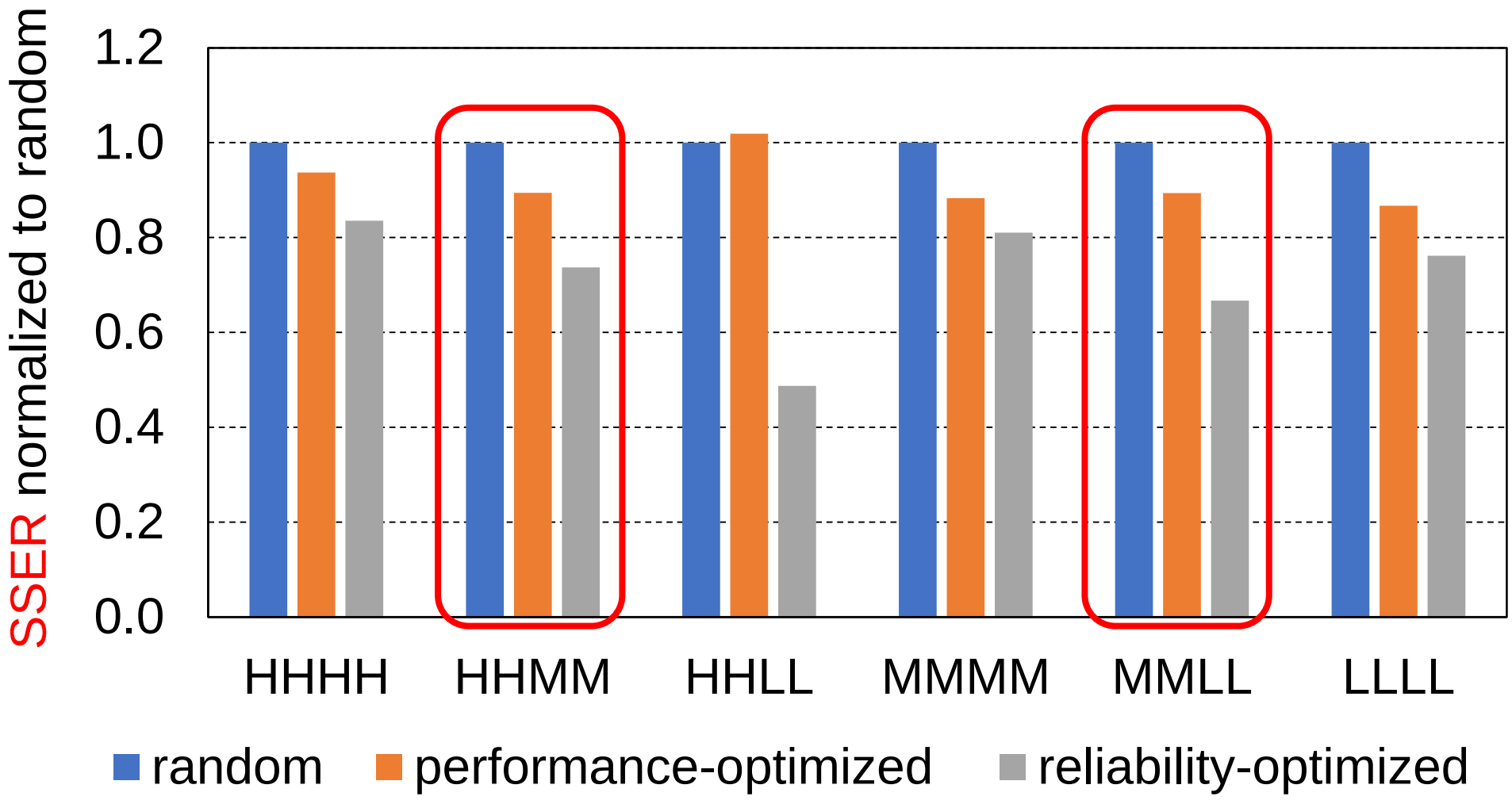


# 2B2S Results – by Workload Category




HHLL 53.2%

# 2B2S Results – by Workload Category

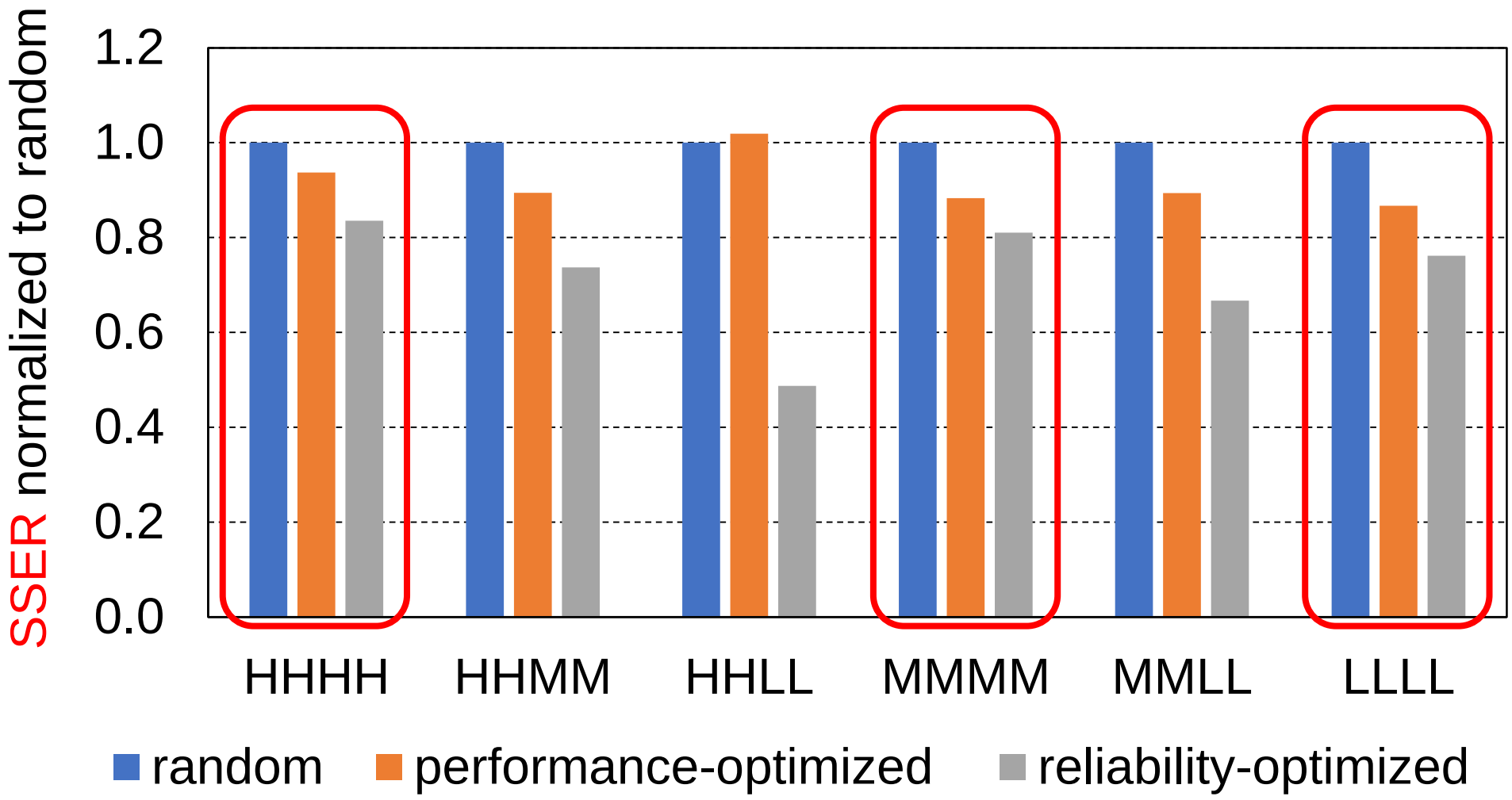



HHLL 53.2%

HHMM 15.8%

MMLL 22.7%

# 2B2S Results – by Workload Category




HHLL 53.2%

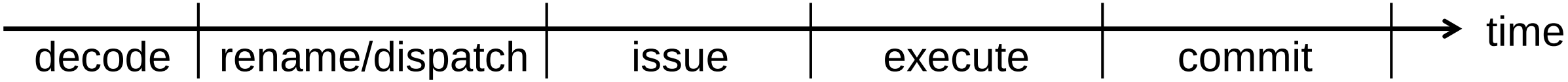
HHMM 15.8%
MMLL 22.7%

HHHH 10.2%
MMMM 7.3%
LLLL 10.6%

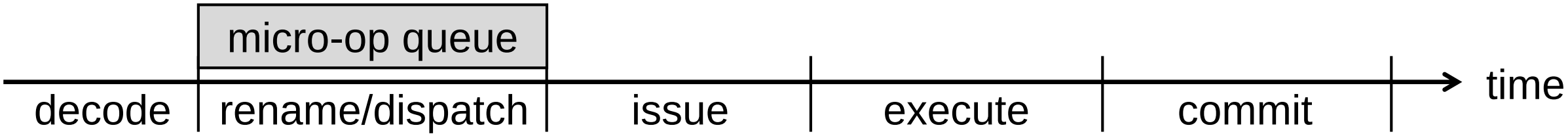
# Contribution #2 [DSN 2020, Under review]

# Dispatch Halting to Improve Out-of-Order Core Reliability

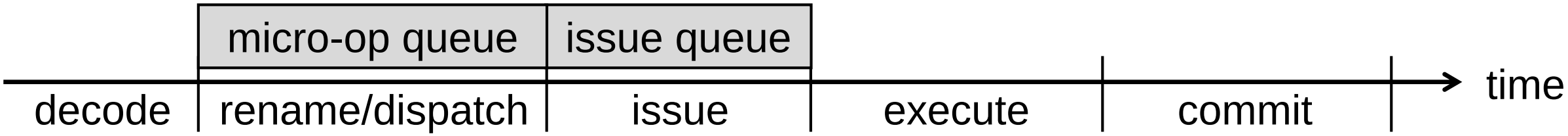
# Vulnerability of Out-of-Order Core Resources



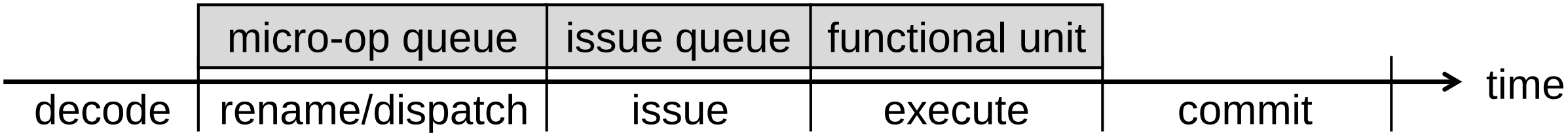
# Vulnerability of Out-of-Order Core Resources



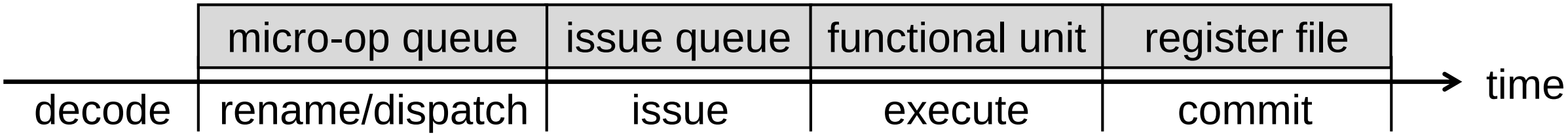
# Vulnerability of Out-of-Order Core Resources



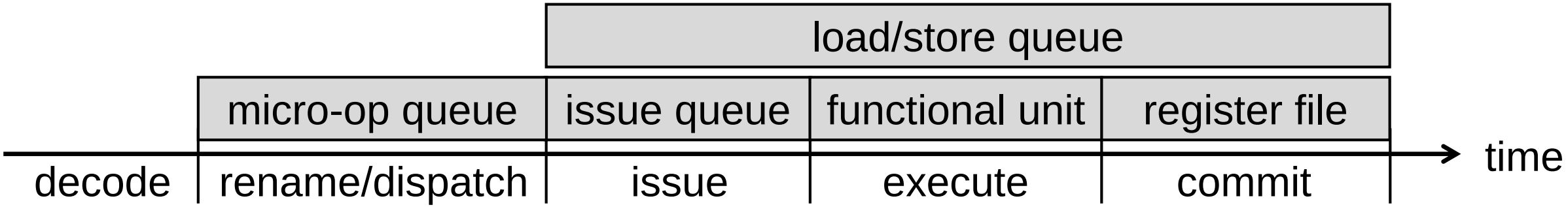
# Vulnerability of Out-of-Order Core Resources



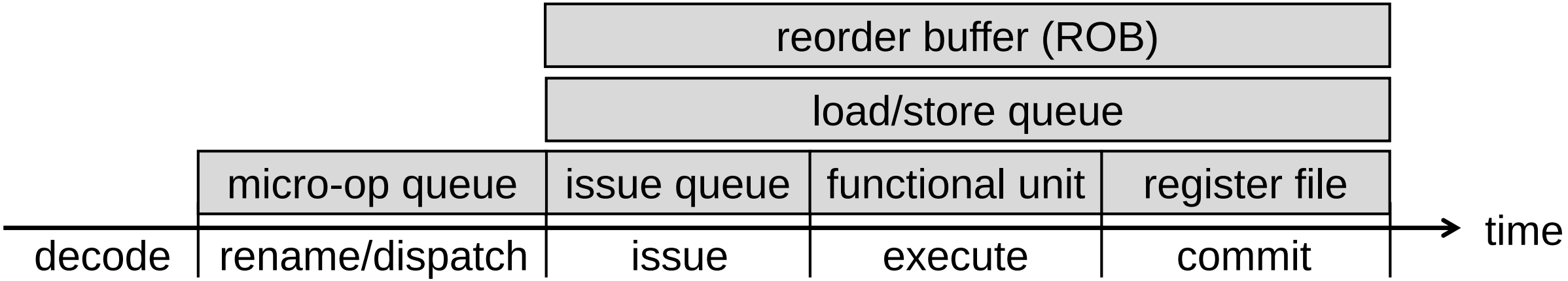
# Vulnerability of Out-of-Order Core Resources



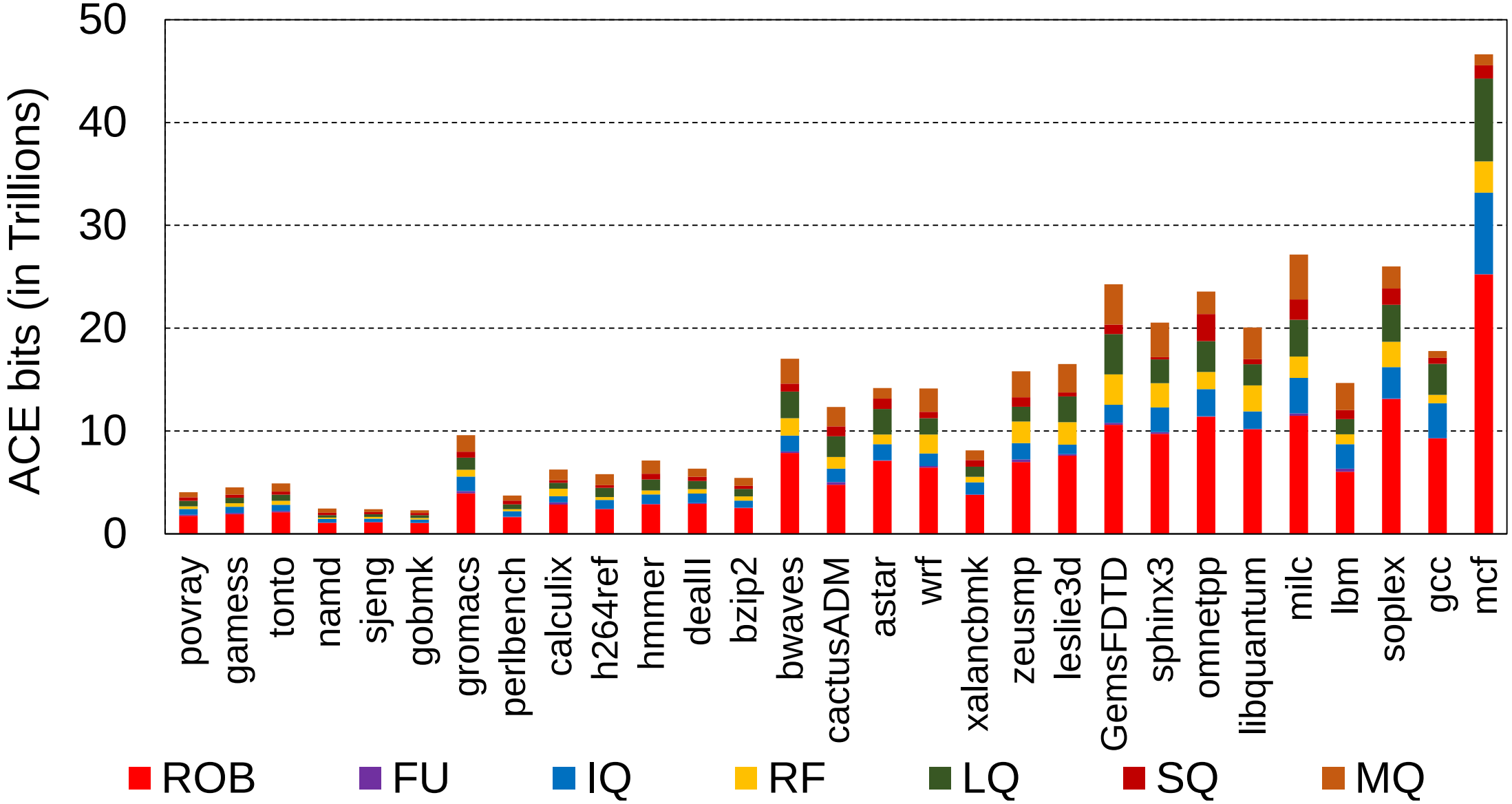
# Vulnerability of Out-of-Order Core Resources



# Vulnerability of Out-of-Order Core Resources



# ACE Bit Count for OoO Resources



# Vulnerable State under Full-ROB Stalls

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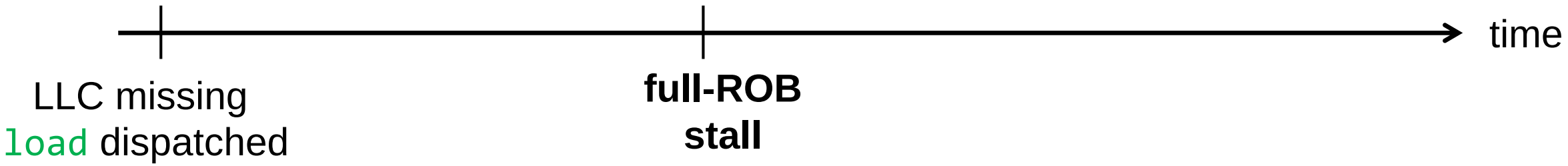

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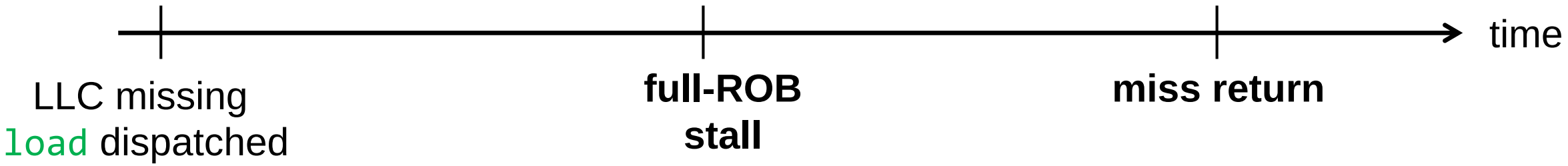
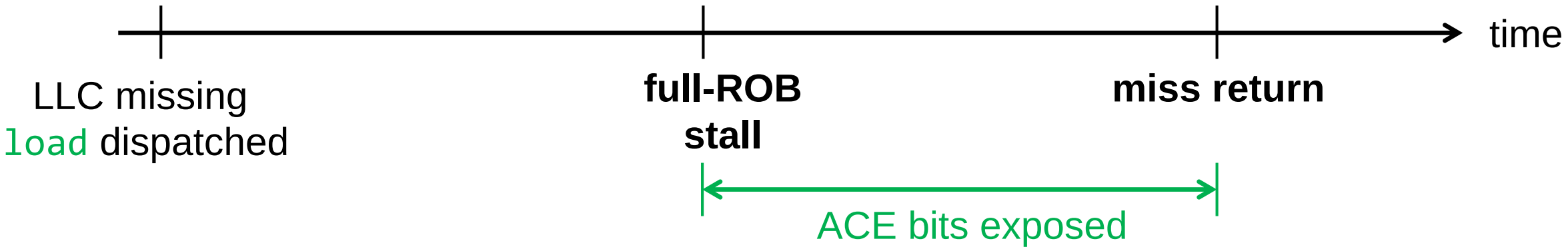
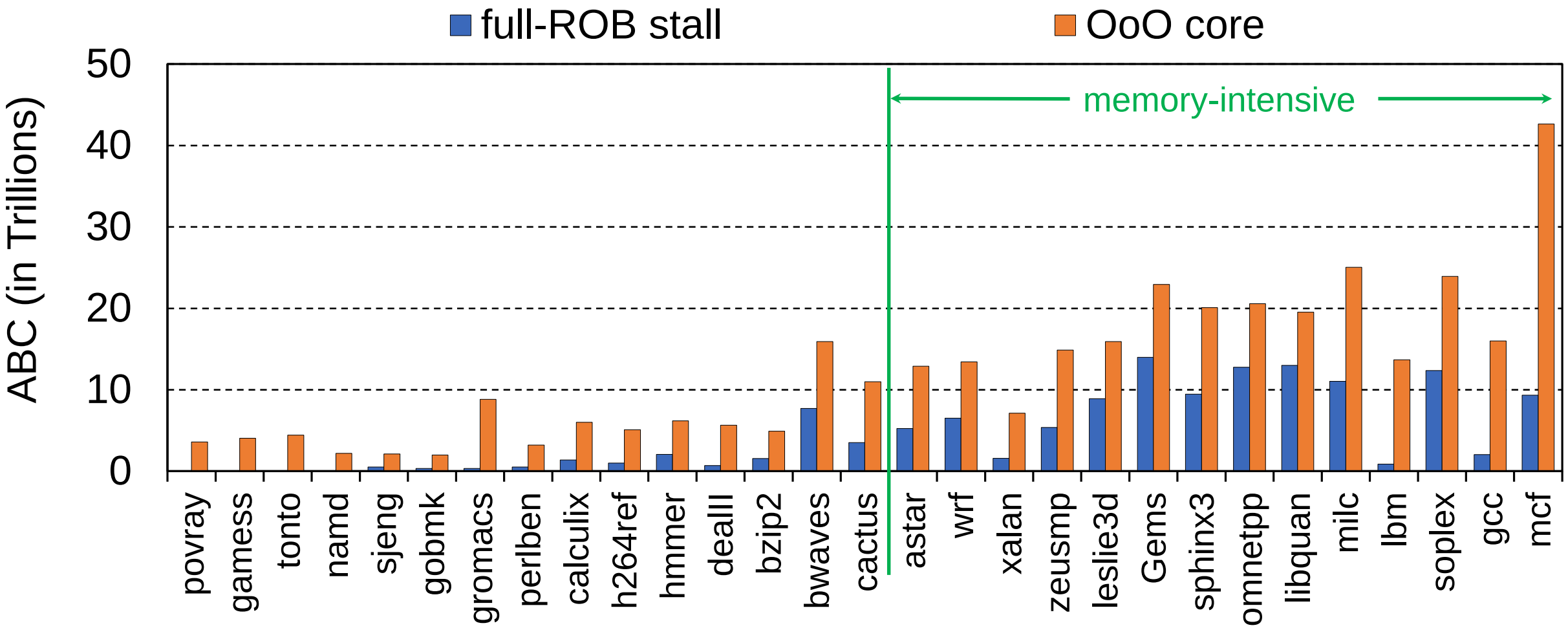


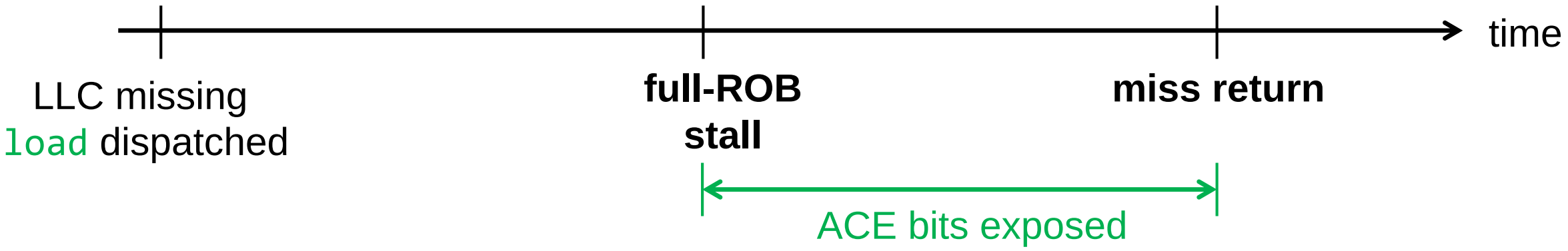
# Vulnerable State under Full-ROB Stalls



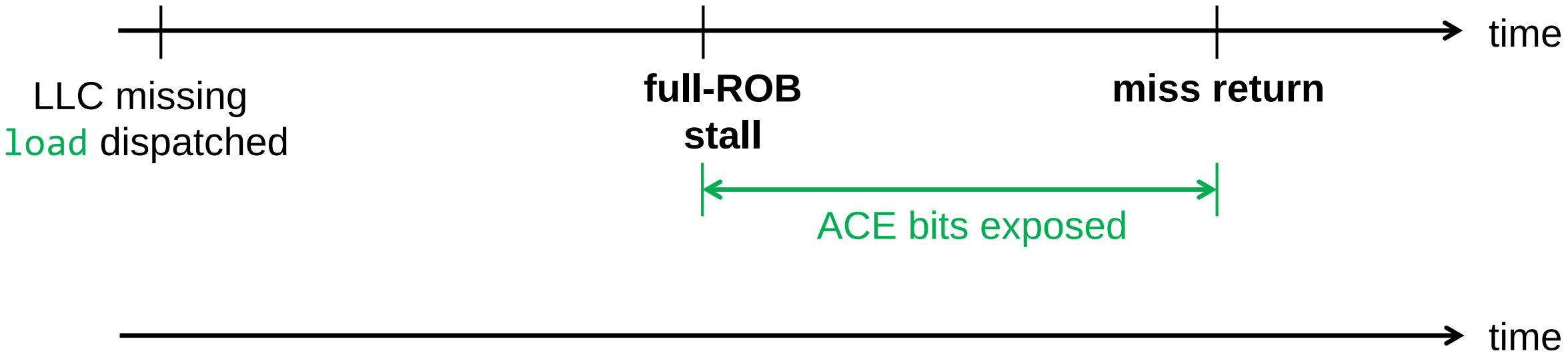
# Vulnerable State under Full-ROB Stalls



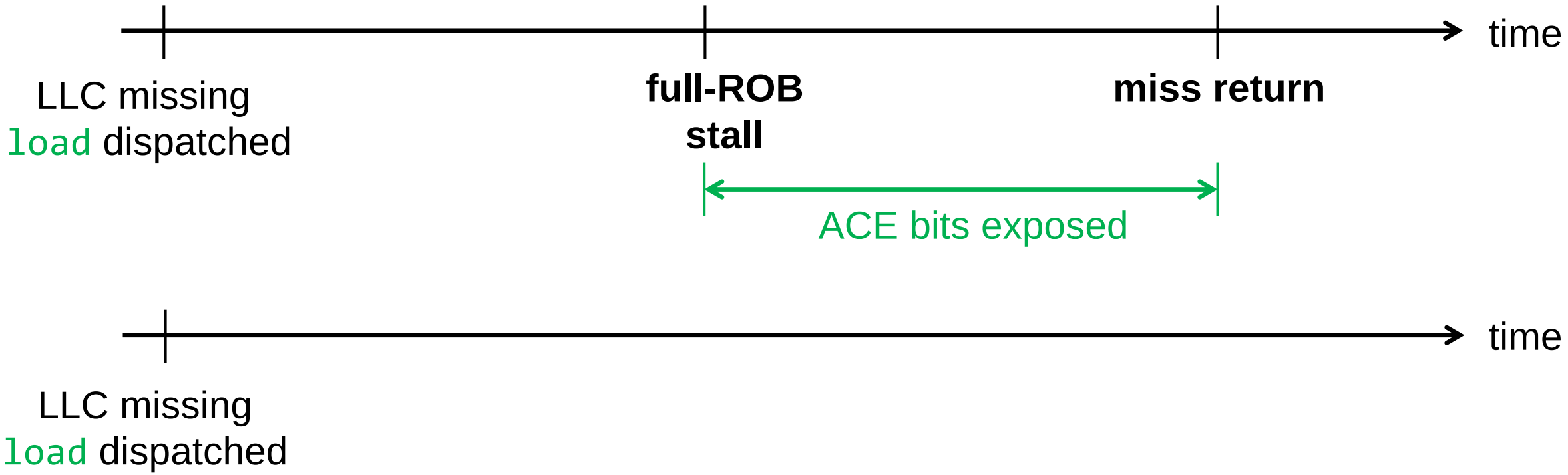
# Vulnerable State under Blocked ROB Head



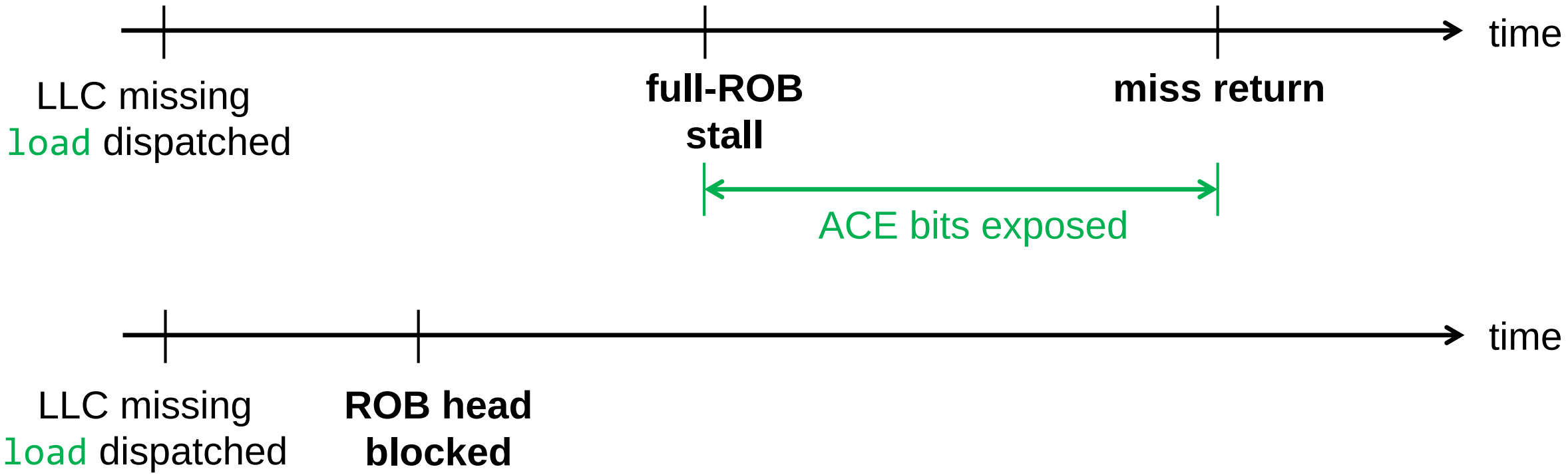
# Vulnerable State under Blocked ROB Head



# Vulnerable State under Blocked ROB Head



# Vulnerable State under Blocked ROB Head



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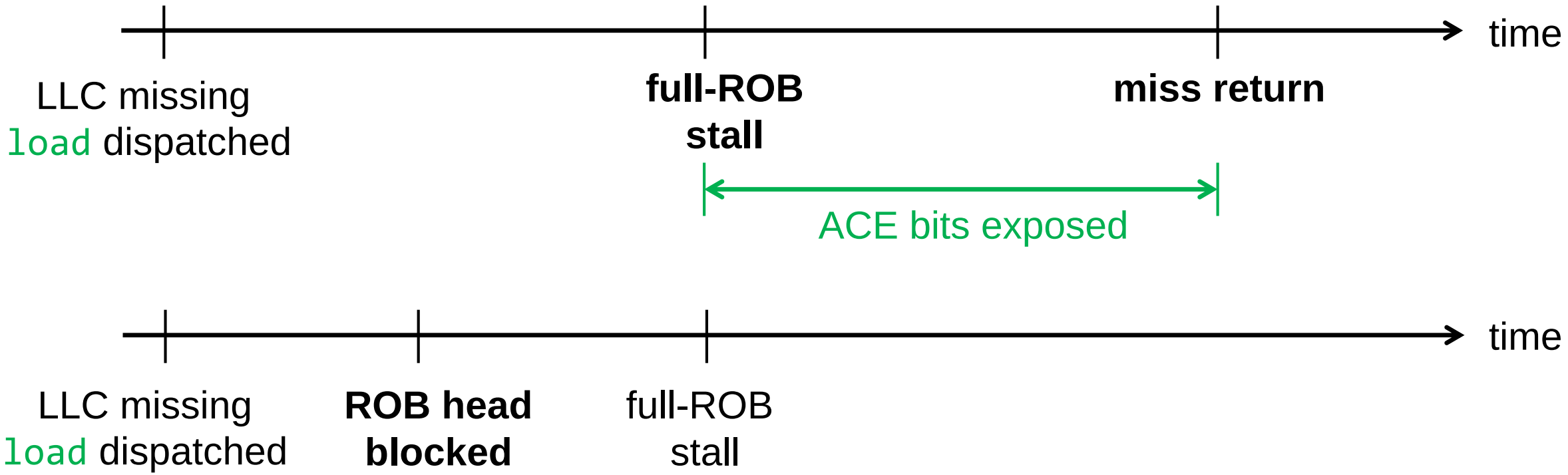
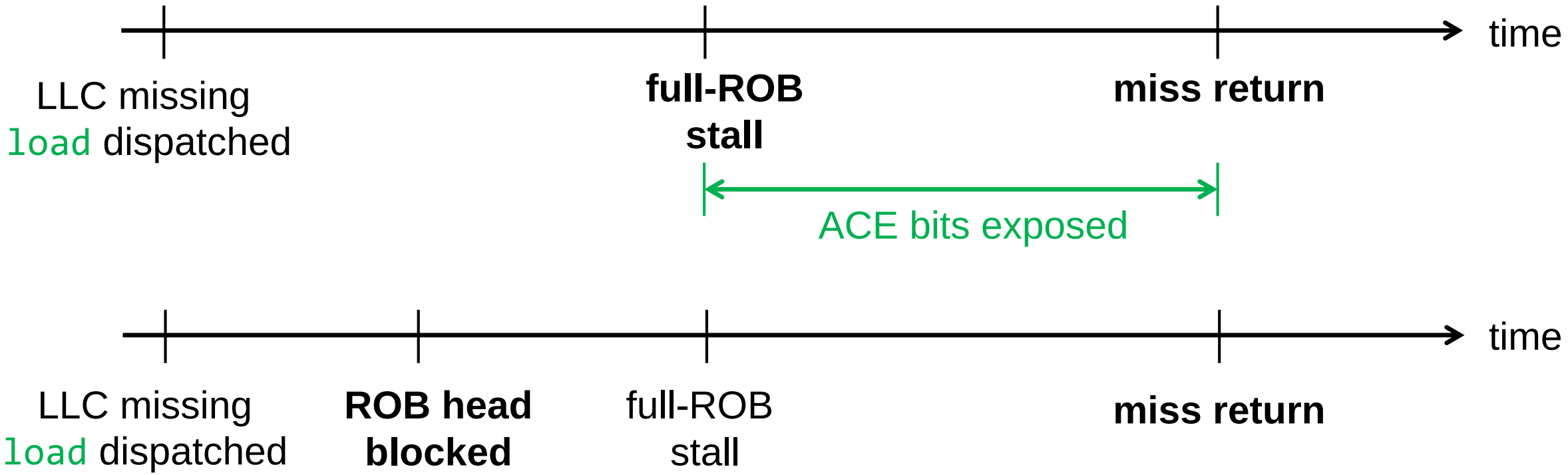
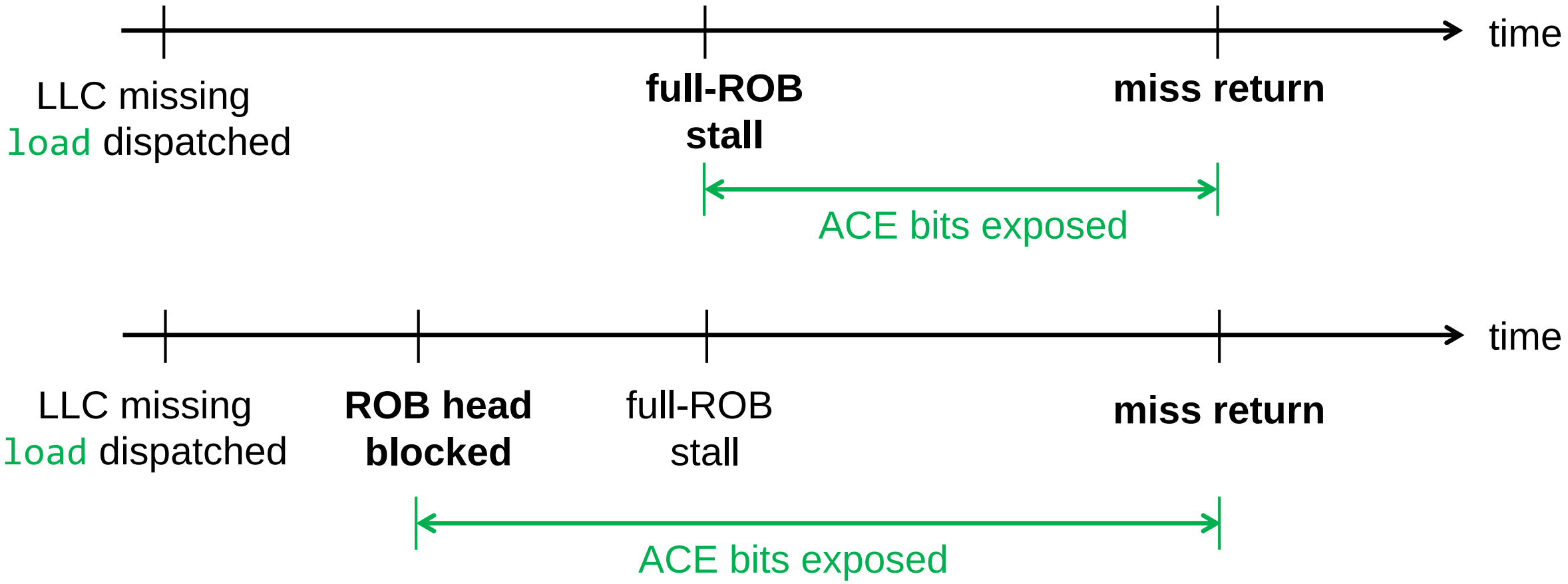


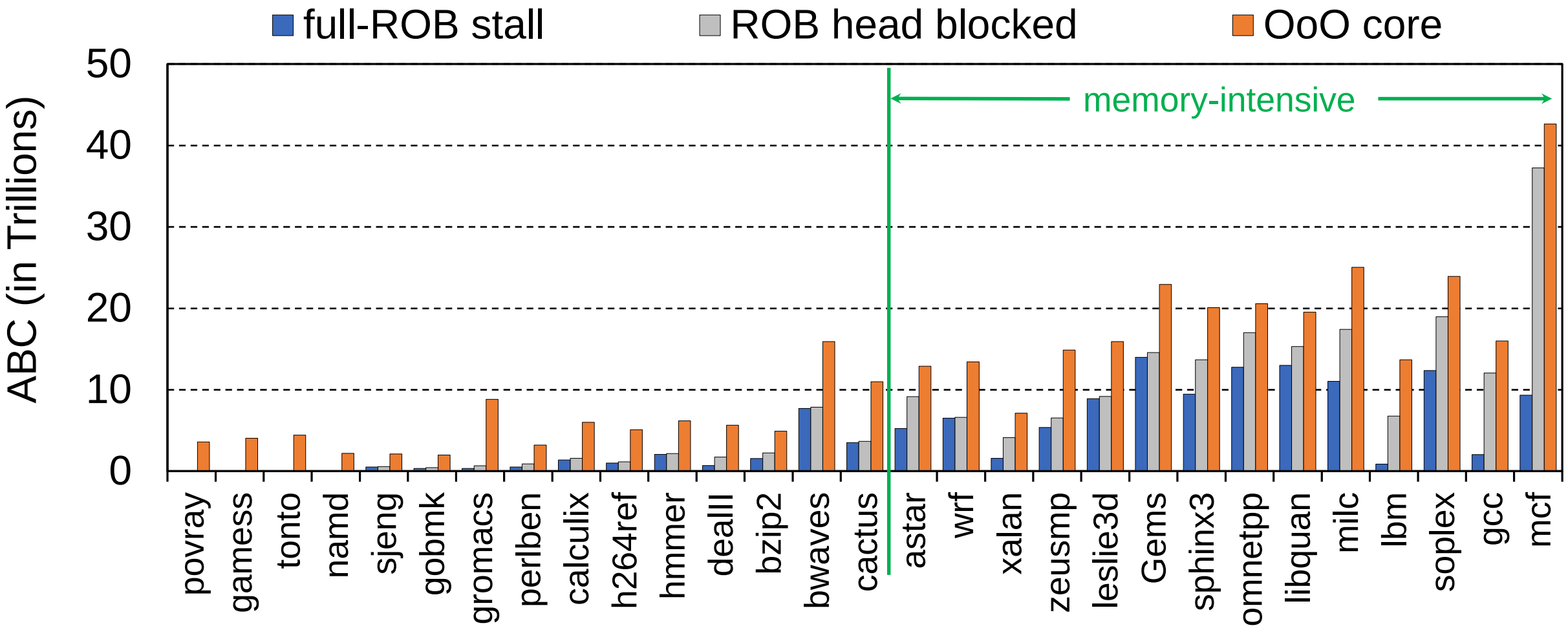
# Vulnerable State under Blocked ROB Head



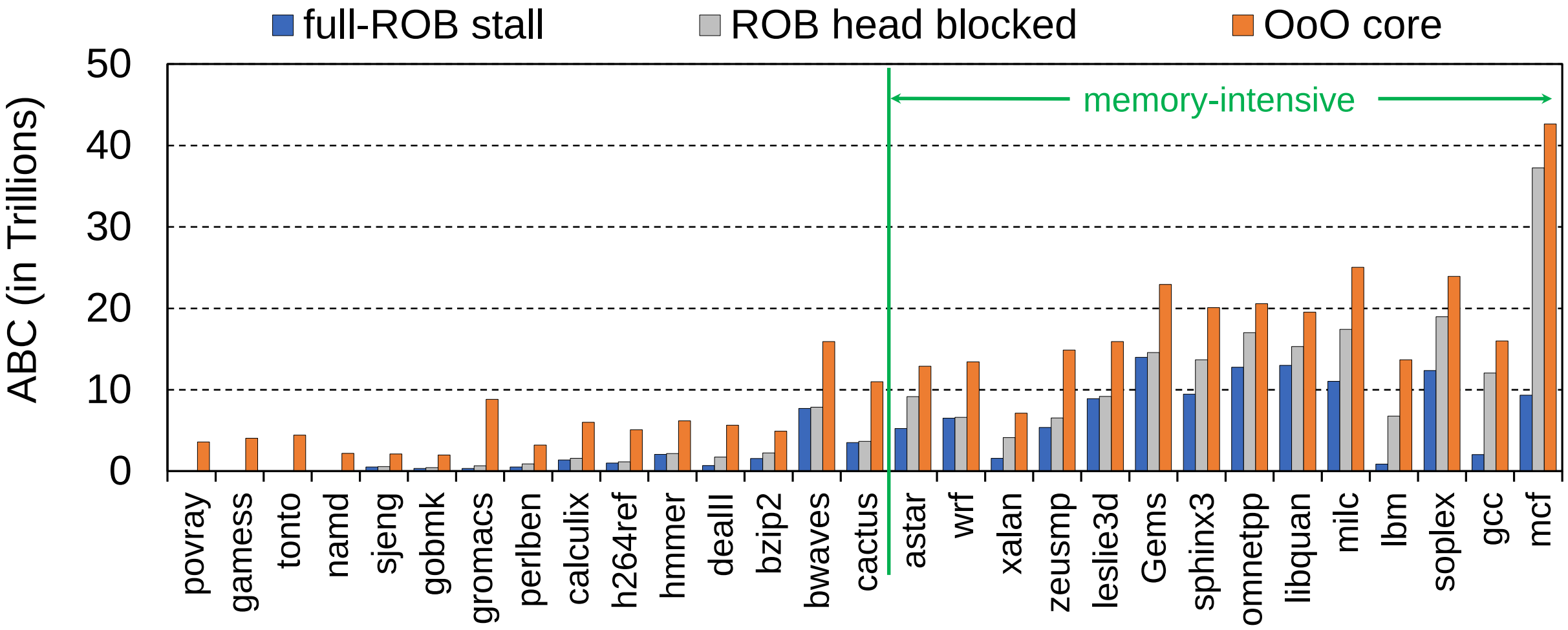
# Vulnerable State under Blocked ROB Head



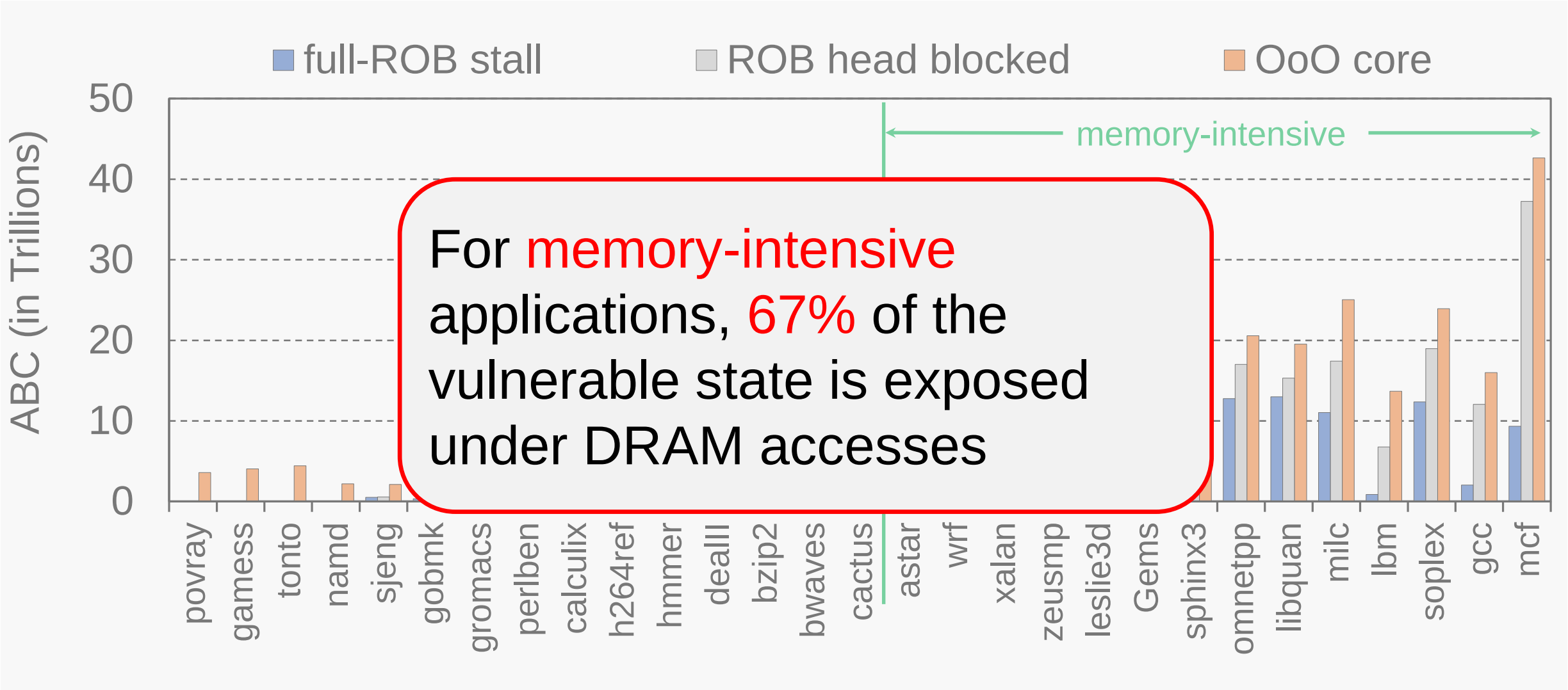
# Vulnerable State under Blocked ROB Head



# Quantifying the Potential



# Quantifying the Potential




For memory-intensive applications, 67% of the vulnerable state is exposed under DRAM accesses

# Dispatch Halting to Improve Reliability

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Proactively prevent instructions following an LLC missing load to allocate entries in the ROB (or back-end structures)

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⇒

Proactive Dispatch Halting

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⇒ Proactive Dispatch Halting

Reactively mark the back-end speculative after a blocked ROB head

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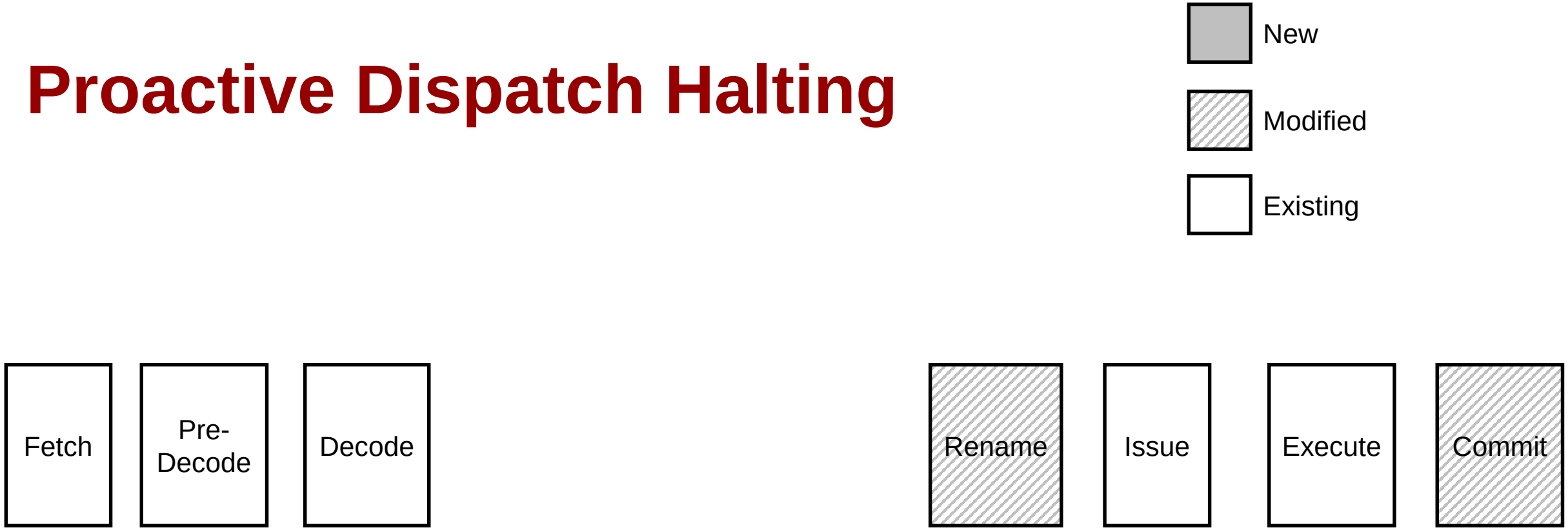
Proactively prevent instructions following an LLC missing load to allocate entries in the ROB (or back-end structures) ⇒ Proactive Dispatch Halting

Reactively mark the back-end speculative after a blocked ROB head ⇒ Reactive Dispatch Halting

# Proactive Dispatch Halting



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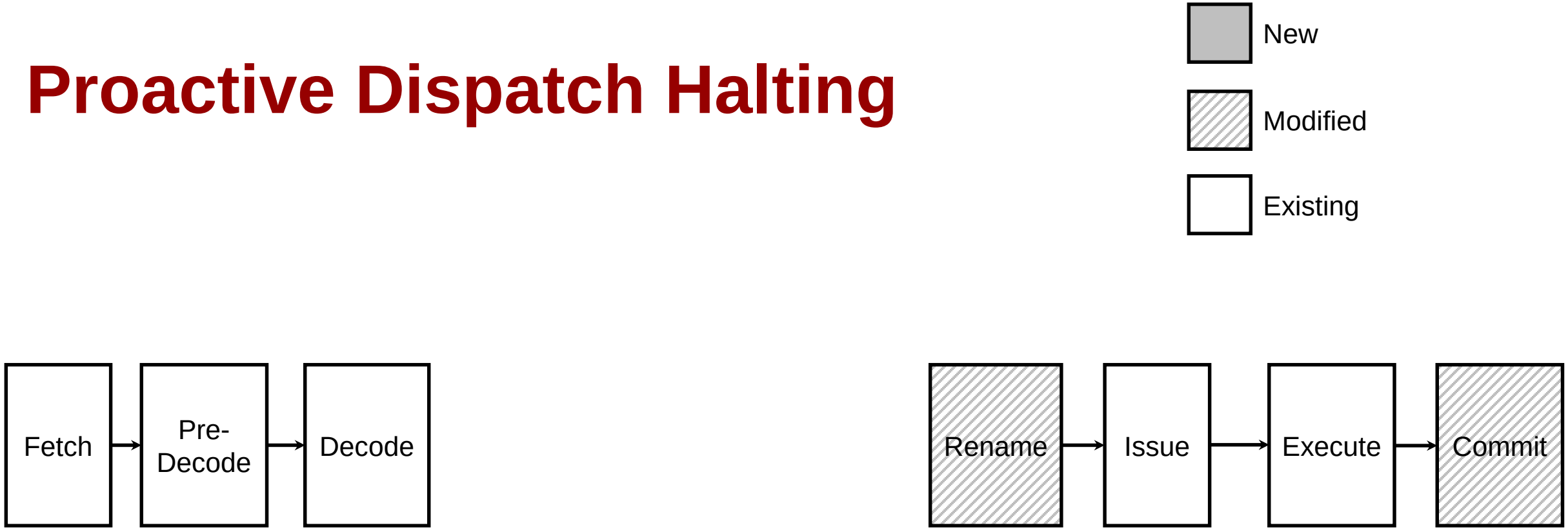

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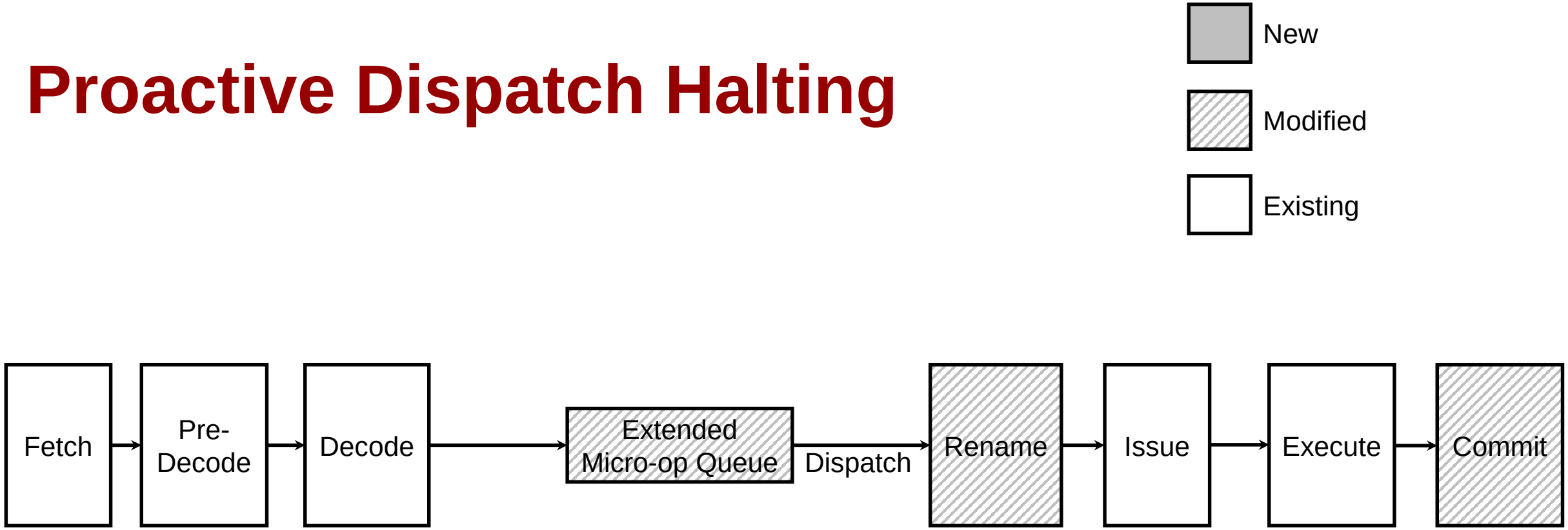

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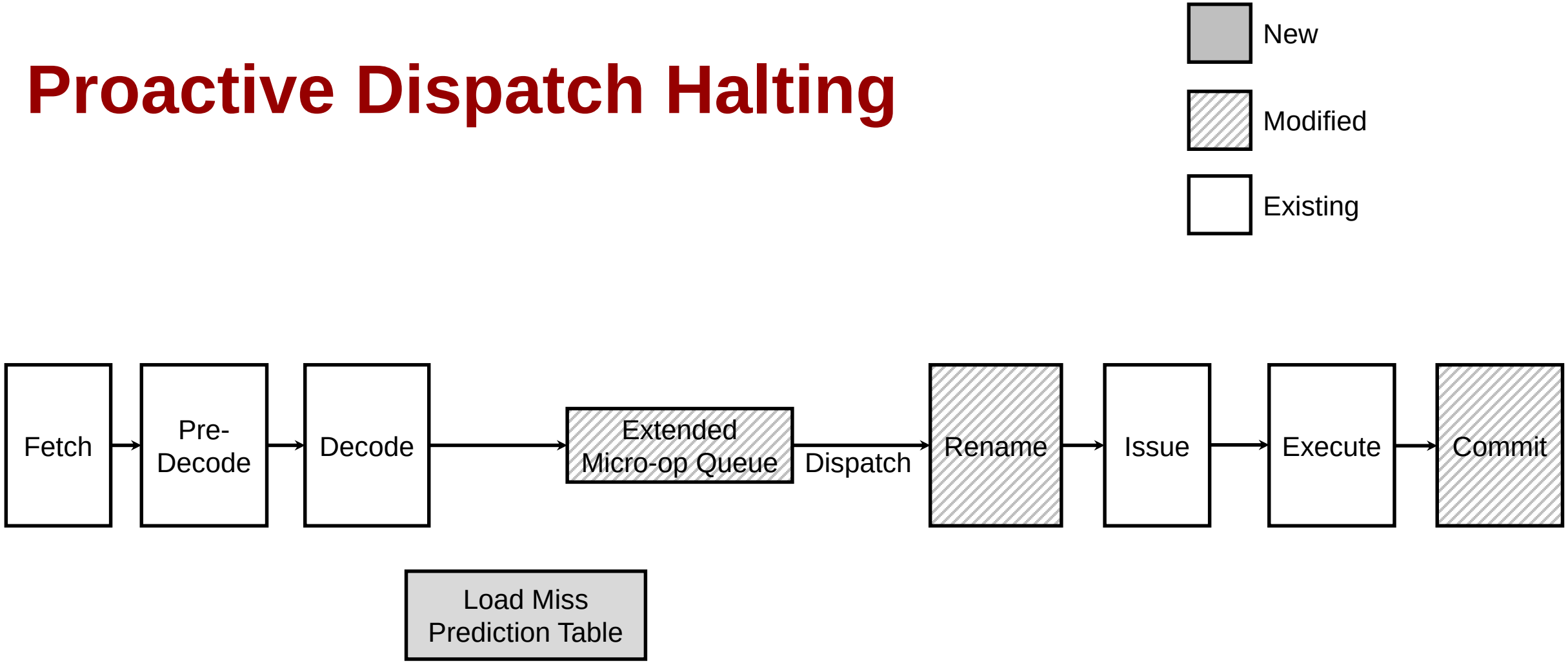

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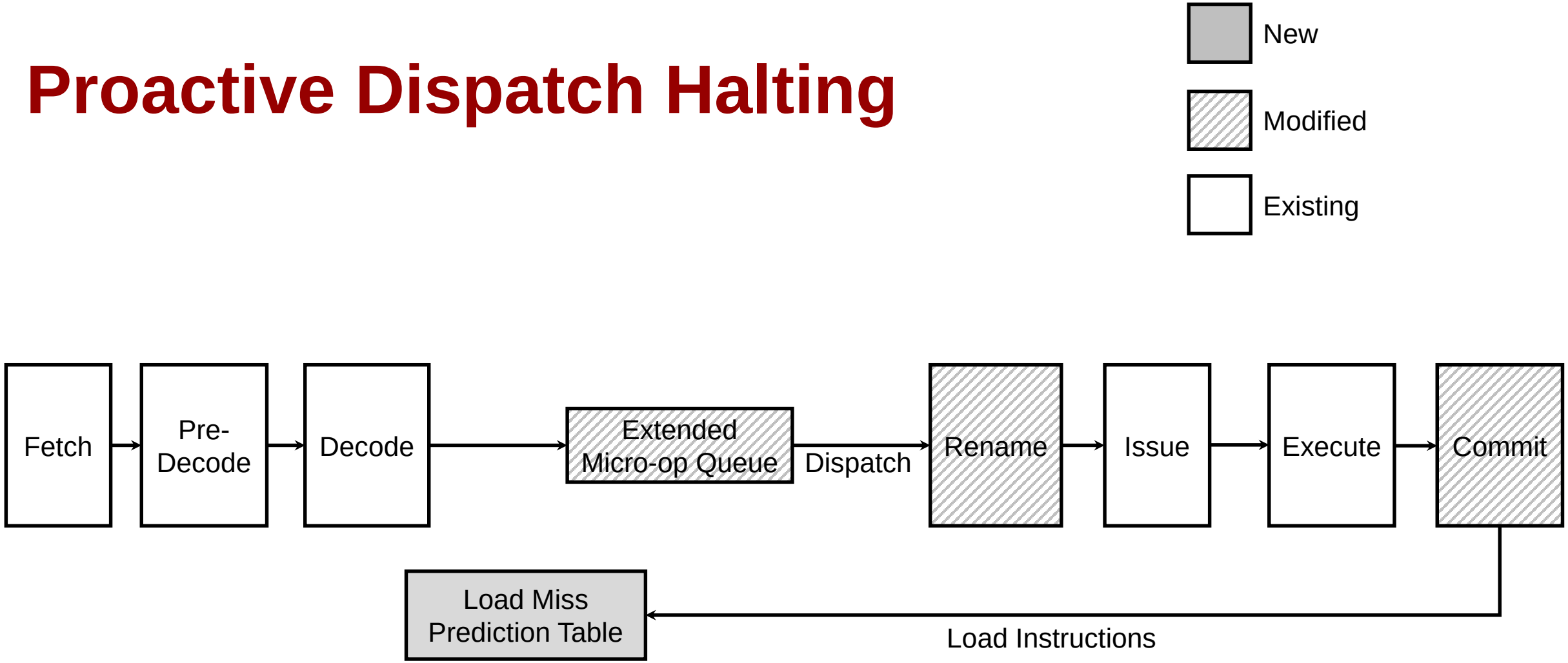

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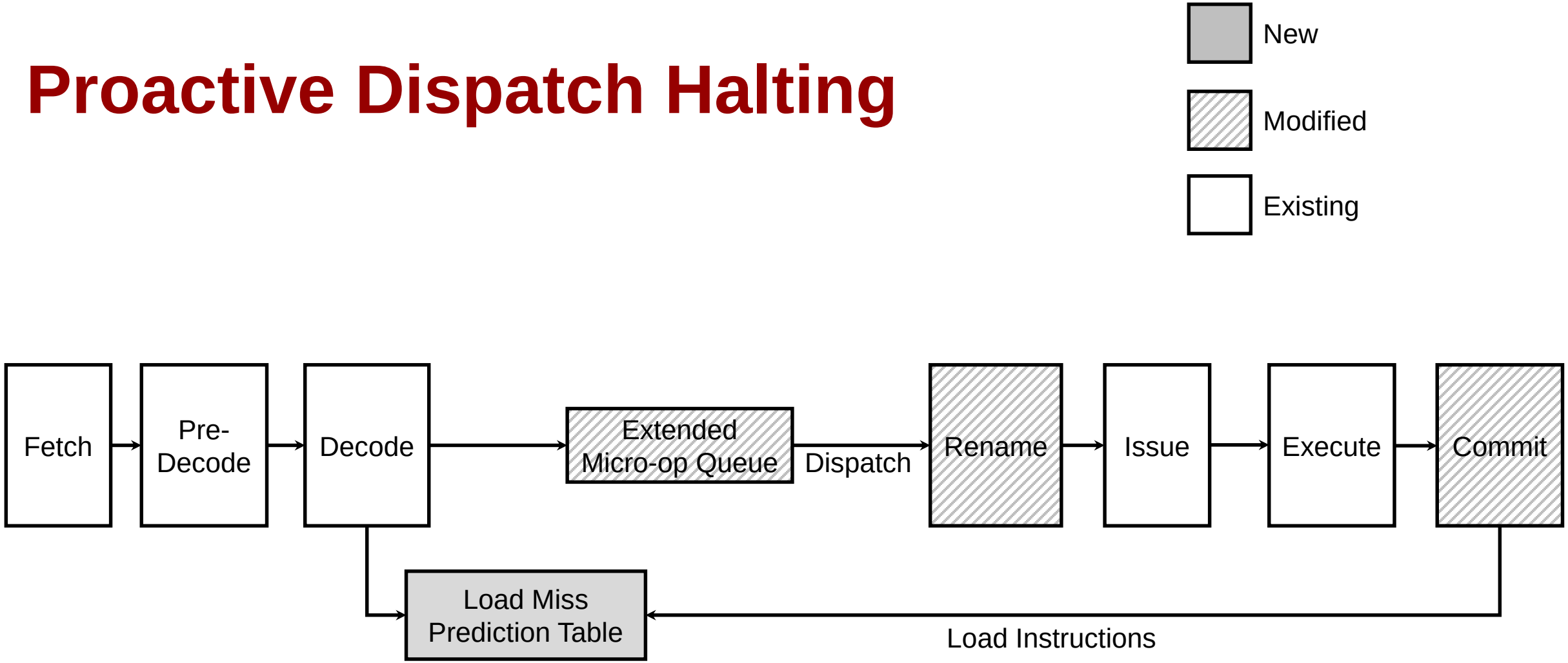
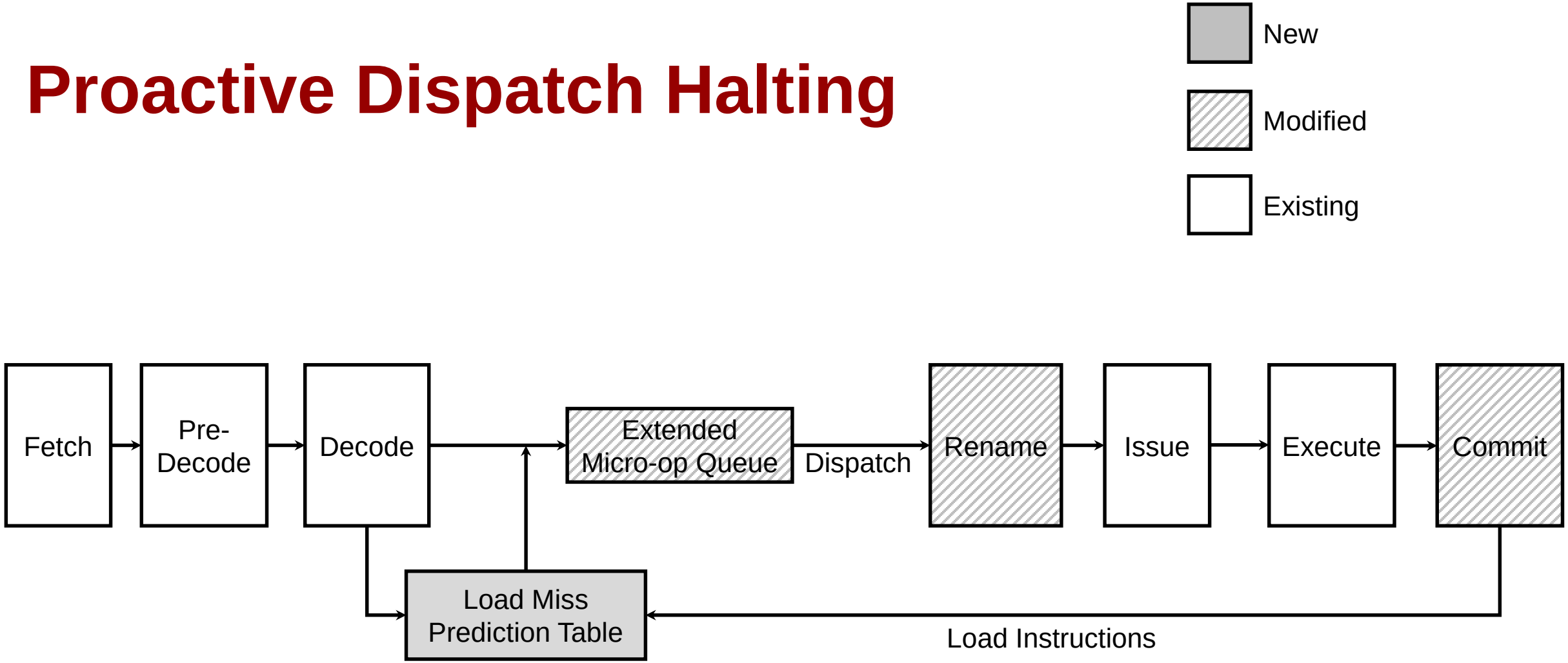
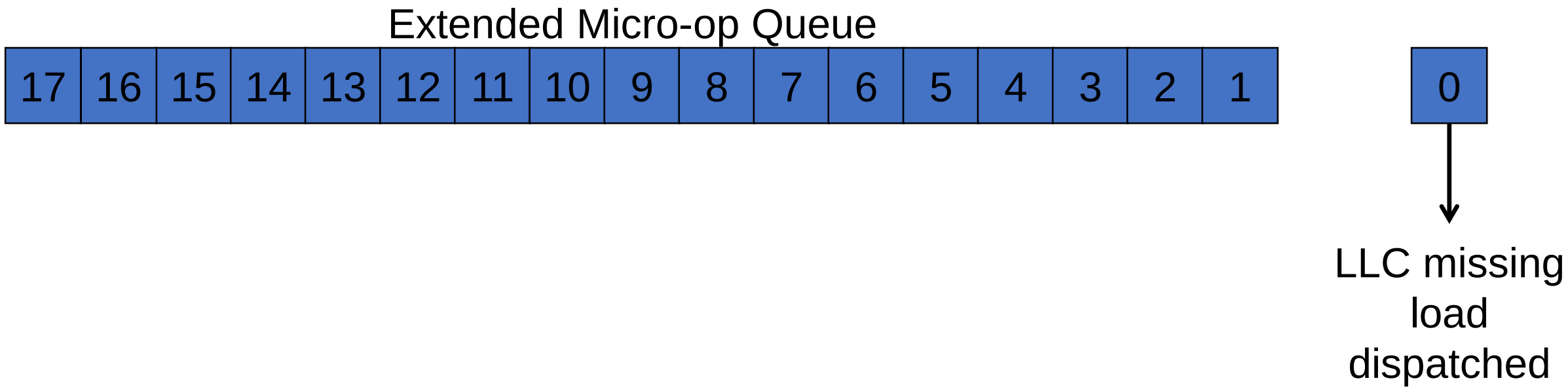


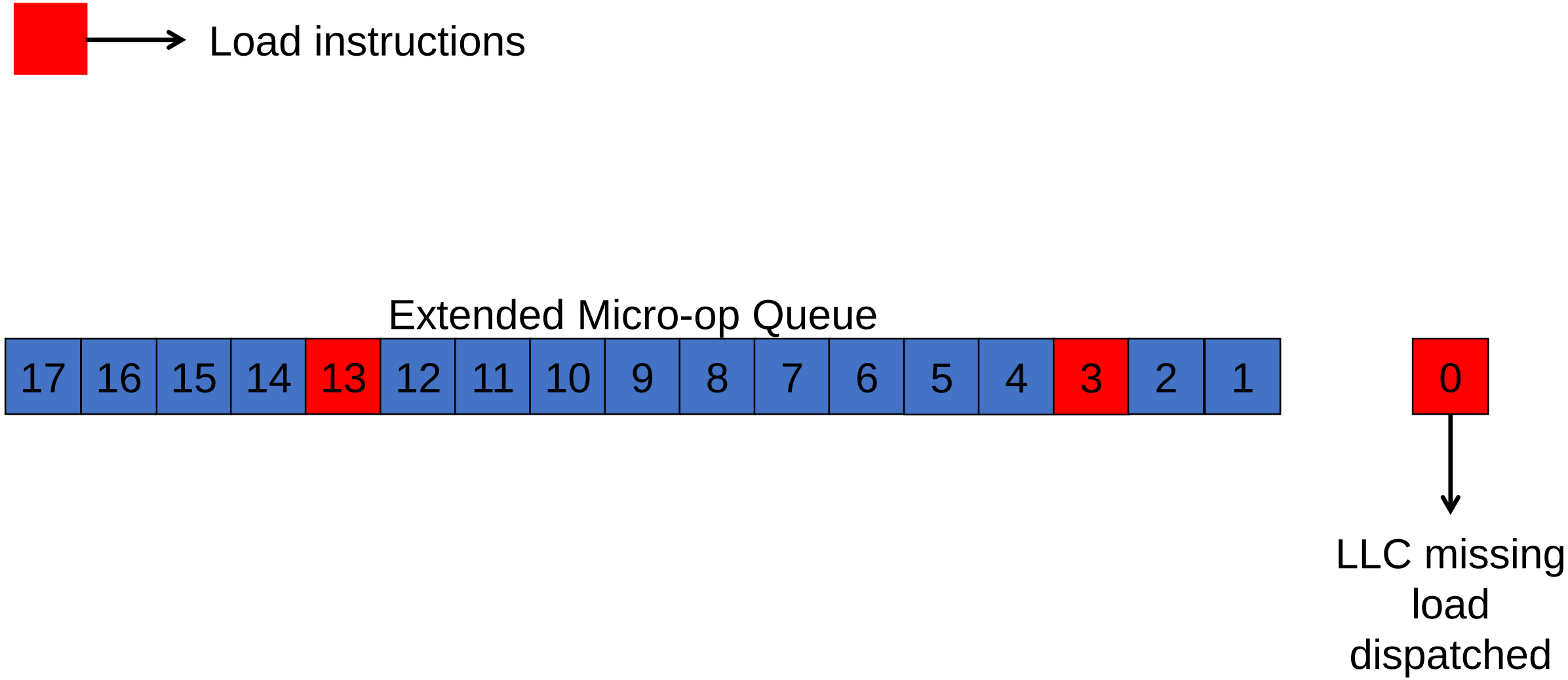
# Proactive Dispatch Halting



# Performance Bottlenecks



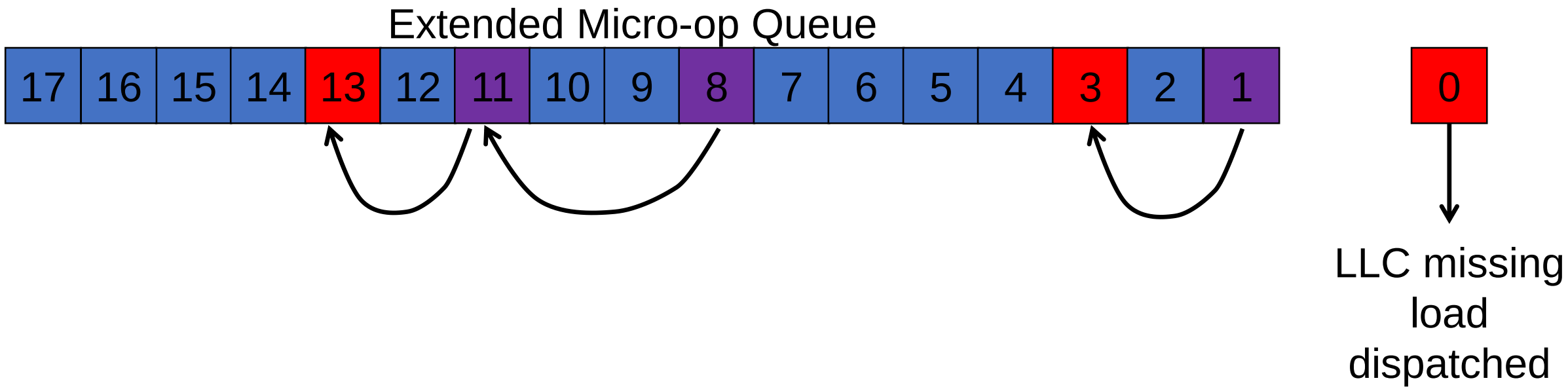
# Performance Bottlenecks



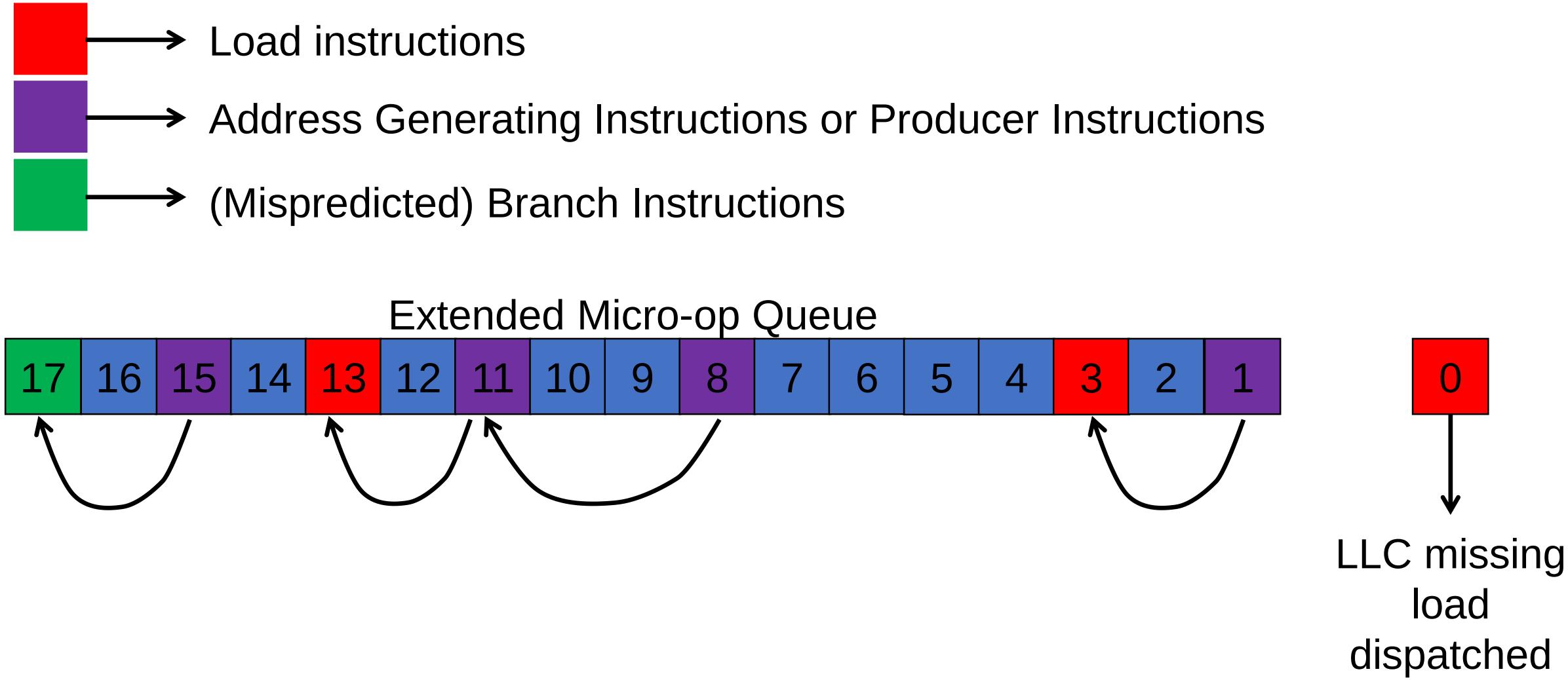
# Performance Bottlenecks

Load instructions

Address Generating Instructions or Producer Instructions



# Performance Bottlenecks



# Handling Performance Bottlenecks

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- Execute load/branch instructions and their producer instructions speculatively

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- Find producer instructions iteratively

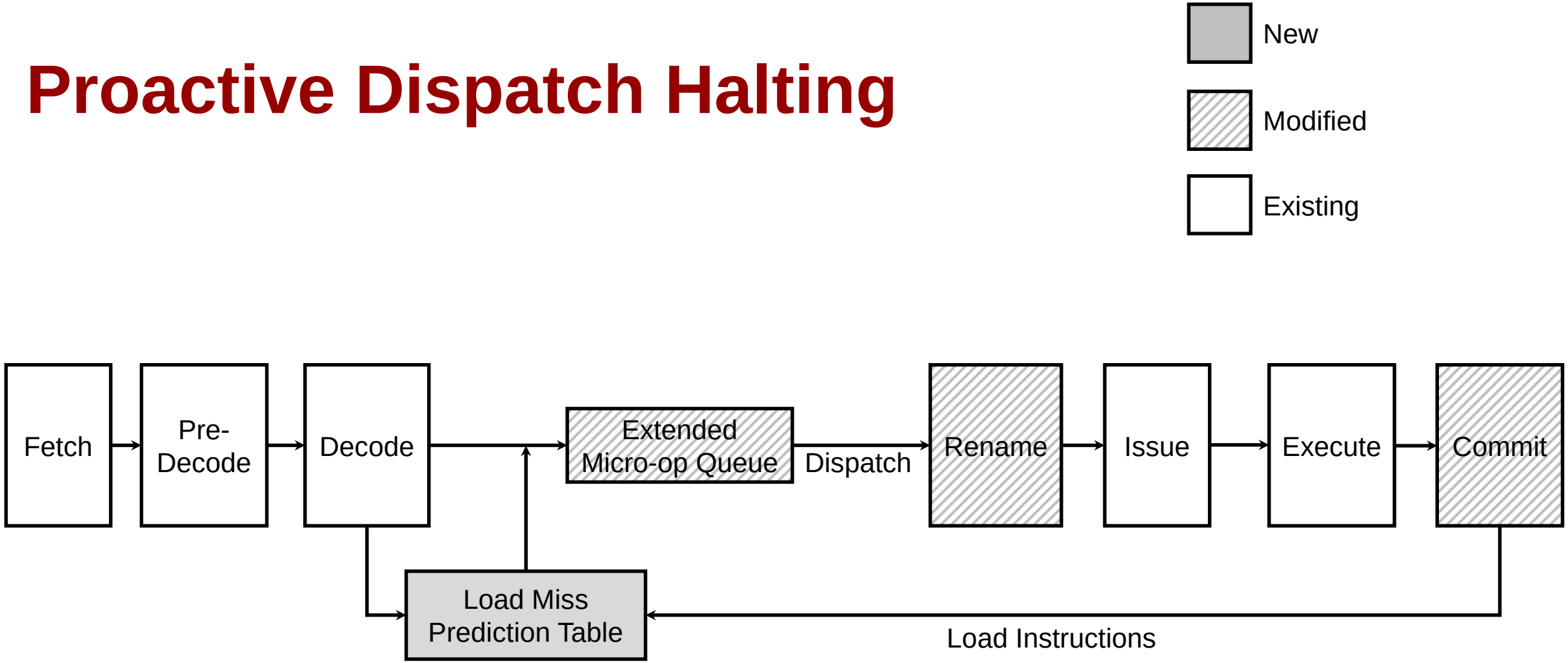
  -- Modify front-end Register Allocation Table (RAT)

# Handling Performance Bottlenecks

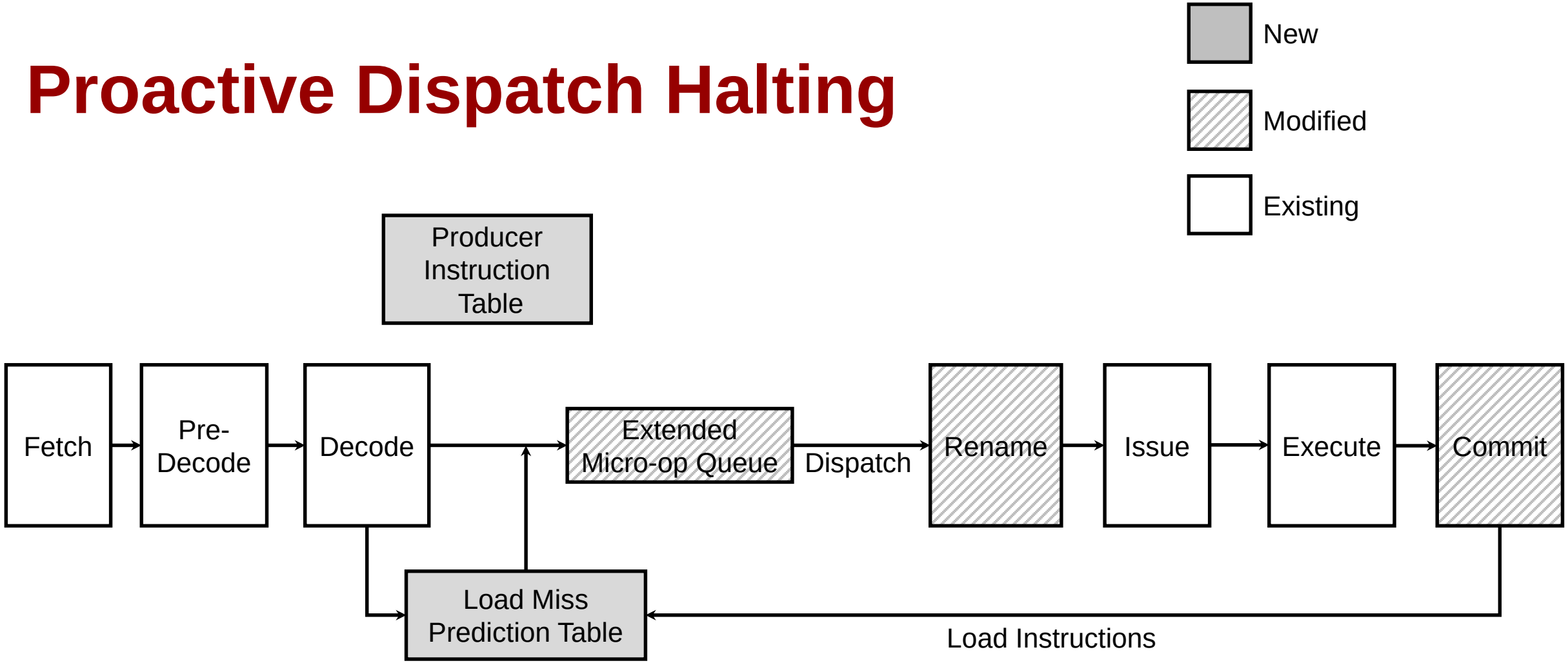
- Execute load/branch instructions and their producer instructions speculatively
- Find producer instructions iteratively

  -- Modify front-end Register Allocation Table (RAT)
- One additional RAT checkpoint

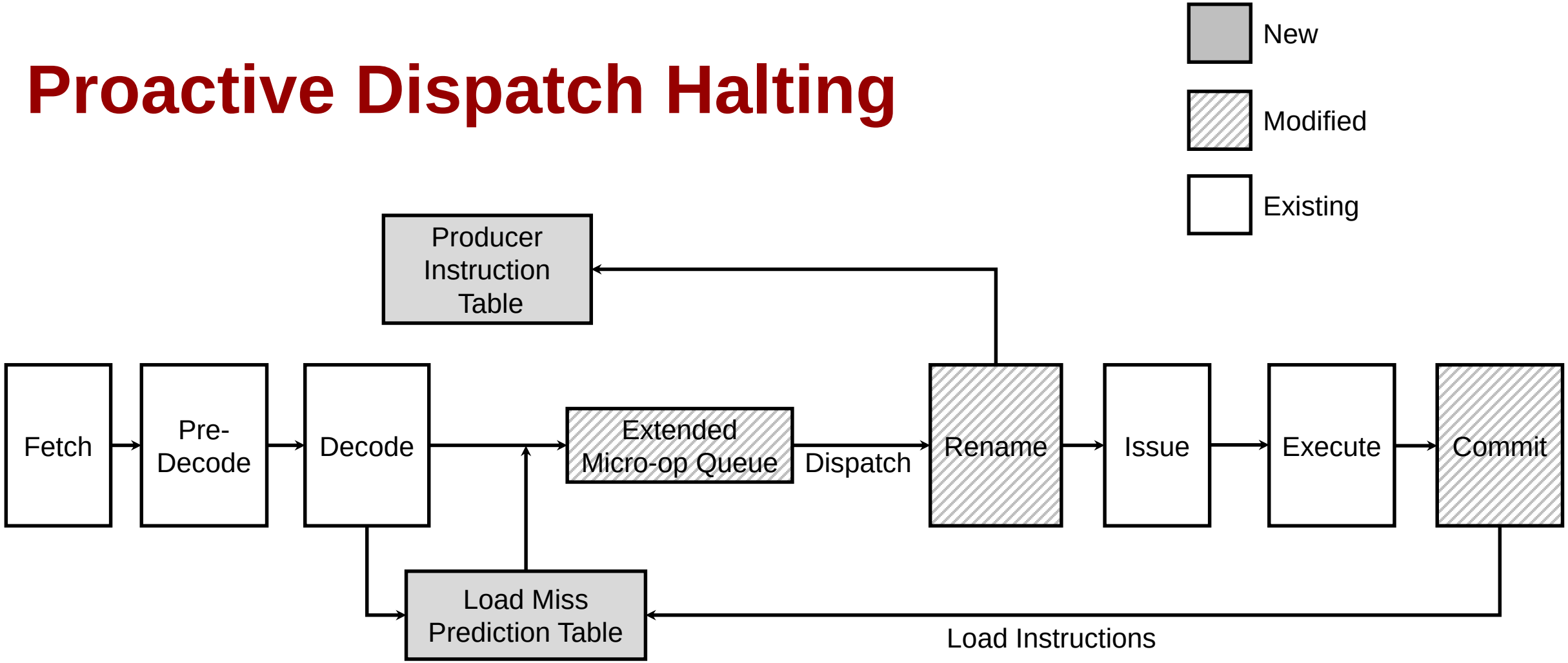
# Proactive Dispatch Halting



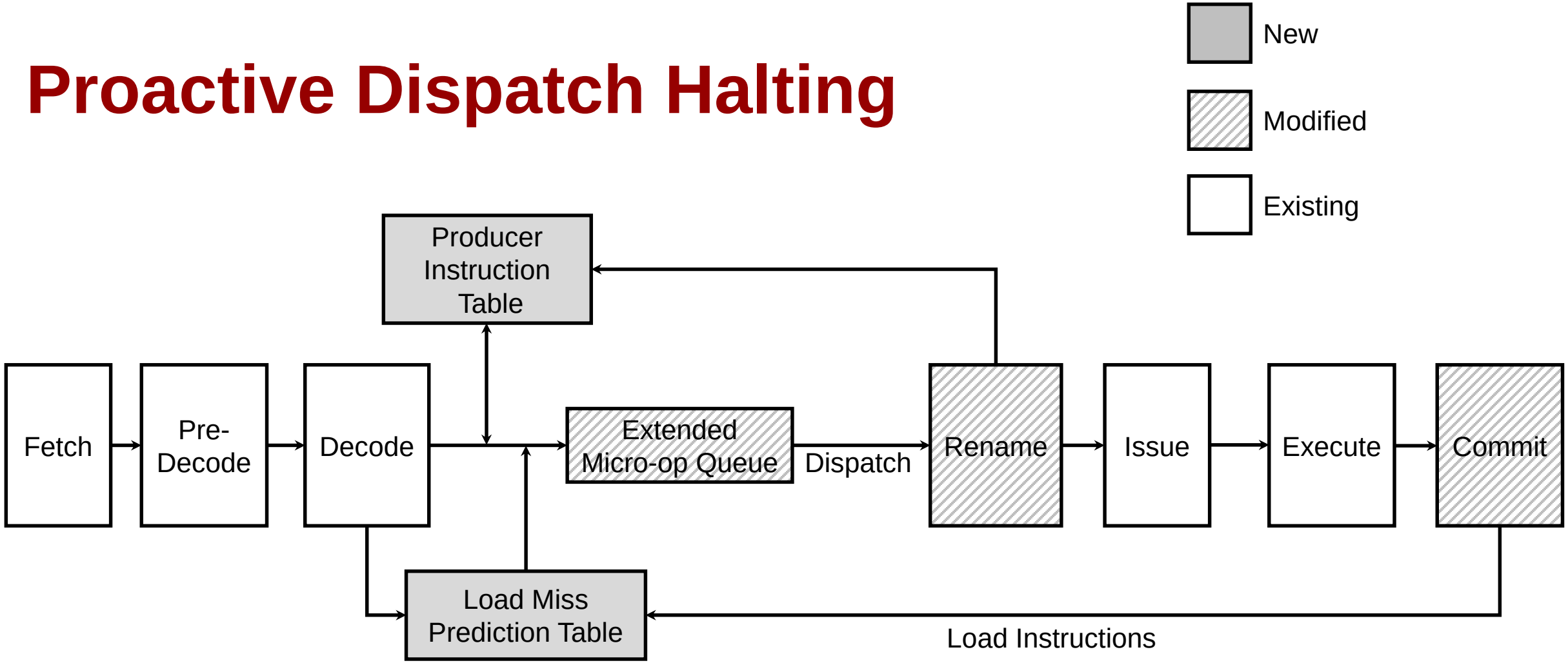
# Proactive Dispatch Halting



# Proactive Dispatch Halting



# Proactive Dispatch Halting



# Reactive Dispatch Halting

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- Mark back-end as speculative after a load miss

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- Mark back-end as speculative after a load miss
- EMQ works as a replay buffer
- Upon resume
  - -- Copy retirement RAT to front-end RAT

Checkpointing RAT does not work

# Reactive Dispatch Halting

- Mark back-end as speculative after a load miss
- EMQ works as a replay buffer
- Upon resume
  - -- Copy retirement RAT to front-end RAT
  - -- Re-execute all instructions from the replay buffer or EMQ

Checkpointing RAT does not work

# Evaluation

OoO: Baseline out-of-order core

# Evaluation

OoO: Baseline out-of-order core

NO-SPEC: Proactive dispatch halting without speculative execution

# Evaluation

OoO: Baseline out-of-order core

NO-SPEC: Proactive dispatch halting without speculative execution

P-DH: Proactive dispatch halting

# Evaluation

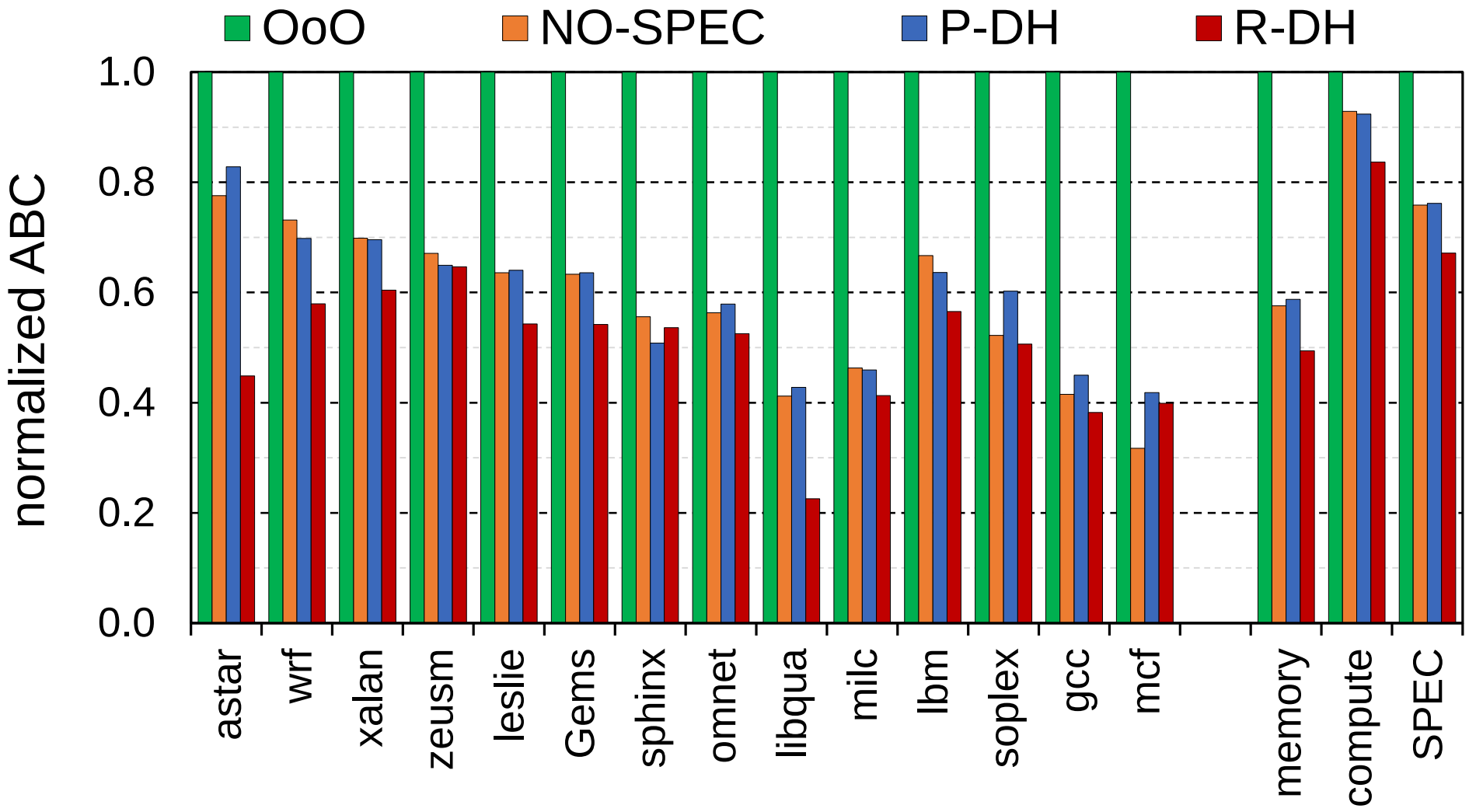
OoO: Baseline out-of-order core

NO-SPEC: Proactive dispatch halting without speculative execution

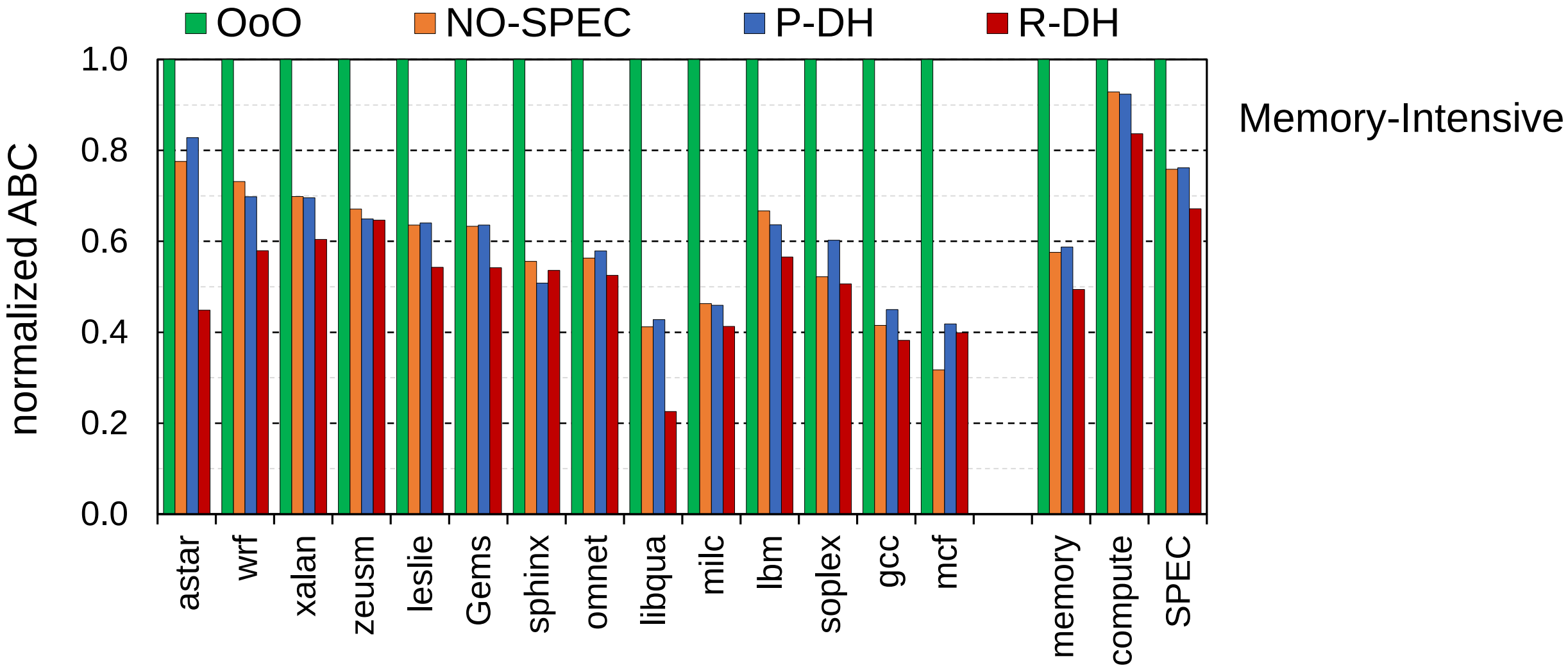
P-DH: Proactive dispatch halting

R-DH: Reactive dispatch halting

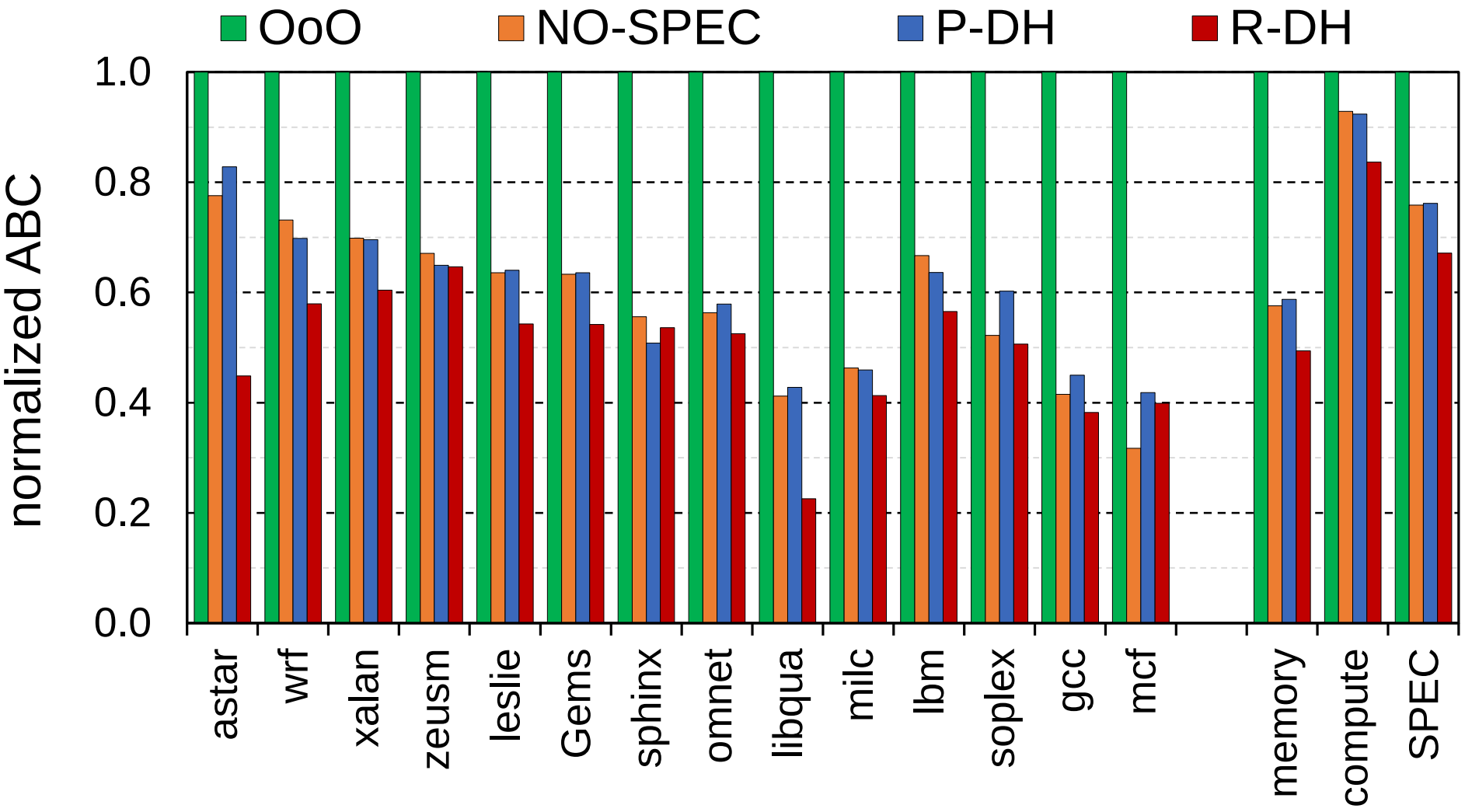
# Evaluation -- Reliability



# Evaluation -- Reliability



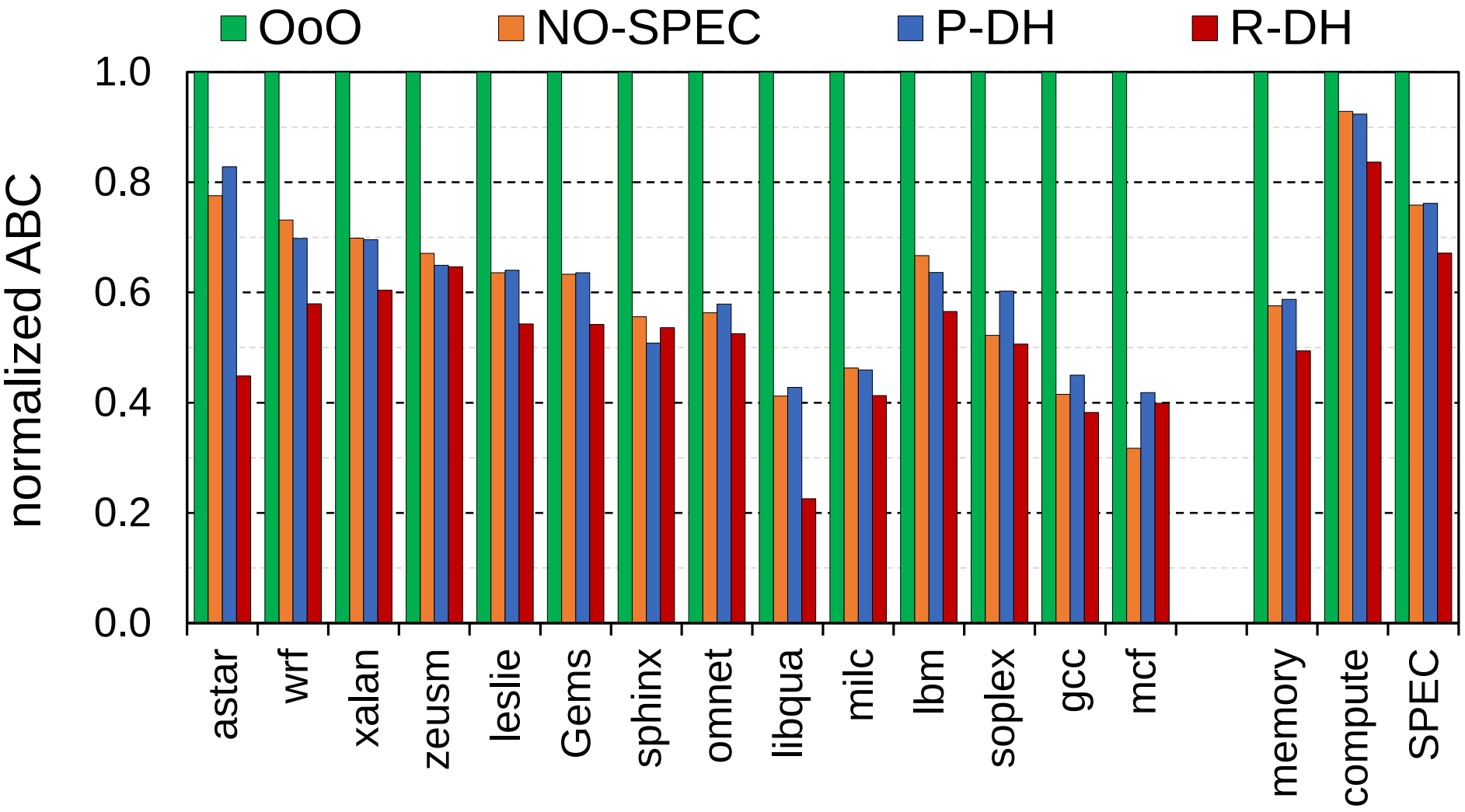
# Evaluation -- Reliability




Memory-Intensive

P-DH: 41.3%

# Evaluation -- Reliability

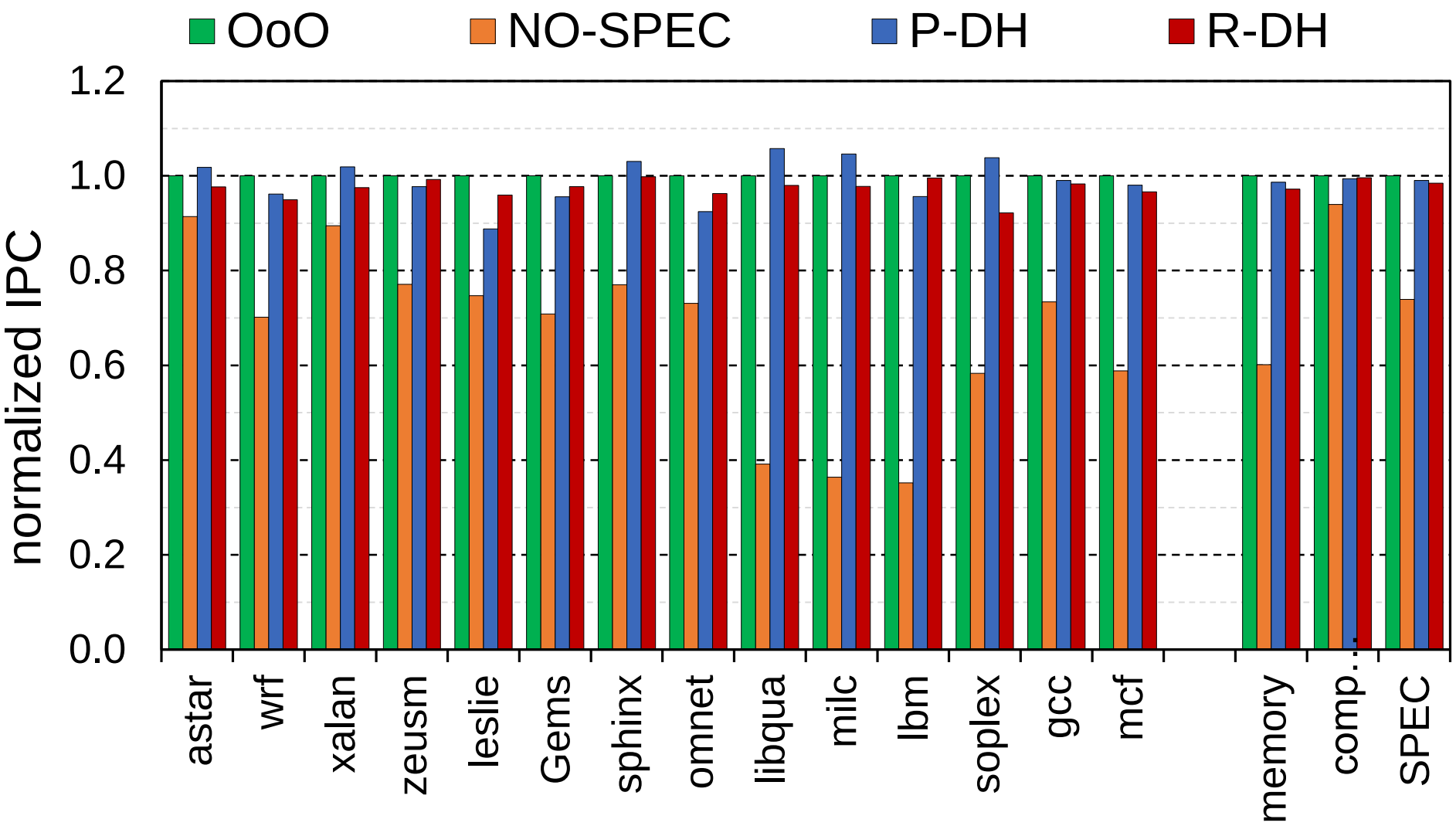



Memory-Intensive

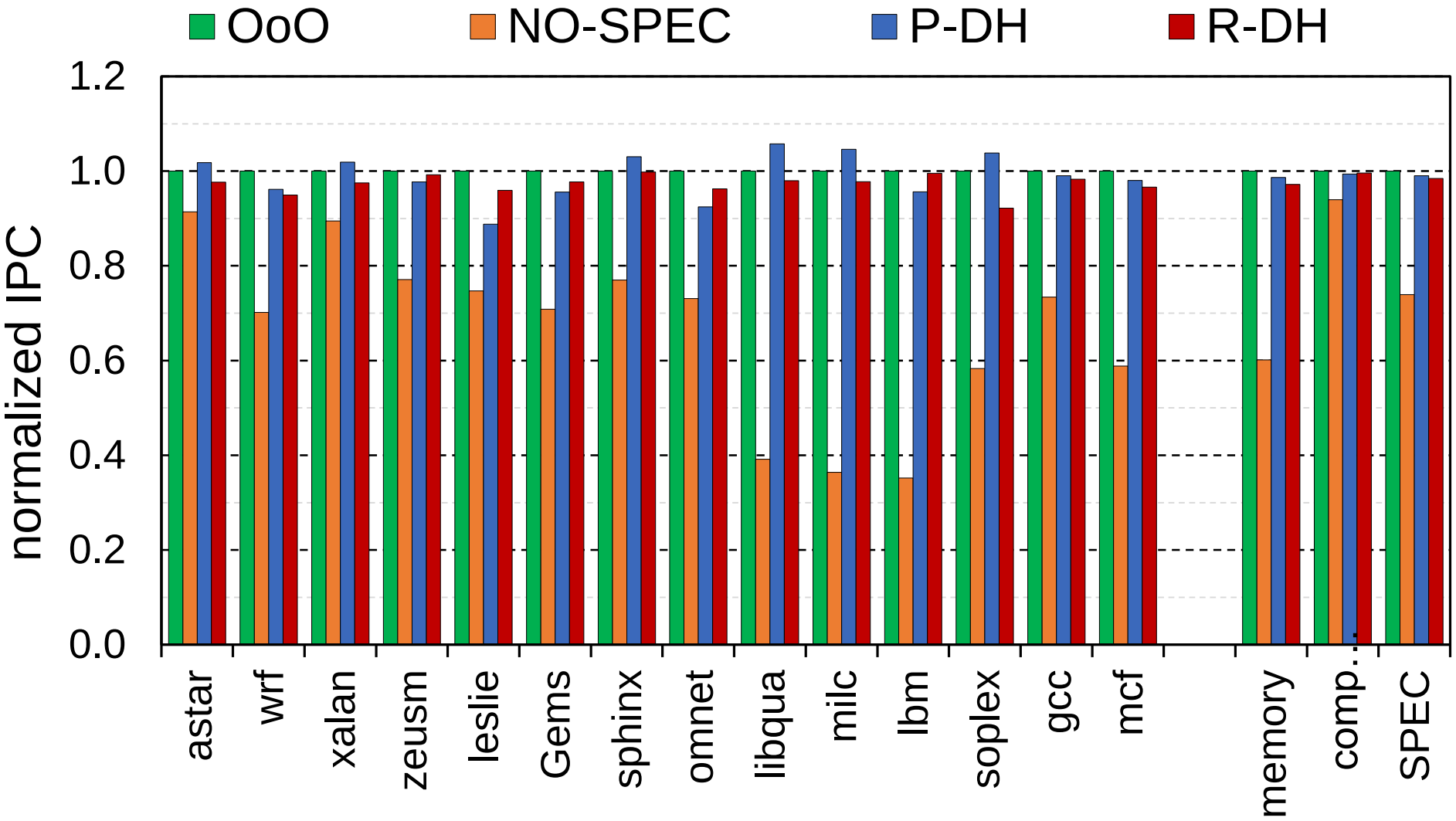
P-DH: 41.3%

R-DH: 50.6%

# Evaluation -- Performance



# Evaluation -- Performance




Dispatch halting does not degrade performance

# Contribution #3 [CAL 2019, HPCA 2020]

# Precise Runahead Execution to Improve Performance and Evaluate Reliability

# Full-ROB Stalls Degrade Performance

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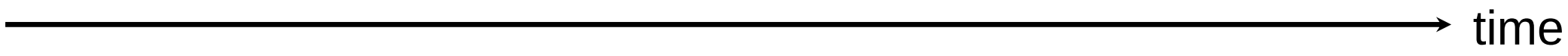

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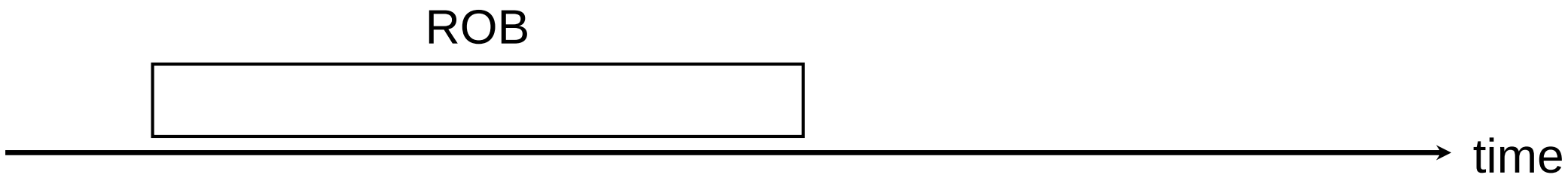

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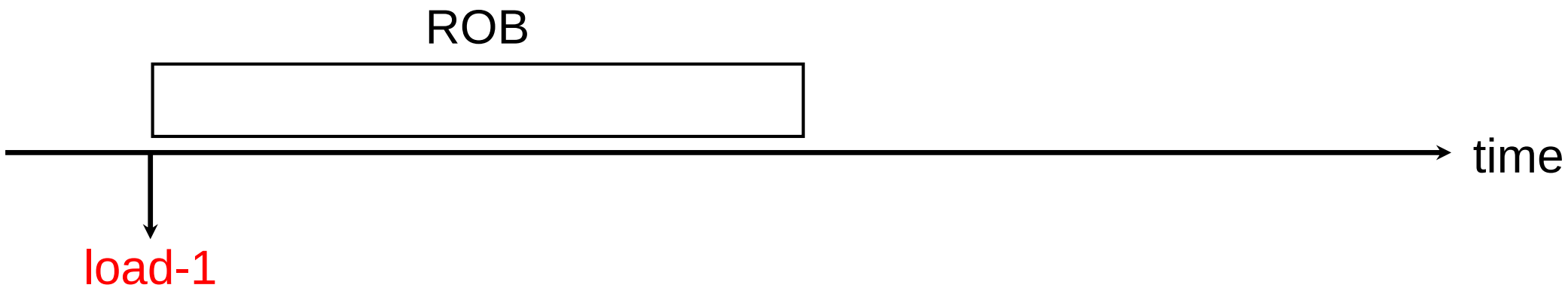

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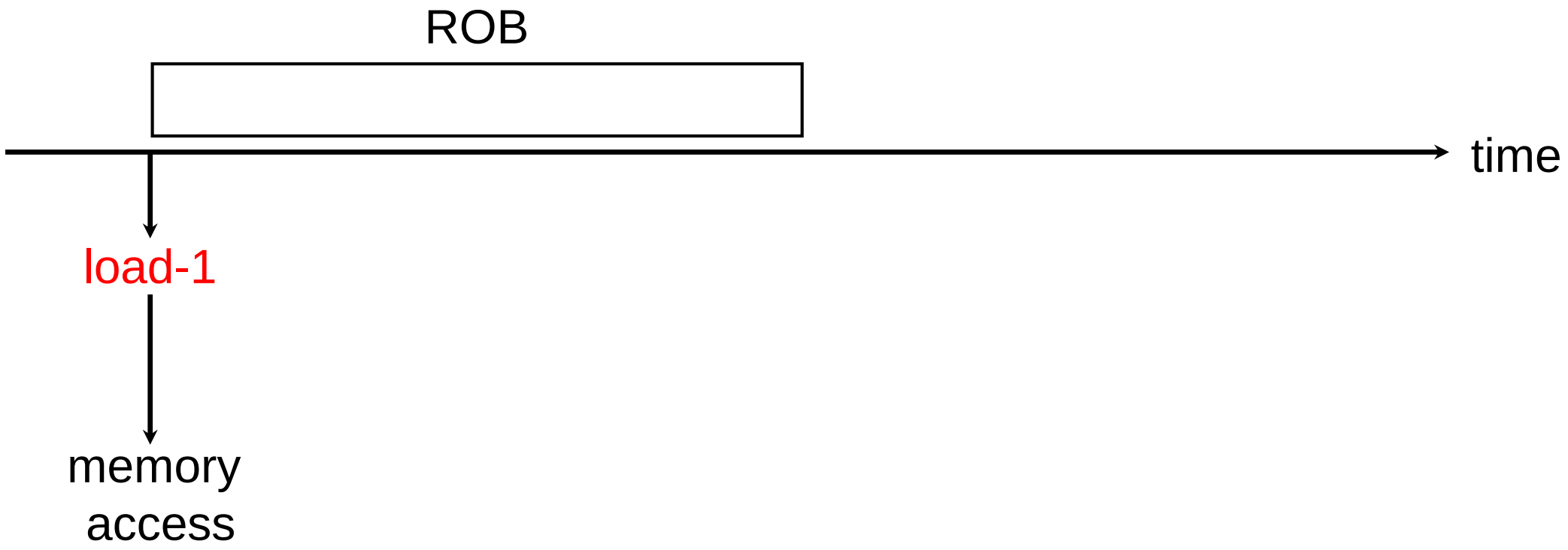

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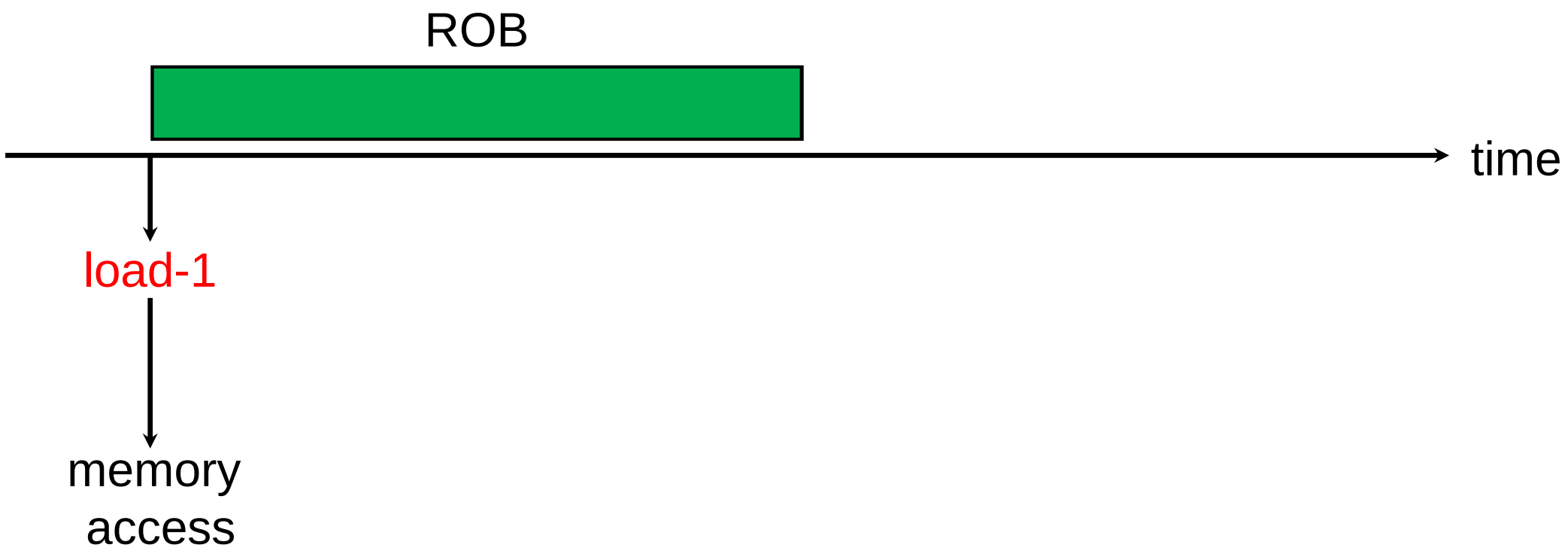

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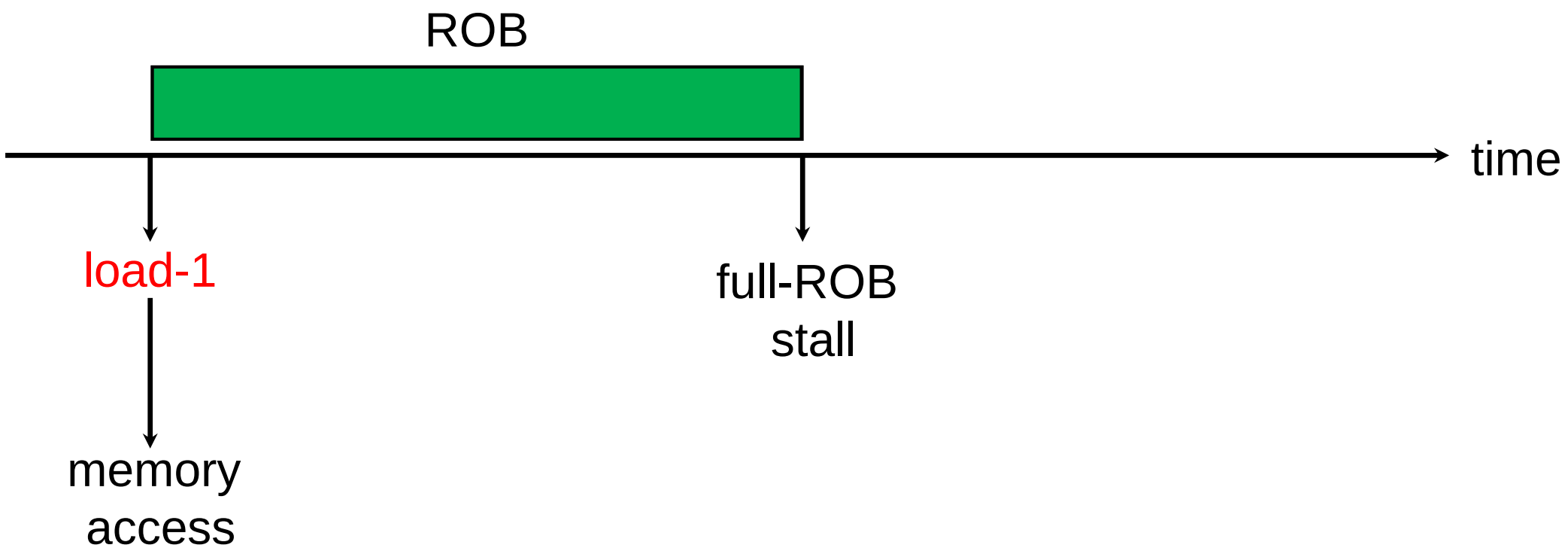

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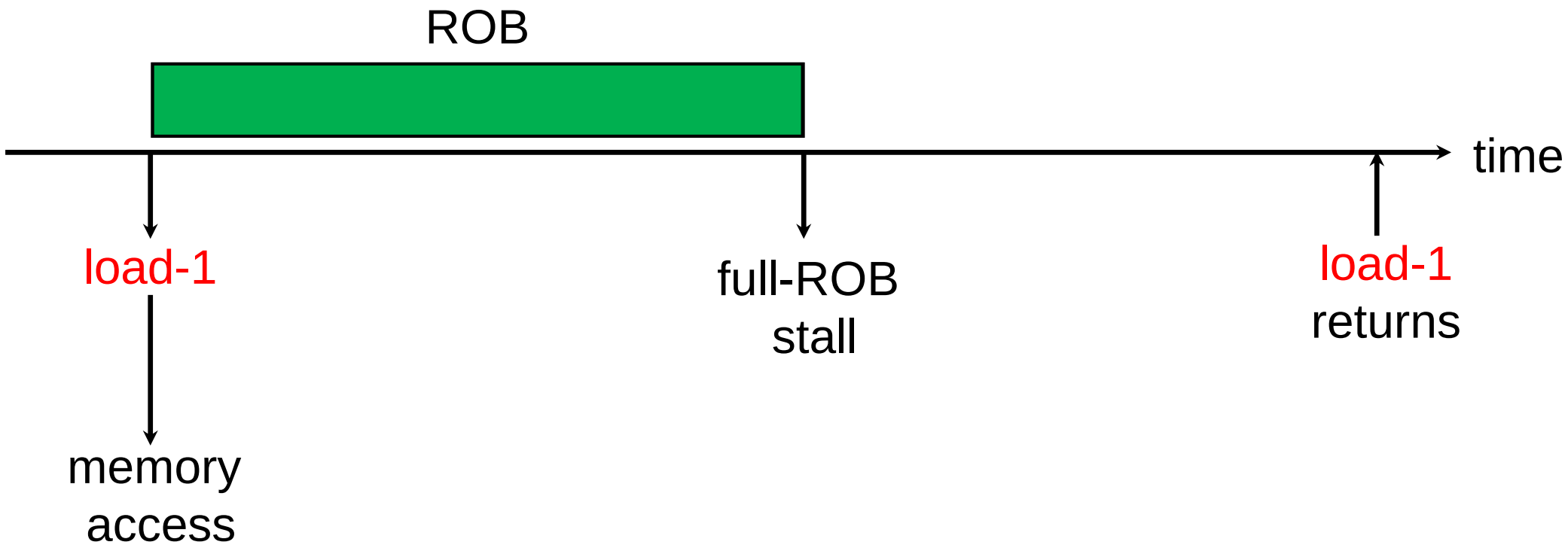

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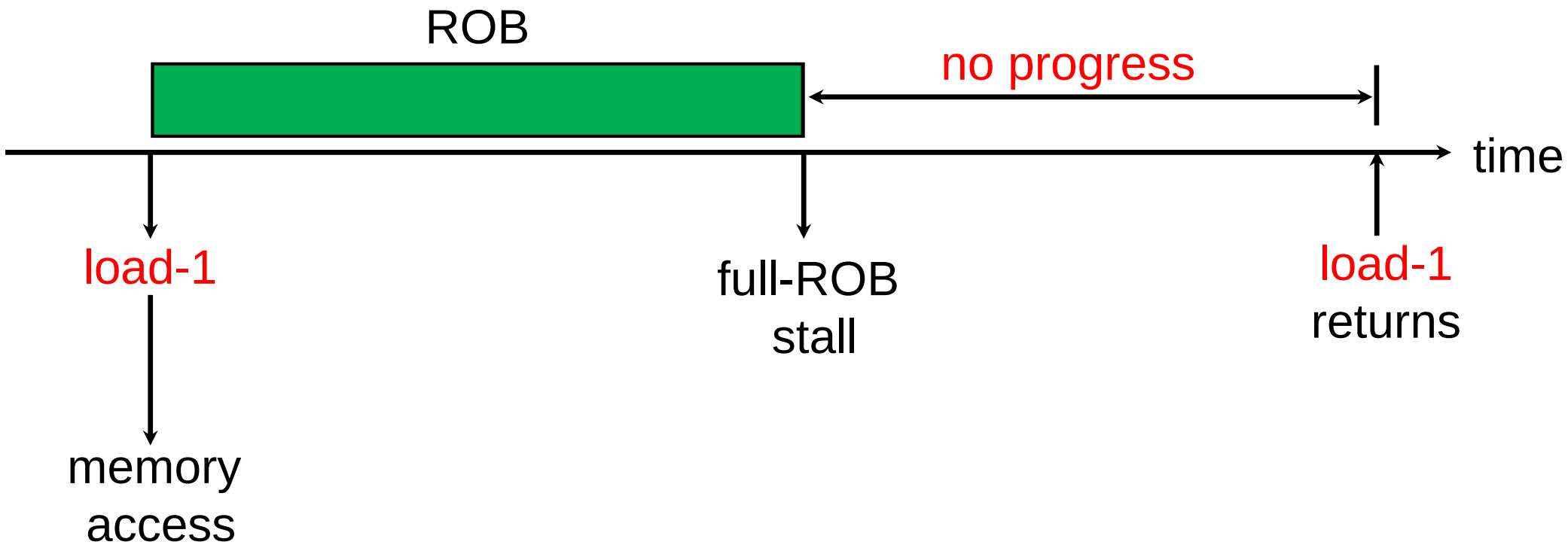

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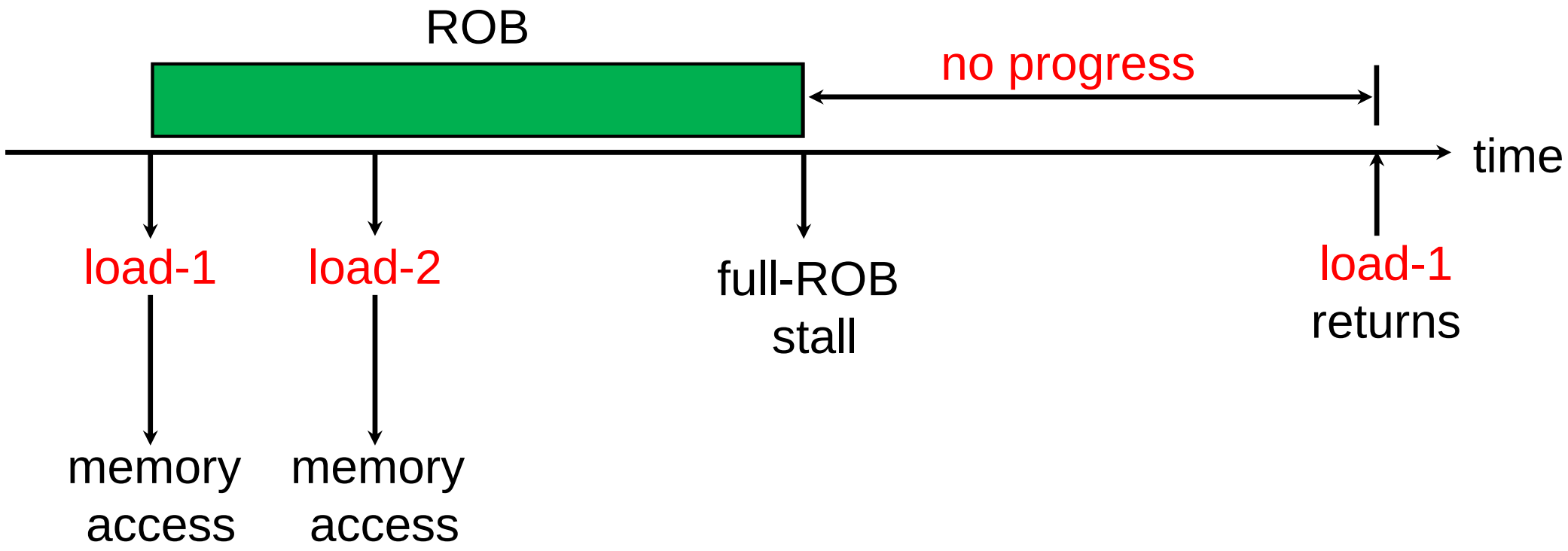

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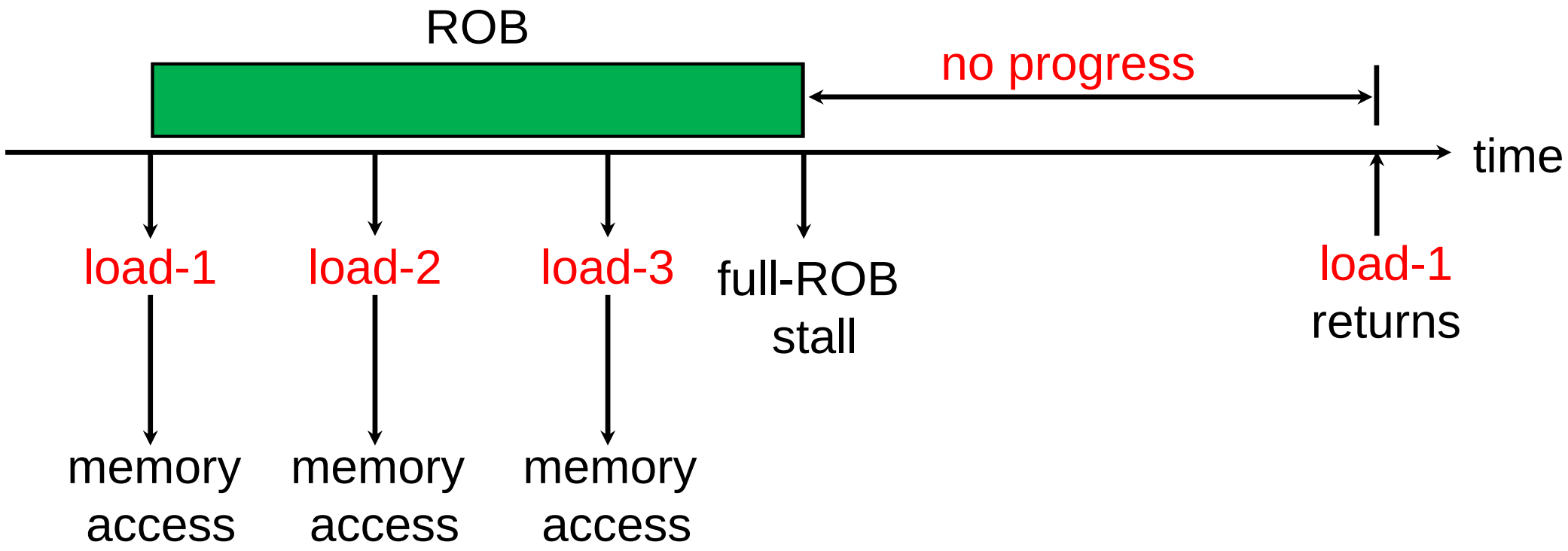

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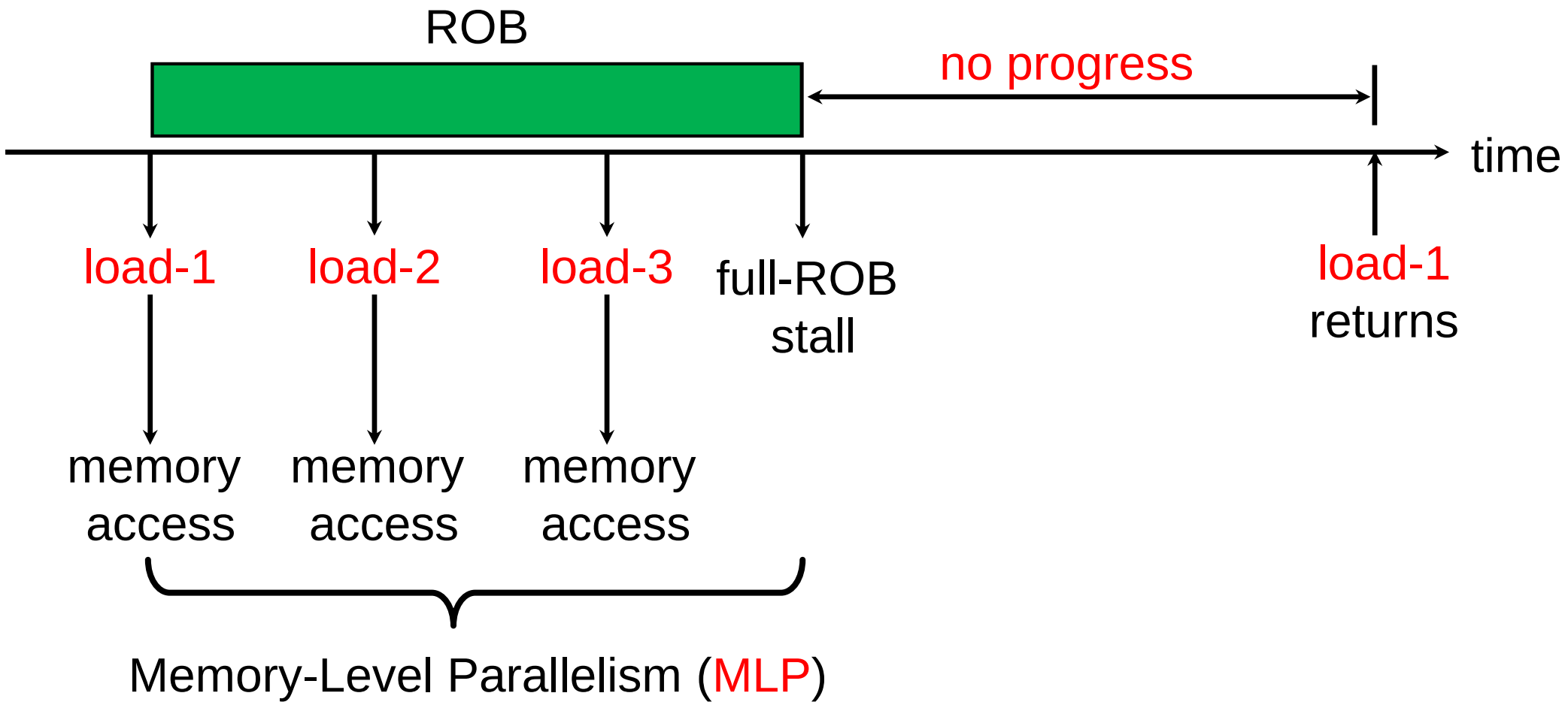

# Full-ROB Stalls Degrade Performance

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**Larger ROB**

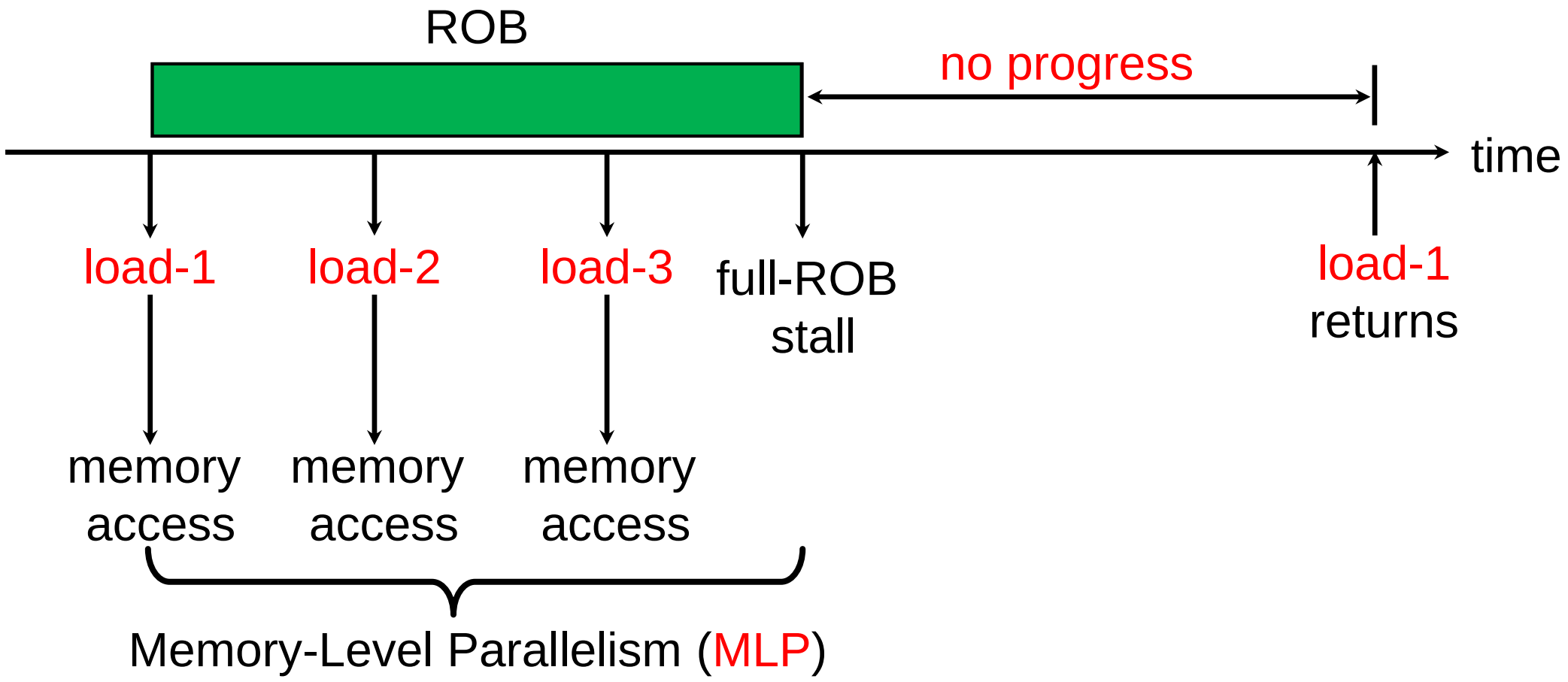
# Full-ROB Stalls Degrade Performance

**Larger ROB** ⇒ **Increased MLP**

# Full-ROB Stalls Degrade Performance

**Larger ROB** ⇒ **Increased MLP** ⇒ **Better performance**

# Runahead Execution Prefetches under a Full-ROB Stall



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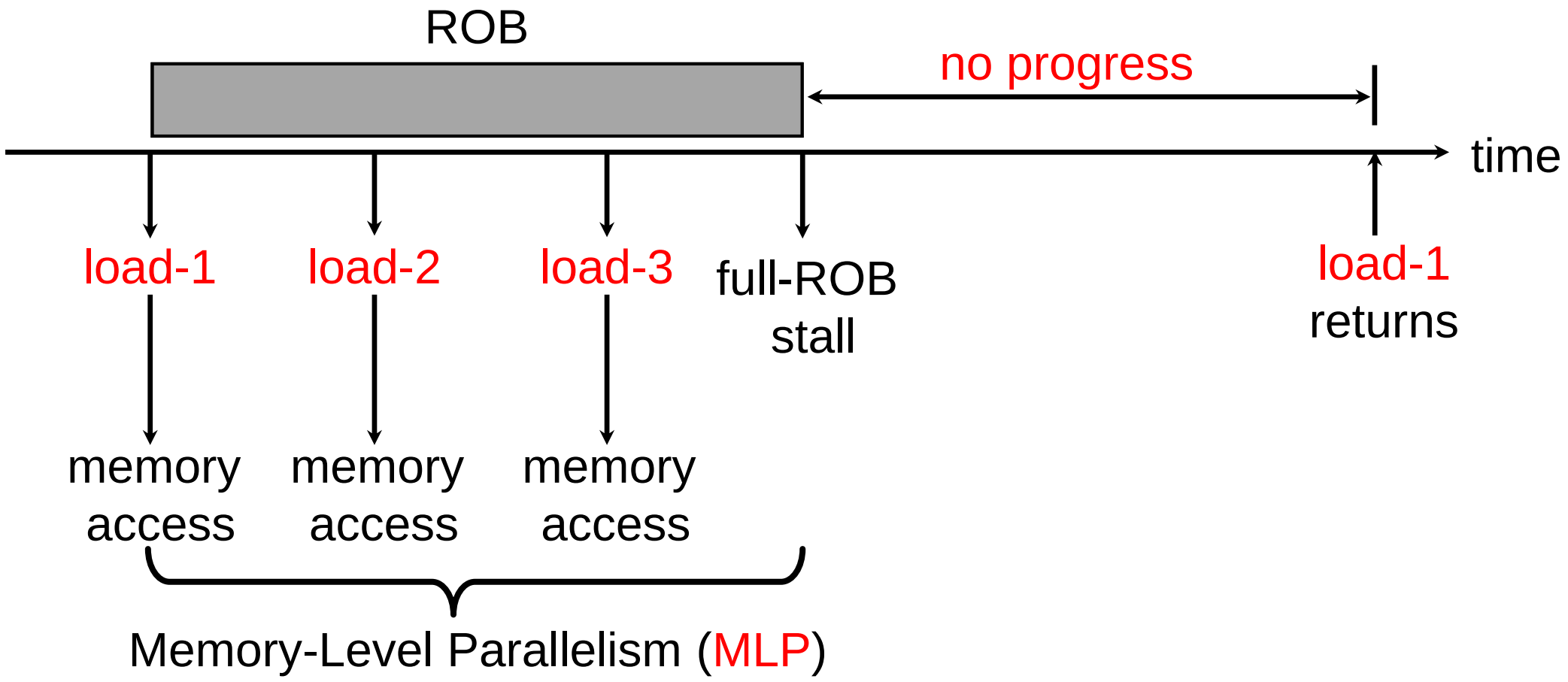

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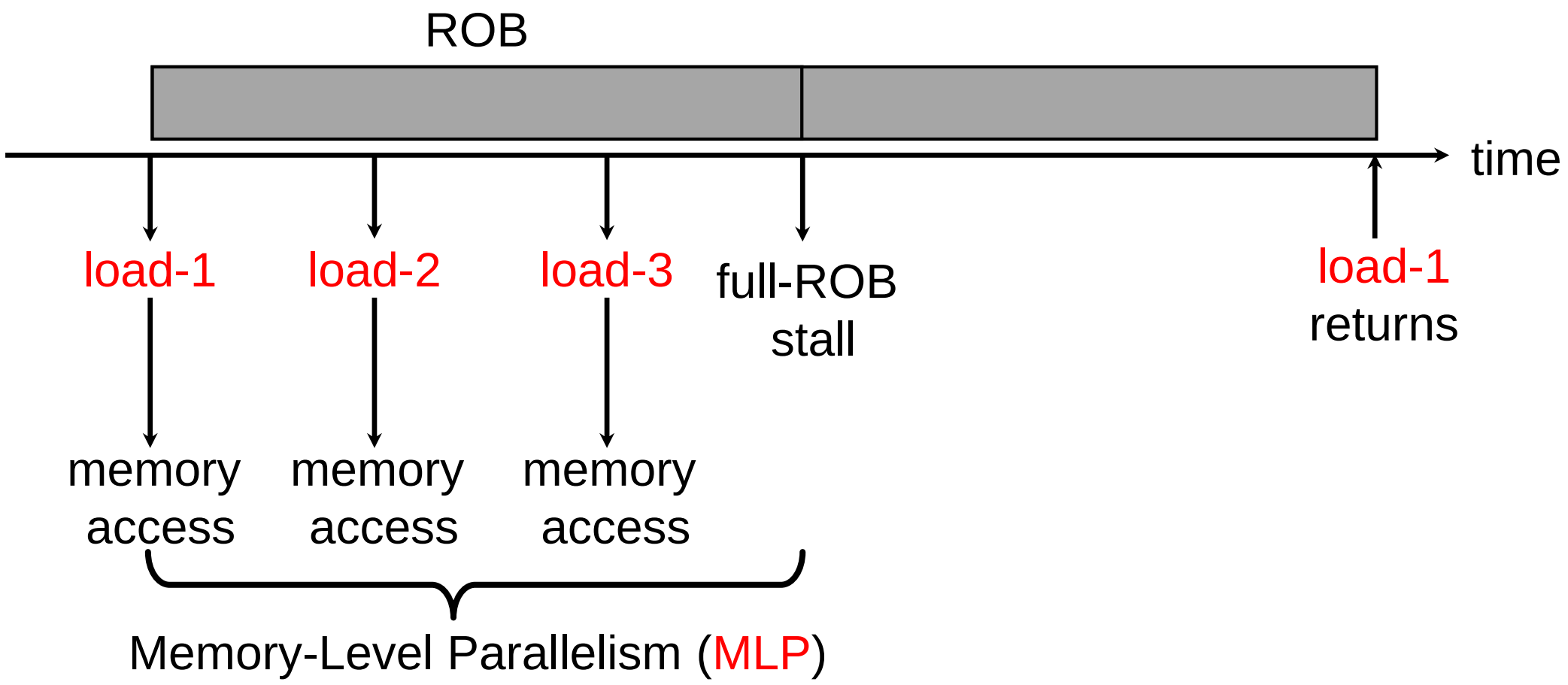

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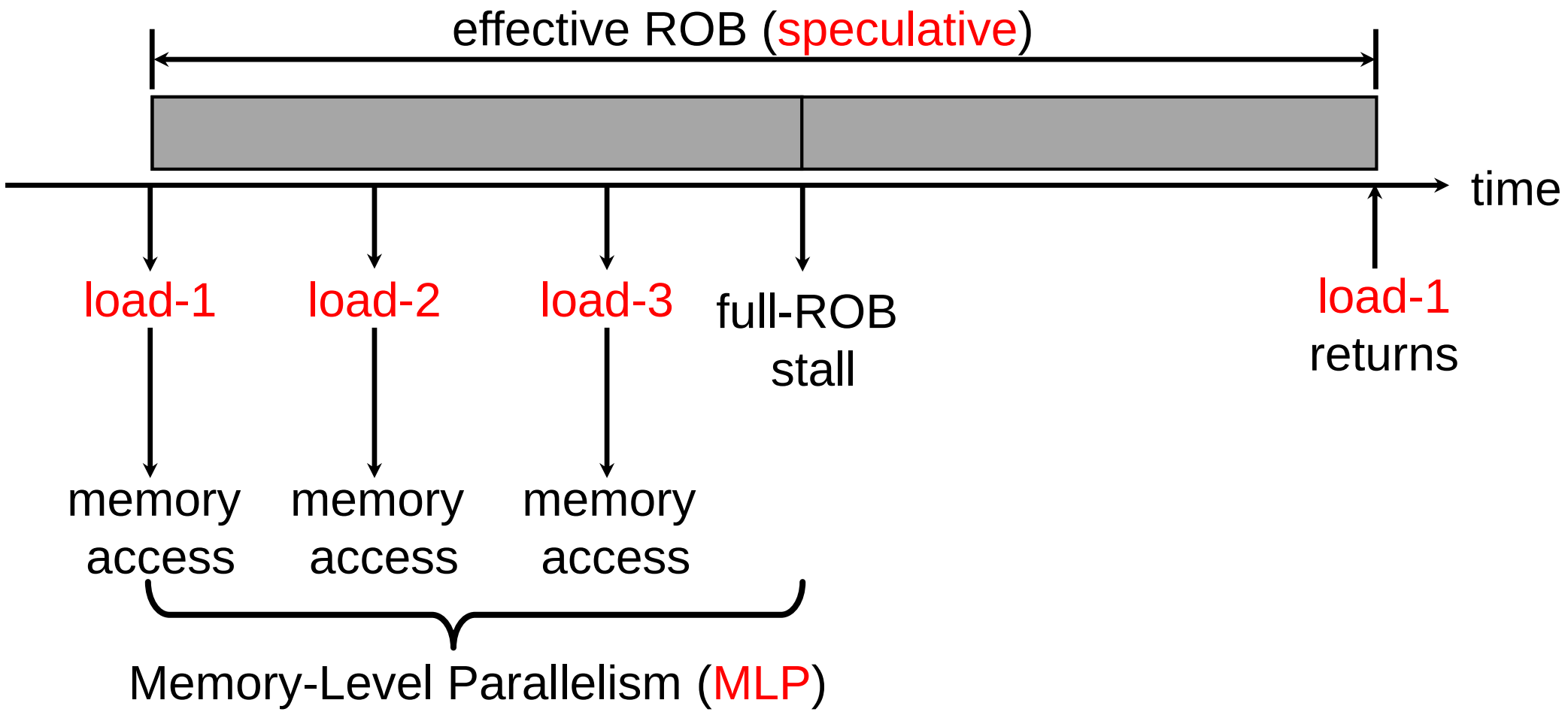
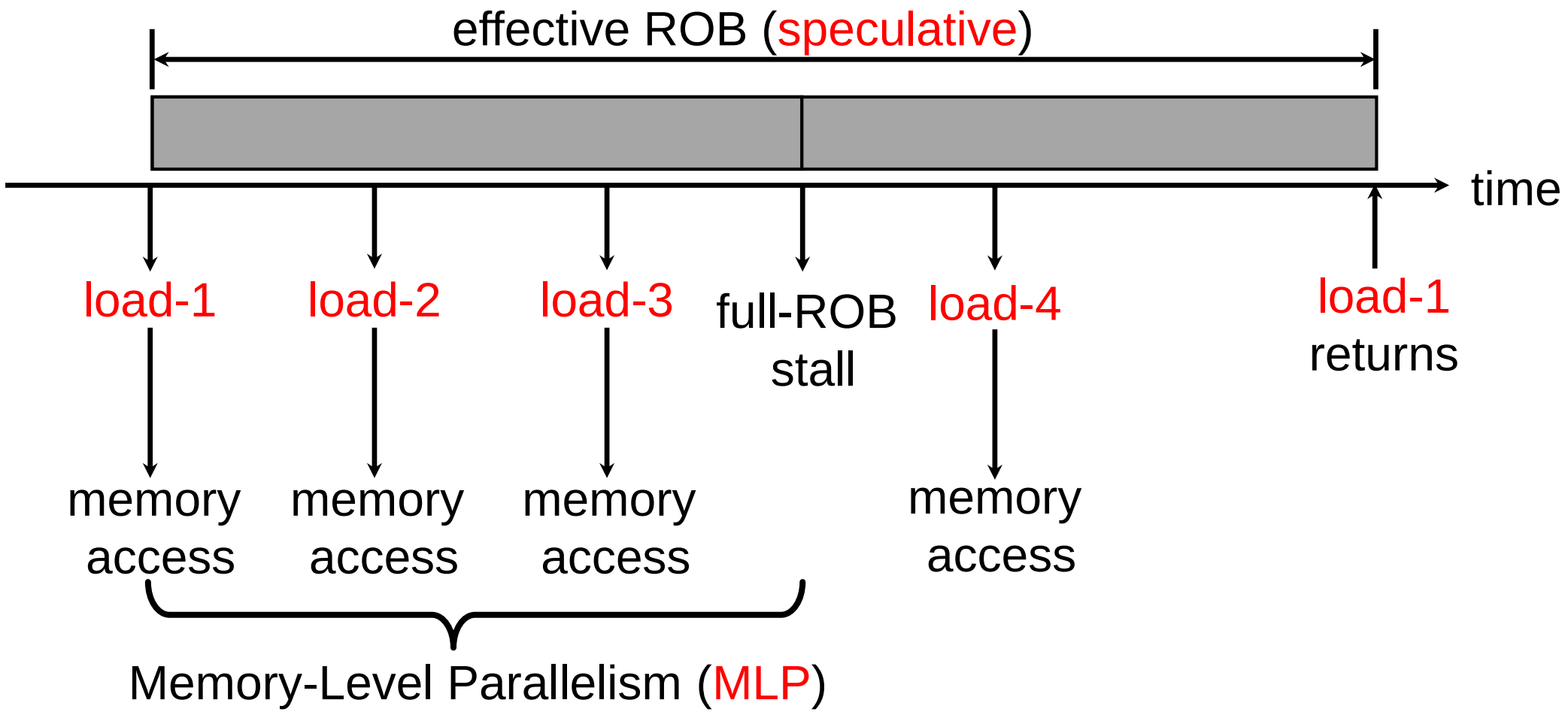


# Runahead Execution Prefetches under a Full-ROB Stall



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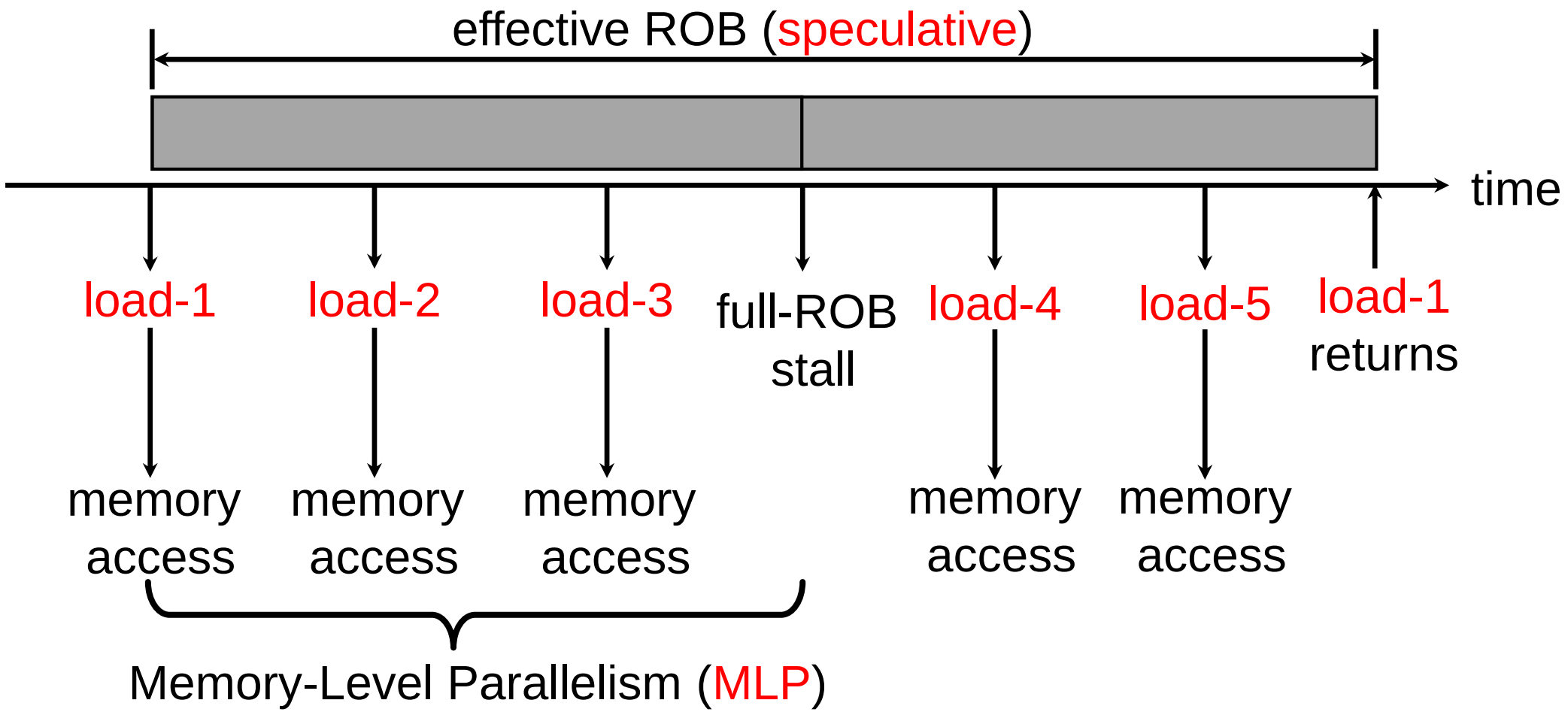

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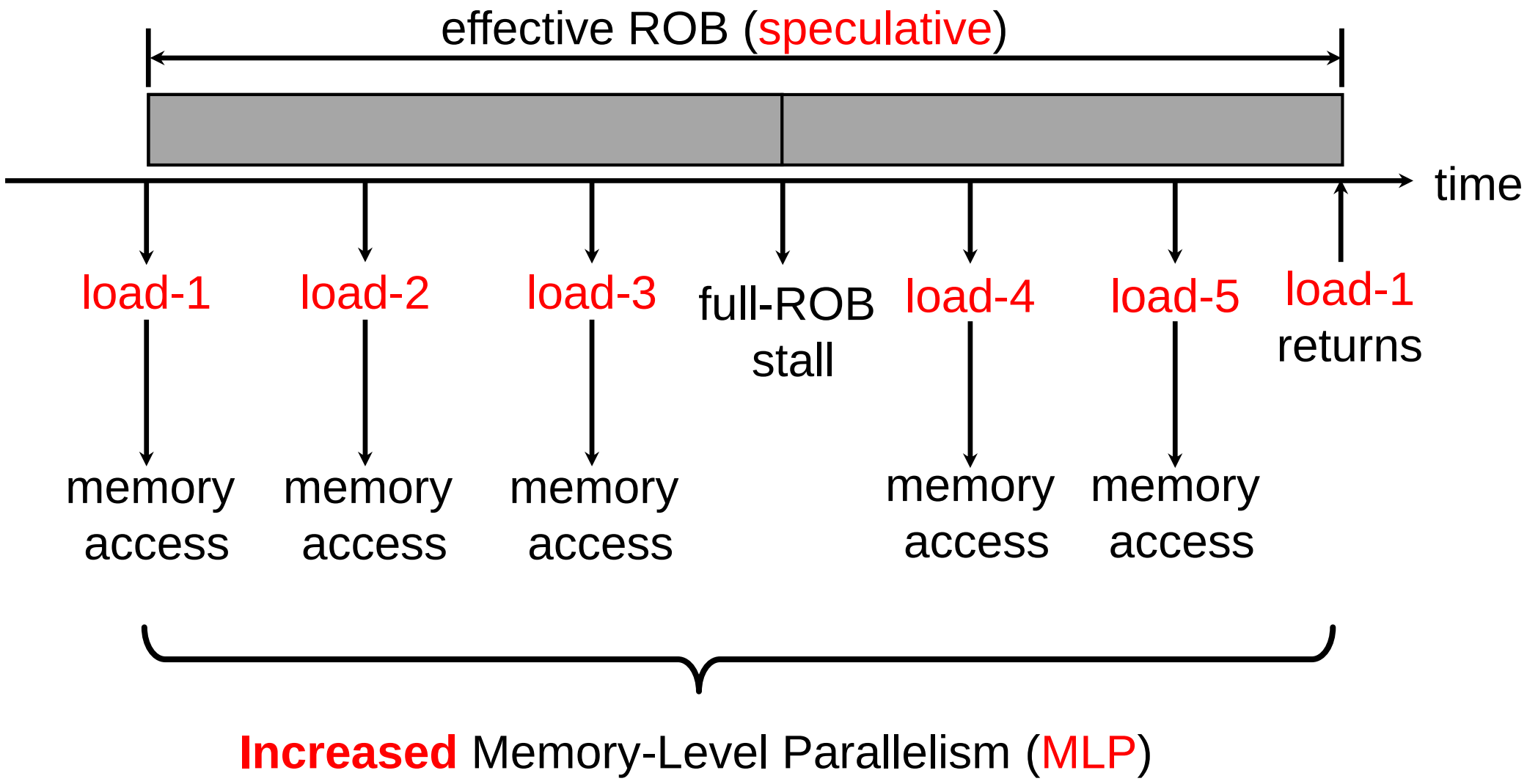

# Runahead Execution Re-Executes Instructions

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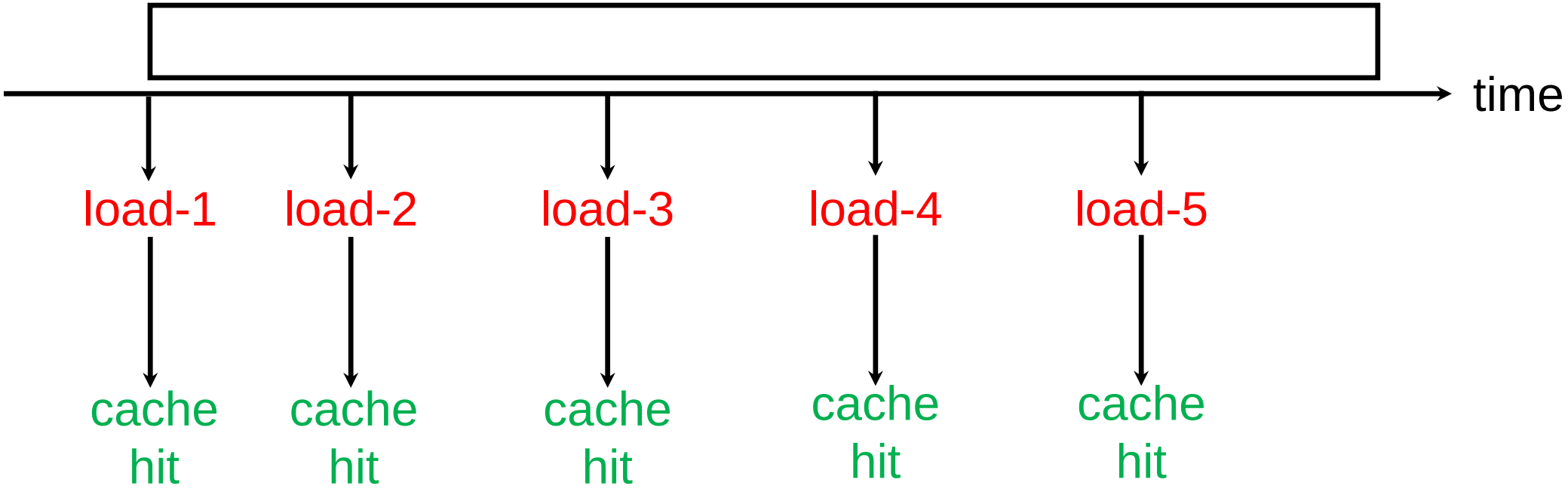

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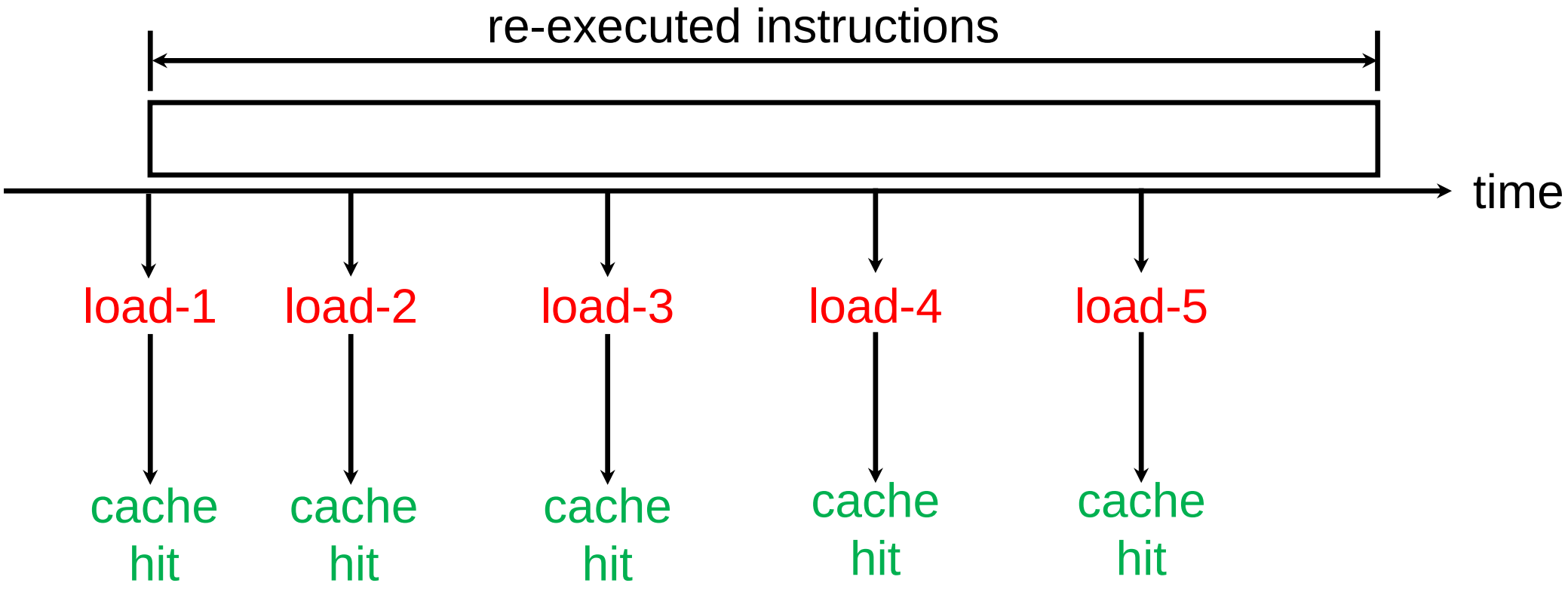

# Runahead Buffer Finds the Most Critical Slice of Instructions

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⇩

**Better energy-efficiency and similar performance**

# Runahead Techniques Relative to OoO Core

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| Runahead execution | Runahead buffer |
| --- | --- |

# Runahead Techniques Relative to OoO Core

| | Runahead execution | Runahead buffer | |
|---|---|---|---|
| Flush ROB | | | |

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|---|---|---|---|
| Flush ROB | ✓ | | |

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|---|---|---|---|
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| Execute all future instructions | | | |

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| Performance | | | |

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| Flush ROB | ✓ | ✓ | |
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| Performance | High ↑ | | |

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| Performance | High ↑ | High ↑ | |

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|---|---|---|---|
| Flush ROB | ✓ | ✓ | |
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| Performance | High ↑ | High ↑ | |
| Energy Efficiency | | | |

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| Flush ROB | ✓ | ✓ | |
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| Performance | High ↑ | High ↑ | |
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|---|---|---|---|
| Flush ROB | ✓ | ✓ | |
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| Performance | High ↑ | High ↑ | |
| Energy Efficiency | Low ↓ | Same | |

# Runahead Techniques Relative to OoO Core

| | Runahead execution | Runahead buffer | |
|---|---|---|---|
| Flush ROB | ✓ | ✓ | ✗ |
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| Performance | High ↑ | High ↑ | Very high ↑↑ |
| Energy Efficiency | Low ↓ | Same | High ↑ |

# Runahead Techniques Relative to OoO Core

| | Runahead execution | Runahead buffer | **Precise runahead** |
|---|---|---|---|
| Flush ROB | ✓ | ✓ | ✗ |
| Execute all future instructions | ✓ | Only one slice | All slices |
| Performance | High ↑ | High ↑ | Very high ↑↑ |
| Energy Efficiency | Low ↓ | Same | High ↑ |

# Precise Runahead Exection: Three Key Insights

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1. No need to flush the ROB

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1. No need to flush the ROB

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3. Only physical registers must be recycled

# Precise Runahead Execution

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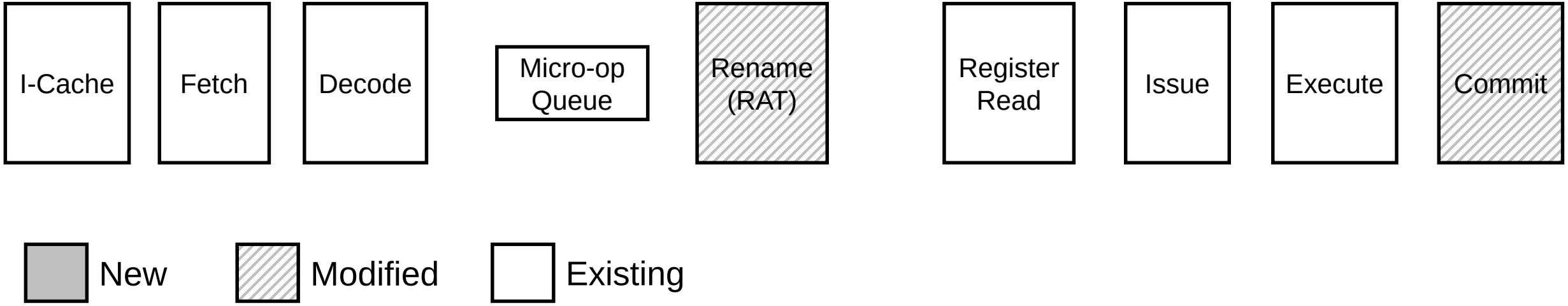

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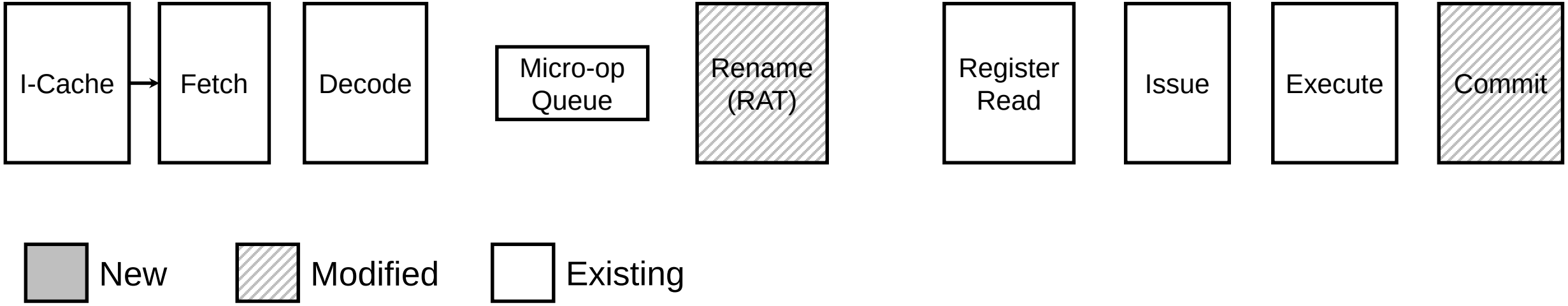

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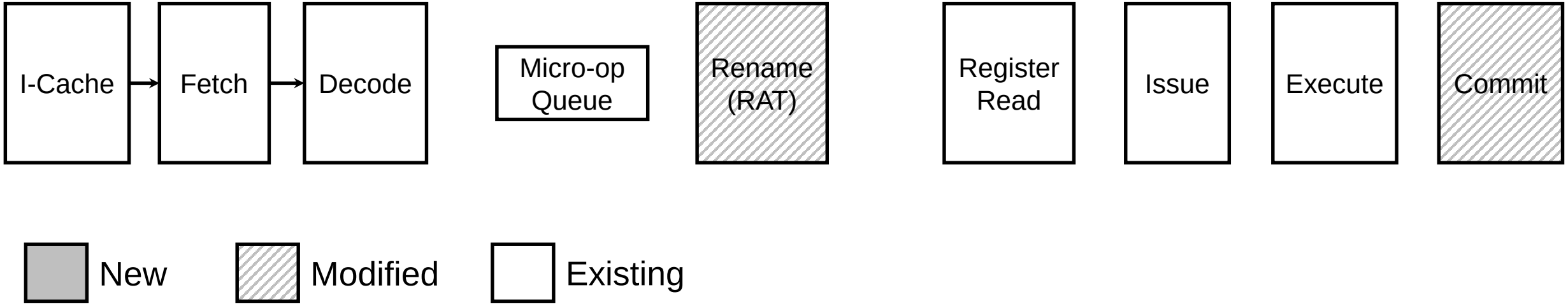

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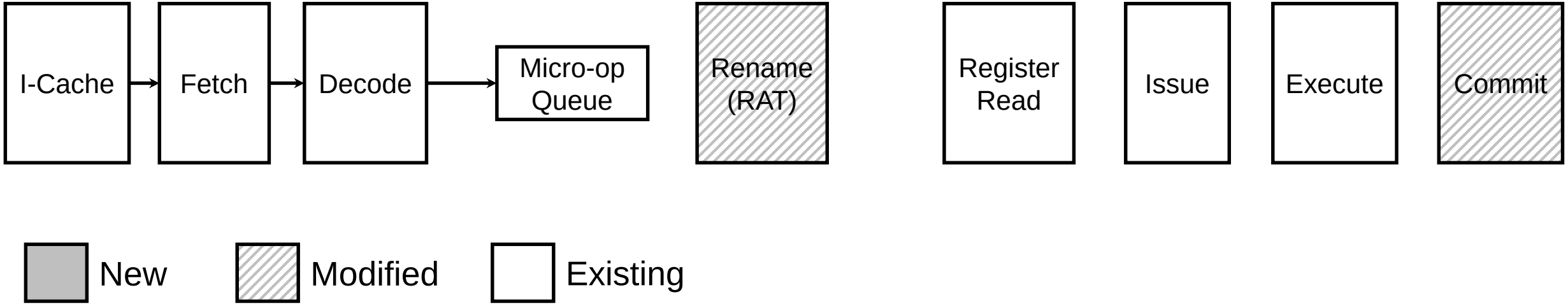

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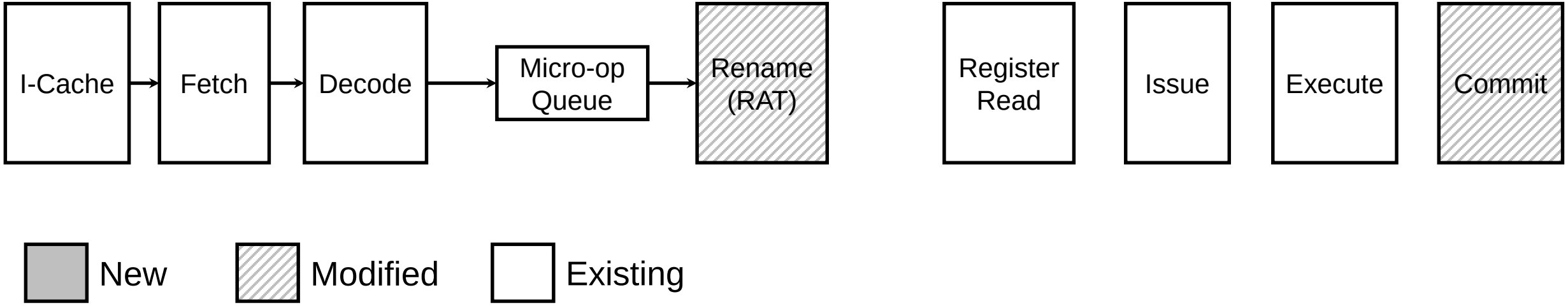

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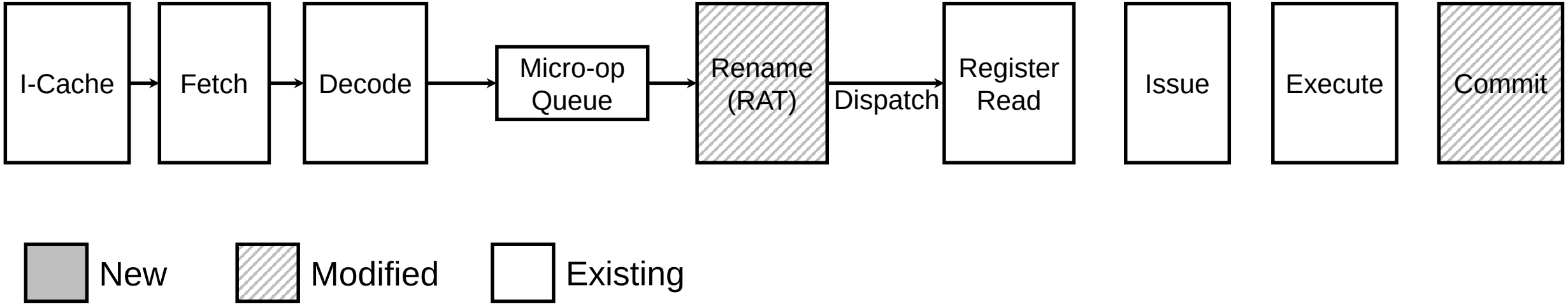

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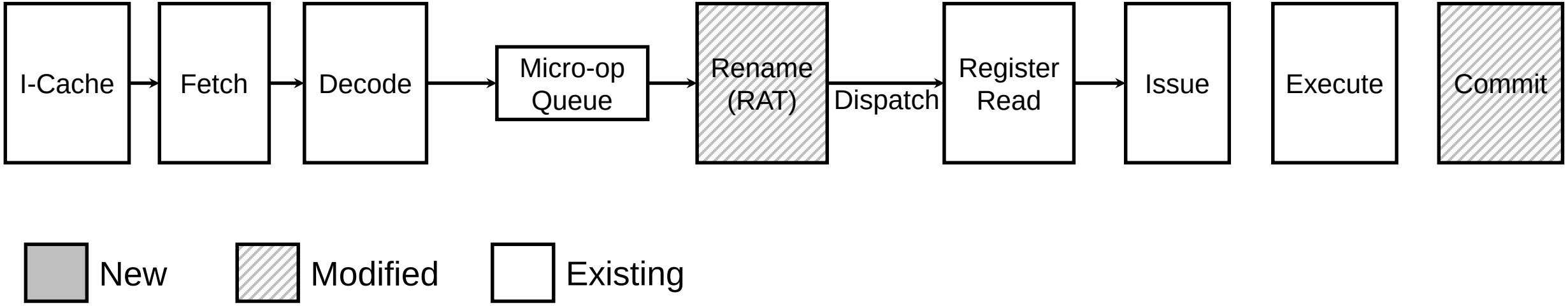

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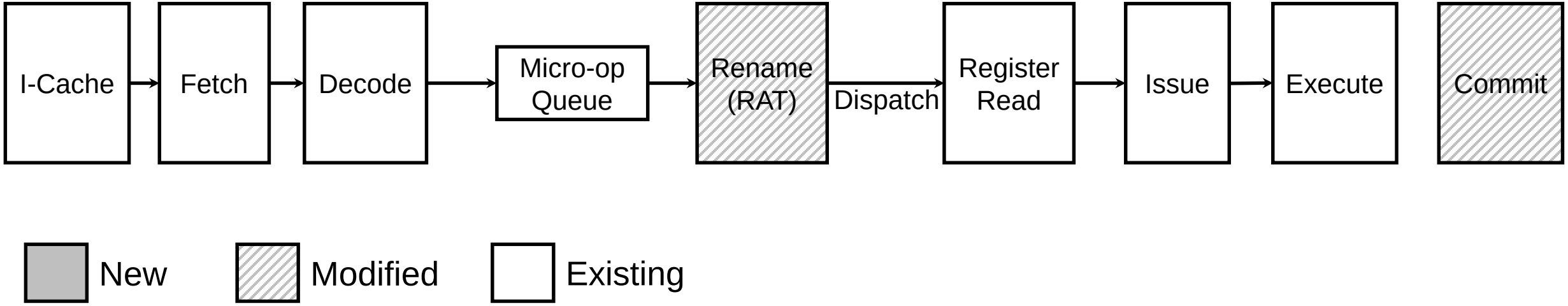

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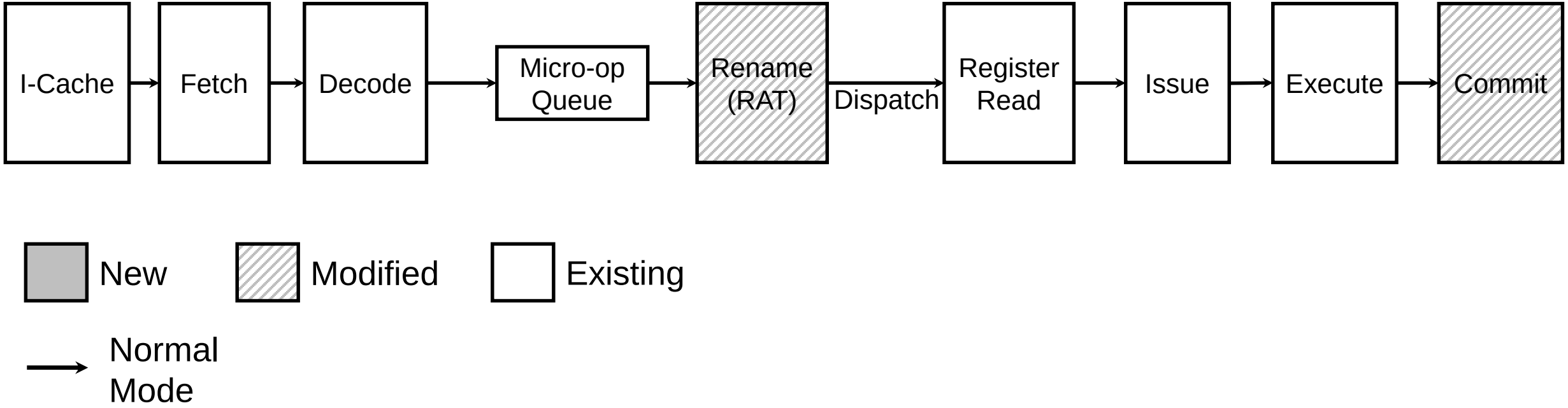

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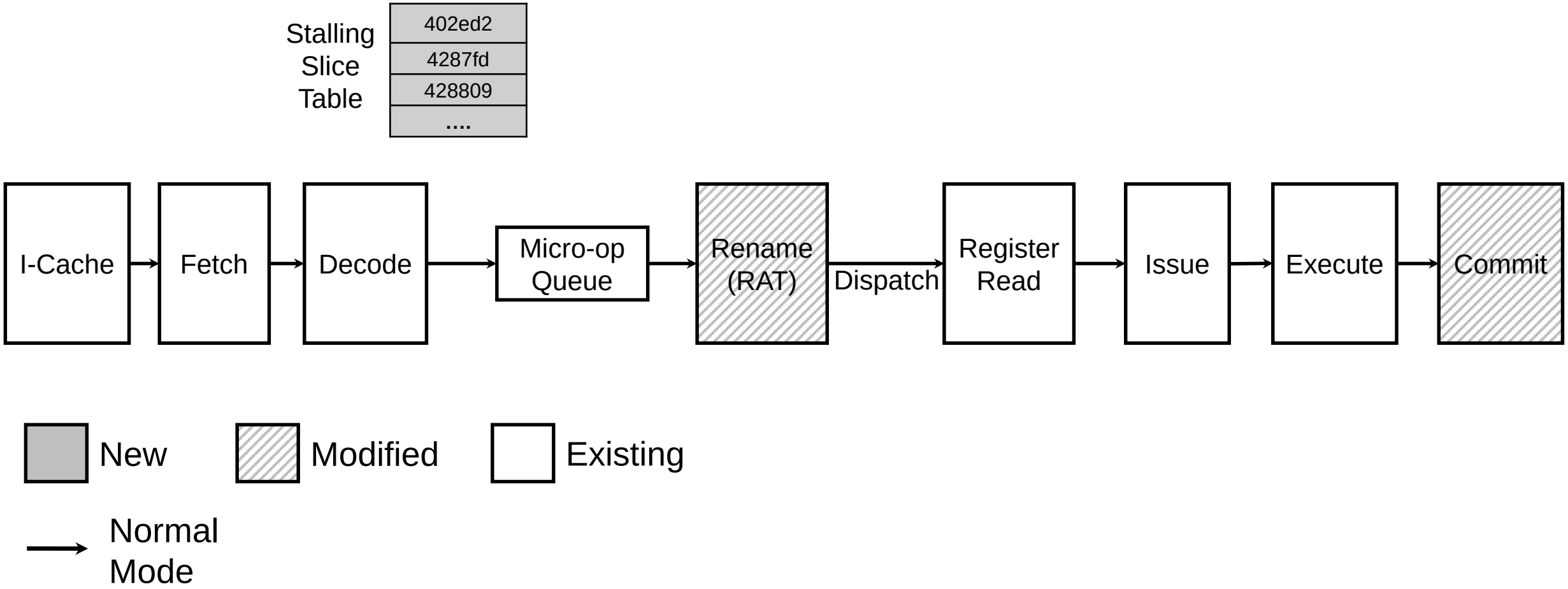

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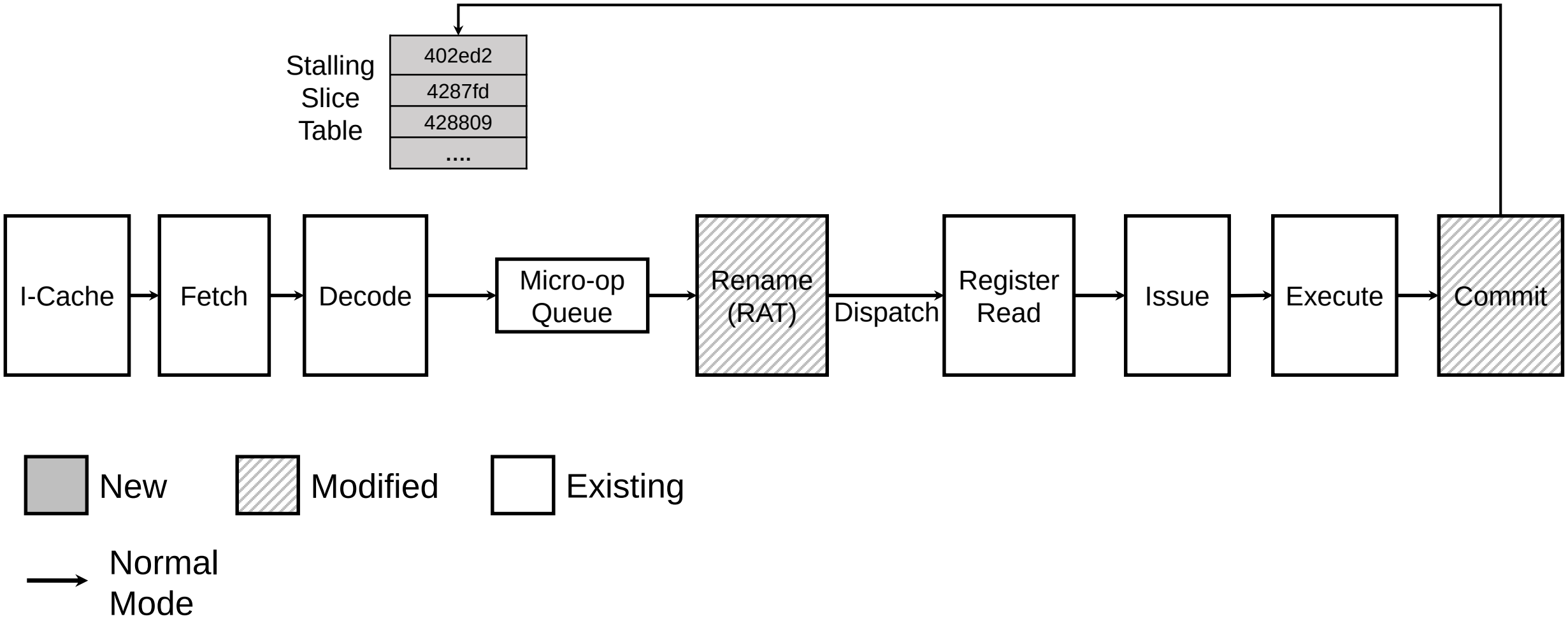

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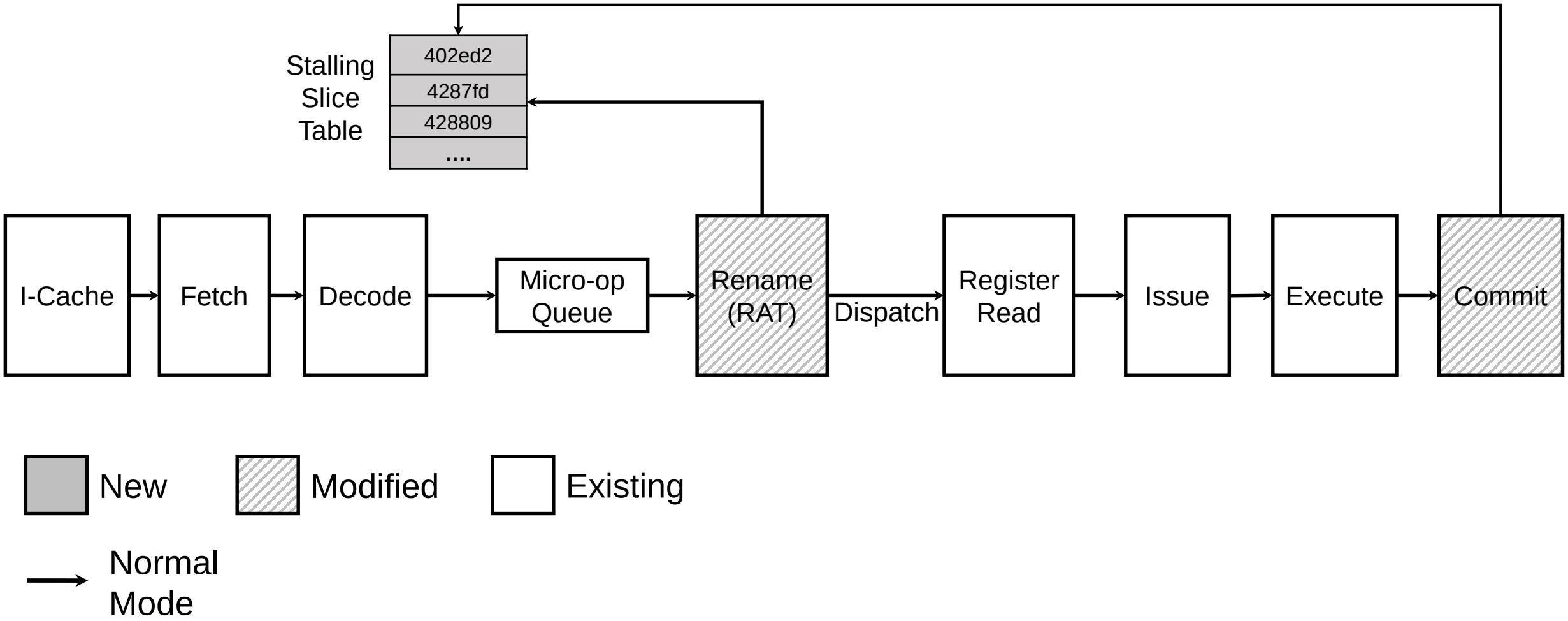

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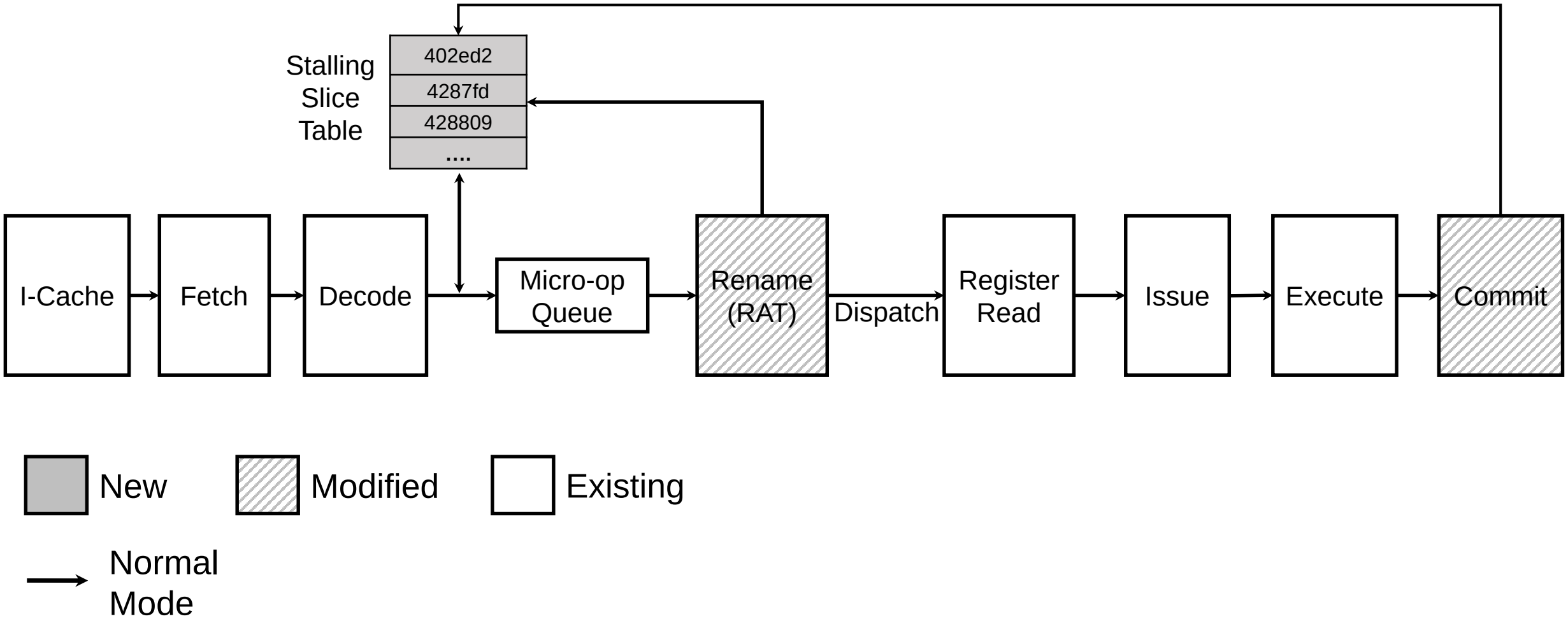

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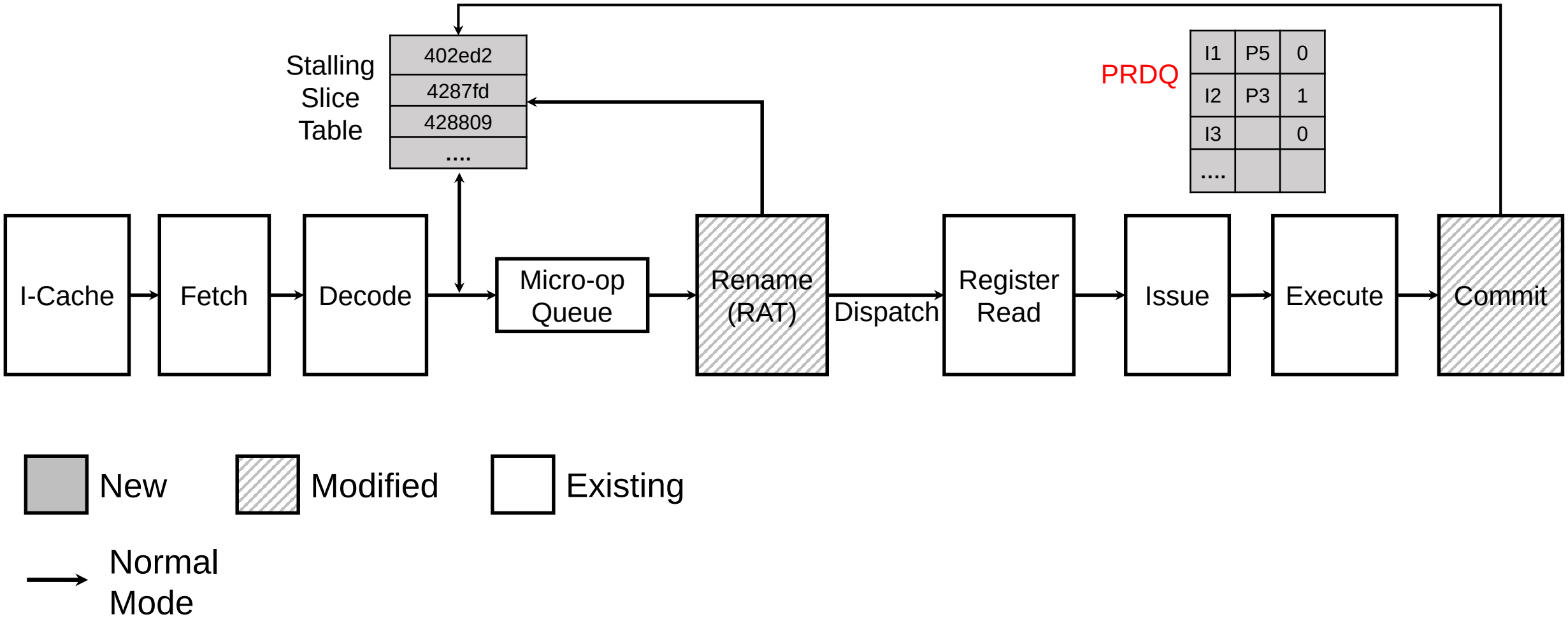

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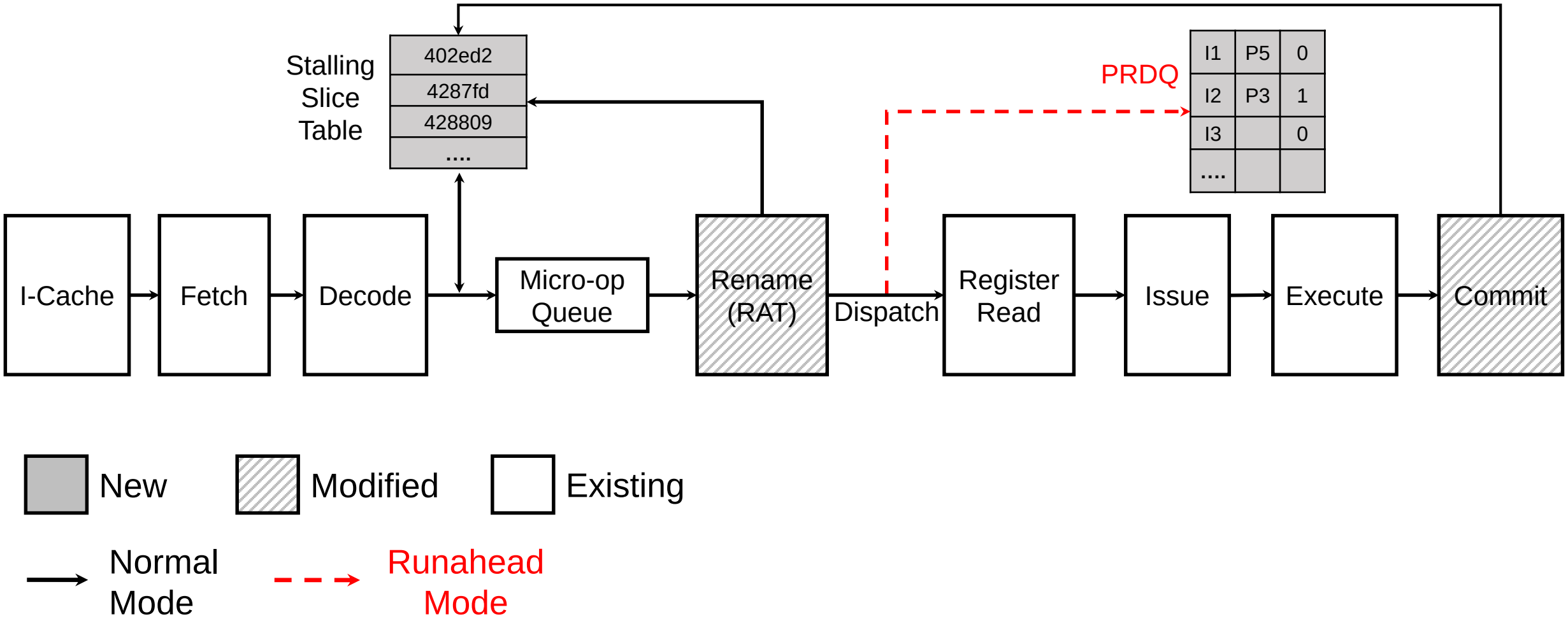

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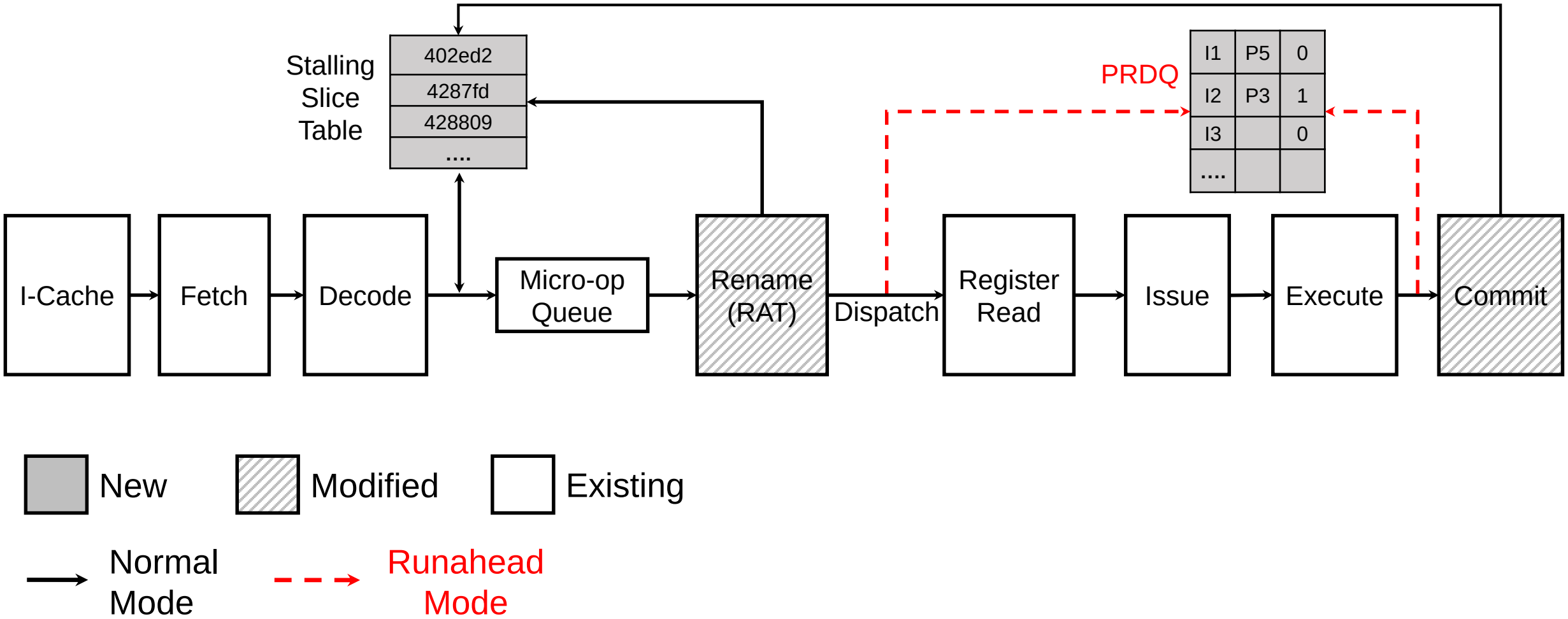

# Evaluation

**OoO:** Baseline out-of-order core

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**RA:** Runahead execution*
-- No short runahead intervals

*[Mutlu et al. ISCA'05]

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-- No overlapping intervals

*[Mutlu et al. ISCA'05]

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**RA-buffer:** Runahead buffer**

*[Mutlu et al. ISCA'05] **[Hashemi et al. MICRO'15]

# Evaluation

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**RA:** Runahead execution*

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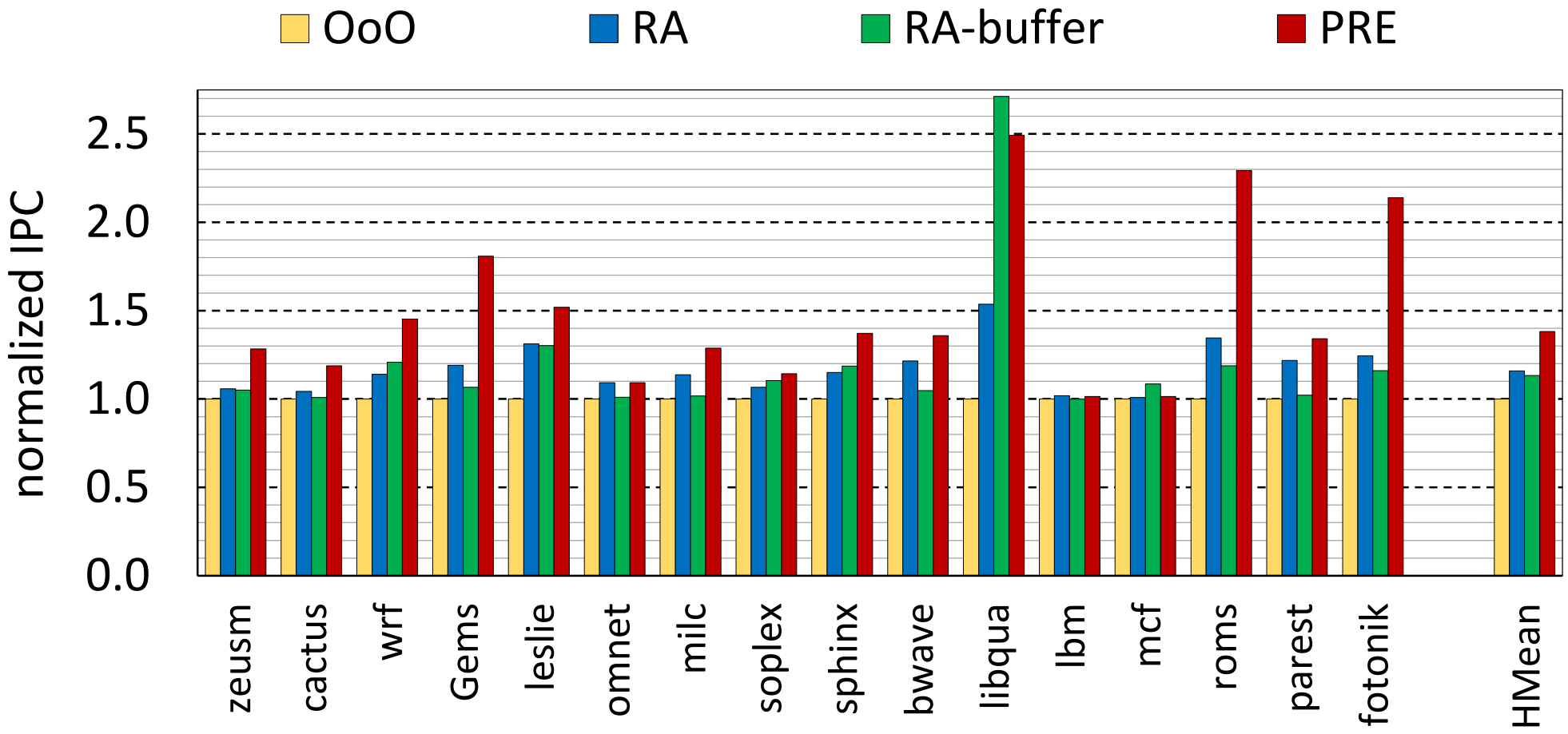
-- No overlapping intervals

**RA-buffer:** Runahead buffer**

**PRE:** Precise runahead execution***

*[Mutlu et al. ISCA'05] **[Hashemi et al. MICRO'15] ***[Naithani et al. HPCA'20]

# Evaluation -- Performance



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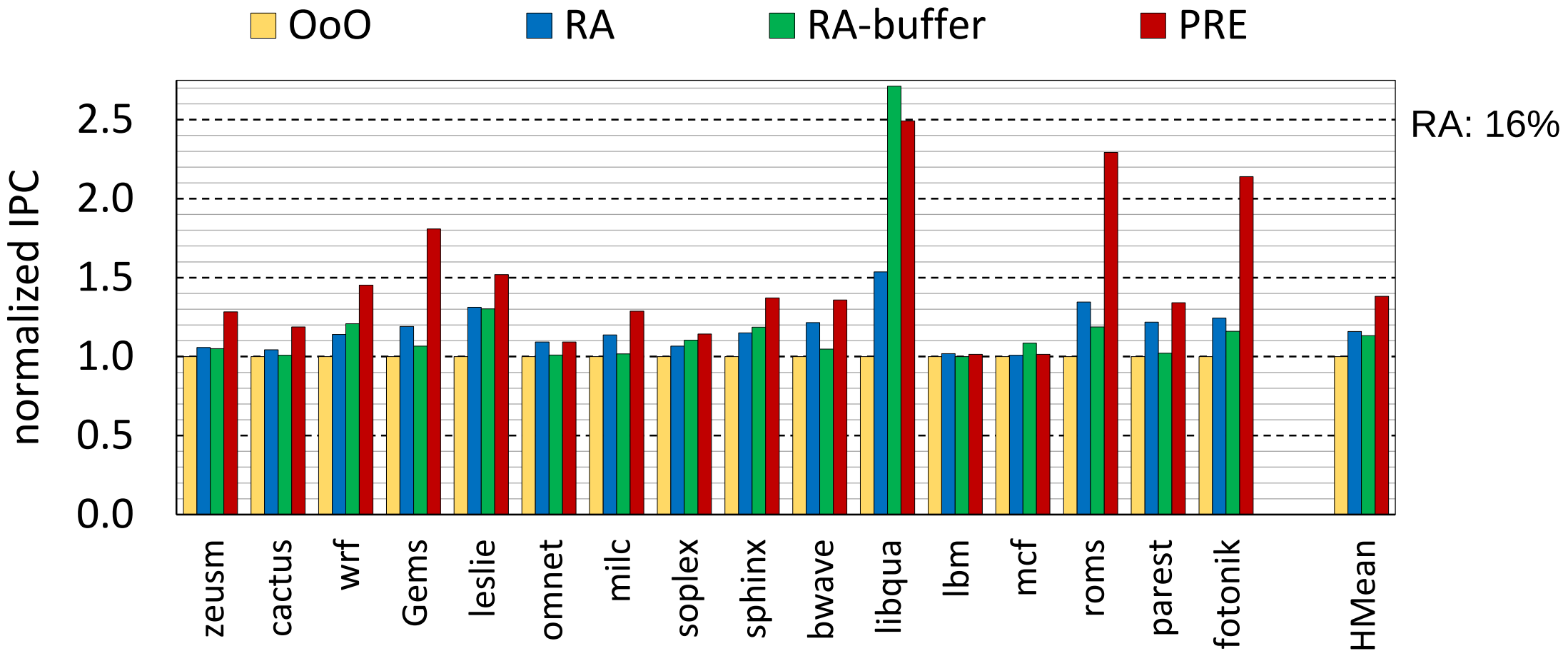

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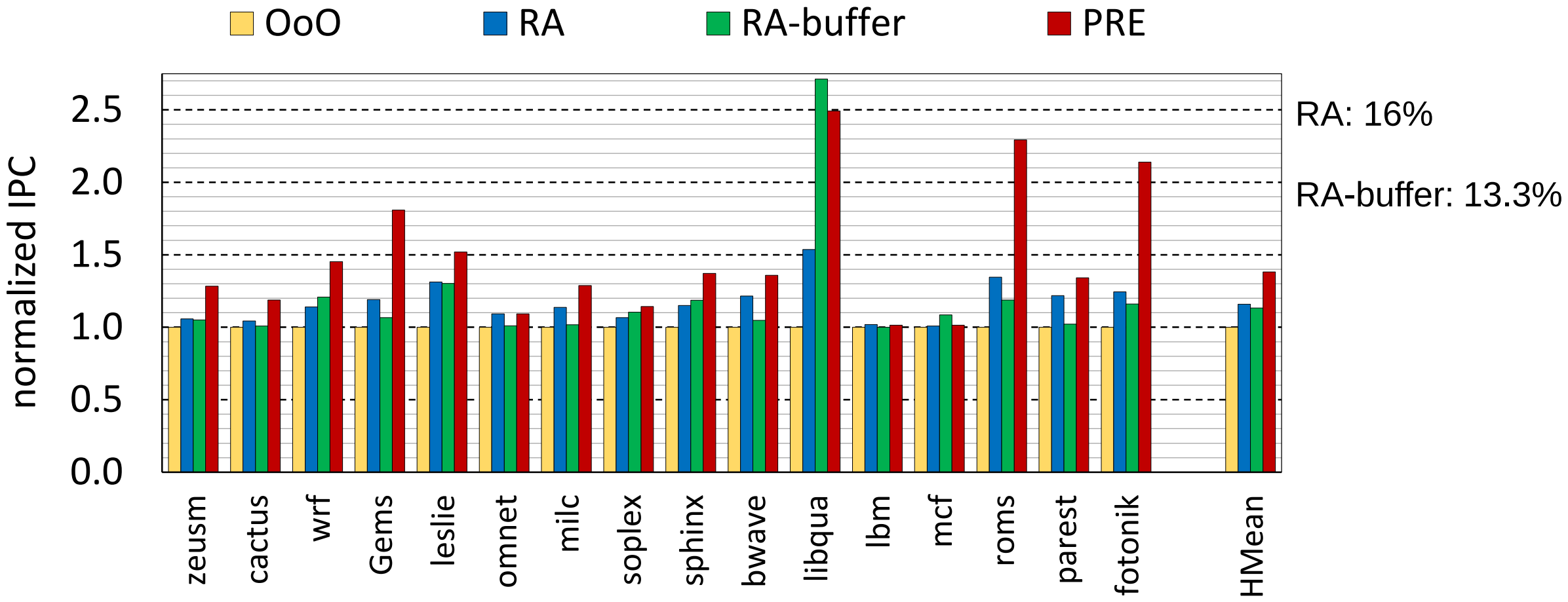

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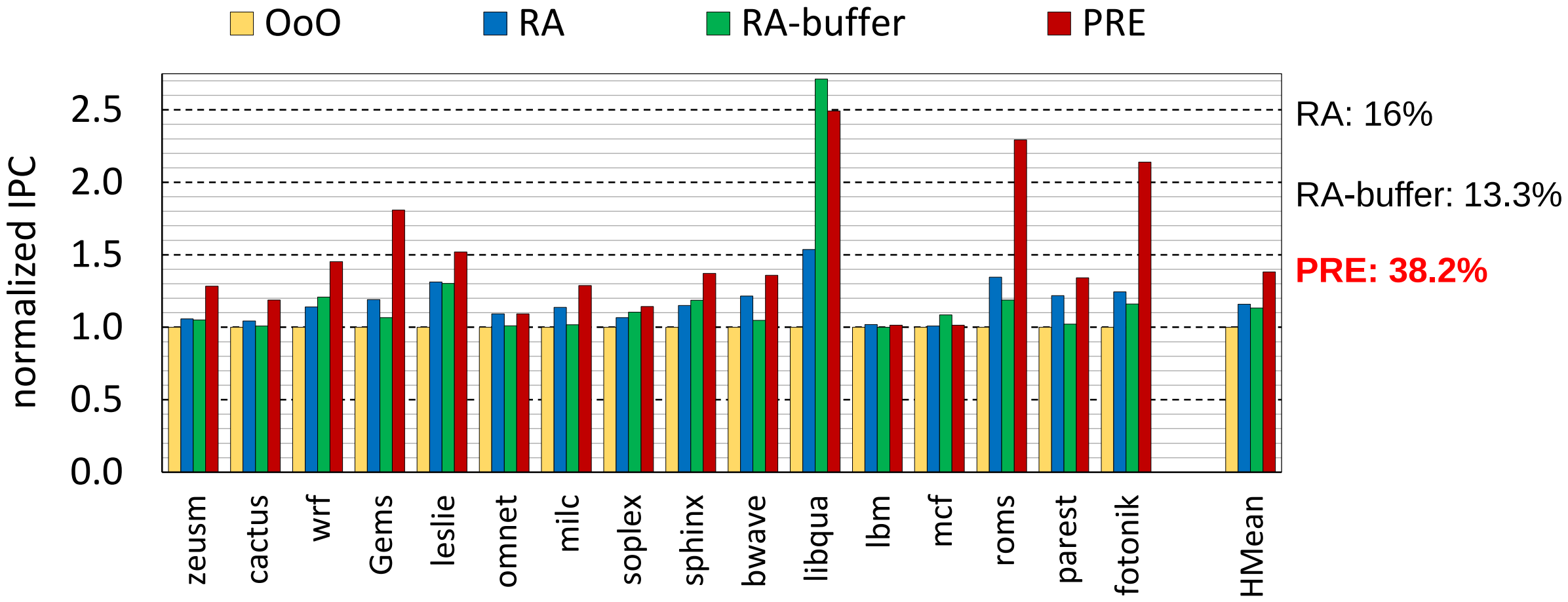
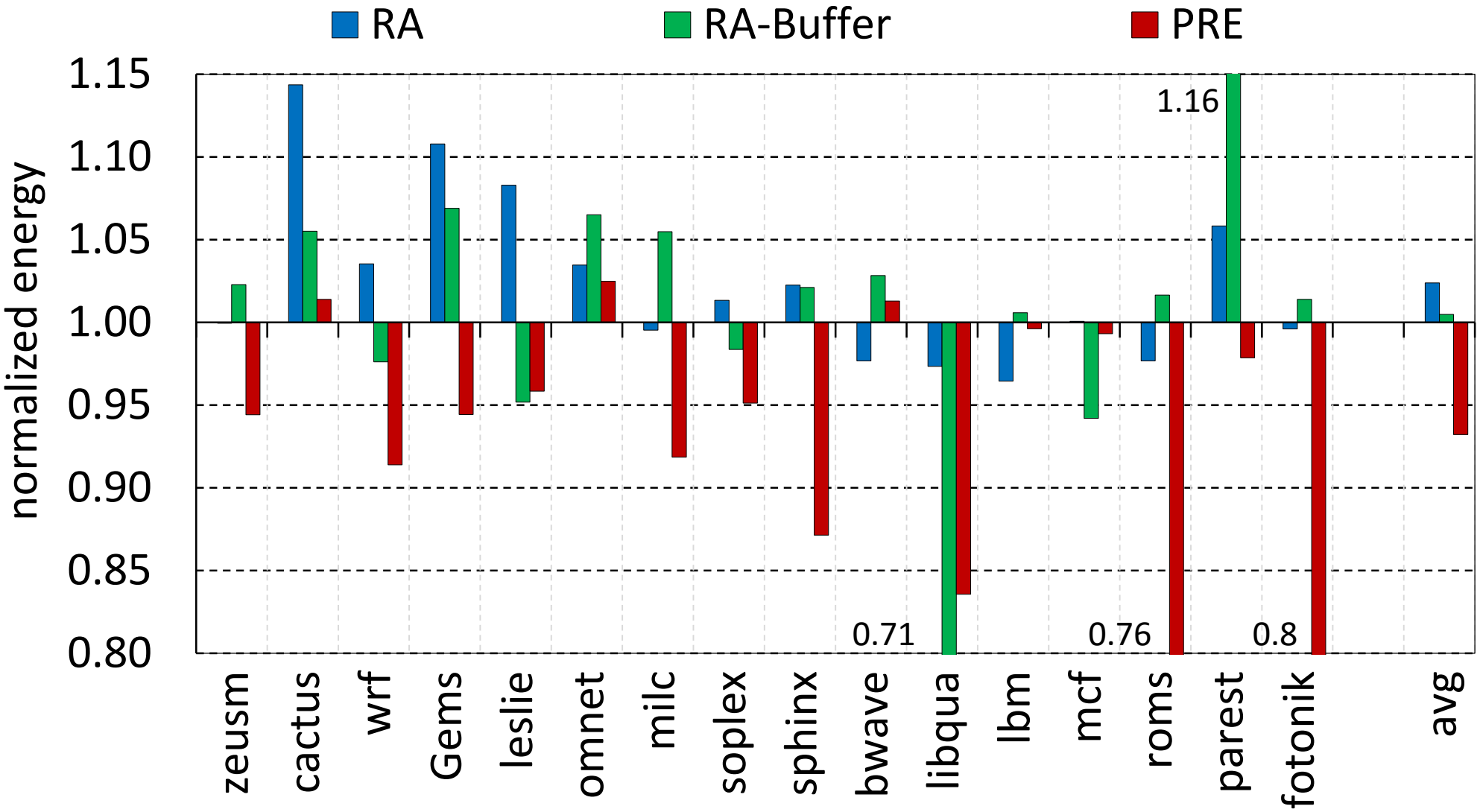
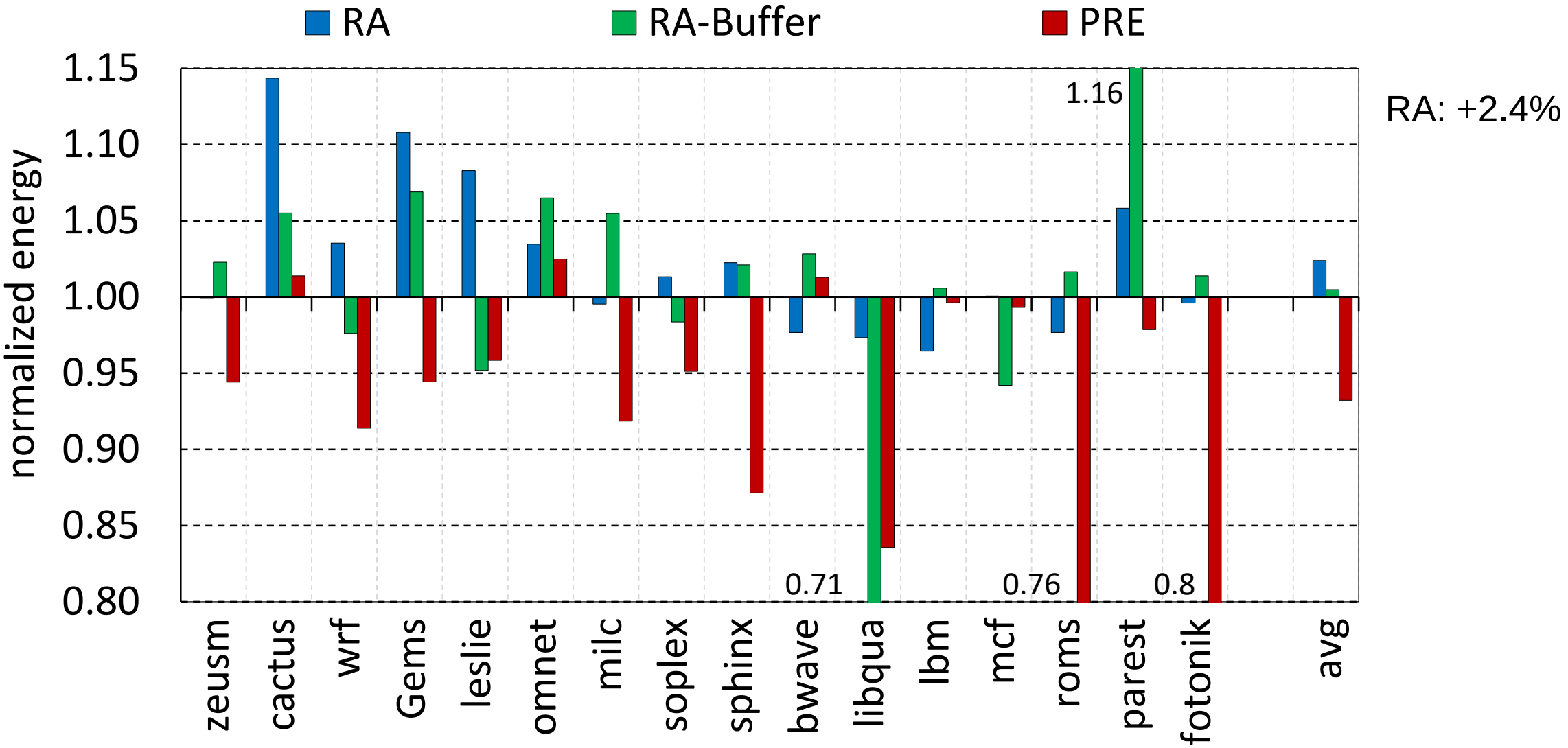


# Evaluation -- Energy

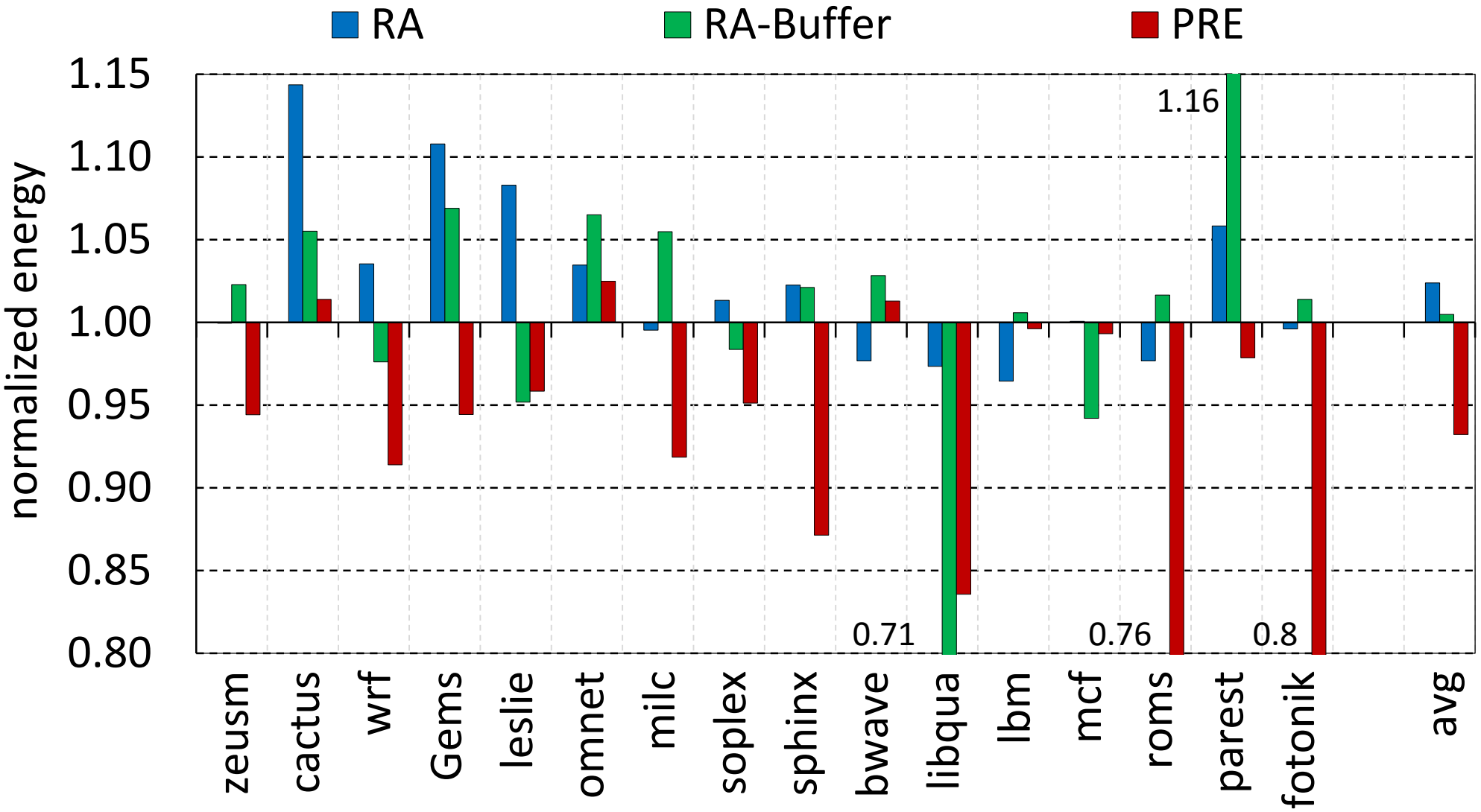


# Evaluation -- Energy




RA: +2.4%

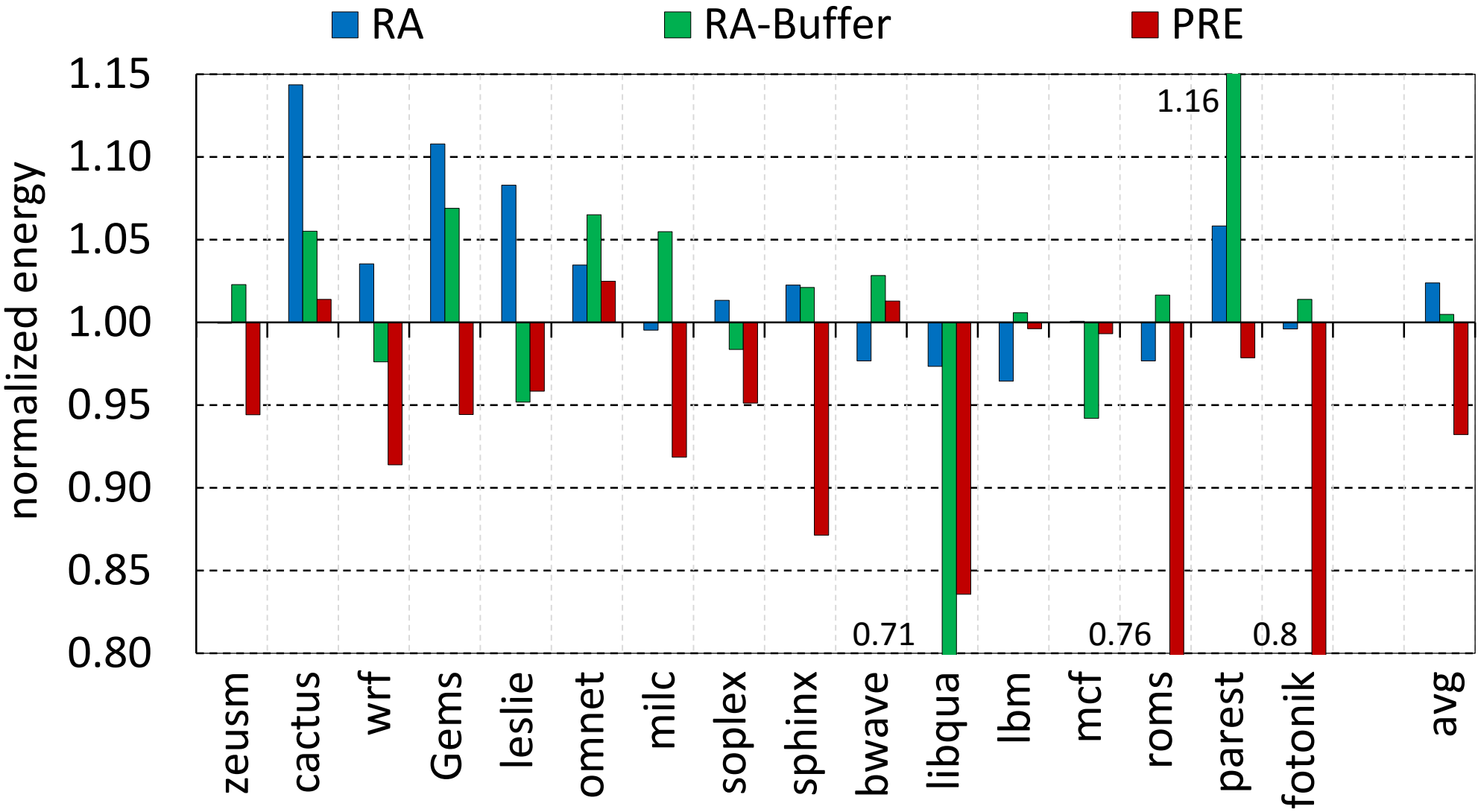
# Evaluation -- Energy




RA: +2.4%

RA-buffer: Same

# Evaluation -- Energy

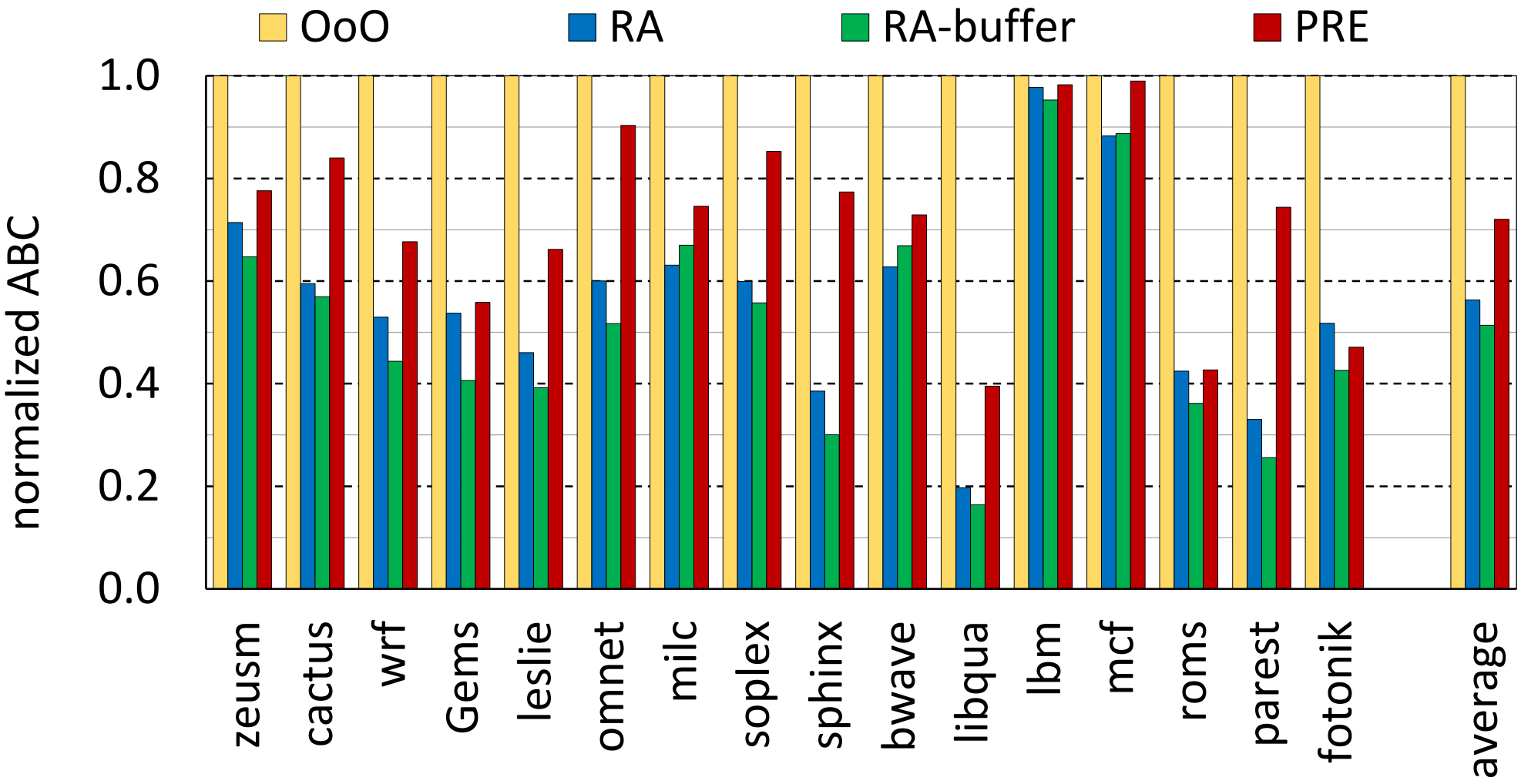



RA: +2.4%

RA-buffer: Same

**PRE: −6.8%**

# Evaluation -- Reliability




RA: 43.7%

RA-buffer: 48.6%

**PRE: 28%**

# Runahead Techniques Relative to OoO Core

| | Runahead execution | Runahead buffer | **Precise runahead** |
|---|---|---|---|
| Flush ROB | ✓ | ✓ | ✗ |
| Execute all future instructions | ✓ | Only one slice | All slices |
| Performance | High ↑ | High ↑ | Very high ↑↑ |
| Energy Efficiency | Low ↓ | Same | High ↑ |

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| Energy Efficiency | Low ↓ | Same | High ↑ |
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| Performance | High ↑ | High ↑ | Very high ↑↑ |
| Energy Efficiency | Low ↓ | Same | High ↑ |
| Reliability | High ↑ | High ↑ | |

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| Performance | High ↑ | High ↑ | Very high ↑↑ |
| Energy Efficiency | Low ↓ | Same | High ↑ |
| Reliability | High ↑ | High ↑ | Medium ↑ |

# Summary of Novel Contributions

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   Exploits the difference in vulnerability between core types to improve reliability

2. Dispatch halting for single-threaded workloads

   Exploits invulnerable speculation to improve reliability under memory accesses

3. Precise runahead execution for single-threaded workloads

   Executes only useful future instructions after a full-ROB stall without flushing the ROB

# Improving Soft Error Reliability in Modern Processors

**Ajeya Naithani**

**Advisor: Prof. Lieven Eeckhout**

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