Vector Runahead

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Vector Runahead Summary

1. Targets indirect memory accesses
   -- Complex address calculation

2. Purely microarchitectural and speculative

3. Executes multiple loop iterations as a single vector instruction
   -- Workload does not have to be vectorizable

4. Independent of front-end bandwidth

Full-Window Stalls Degrade Performance

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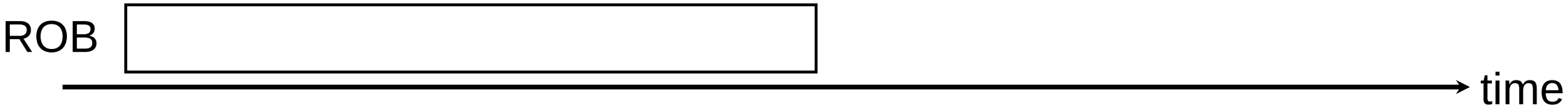

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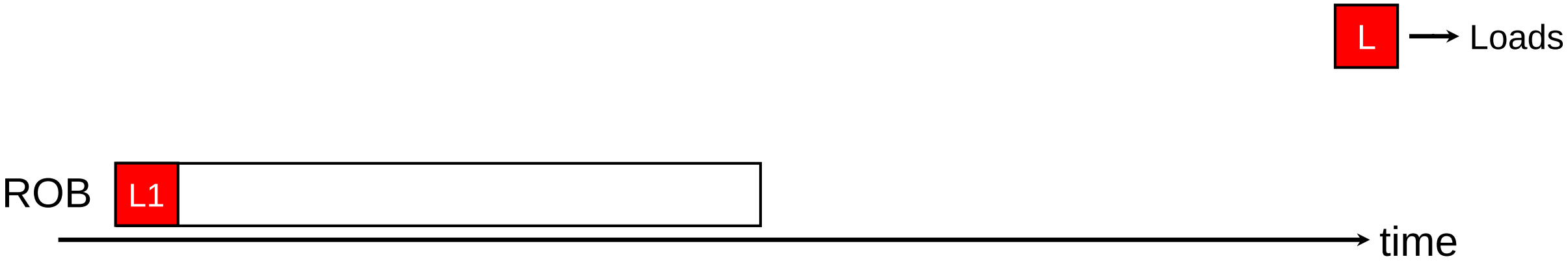

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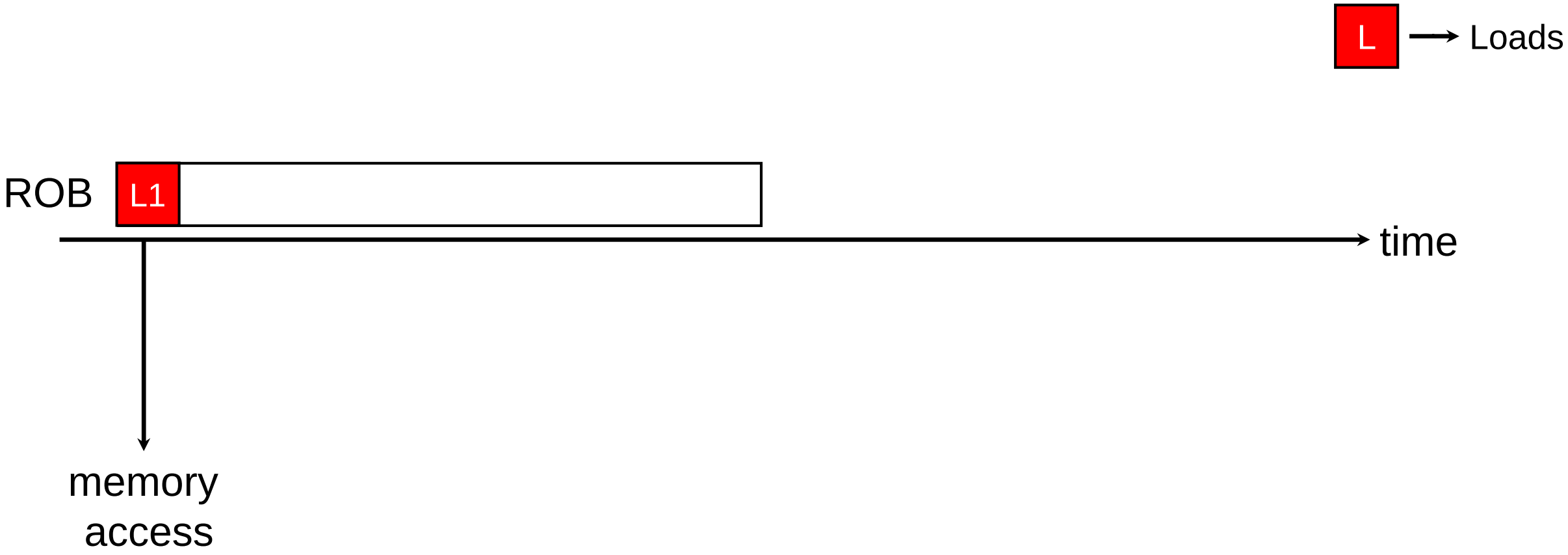

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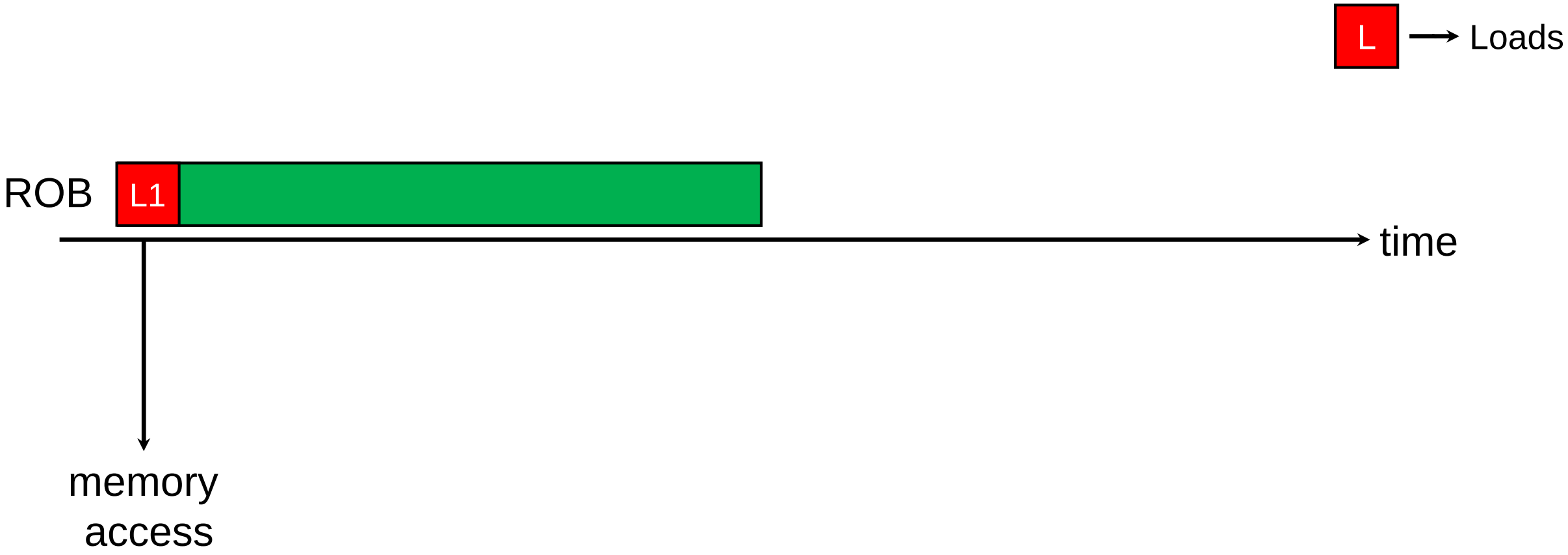

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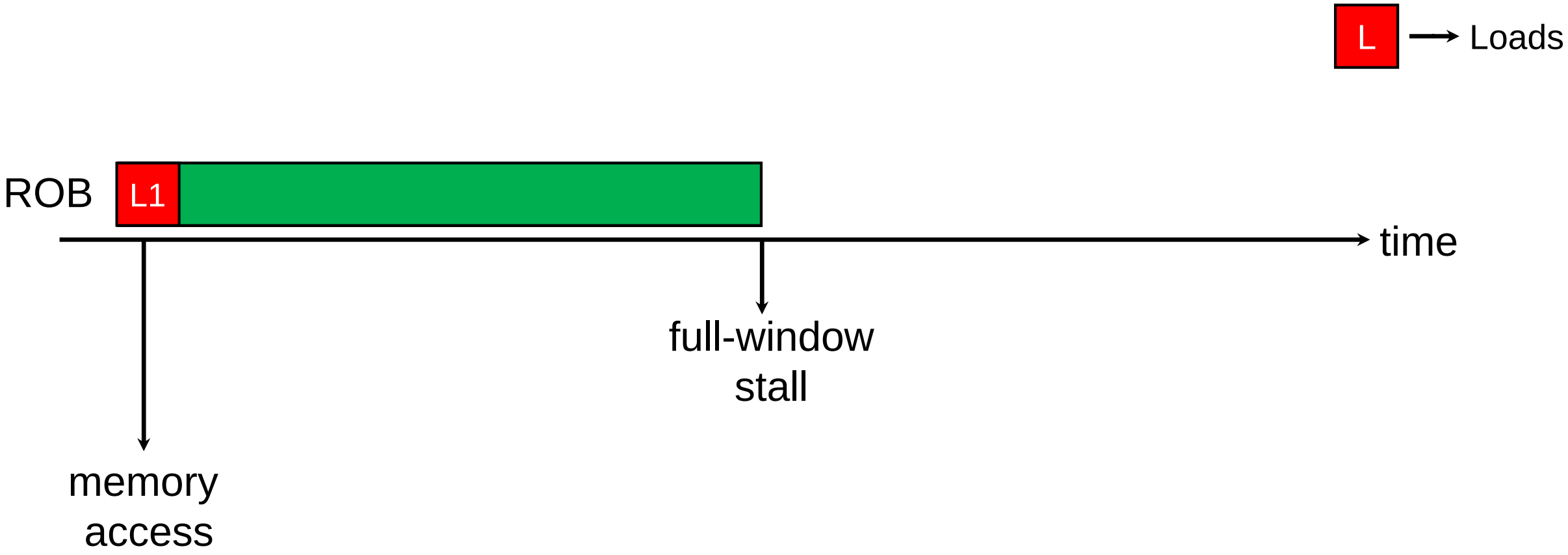

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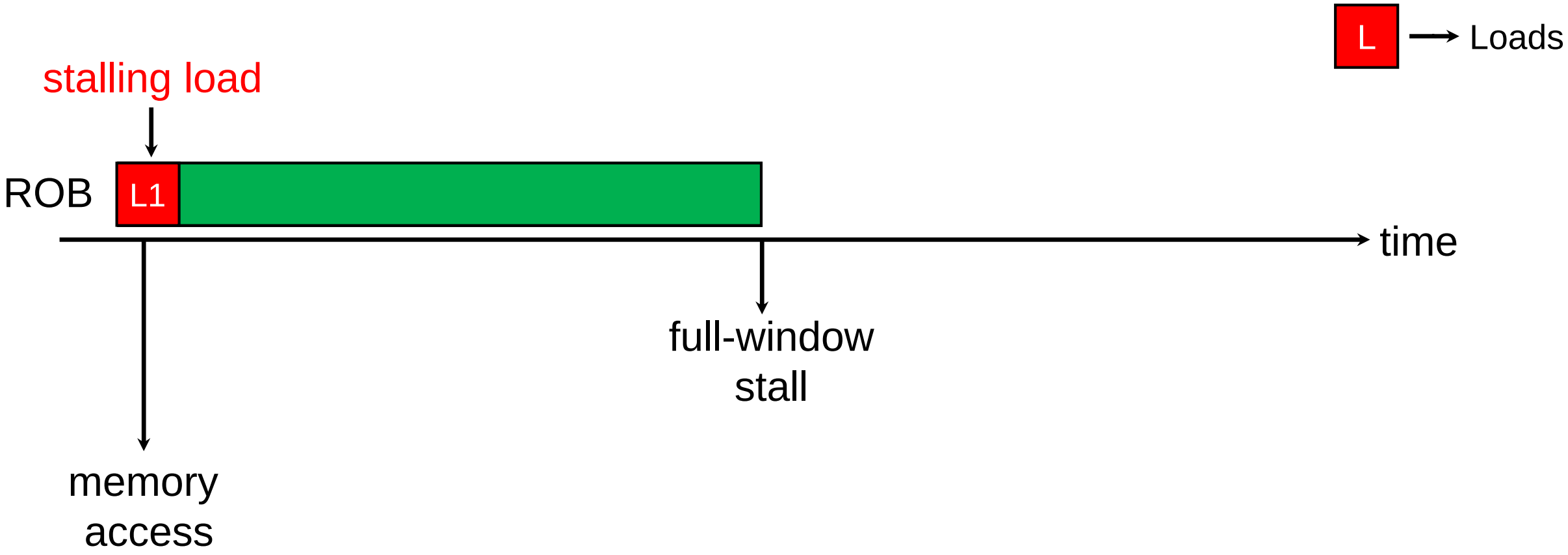

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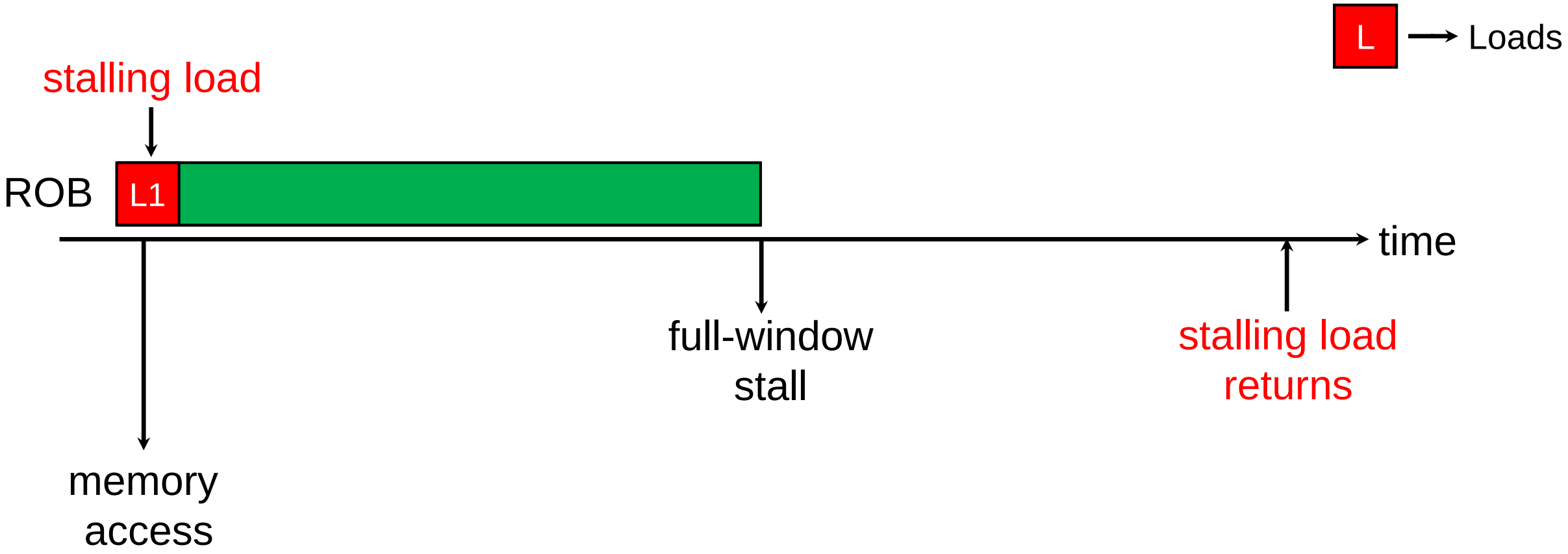

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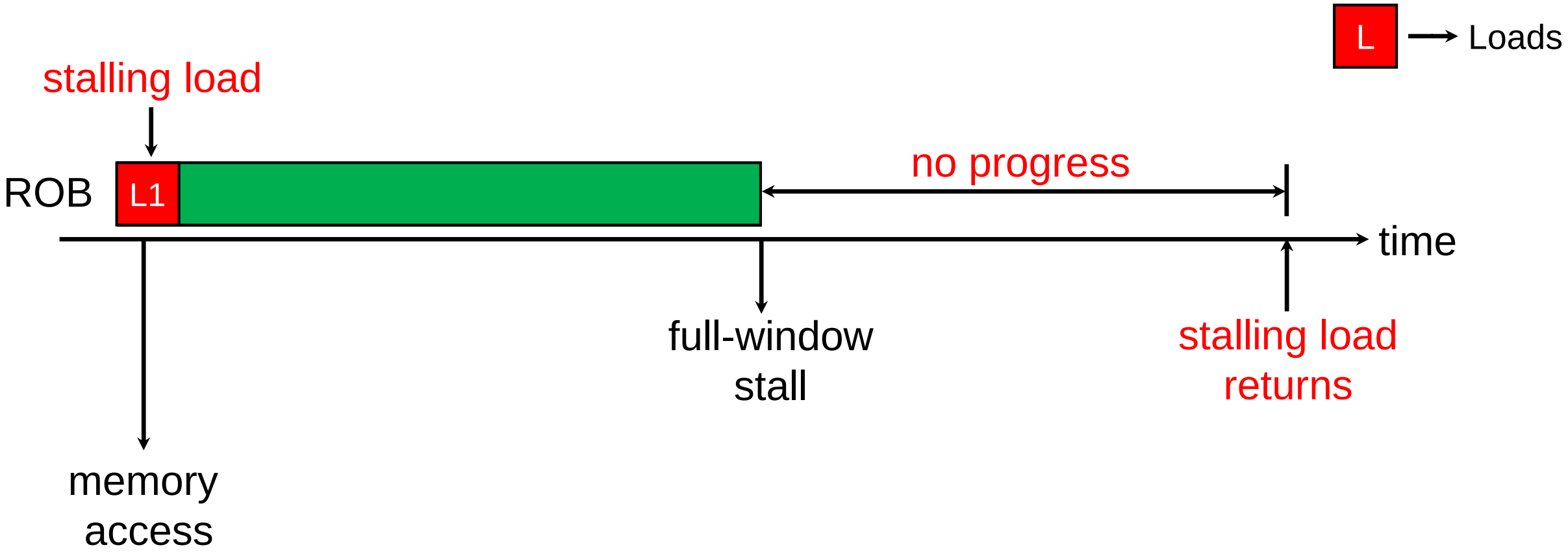

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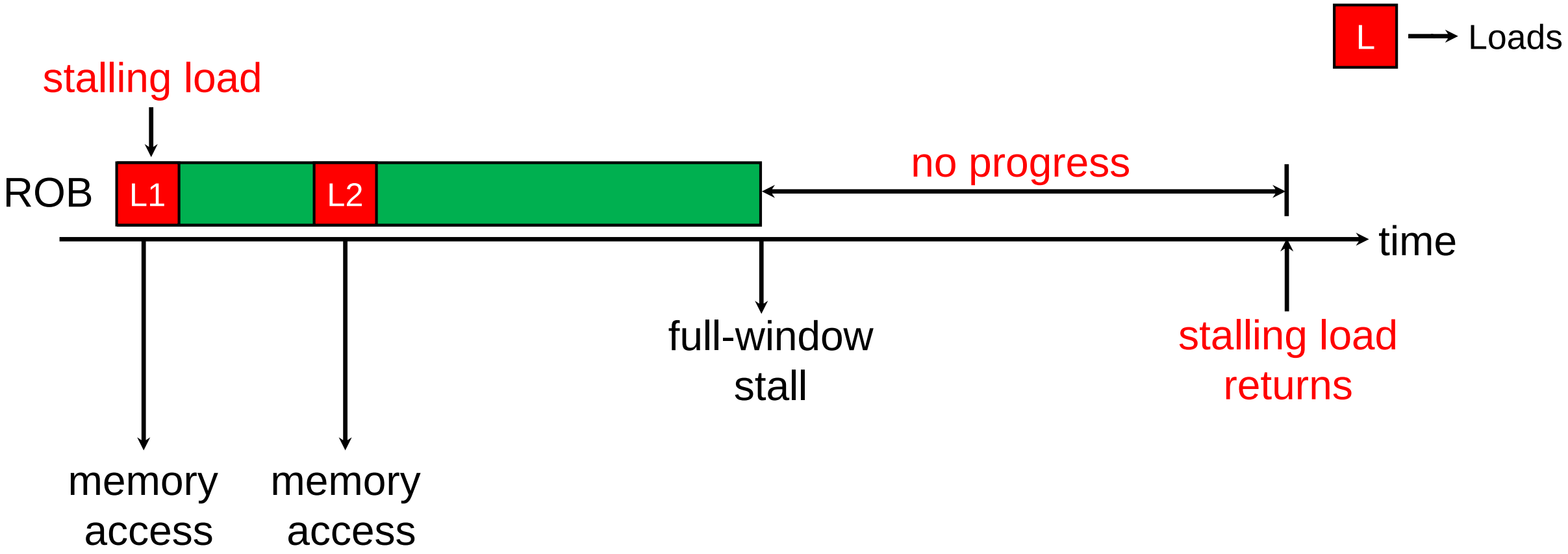

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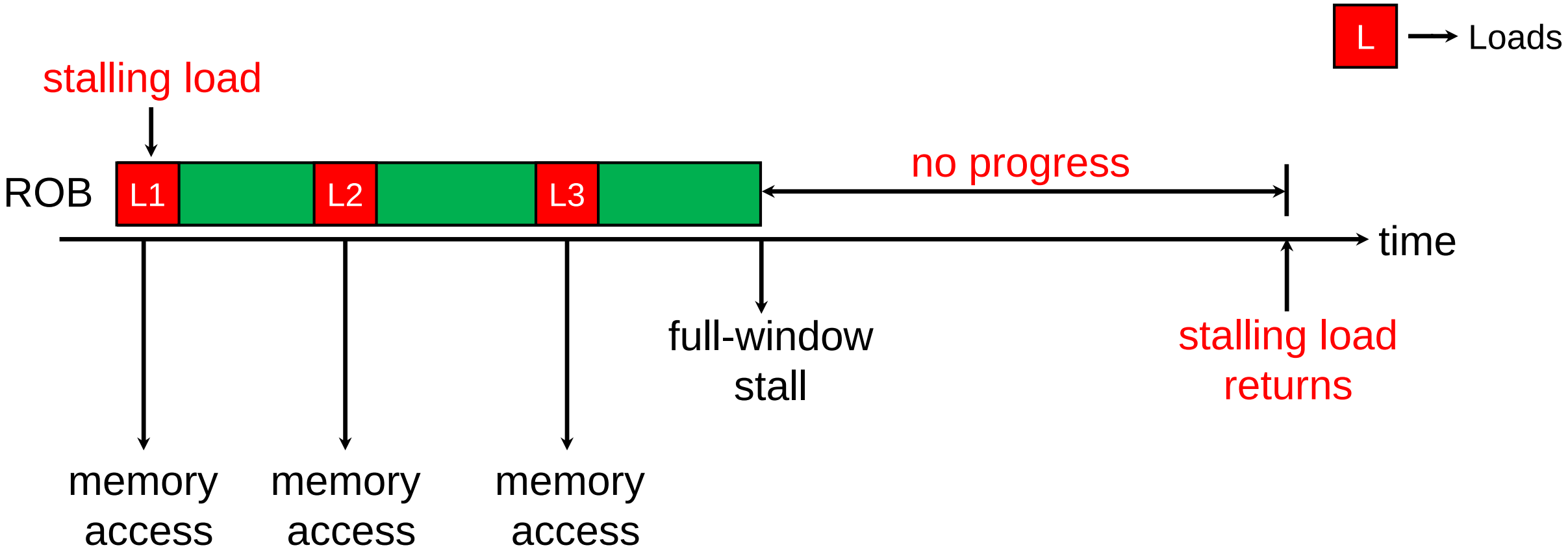

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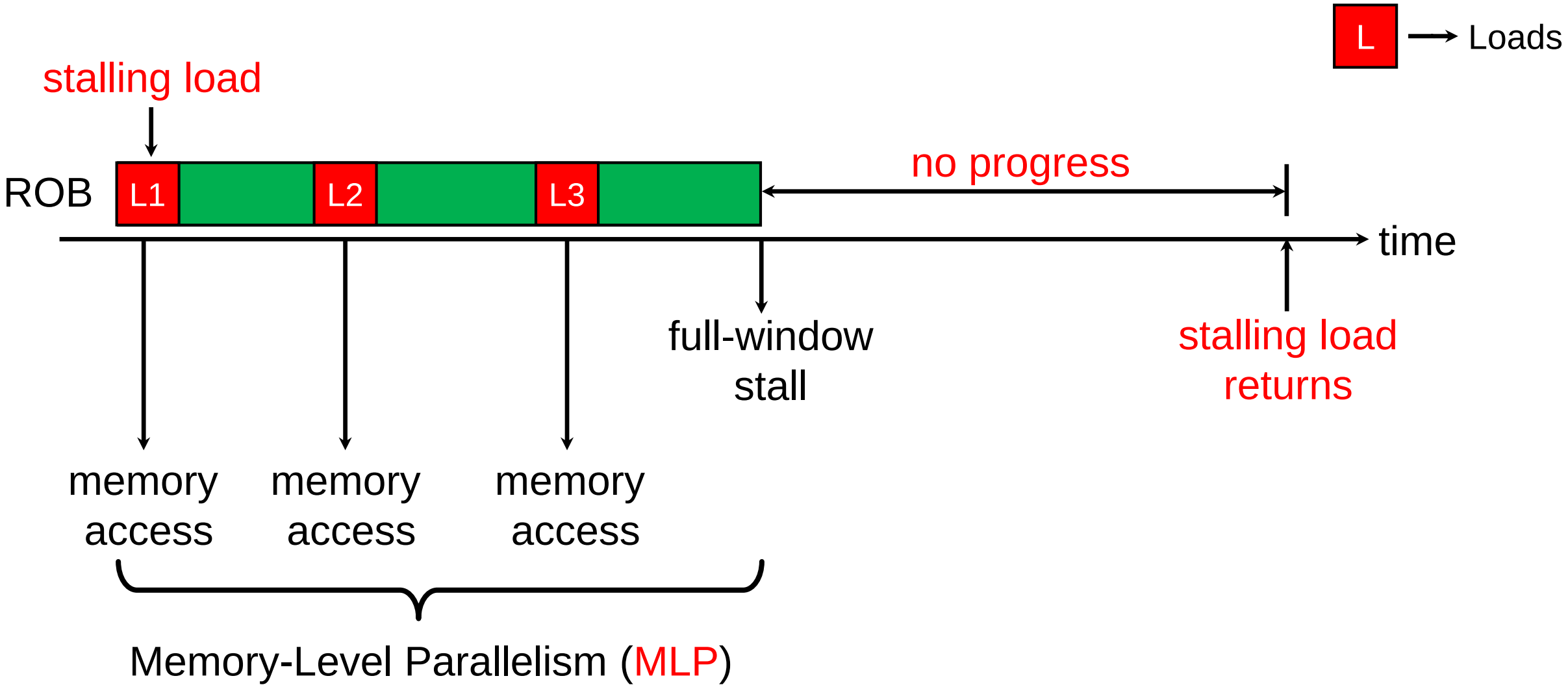
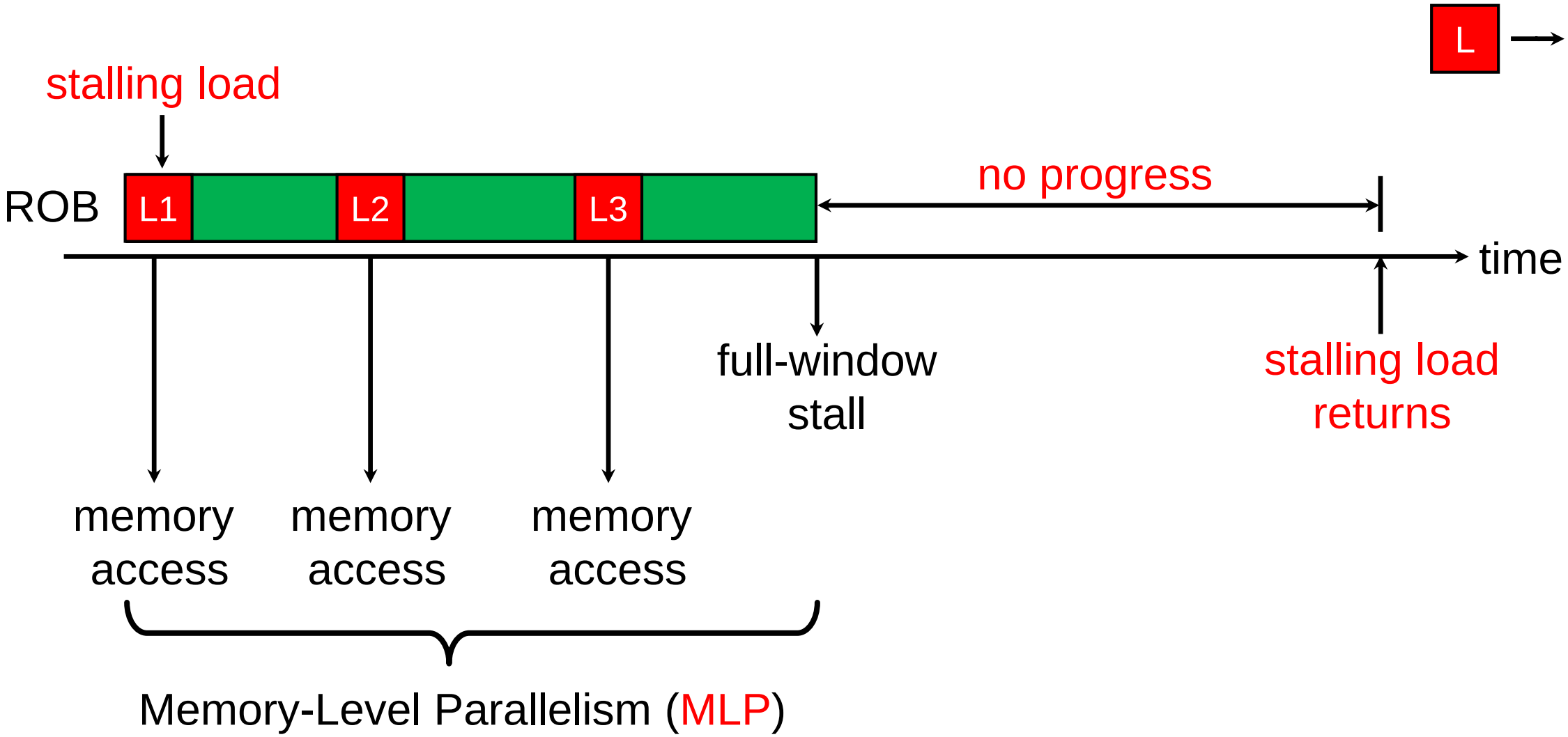


Runahead Execution Prefetches under a Full-Window Stall

ISCA 2005



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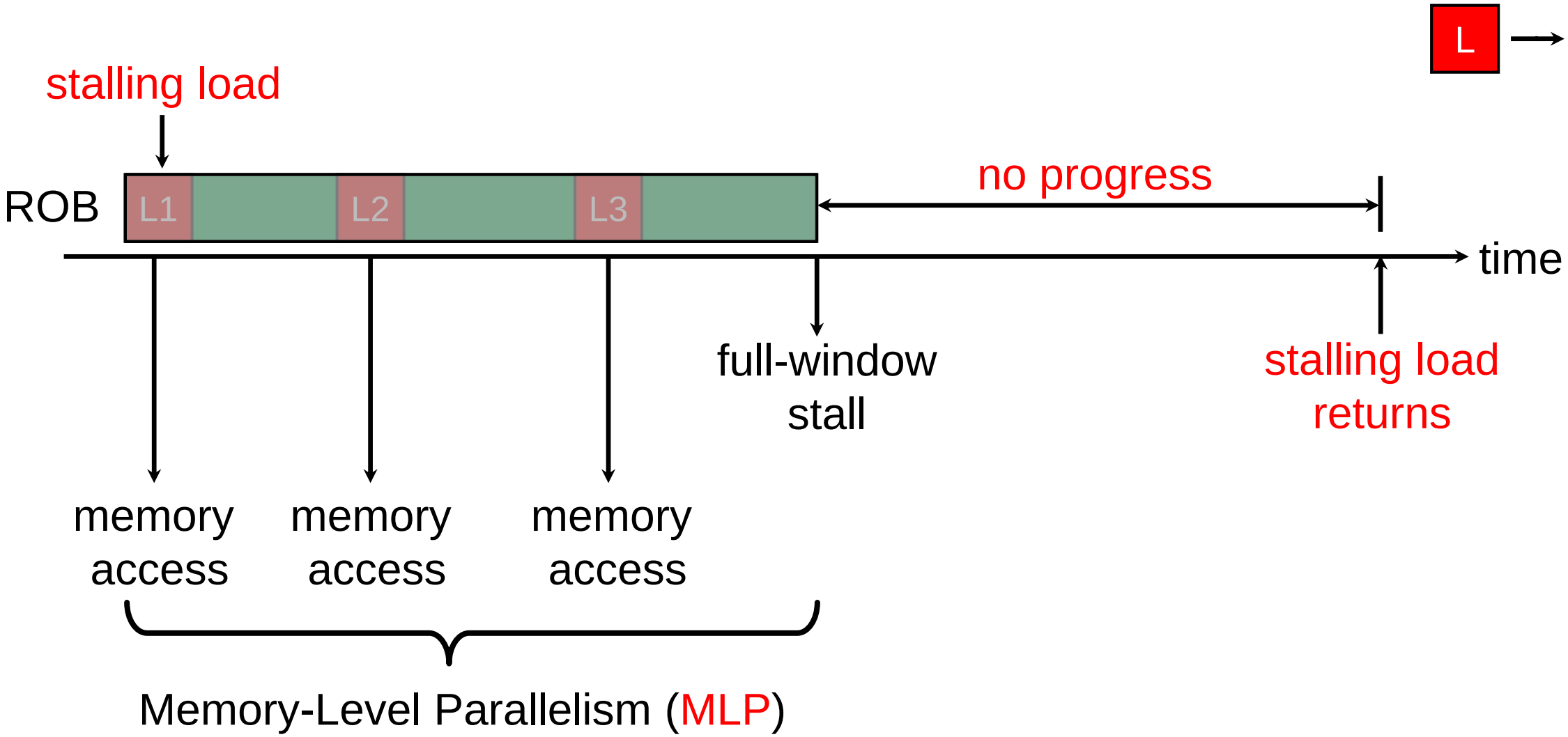

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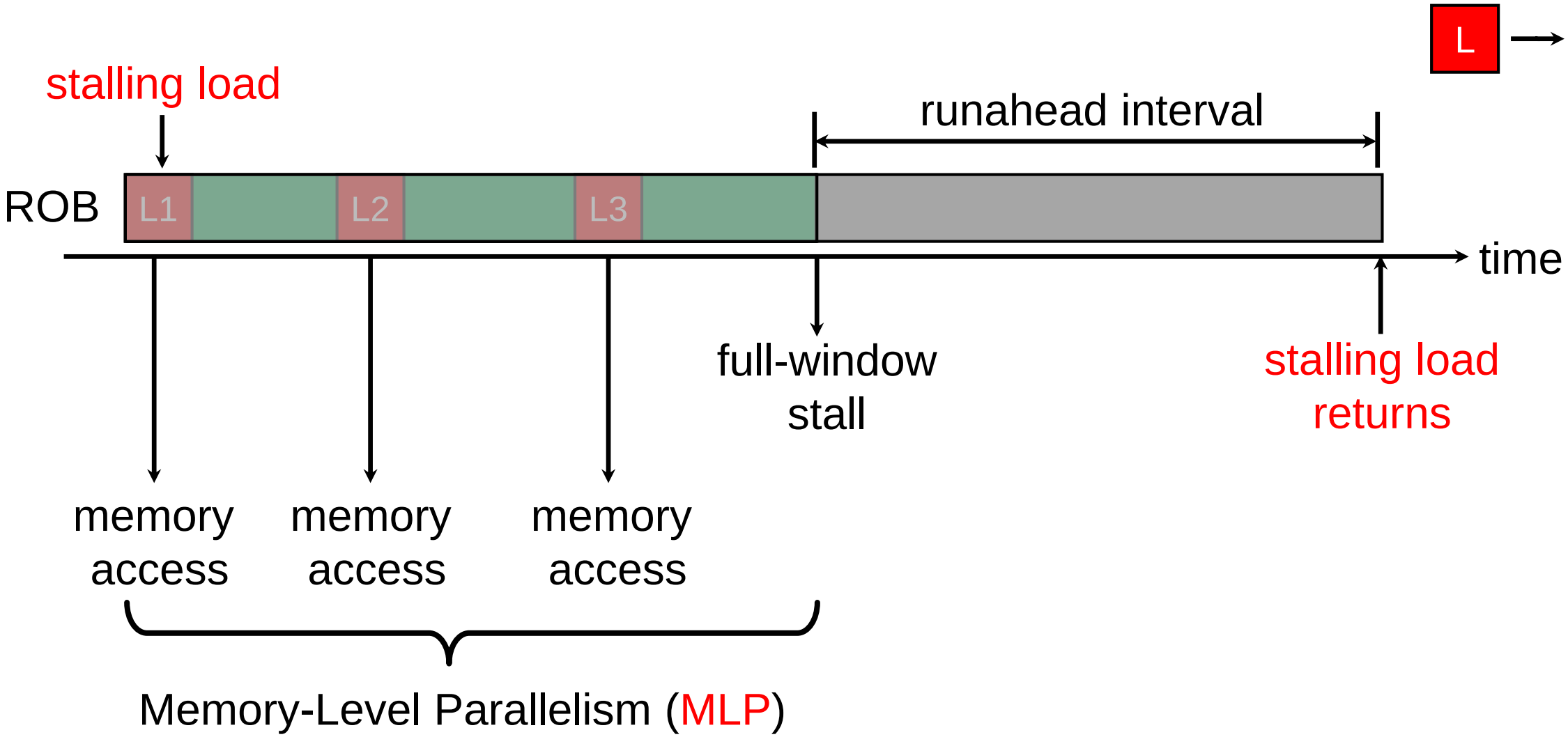

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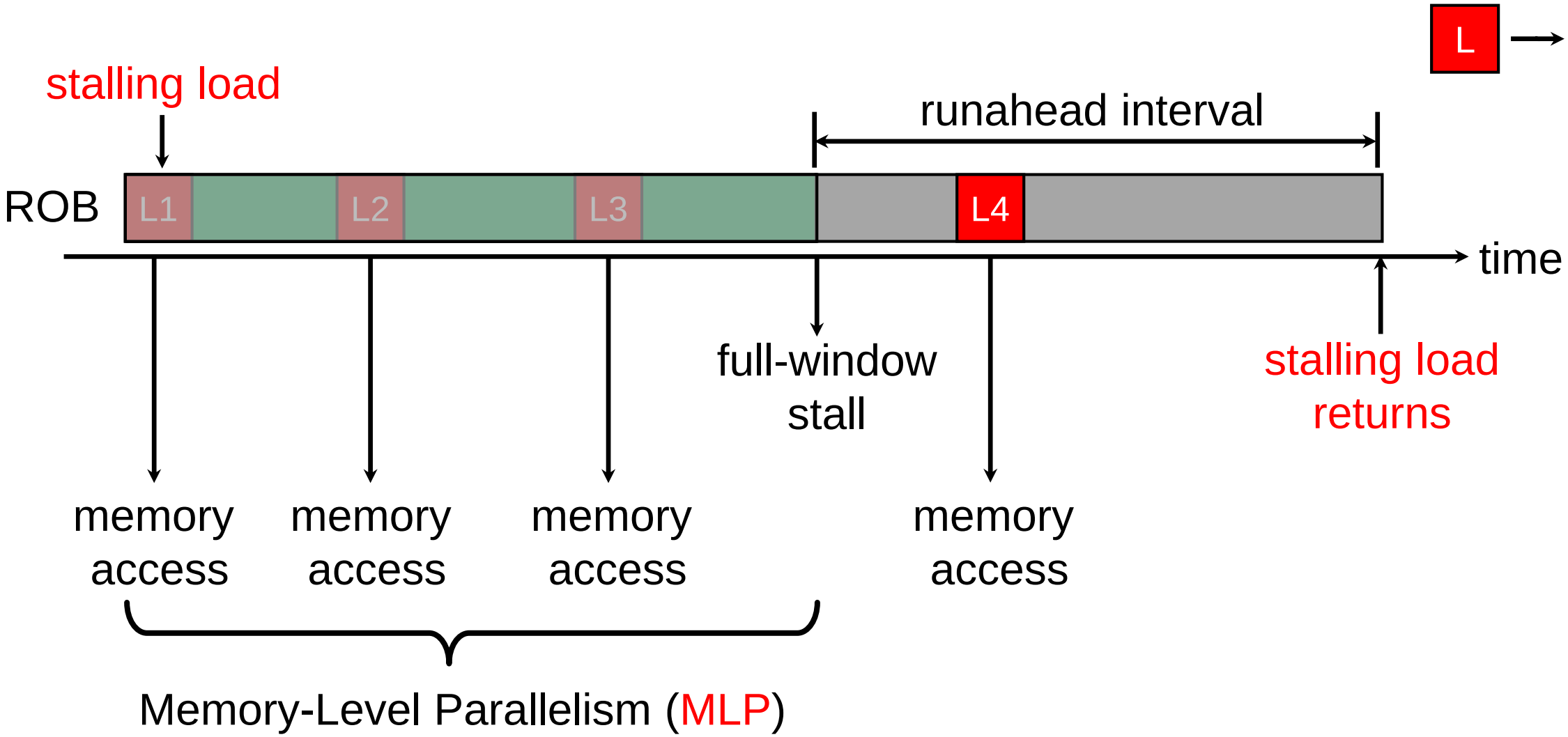

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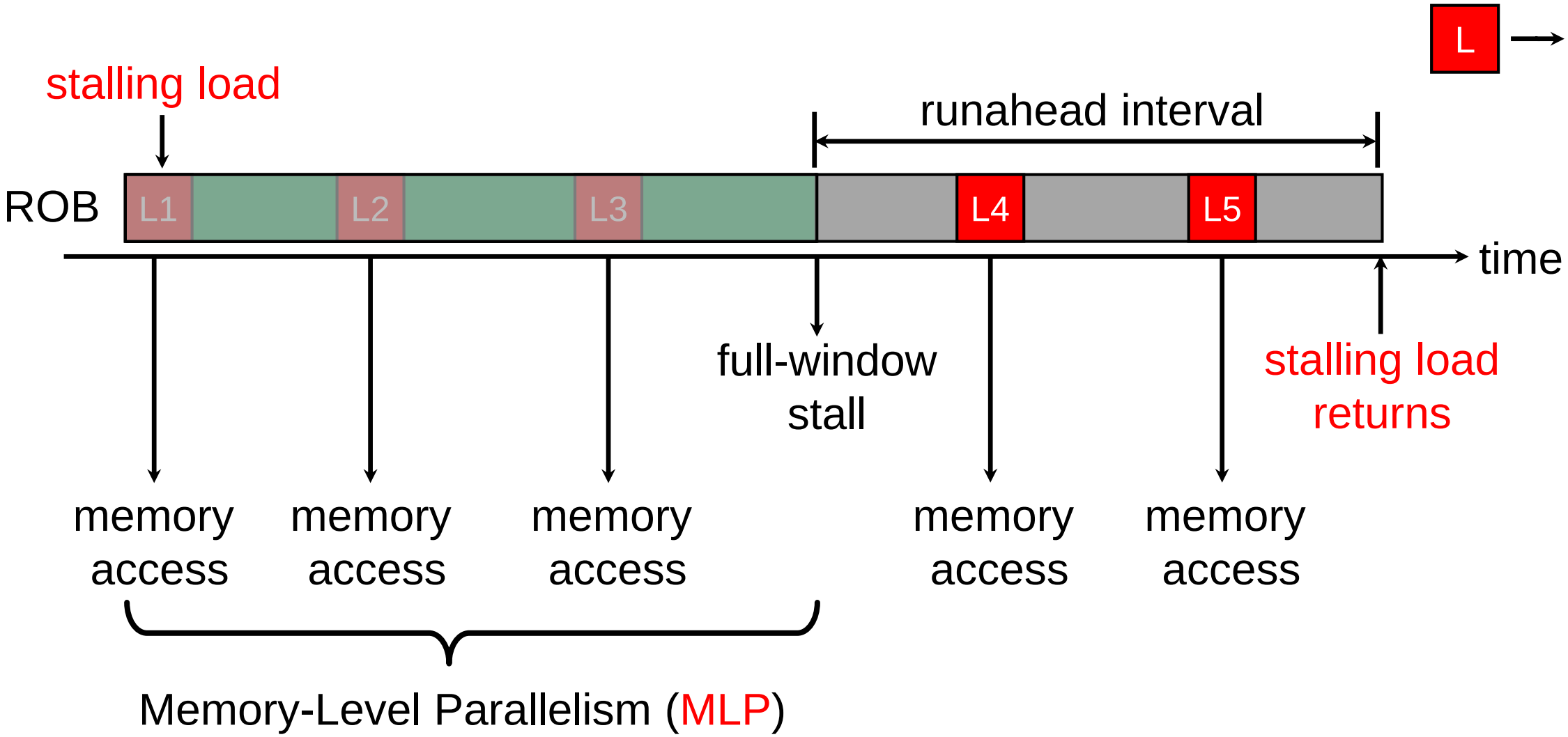

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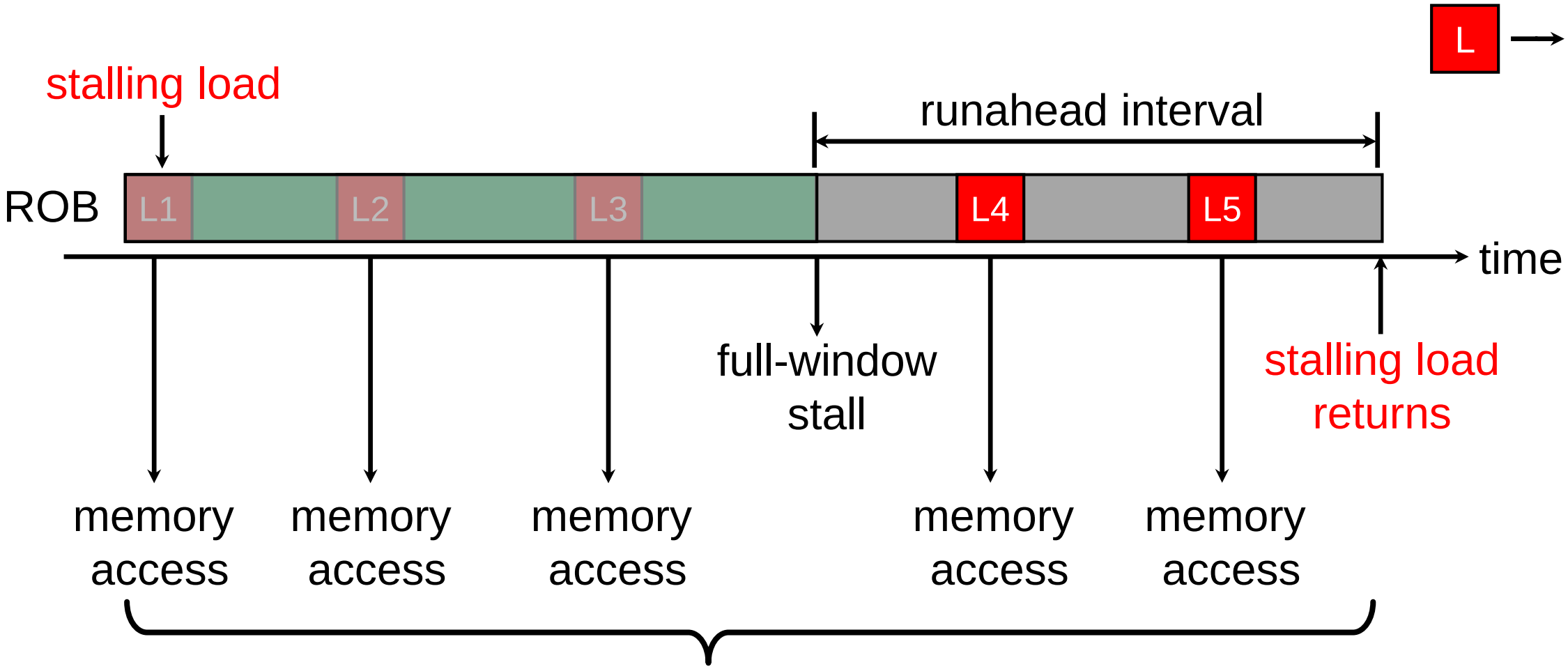

Increased Memory-Level Parallelism (MLP)

Precise Runahead Eliminates Needless Work from Runahead

HPCA 2020

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HPCA 2020

1. Does not flush ROB

2. Executes only useful instructions

3. Runs ahead even for short intervals

Precise Runahead Eliminates Needless Work from Runahead

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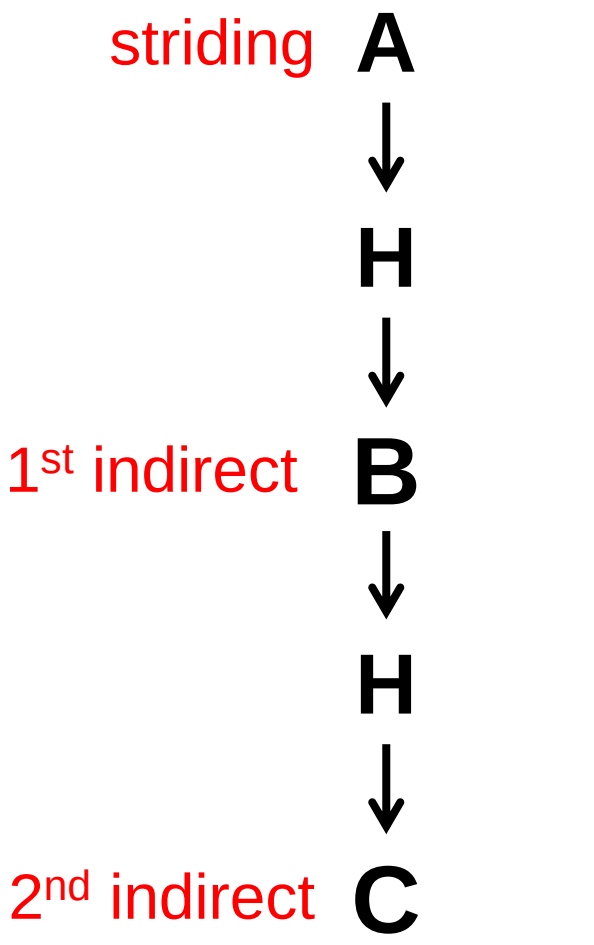
1. Does not flush ROB
2. Executes only useful instructions
3. Runs ahead even for short intervals
4. Efficiently manages microarchitectural resources

Runahead for Indirect Memory Accesses

representative example

```
for(i = 0; i < NUM_KEYS; i++)
  C[hash(B[hash(A[i])])]++;
```



indirect chain

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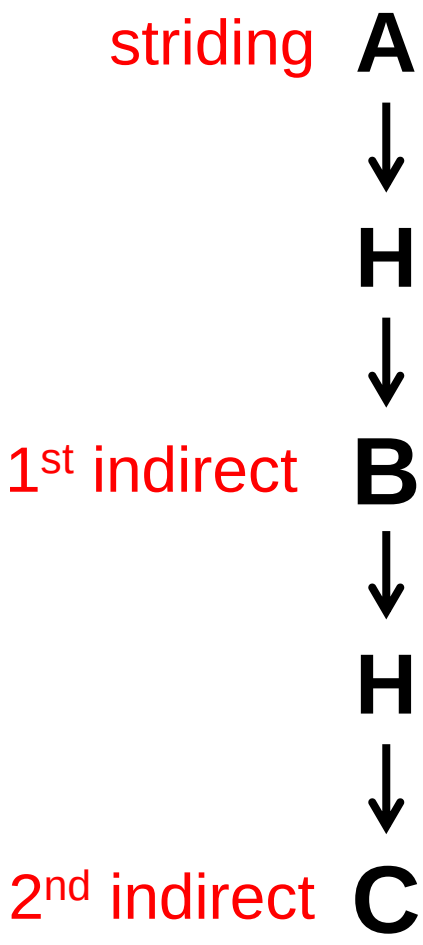


```
for(i = 0; i < NUM_KEYS; i++)
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```
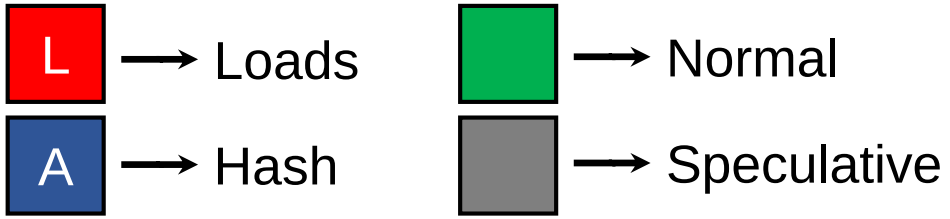

```
unsigned int
hash(unsigned int x) {
  x = ((x >> 16) ^ x) * 0x45d9f3b;
  x = ((x >> 16) ^ x) * 0x45d9f3b;
  x = (x >> 16) ^ x;
return x & (MAX_KEY - 1);
}
```

complex indirect address computation

Runahead for Indirect Memory Accesses

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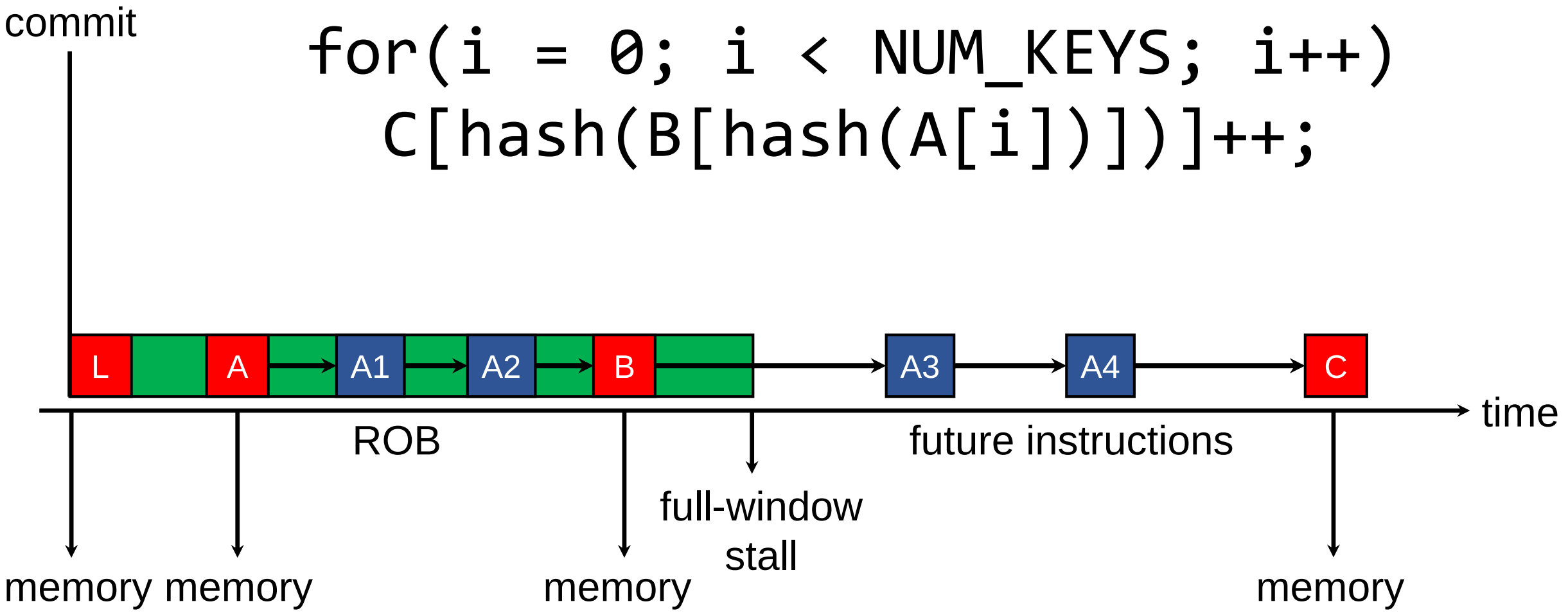

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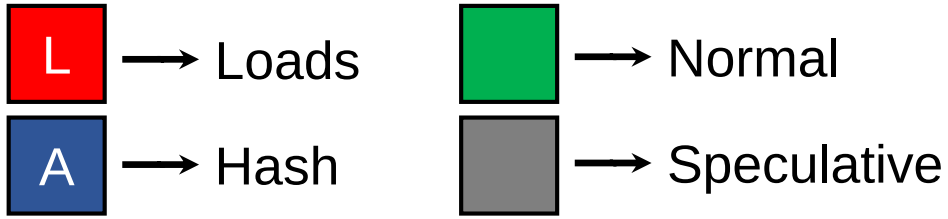

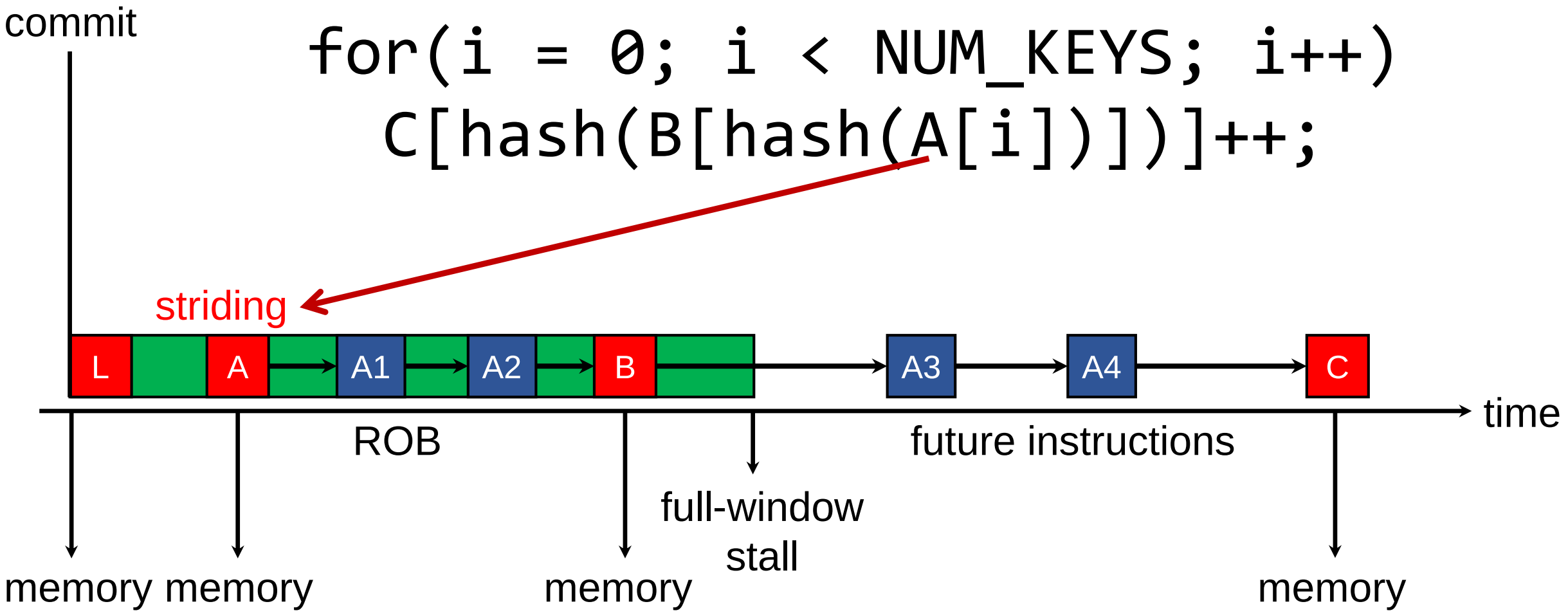

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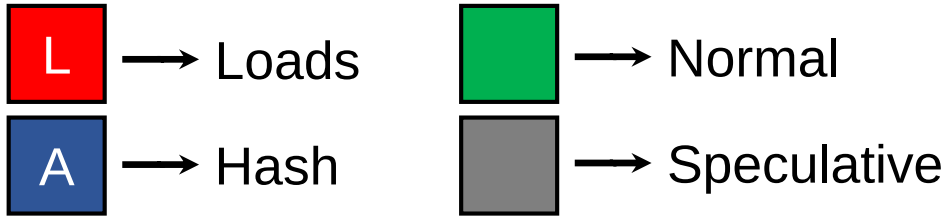

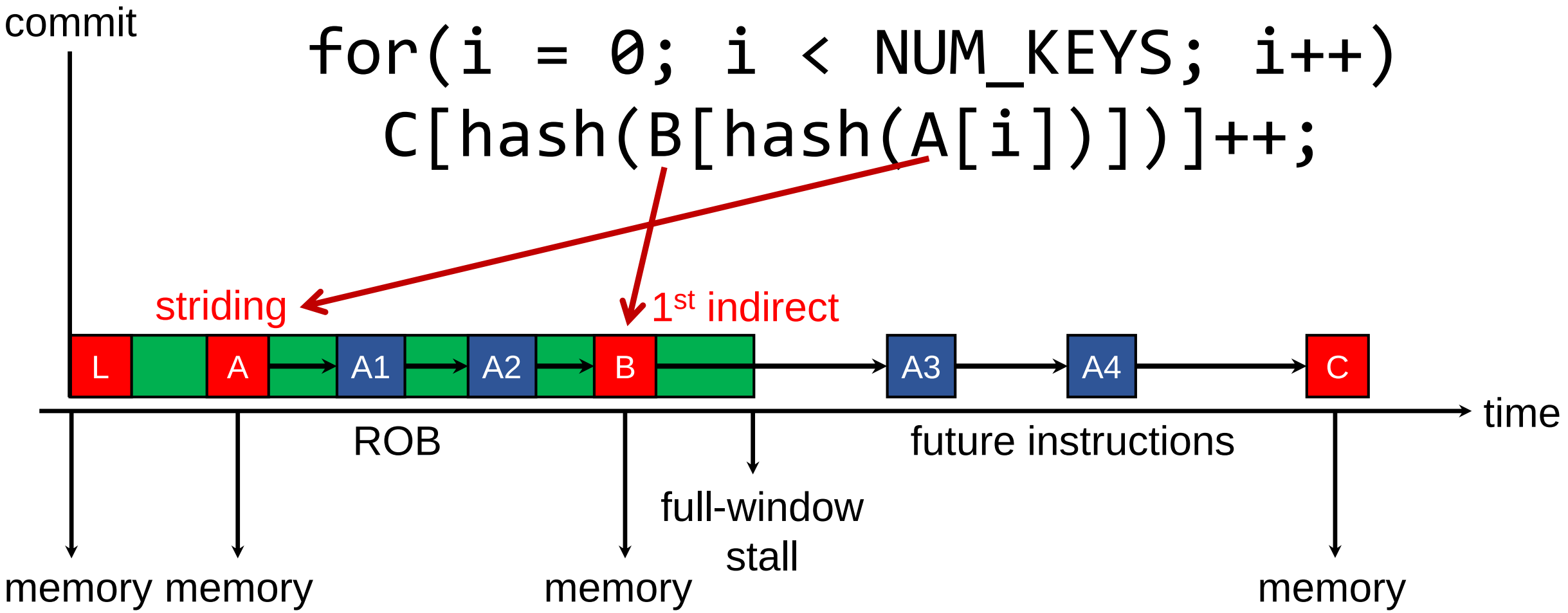

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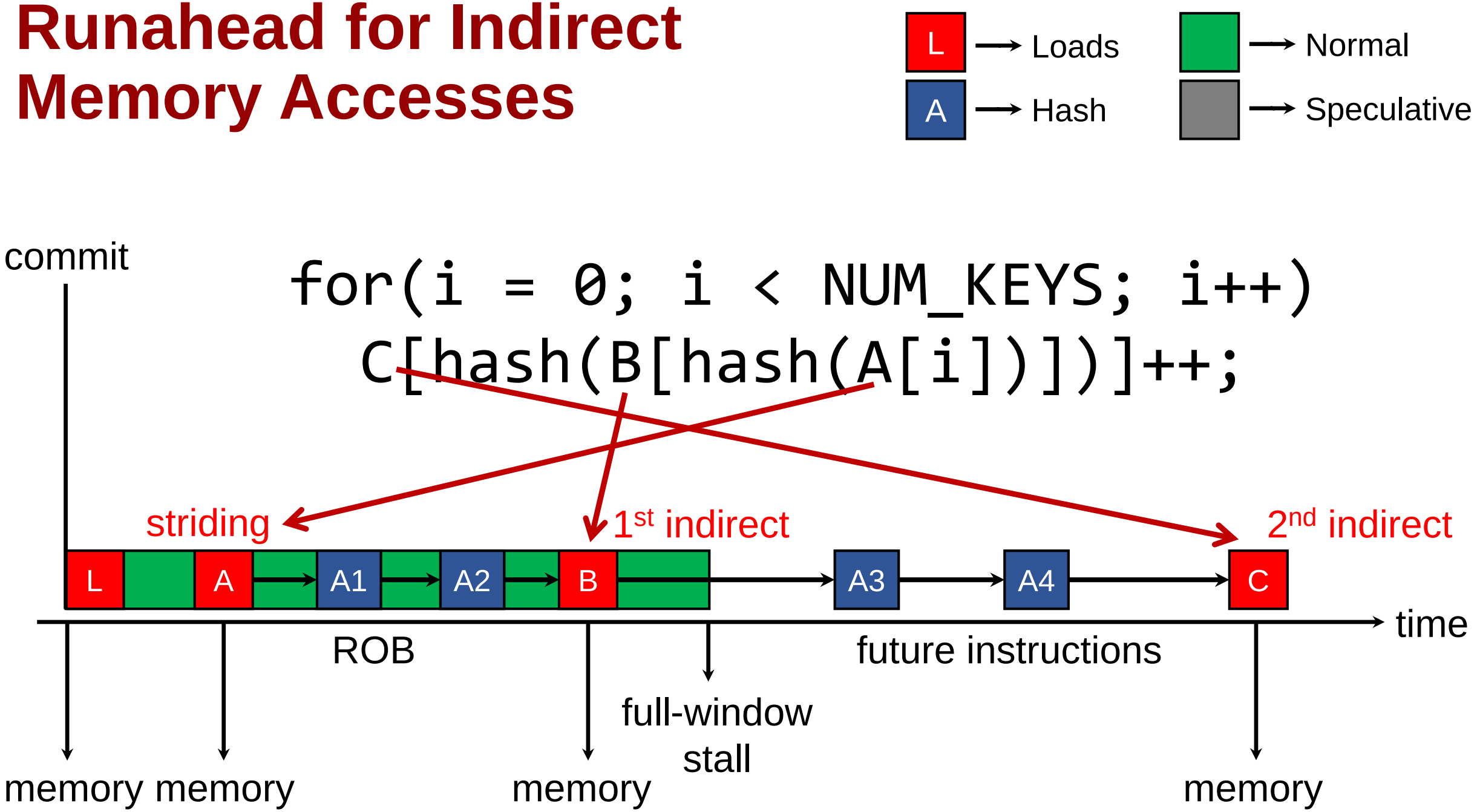

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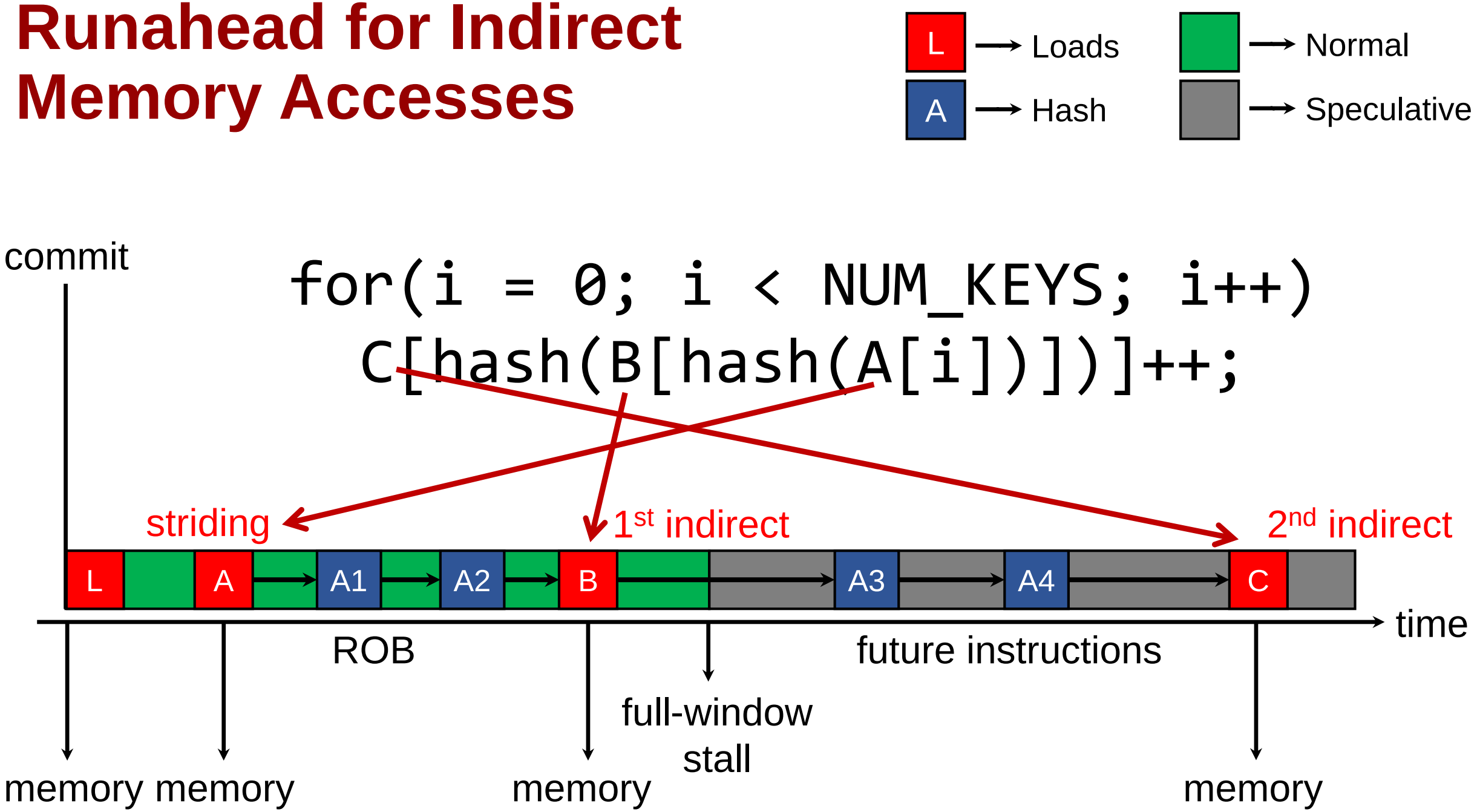

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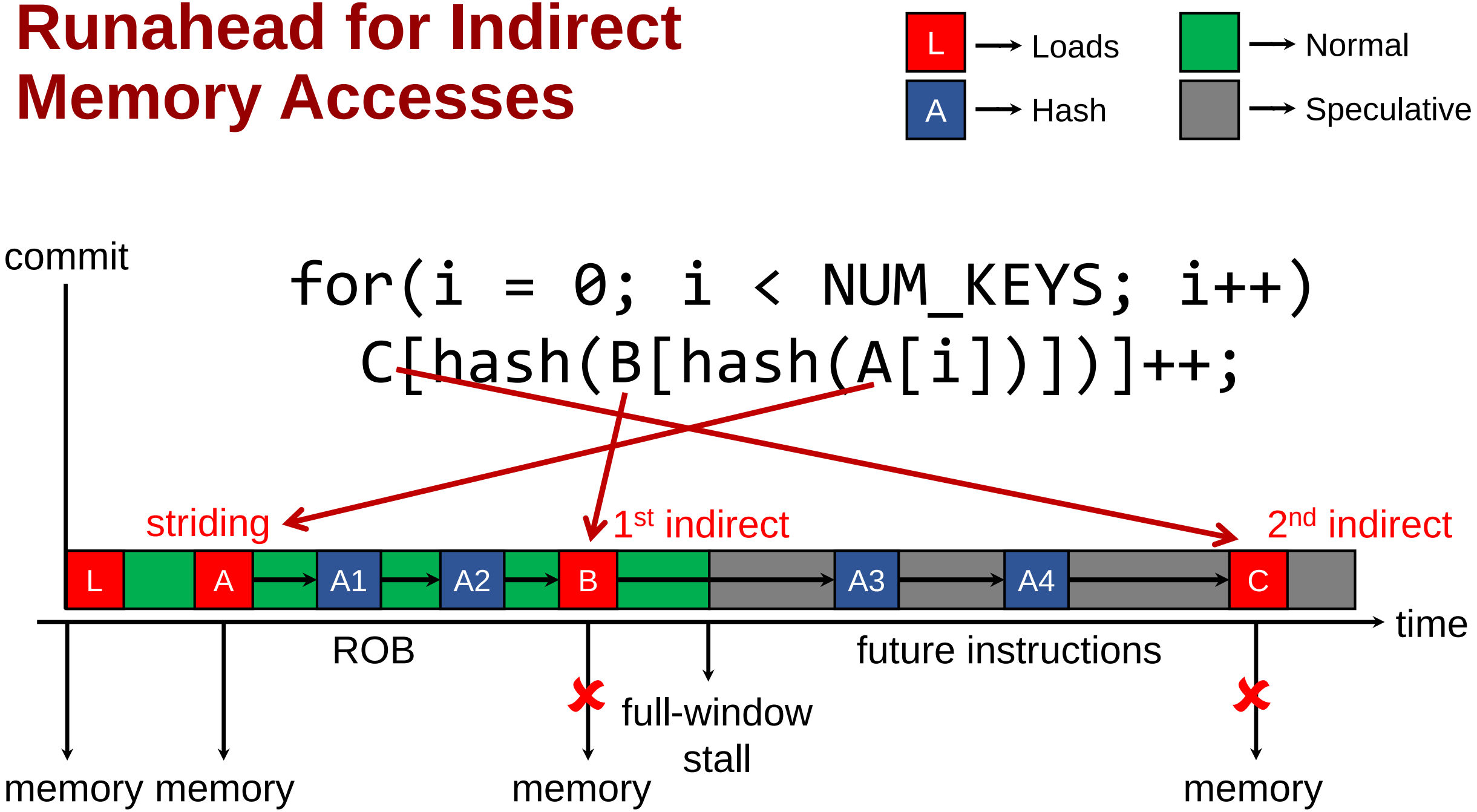

Runahead Cannot Prefetch Indirect Memory Accesses

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1. Core cannot issue indirect loads

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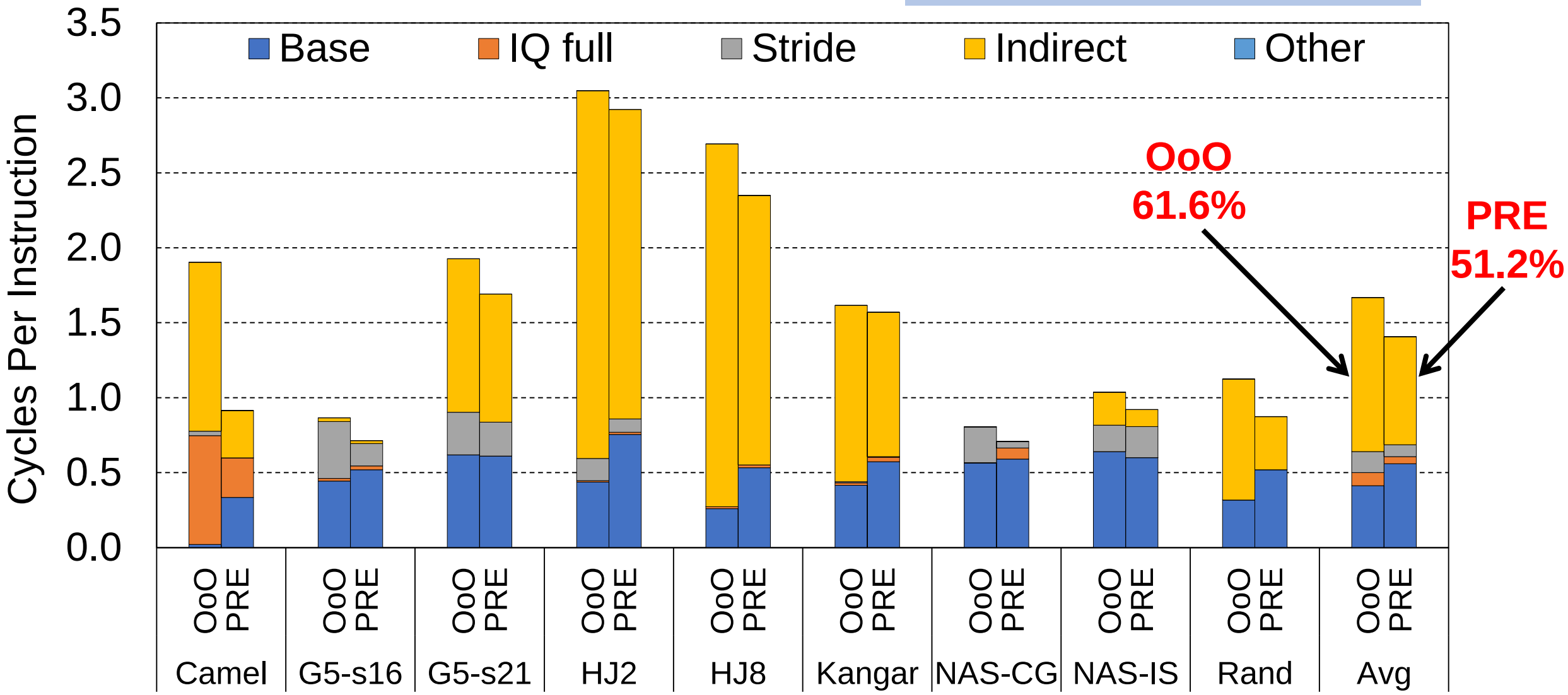
2. Limited by the front-end bandwidth

A New Microarchitectural Technique is Required

with stride prefetcher



Vector Runahead for Indirect Memory Accesses

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1. Accesses to array A are striding

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i = 1	**A[1] → H_2 → B[H_2] → H_3 → C[H_3]**

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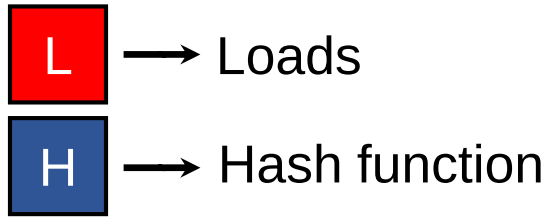
i = 1	A[1] → H_2 → B[H_2] → H_3 → C[H_3]
i = 2	A[2] → H_4 → B[H_4] → H_5 → C[H_5]

Generating Future Indirect Memory Addresses



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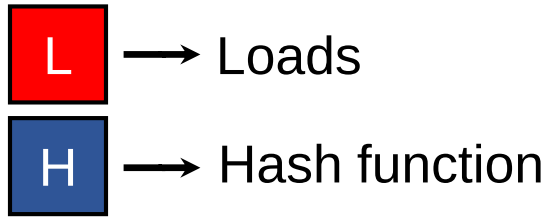

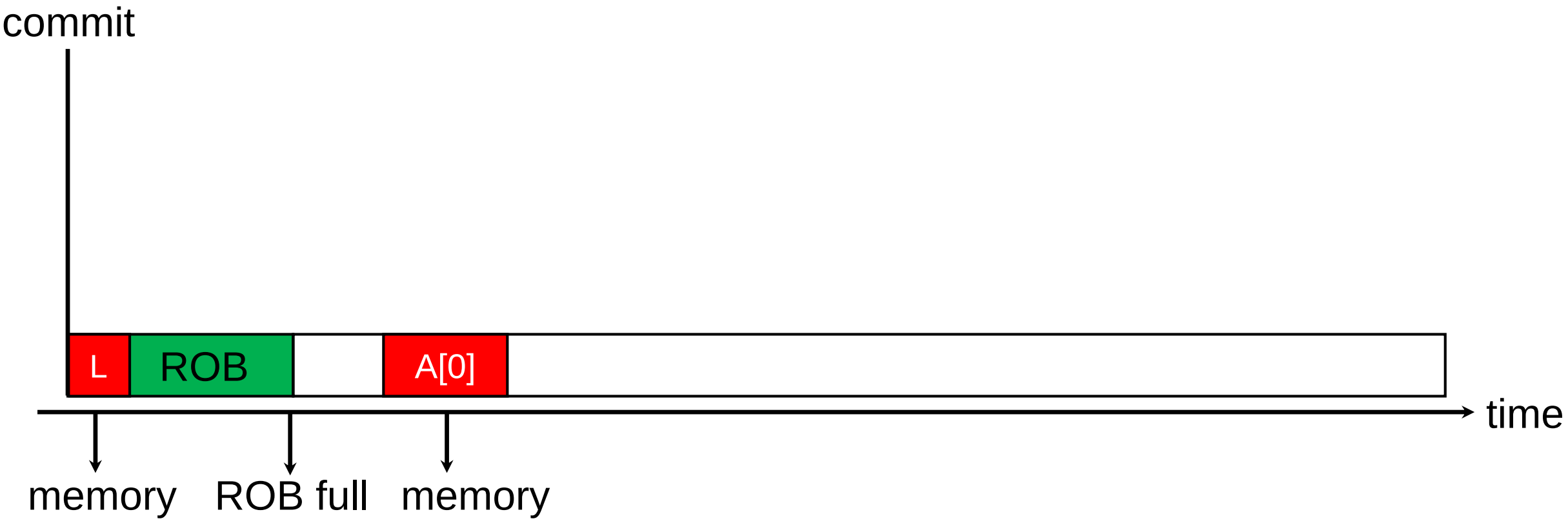

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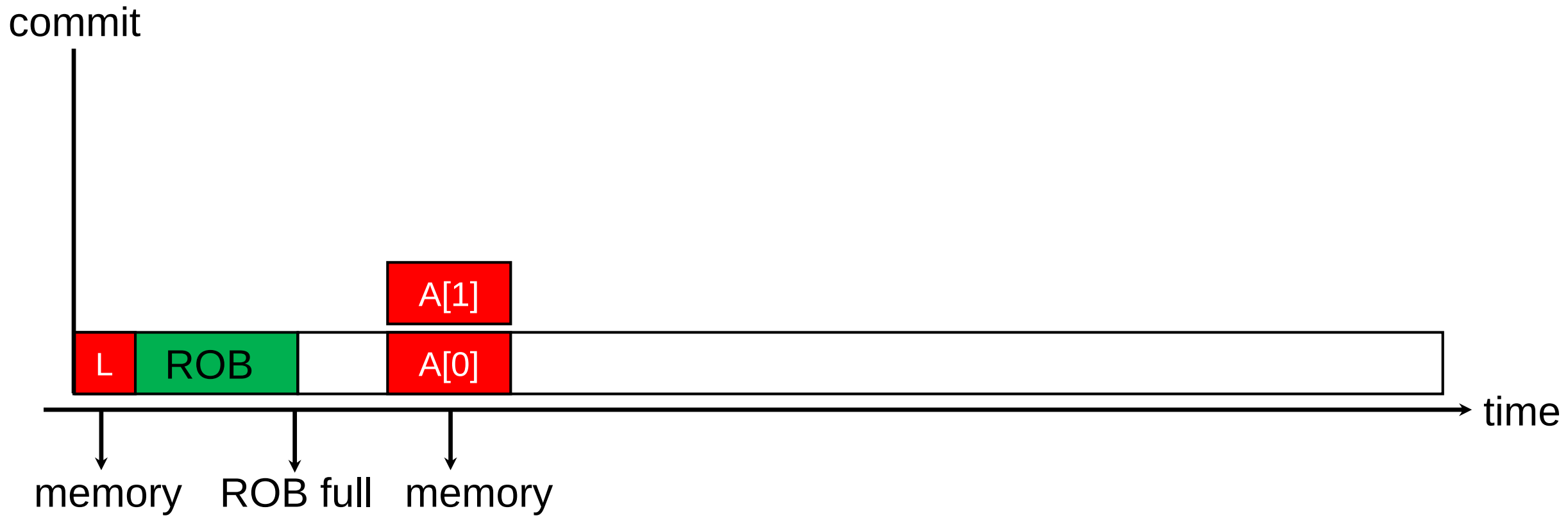

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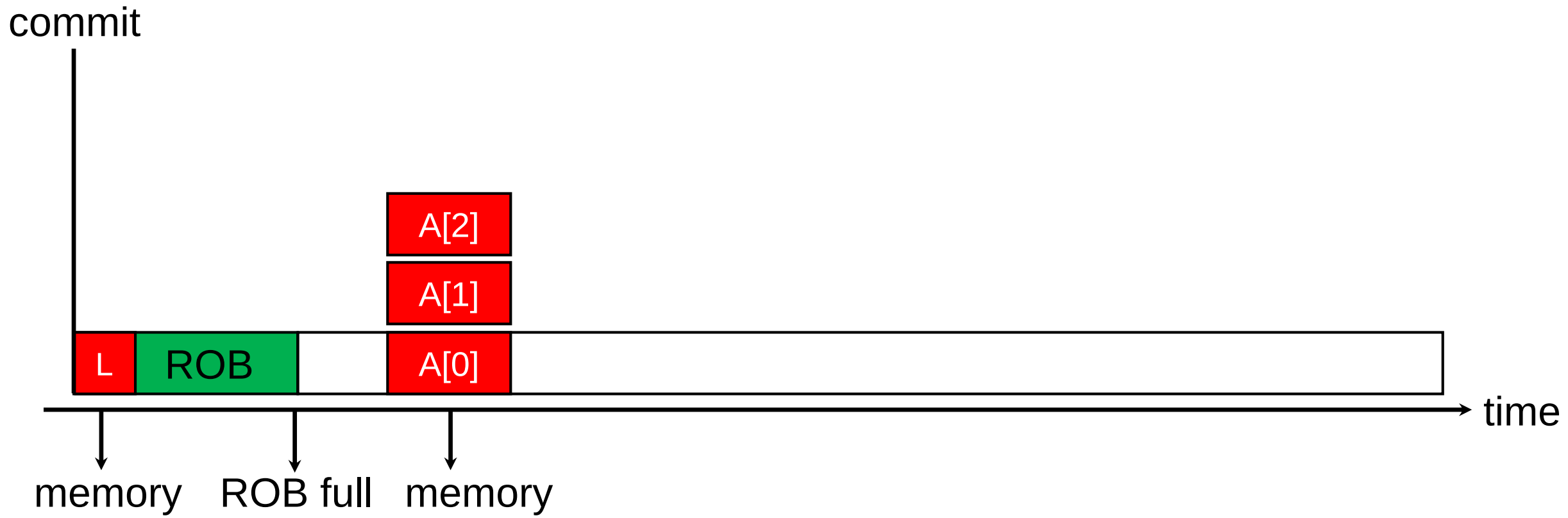

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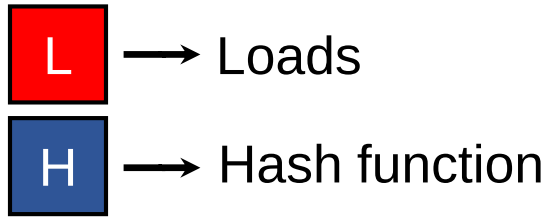

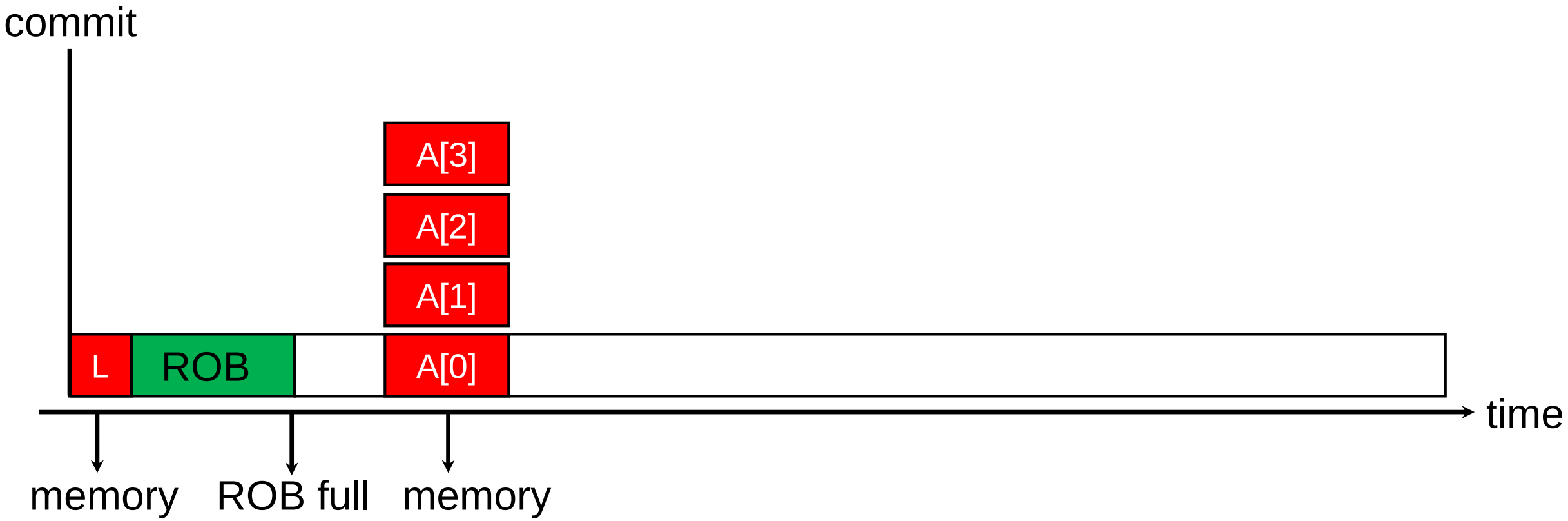

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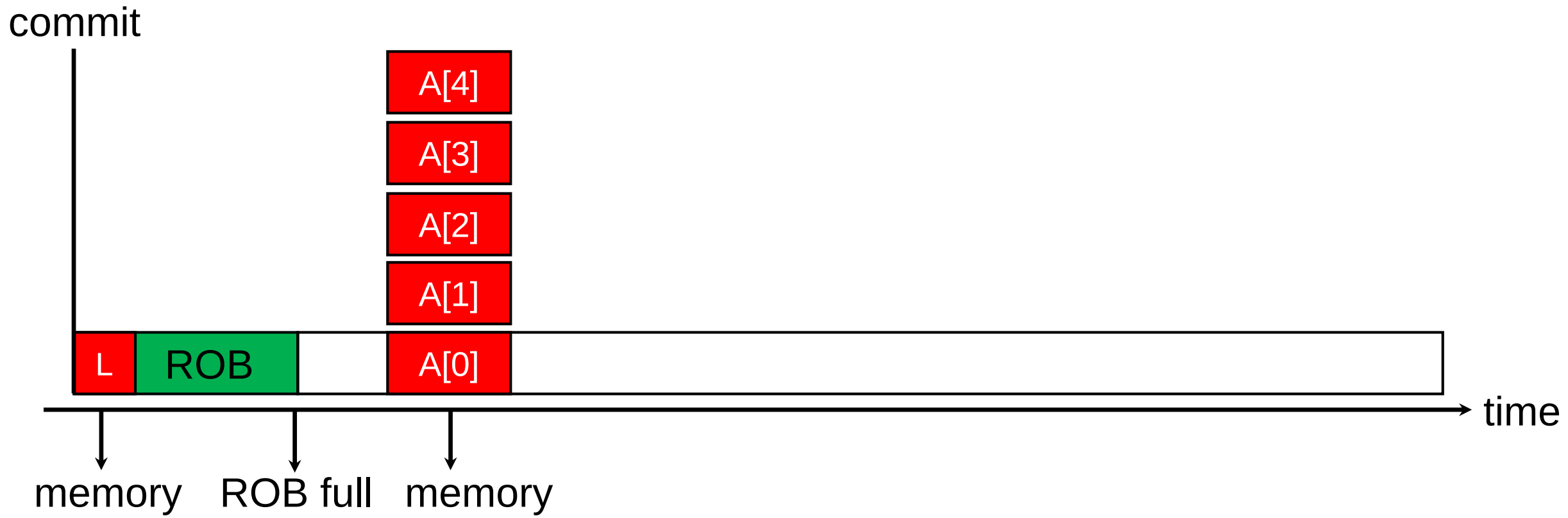

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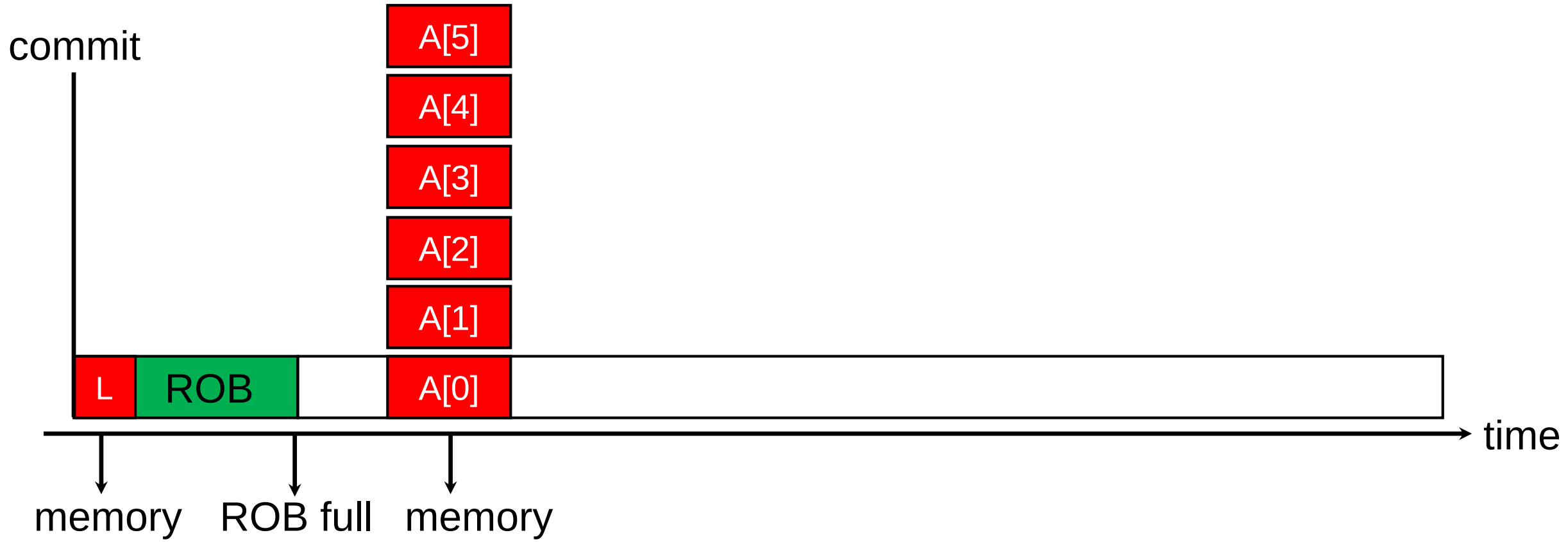

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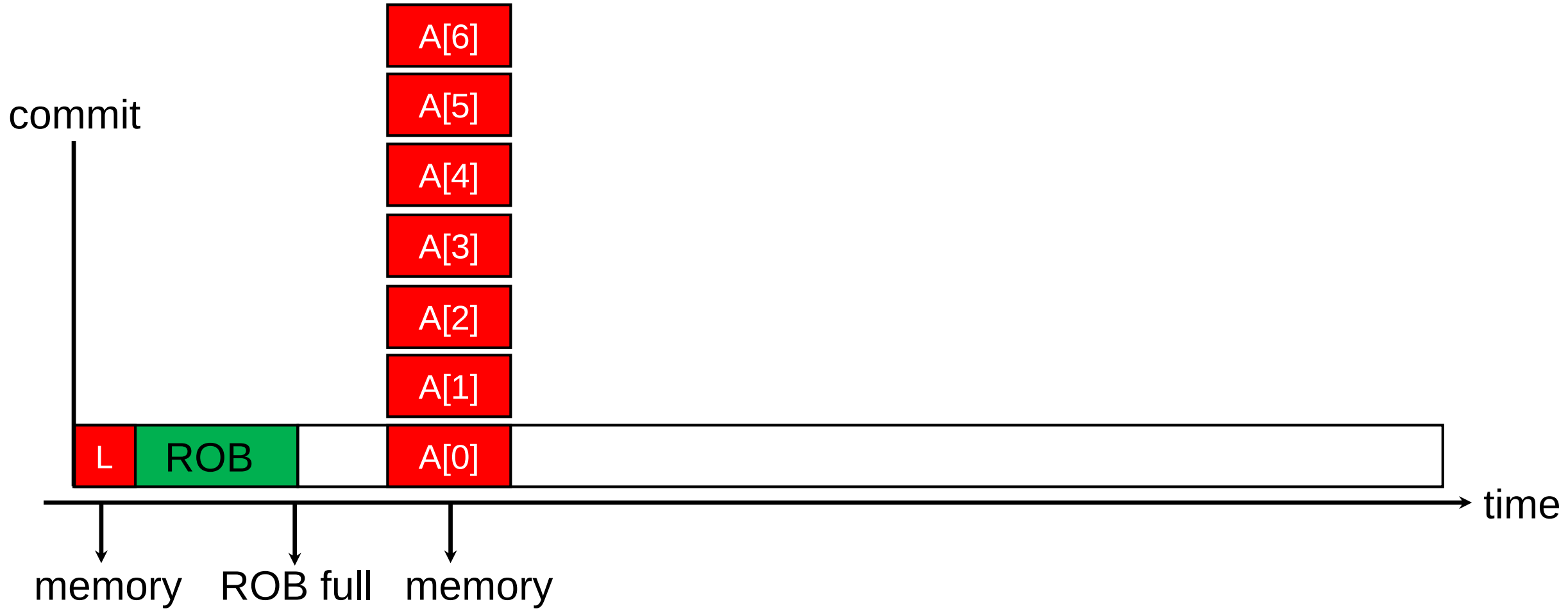

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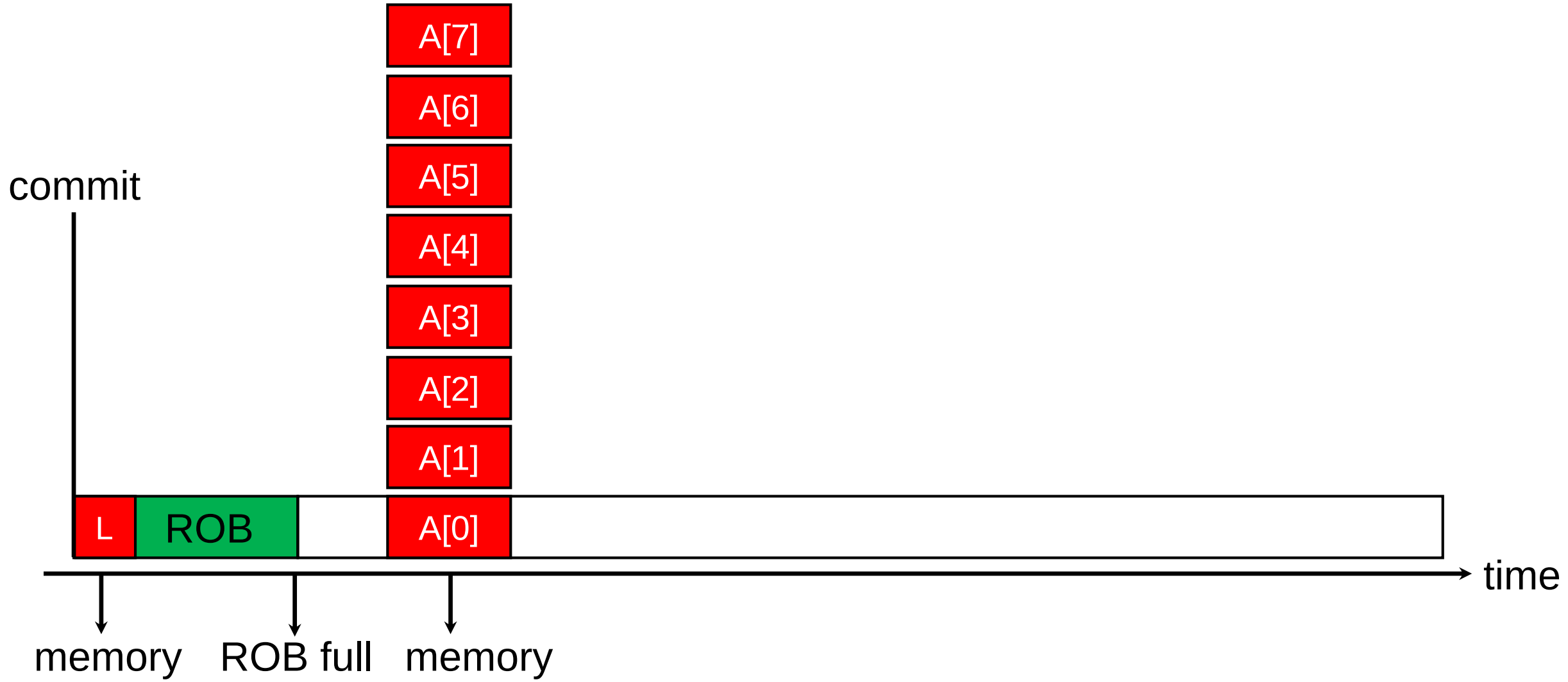

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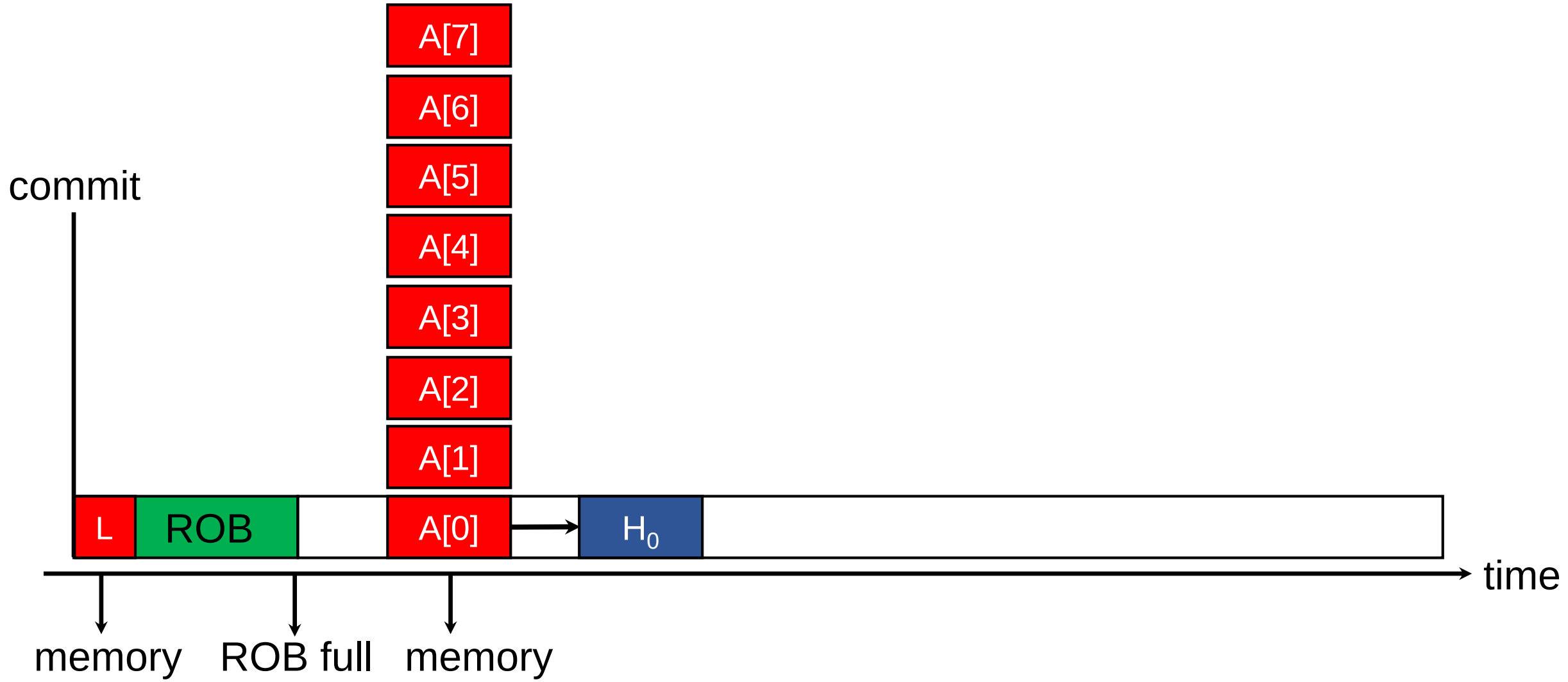
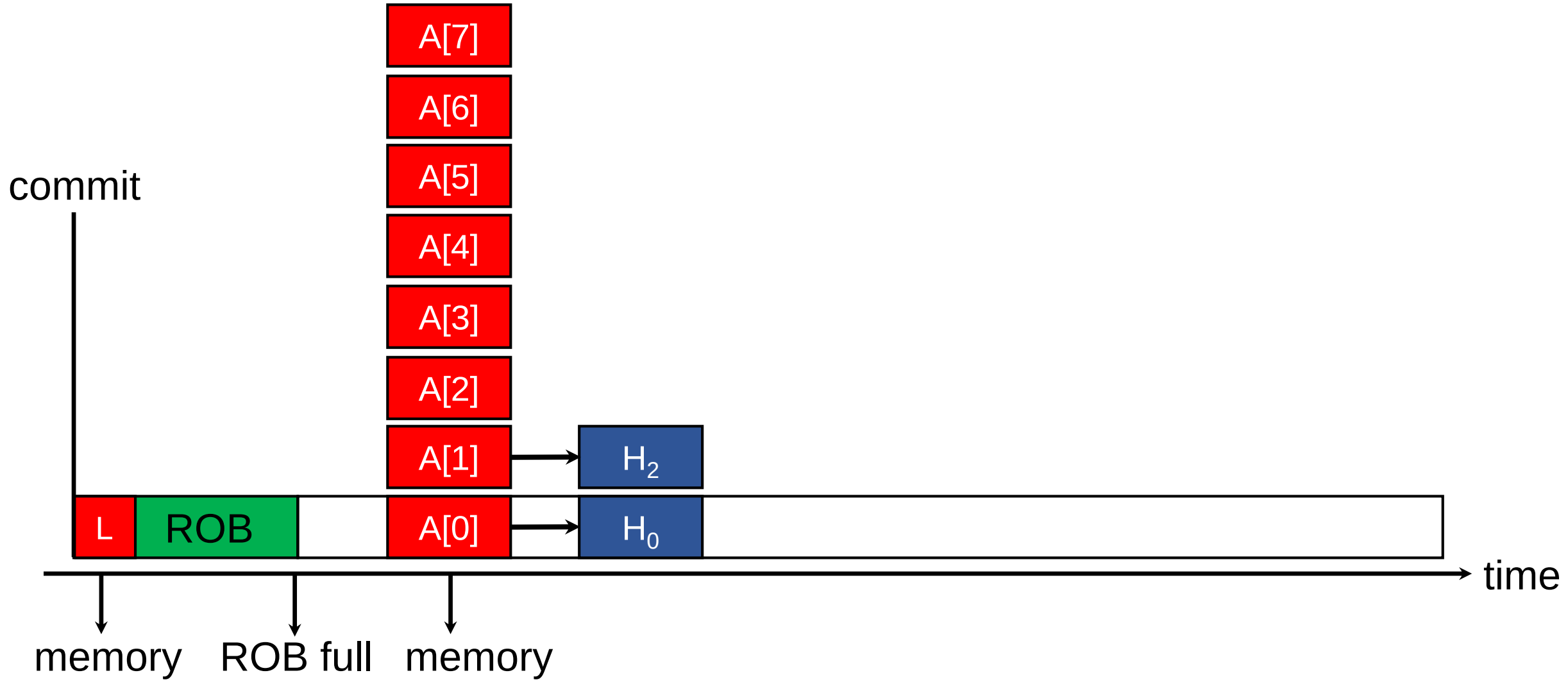
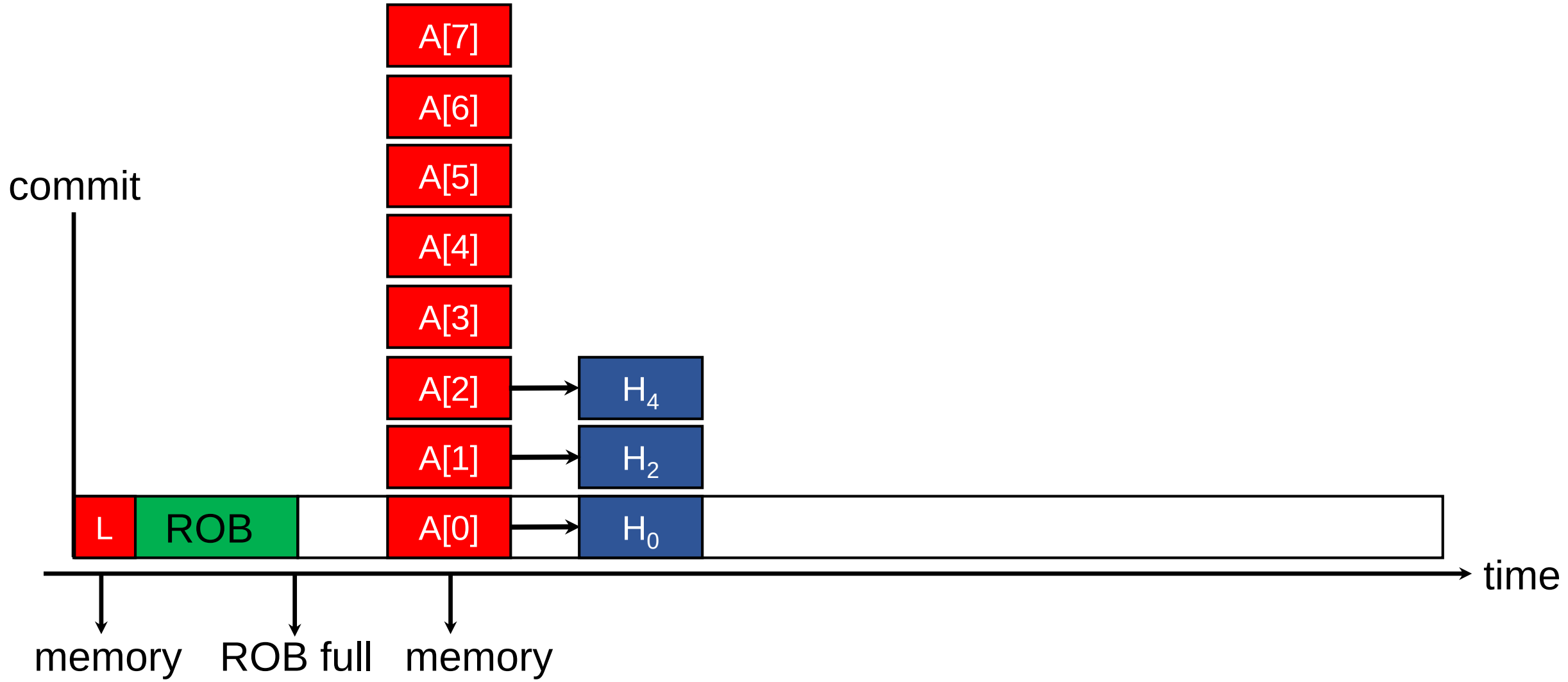


Generating Future Indirect Memory Addresses



Generating Future Indirect Memory Addresses



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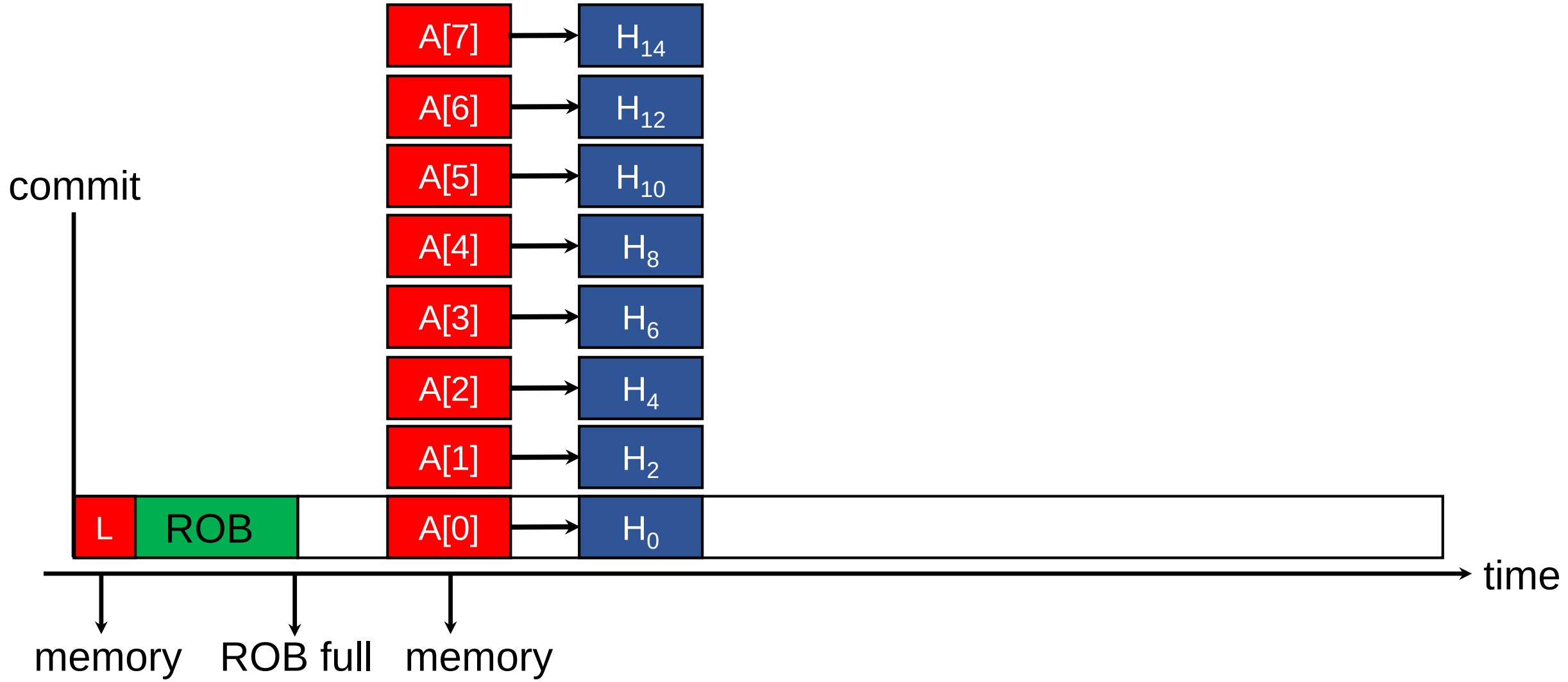

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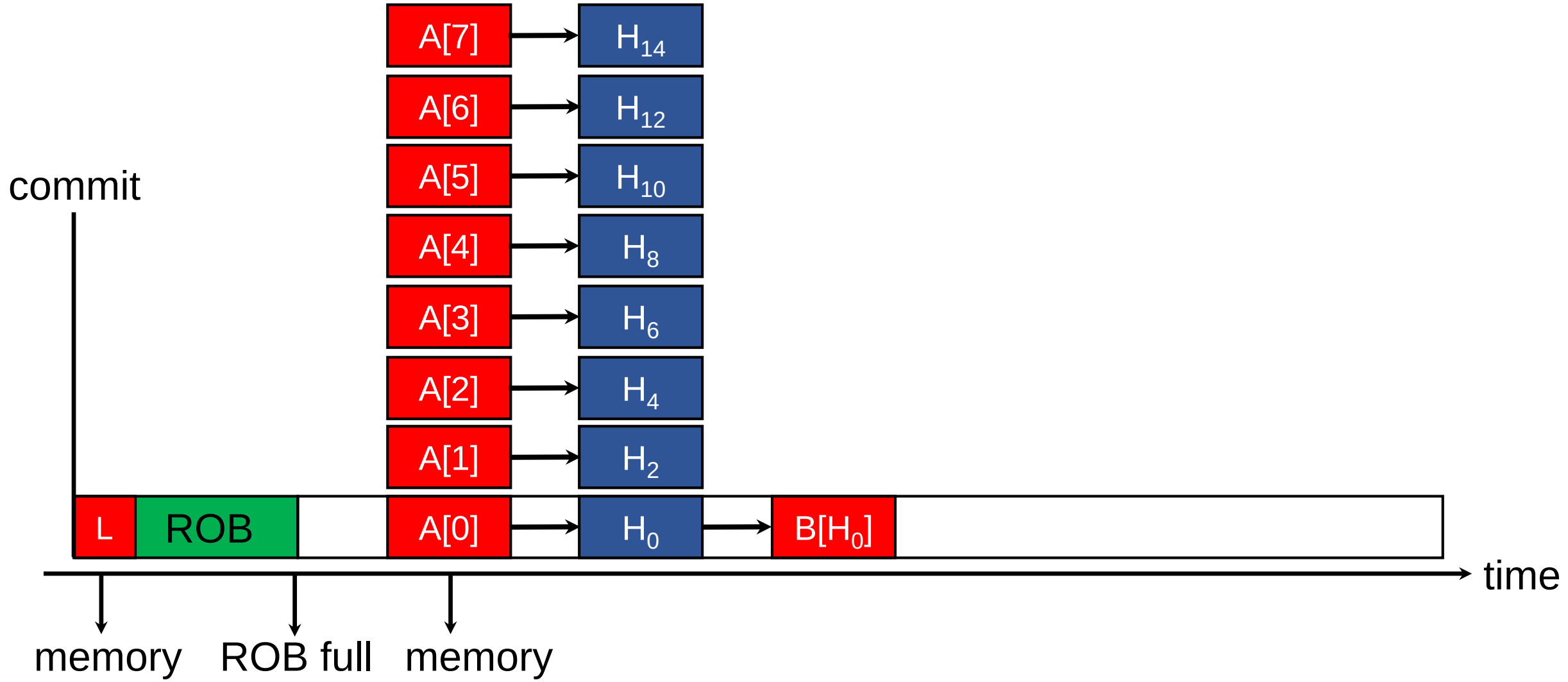

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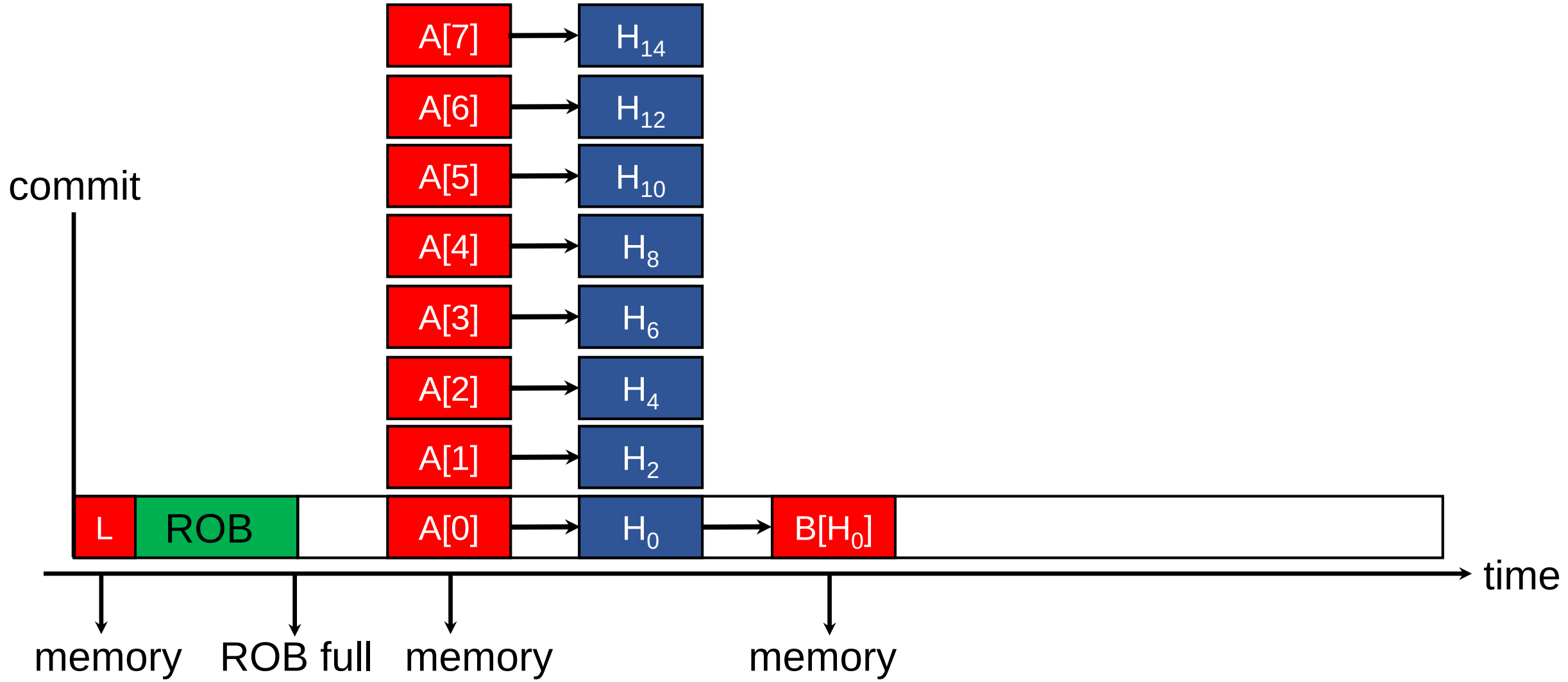

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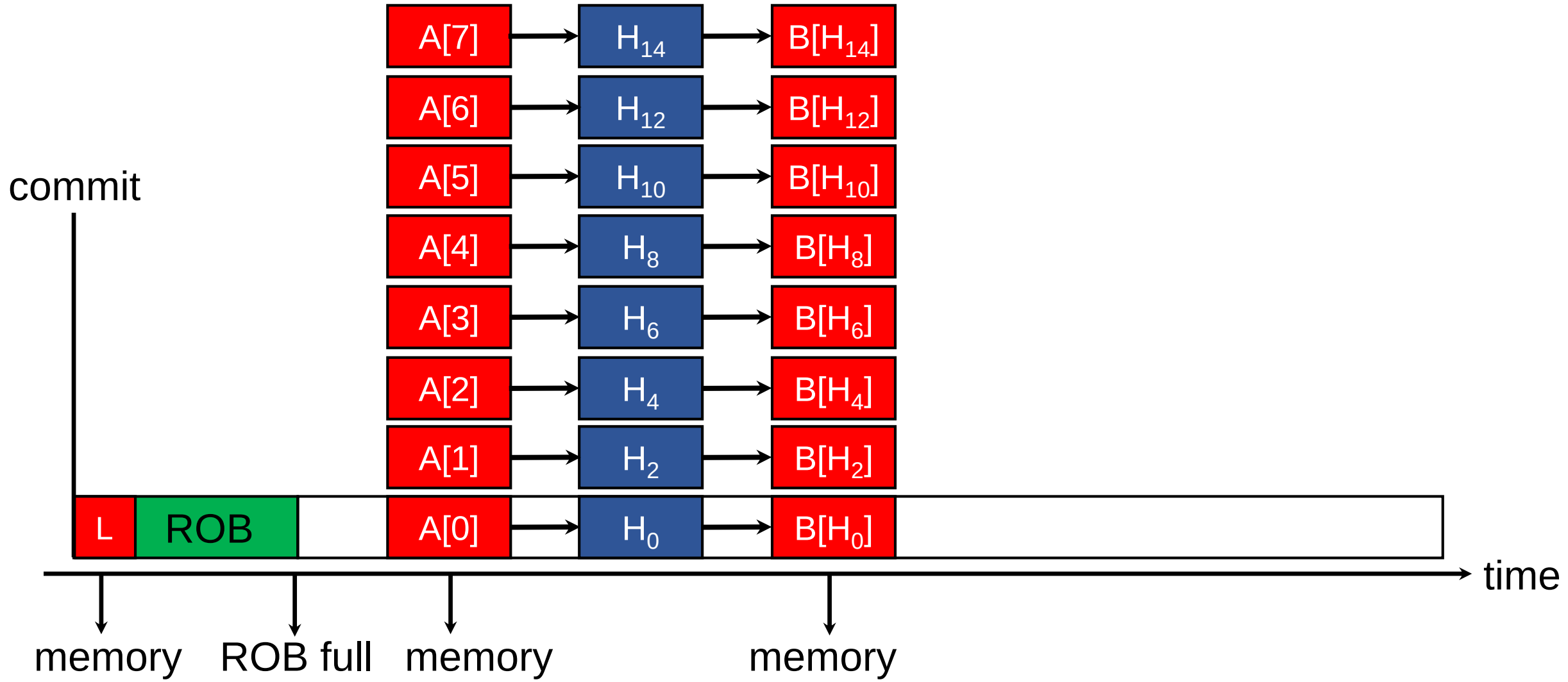

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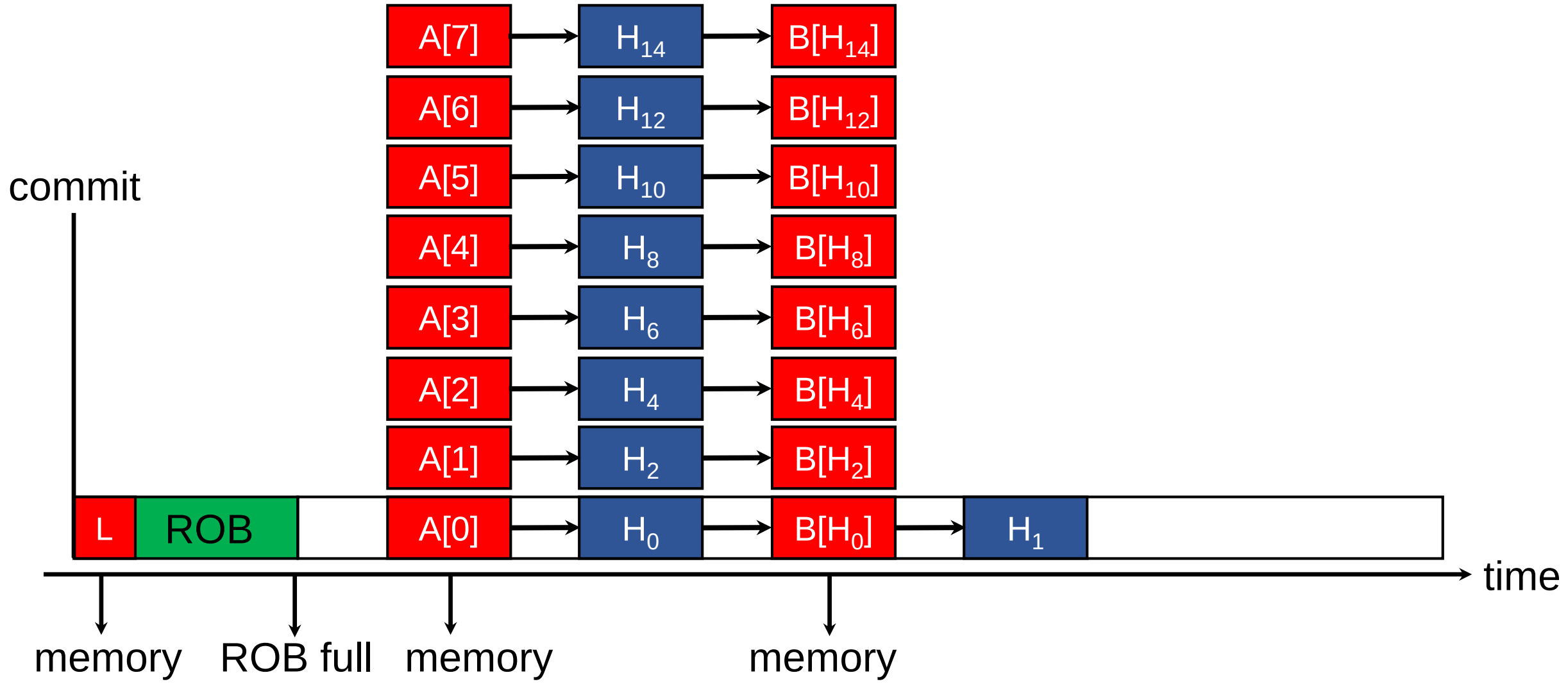

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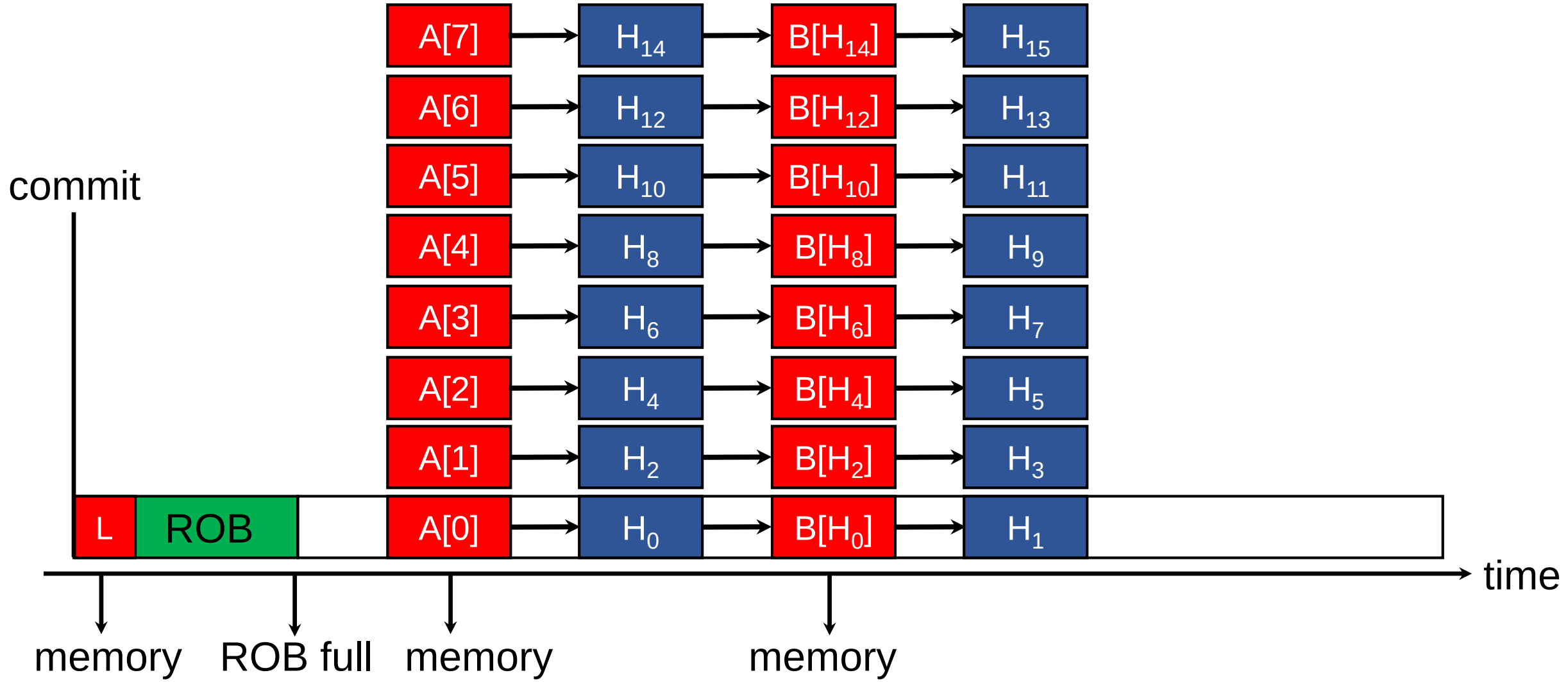
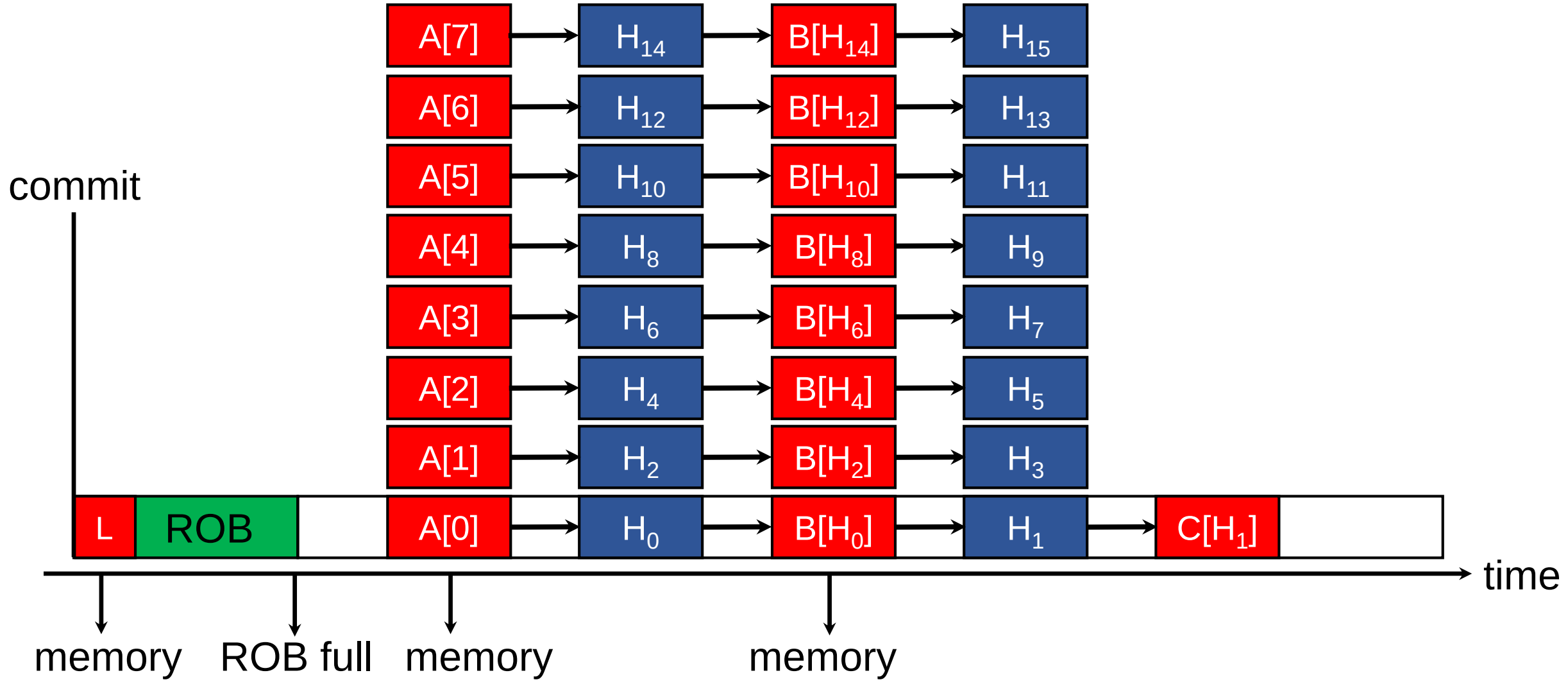
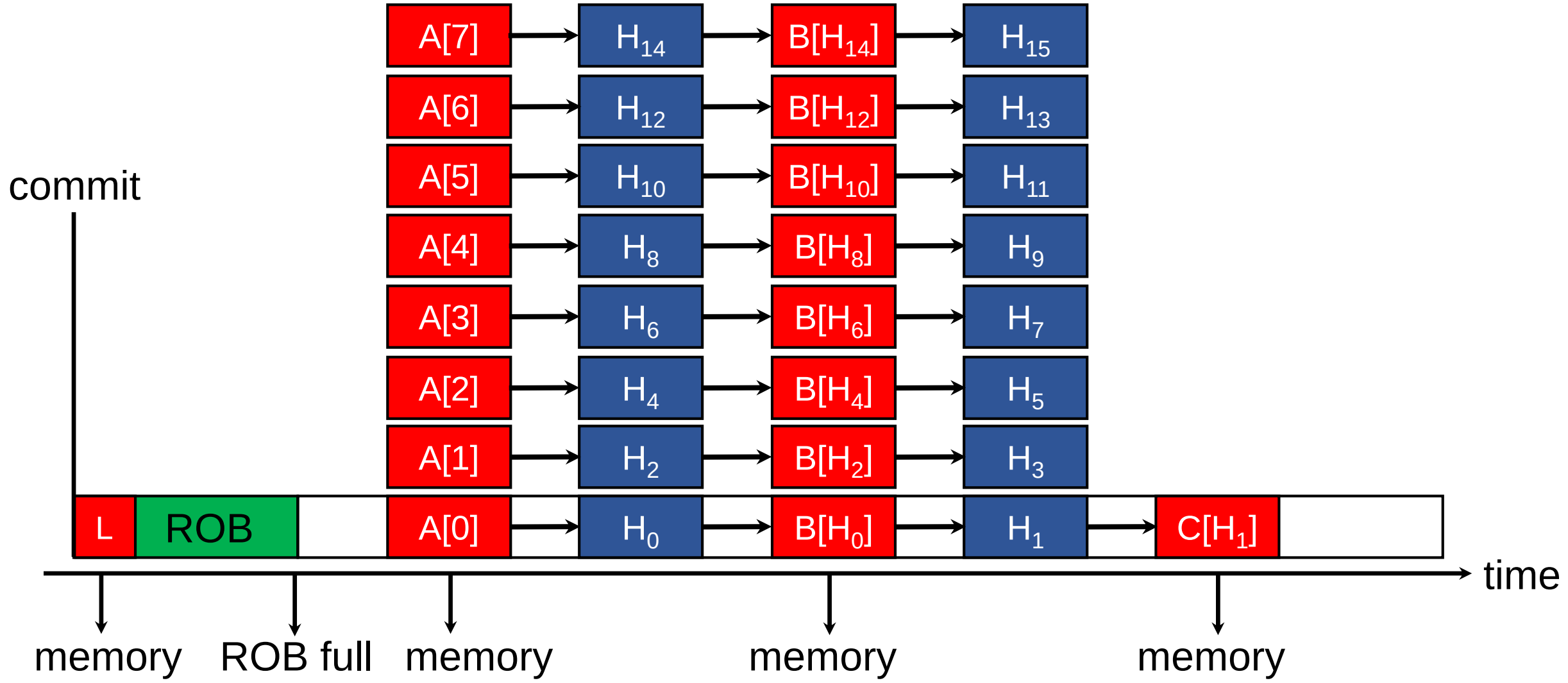


Generating Future Indirect Memory Addresses



Generating Future Indirect Memory Addresses



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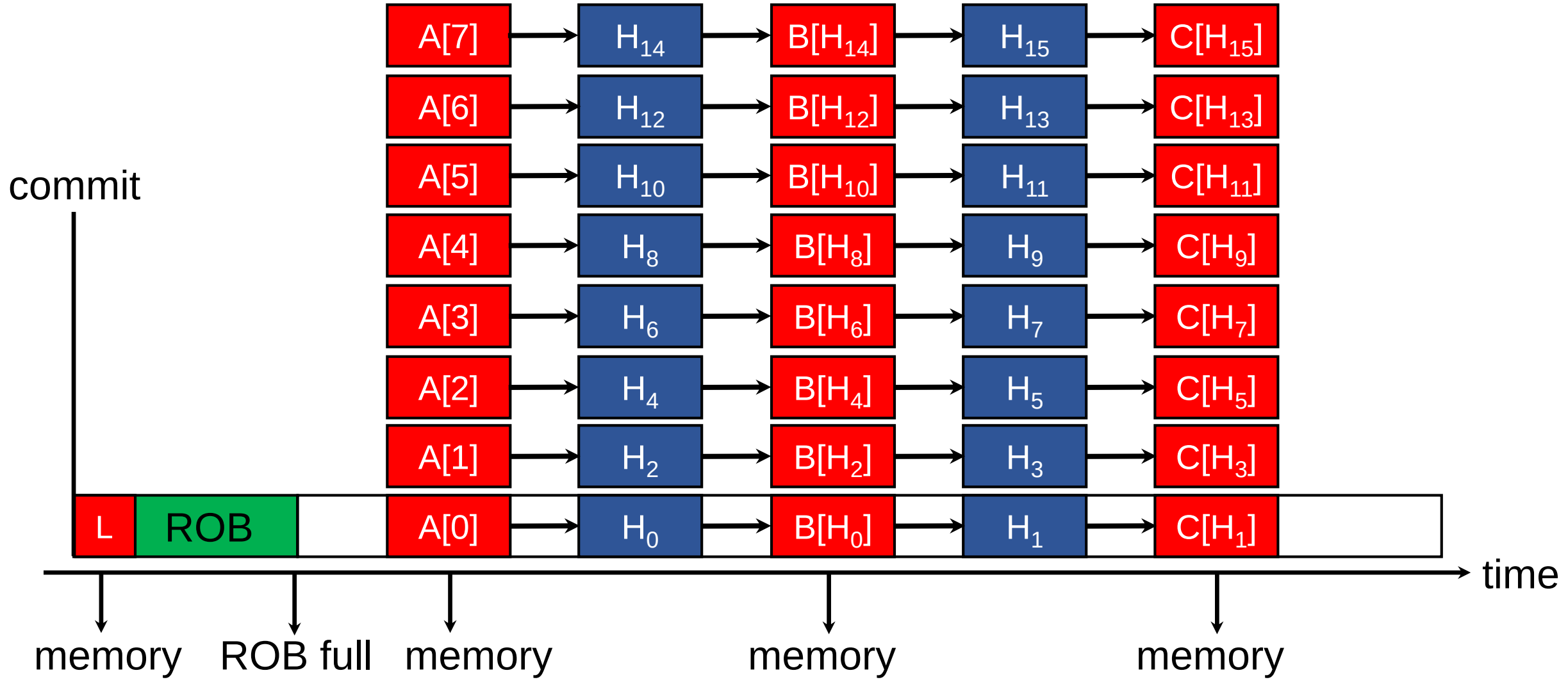

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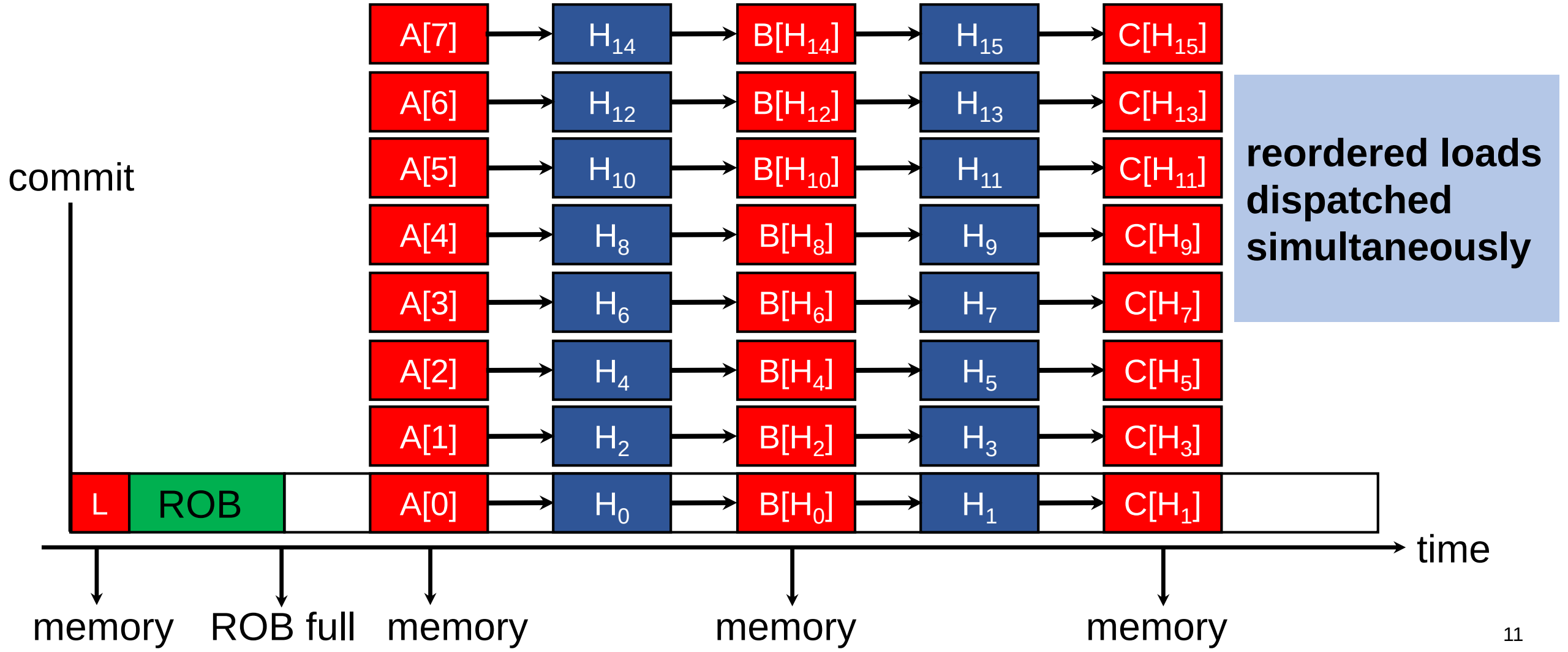
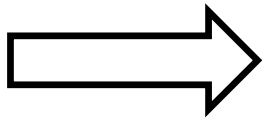


Vectorization for Increasing Back-End Throughput

1. Back-end stalls due to large number of scalar instructions



issue queue
functional units
register file

Vectorization for Increasing Back-End Throughput

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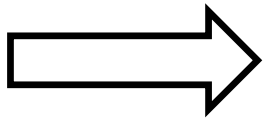

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2. Speculatively vectorize indirect chains
   - Back-end stalls reduce by **~8x**
   - Use vector (physical) register file instead

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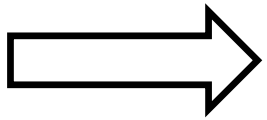

issue queue
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2. Speculatively vectorize indirect chains
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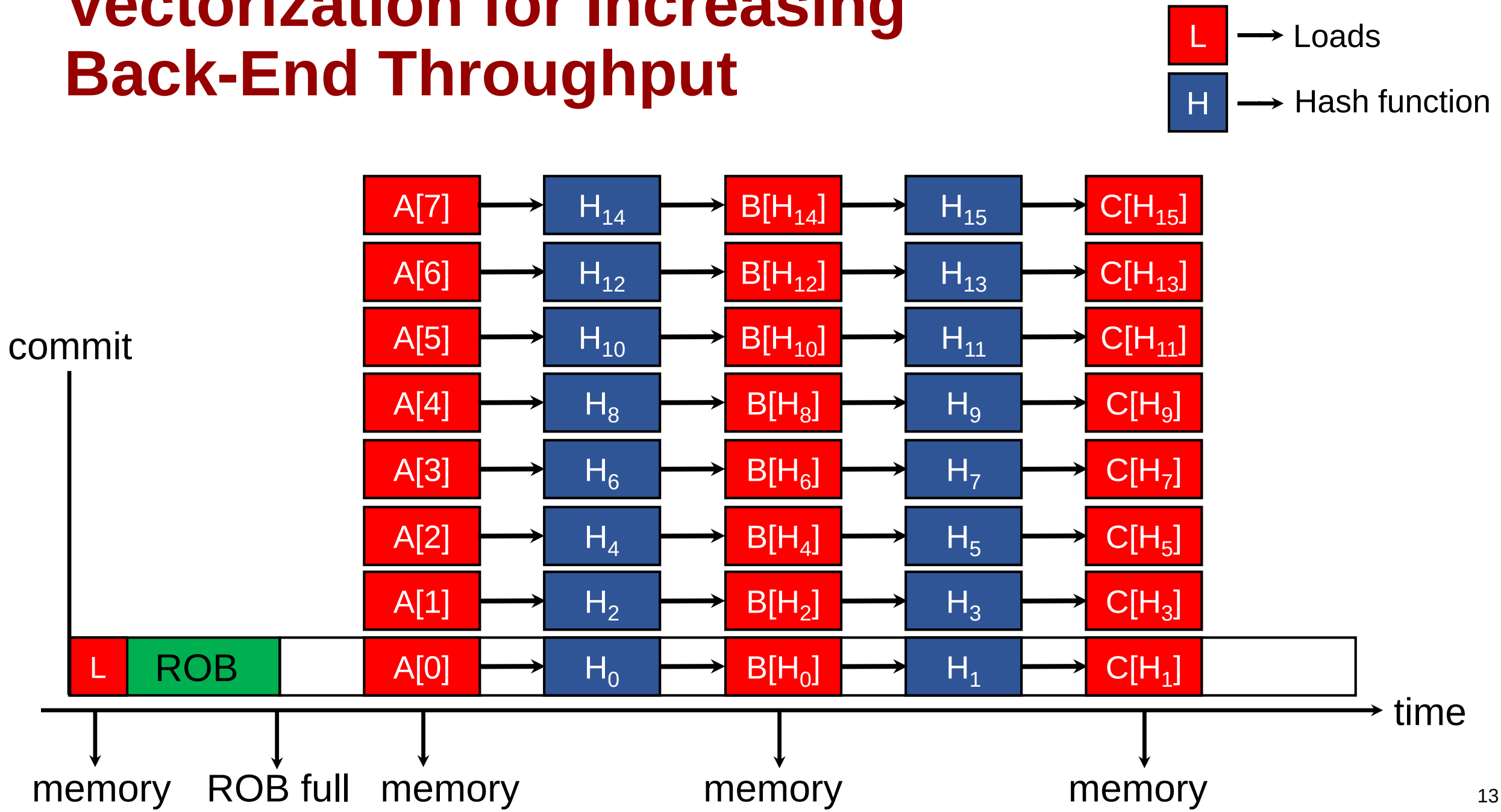
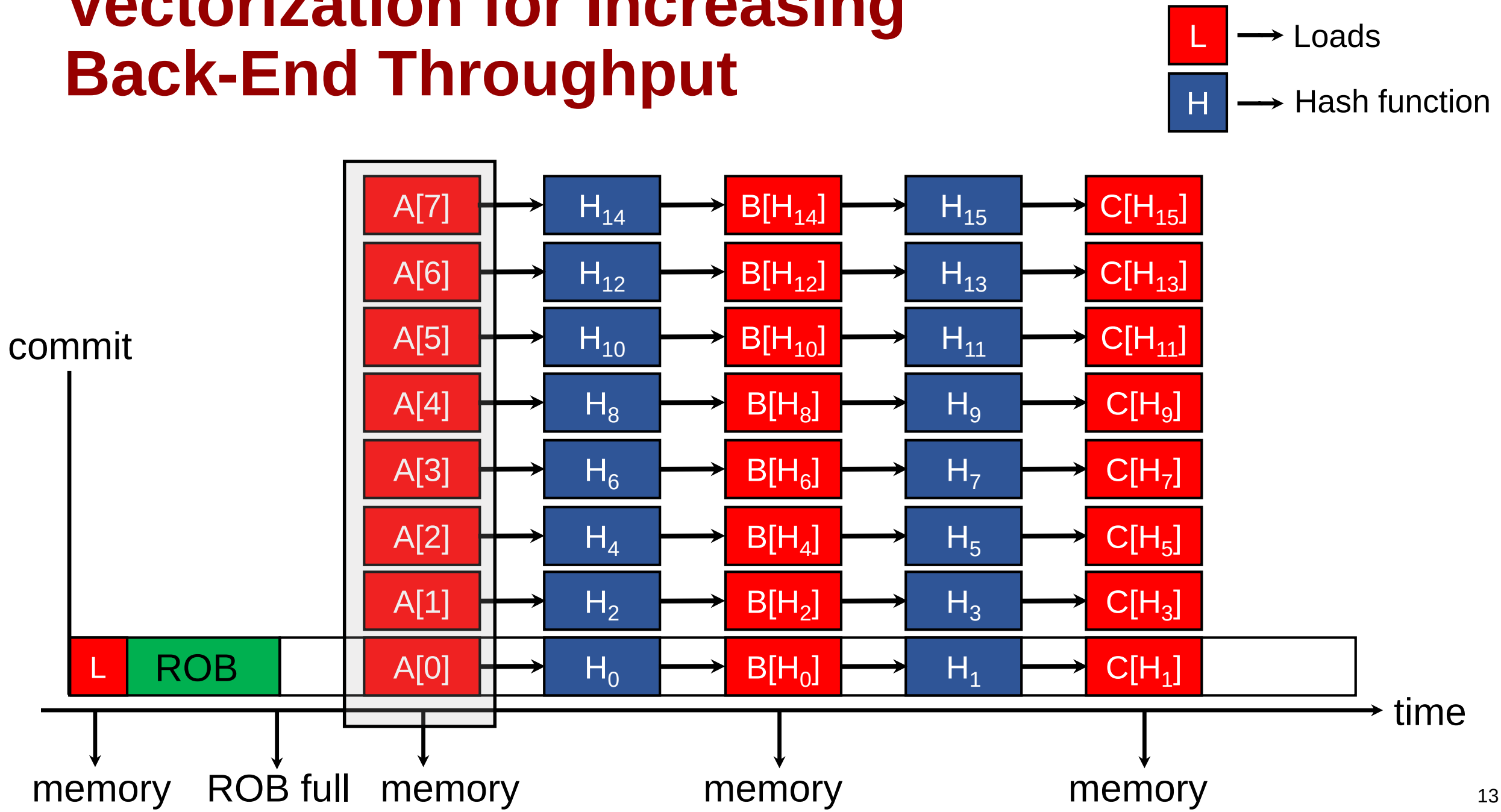
   - Use vector (physical) register file instead

3. Workloads do not have to be vectorizable

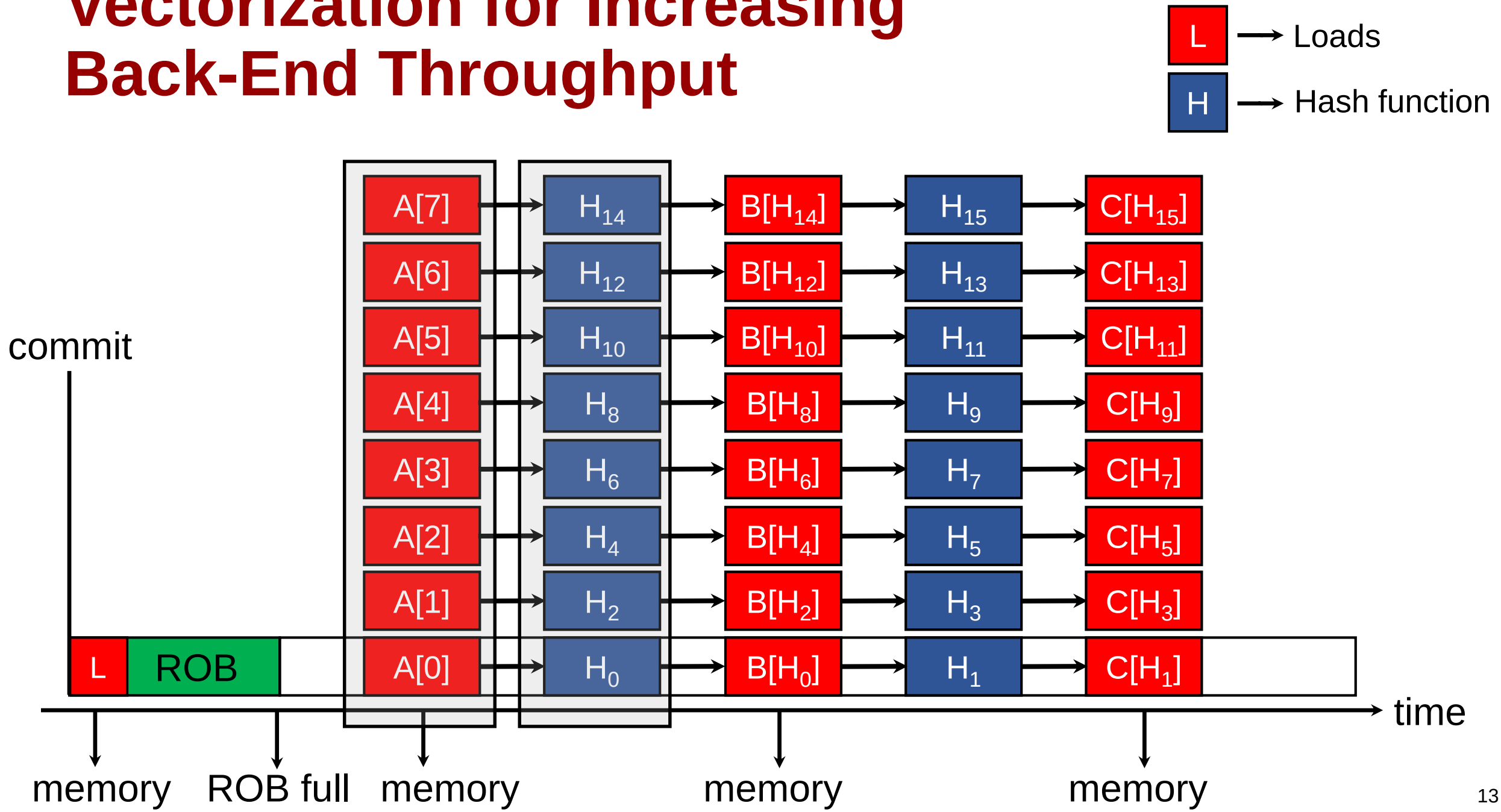
Vectorization for Increasing Back-End Throughput



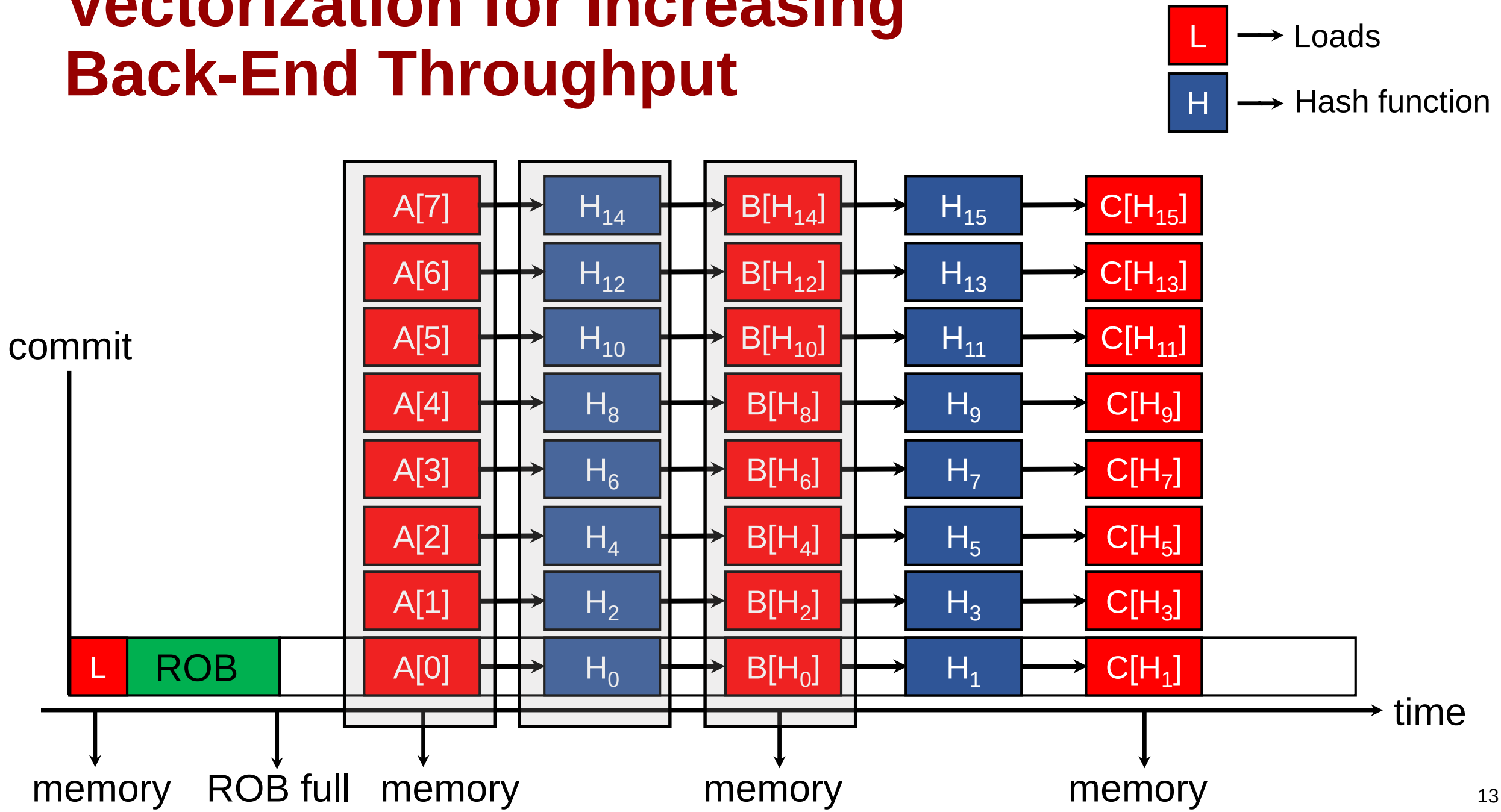
Vectorization for Increasing Back-End Throughput



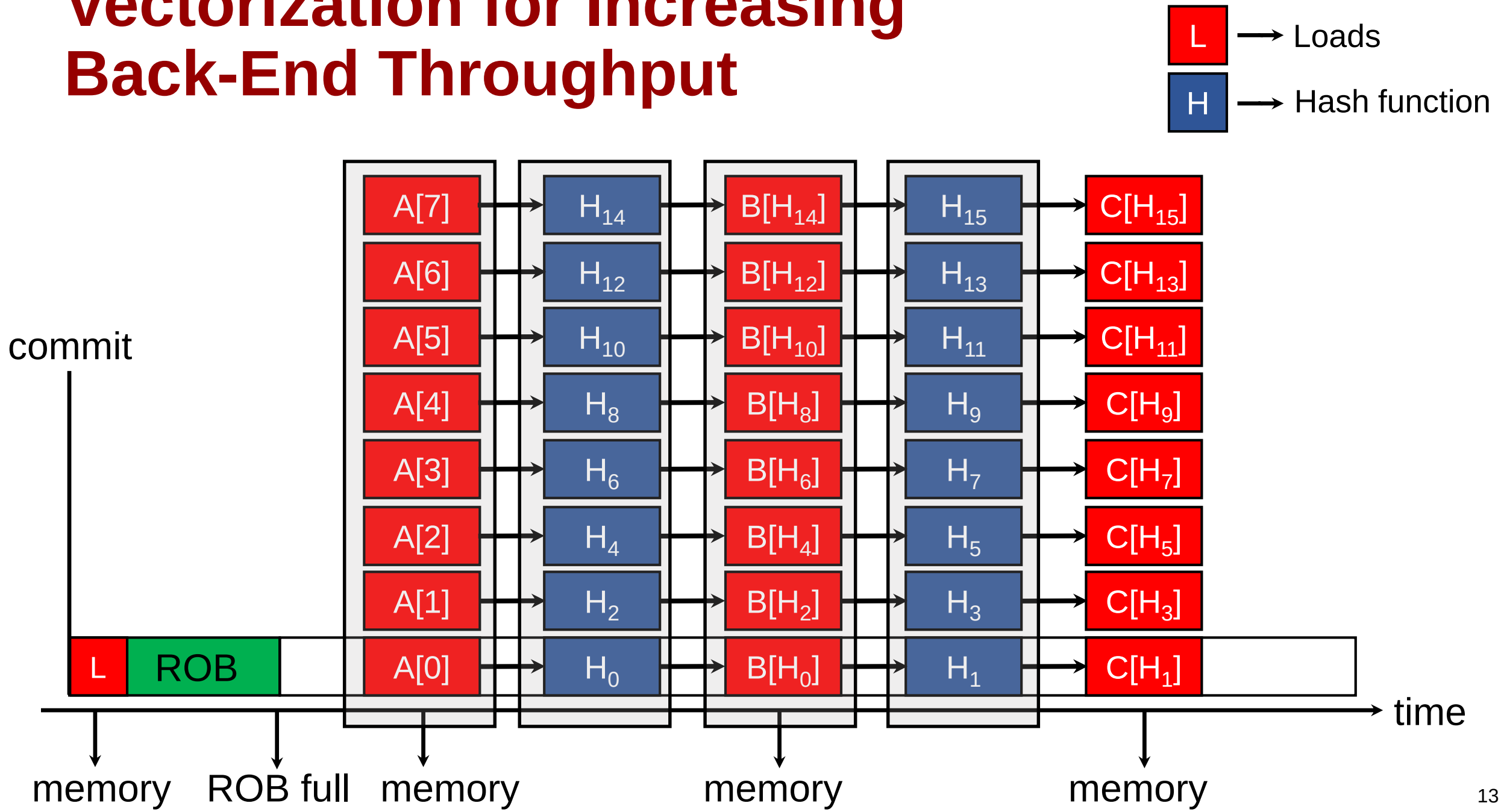
Vectorization for Increasing Back-End Throughput



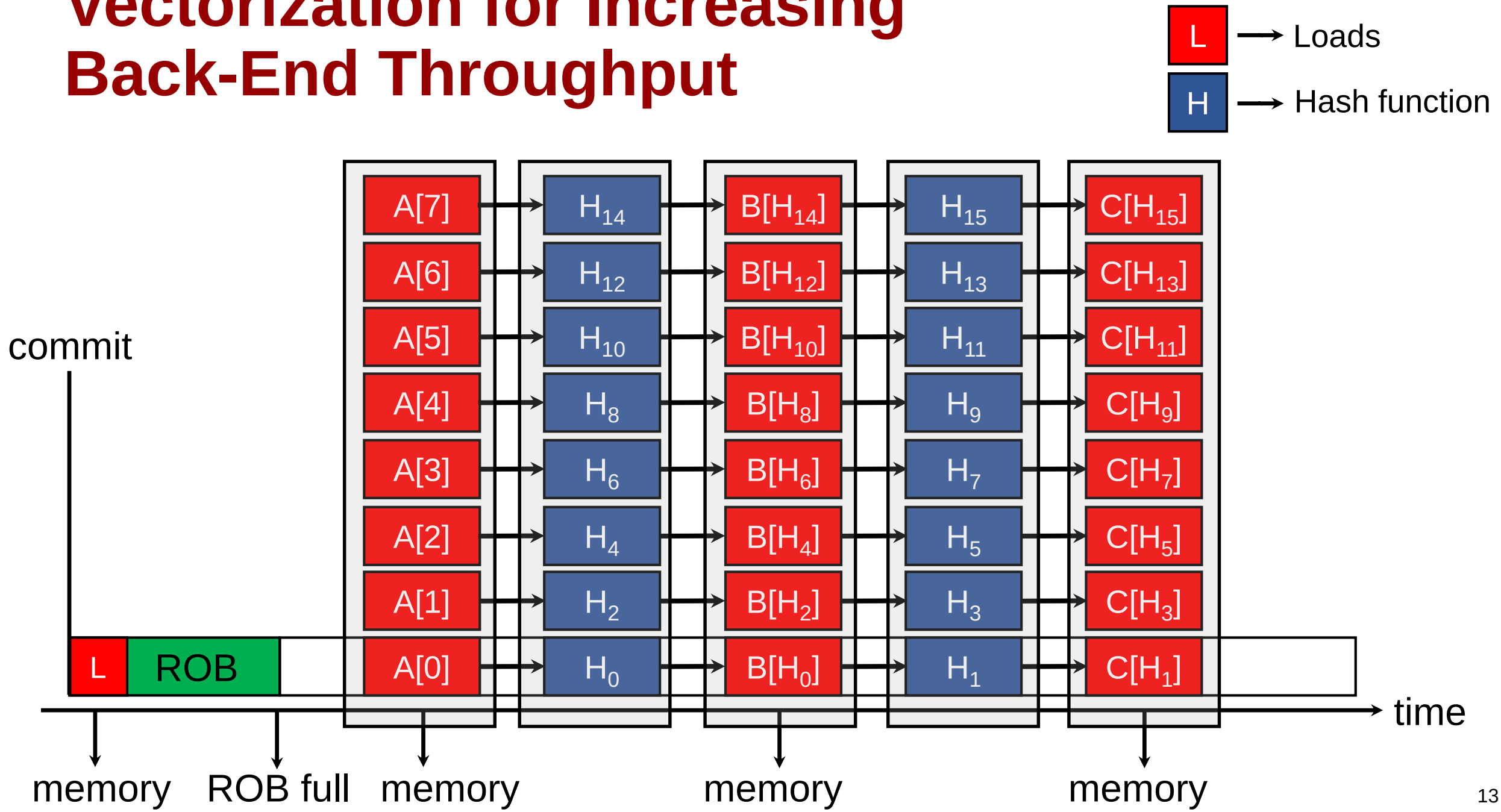
Vectorization for Increasing Back-End Throughput



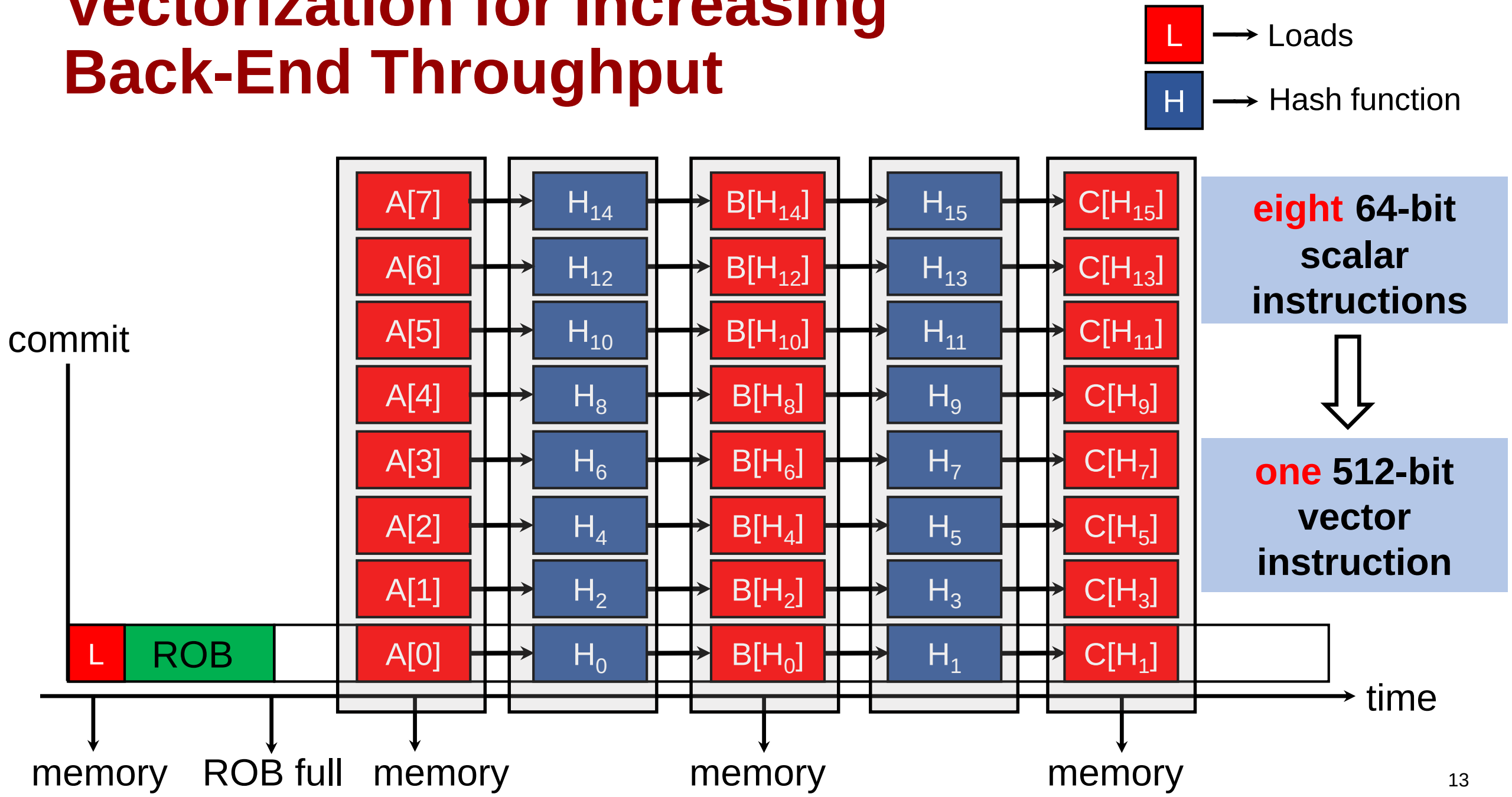
Vectorization for Increasing Back-End Throughput



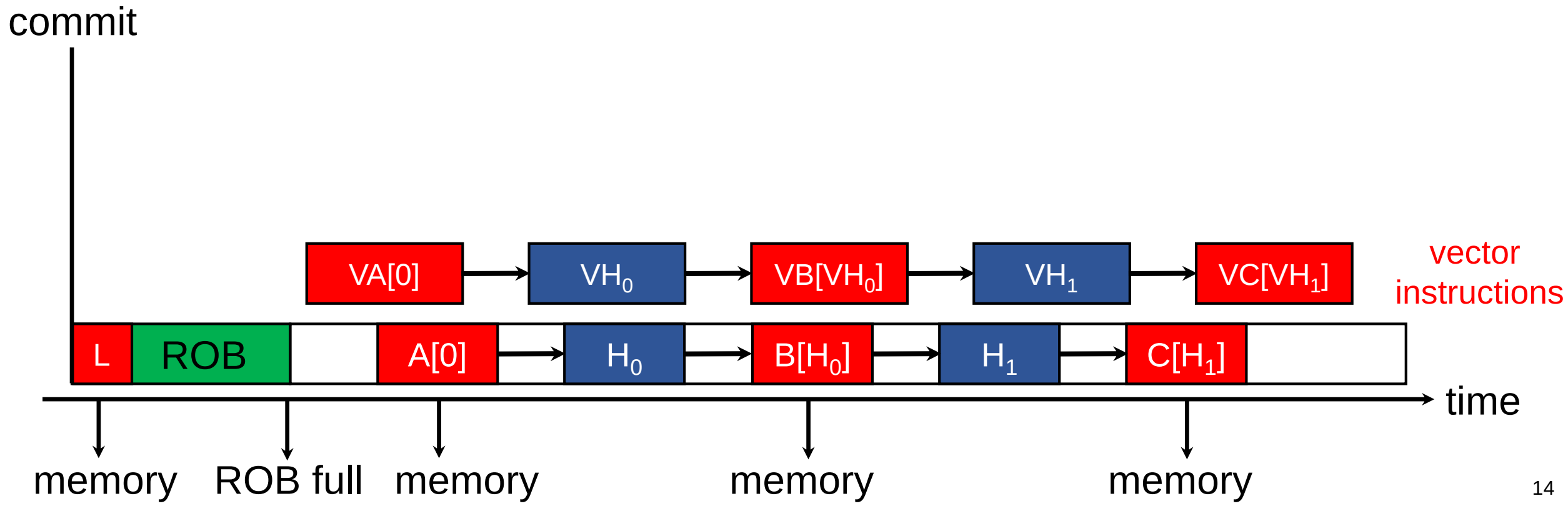
Vectorization for Increasing Back-End Throughput



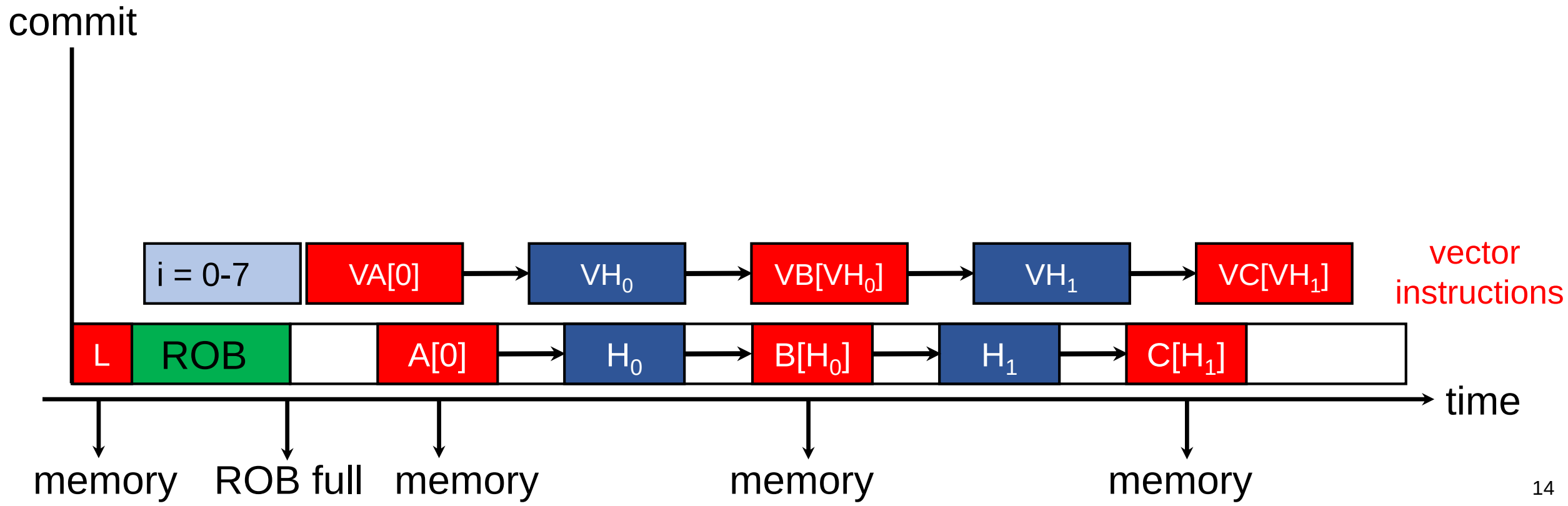
Vectorization for Increasing Back-End Throughput



Vectorization for Increasing Back-End Throughput



Vectorization for Increasing Back-End Throughput



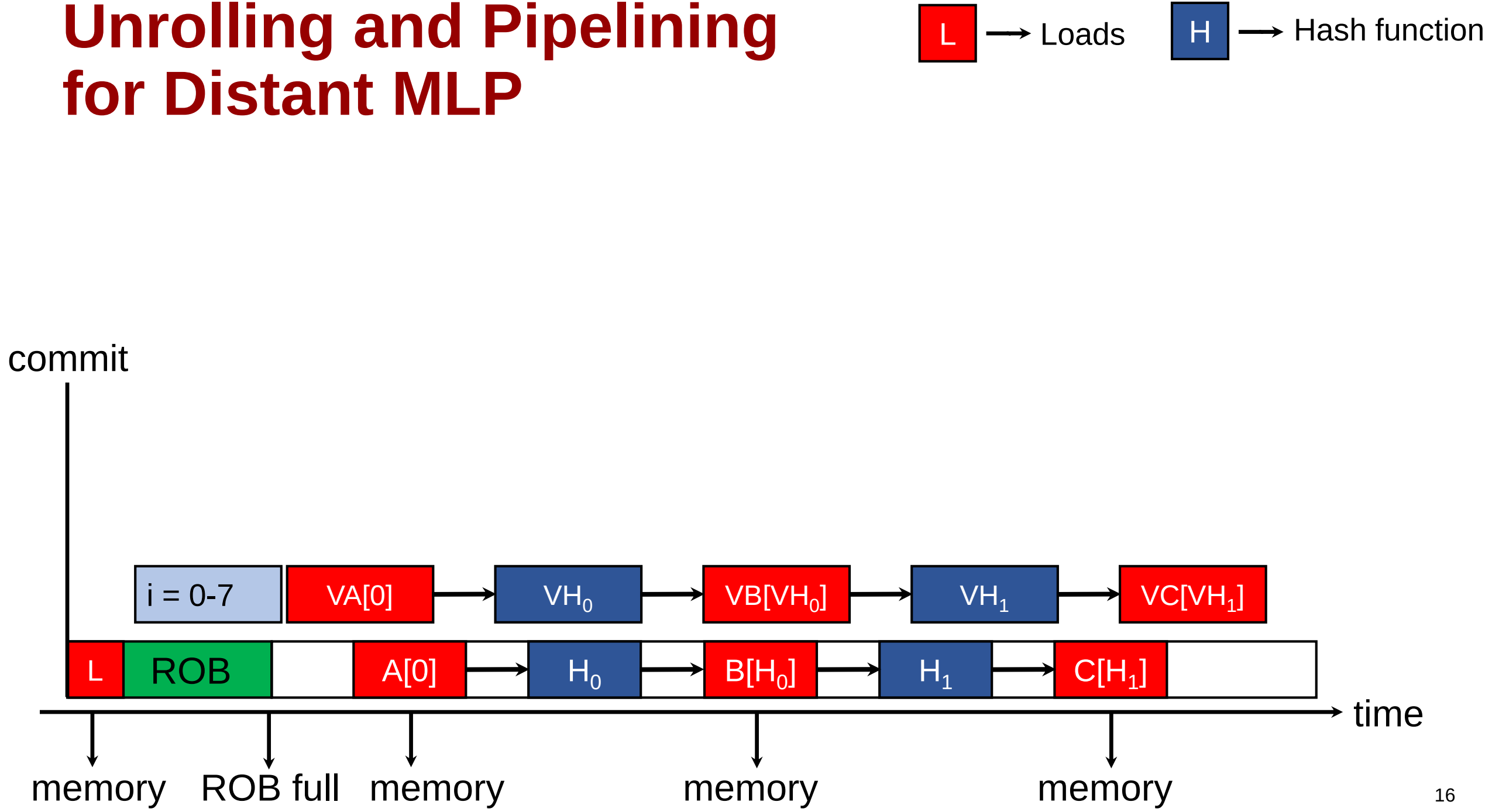
Unrolling and Pipelining for Distant MLP

1. Future instructions are generated automatically
   -- Independent of the front-end bandwidth

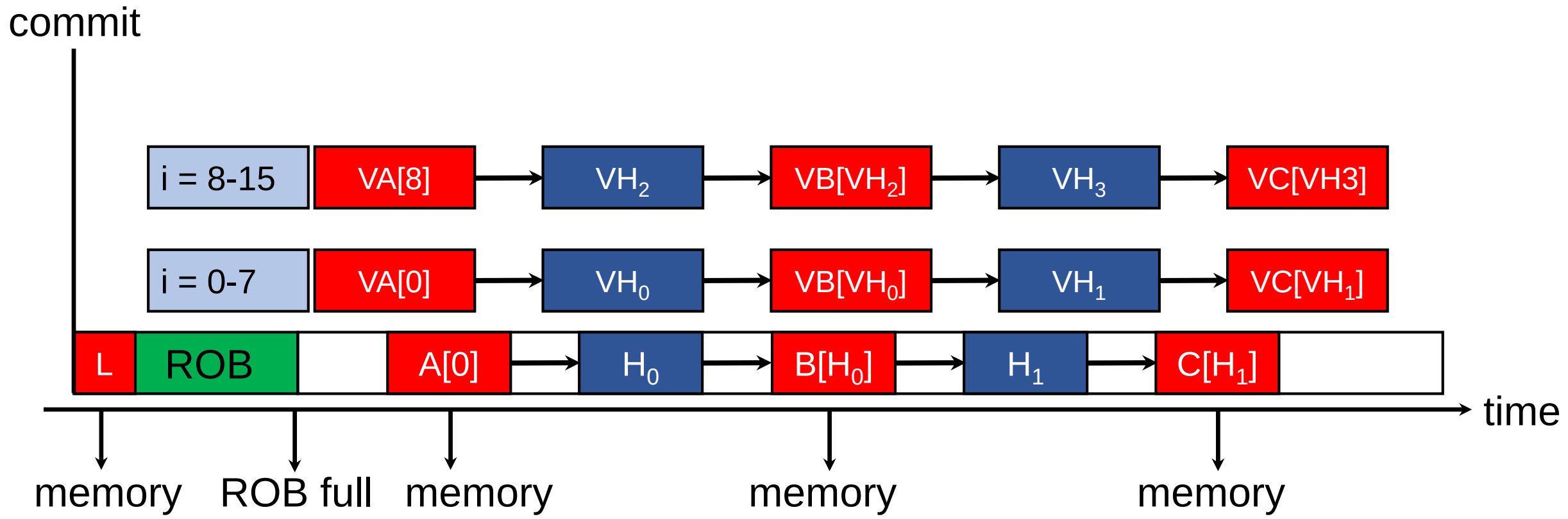
2. Issue more than one vector instructions for each scalar instruction
   -- Unrolling: Dispatch next round of vector instructions after issuing the first

   -- Pipelining: Dispatch multiple vector instructions for each scalar instruction

Unrolling and Pipelining for Distant MLP



Unrolling and Pipelining for Distant MLP



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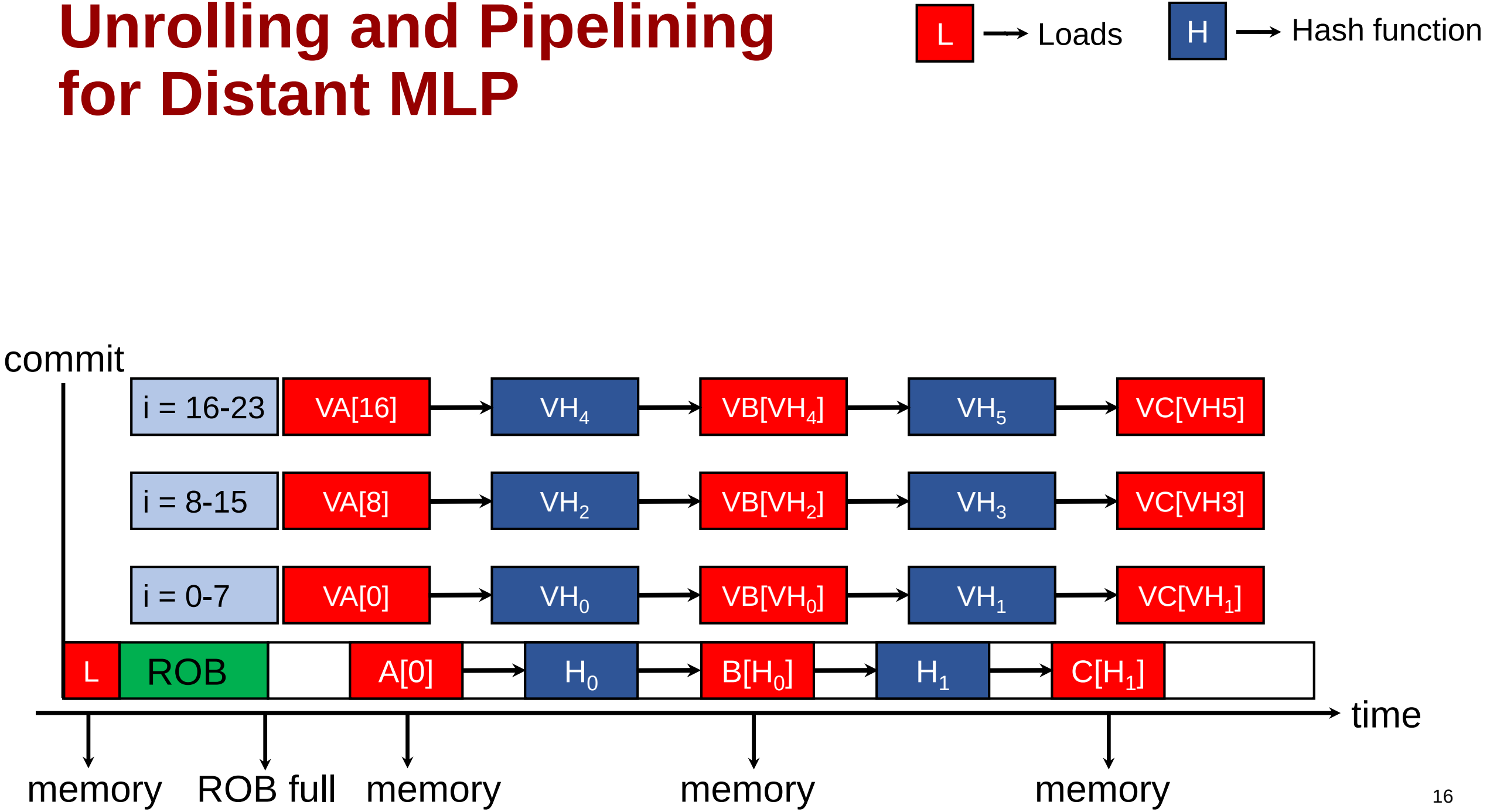

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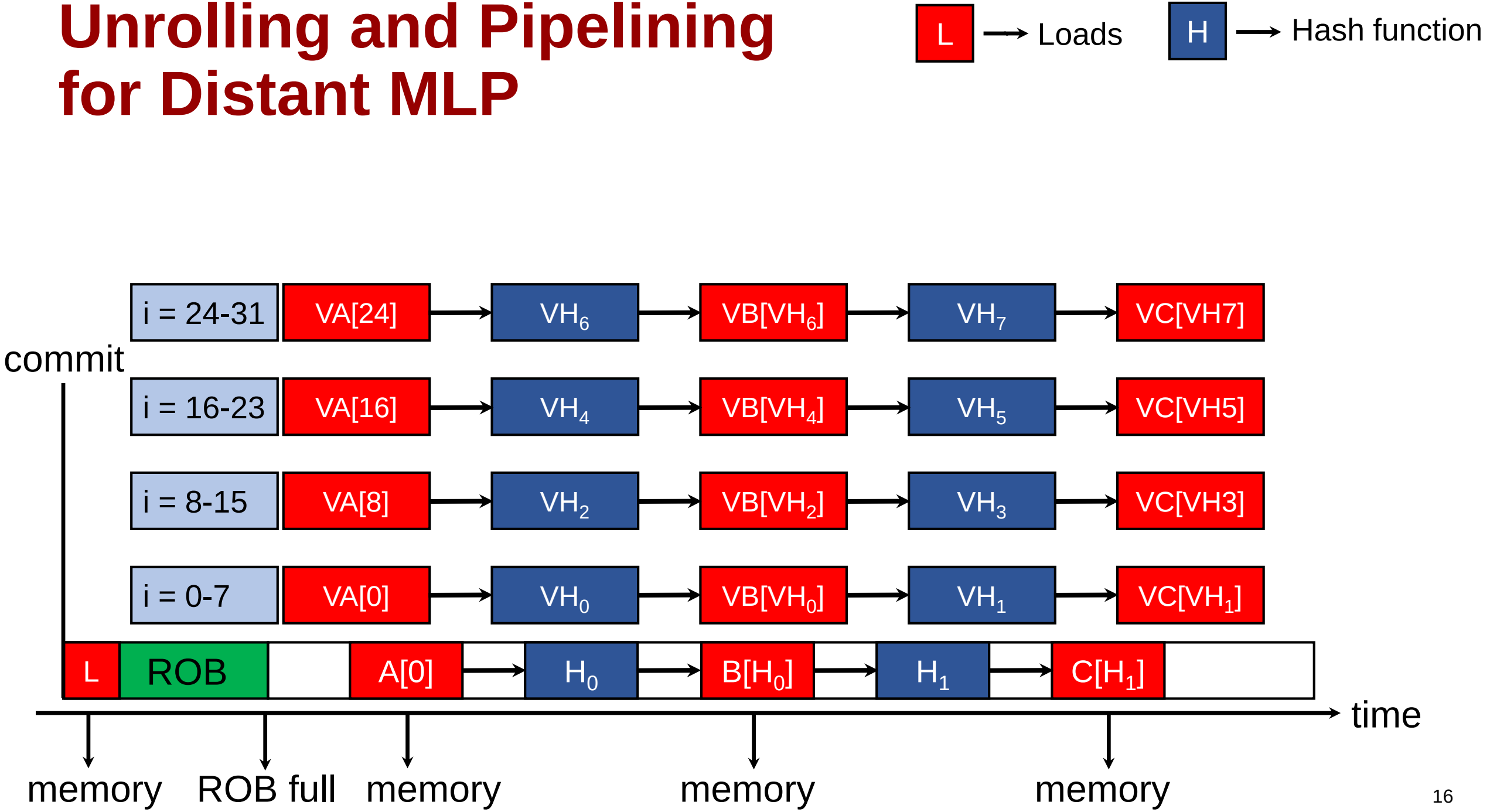
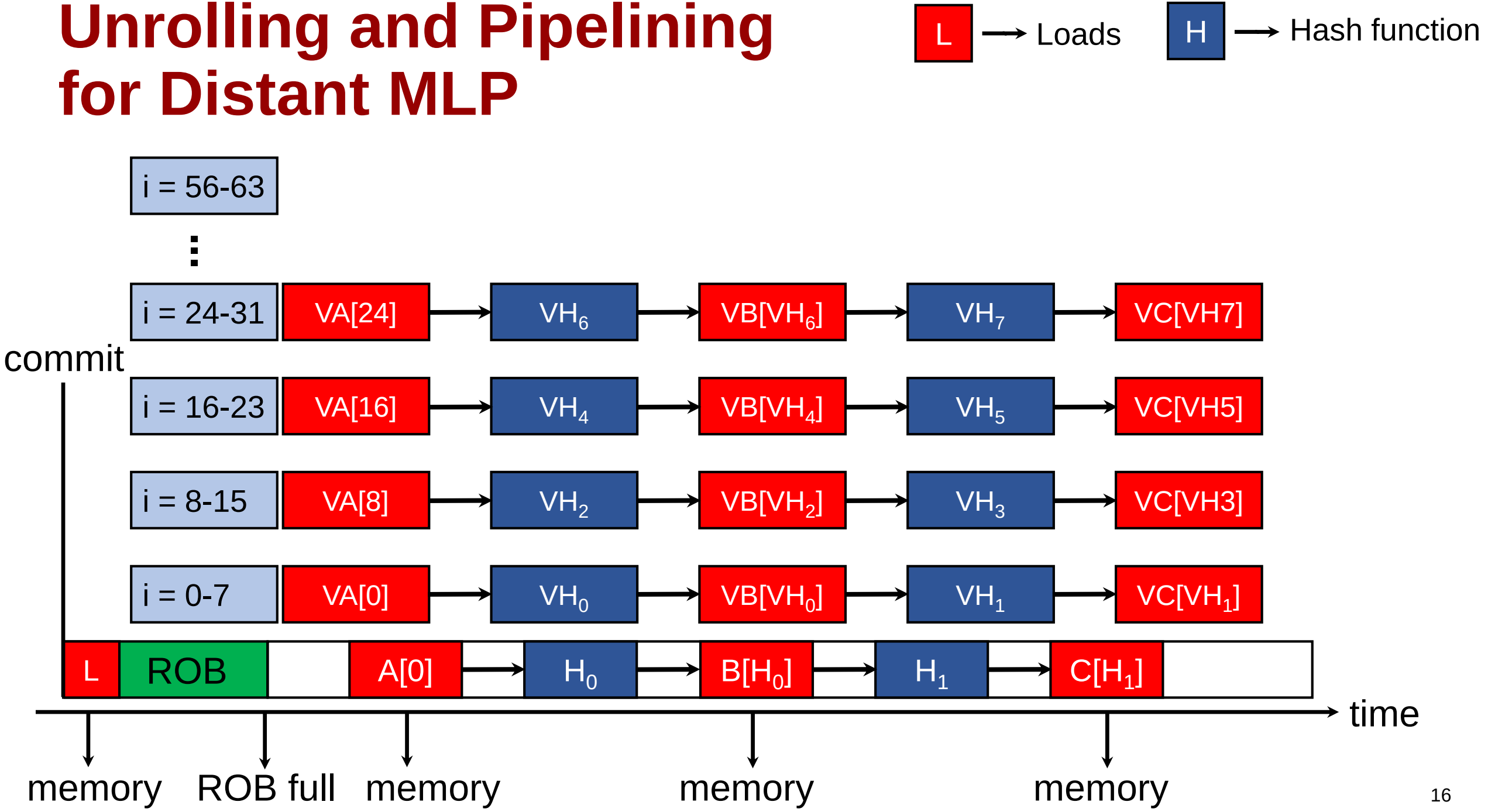


Unrolling and Pipelining for Distant MLP



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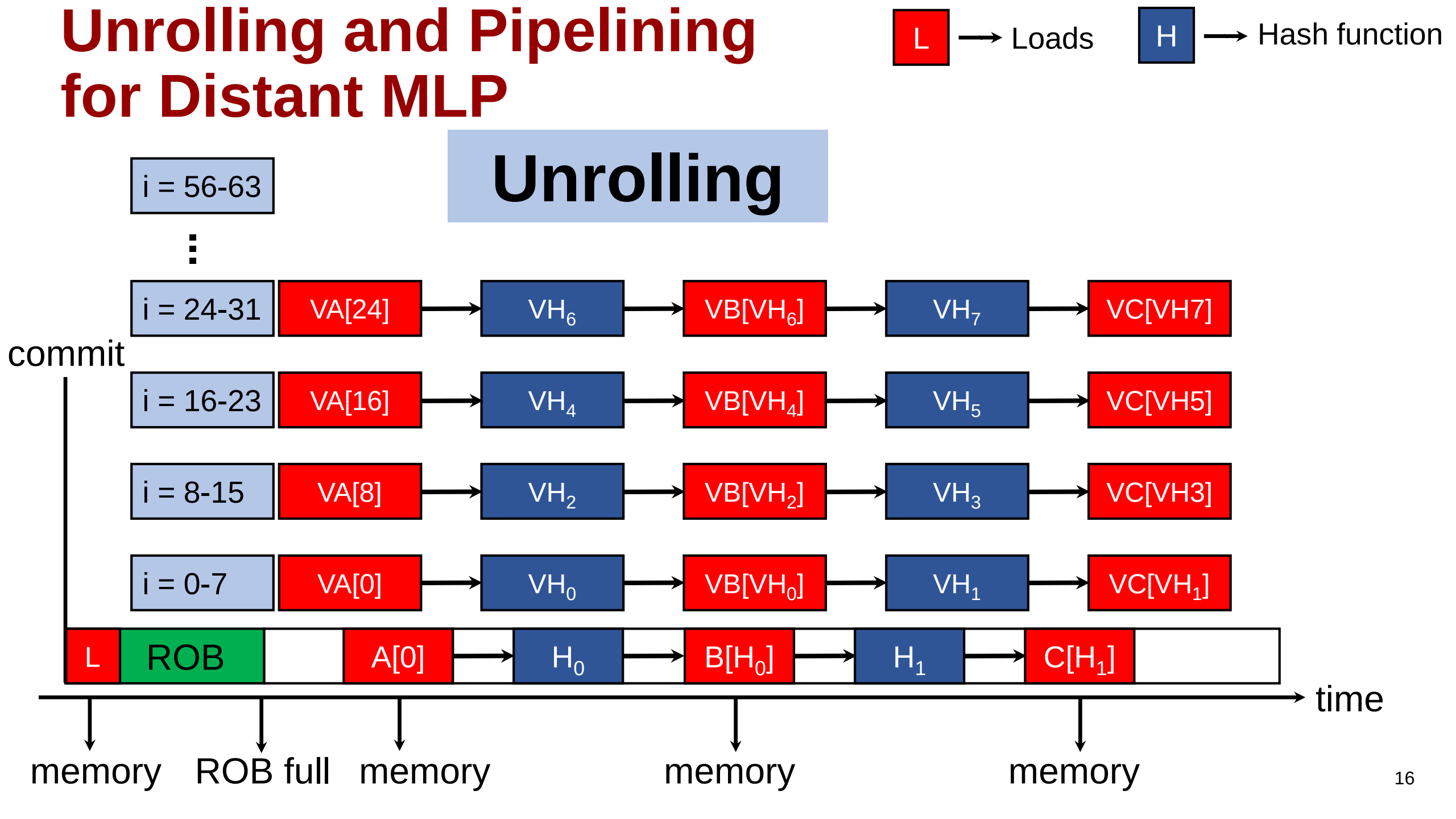

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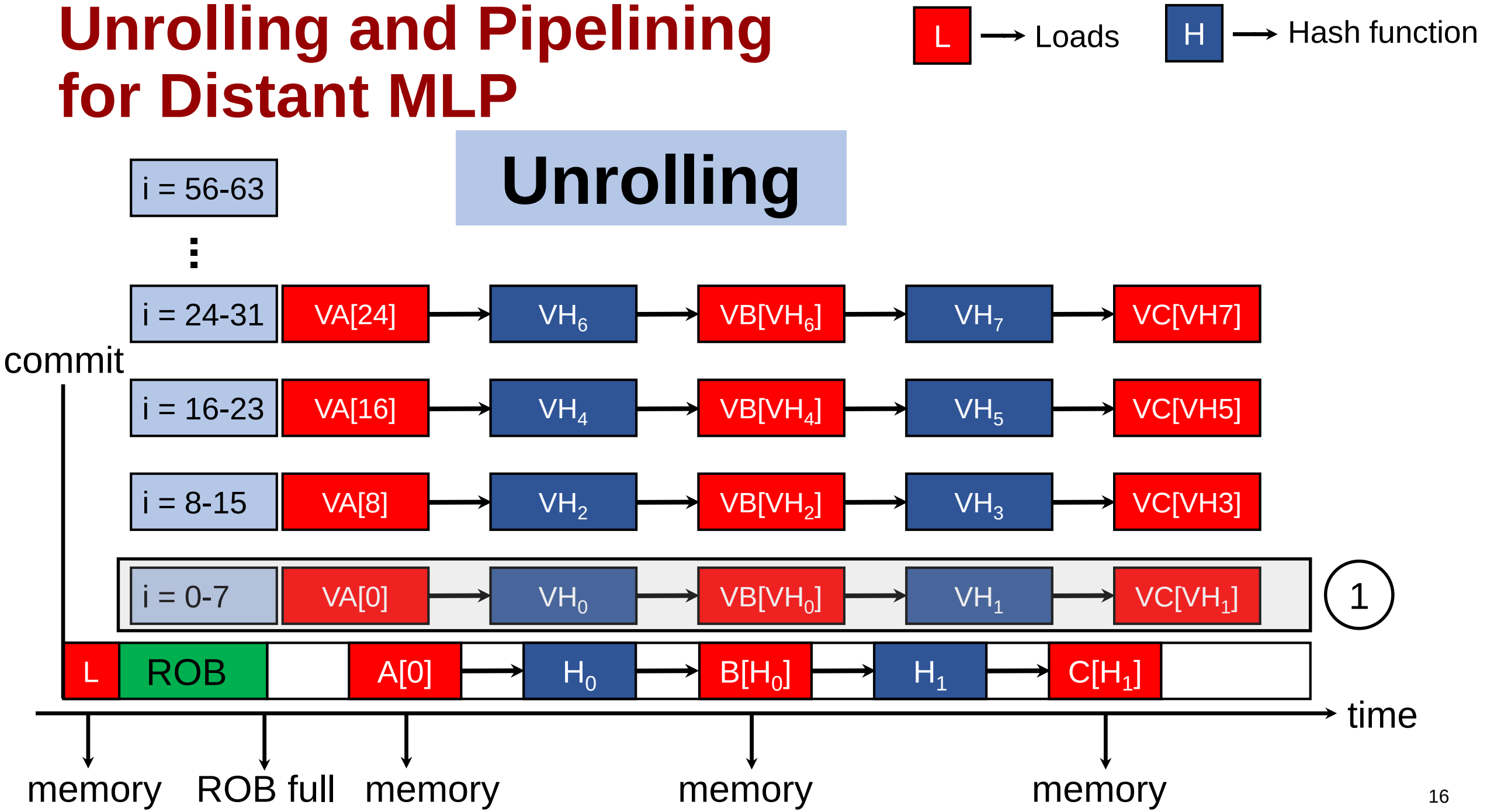

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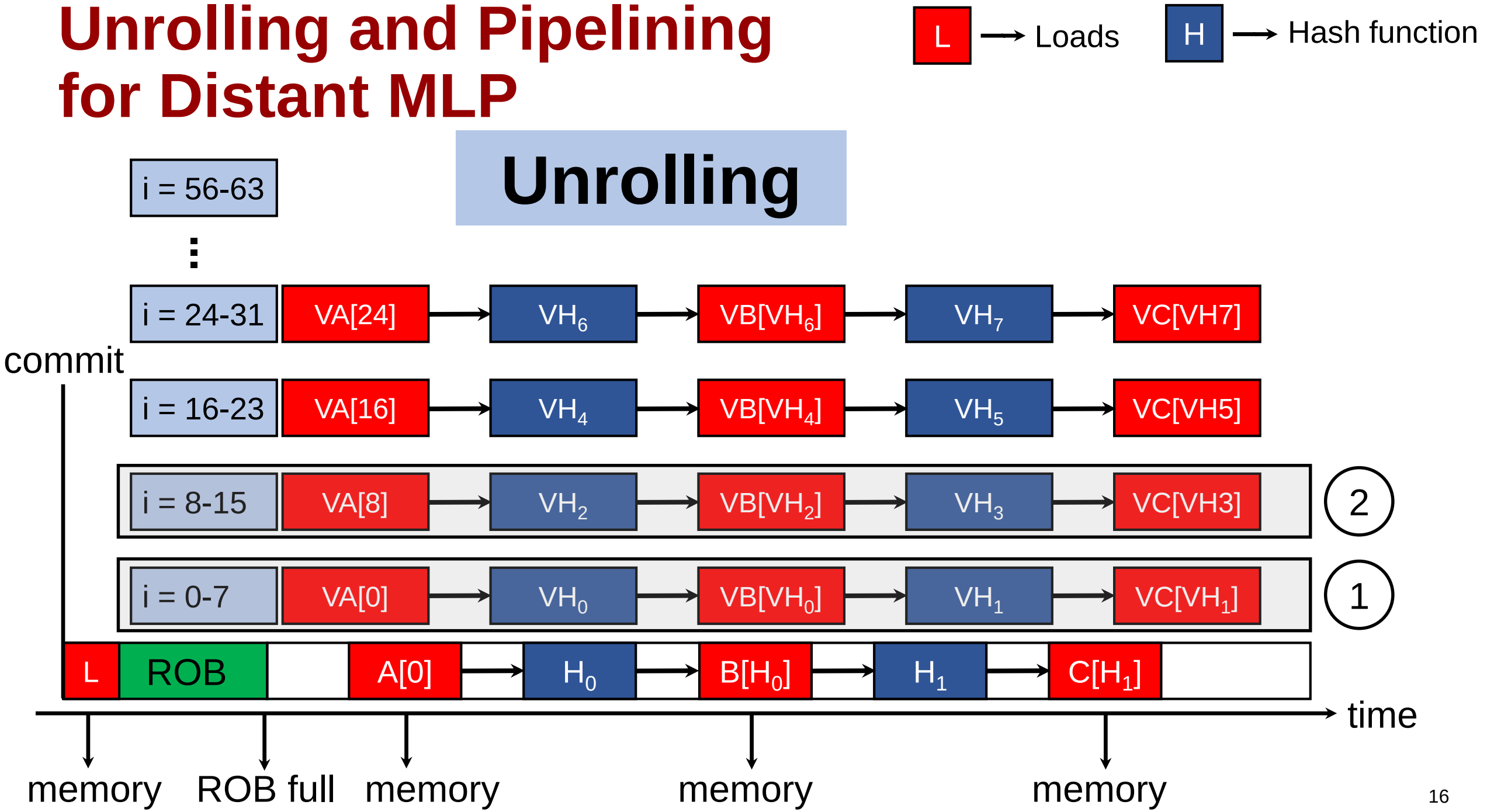

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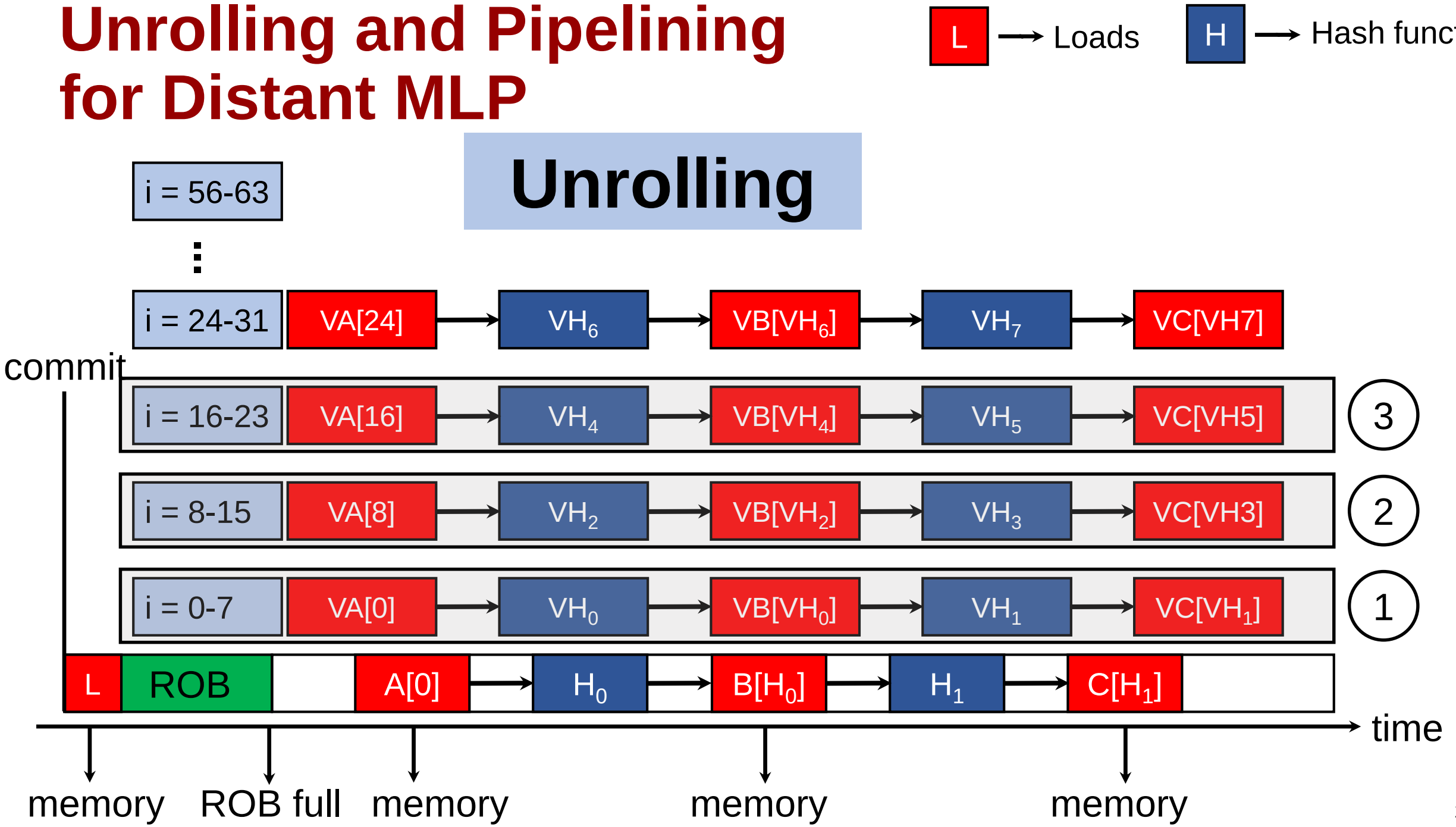

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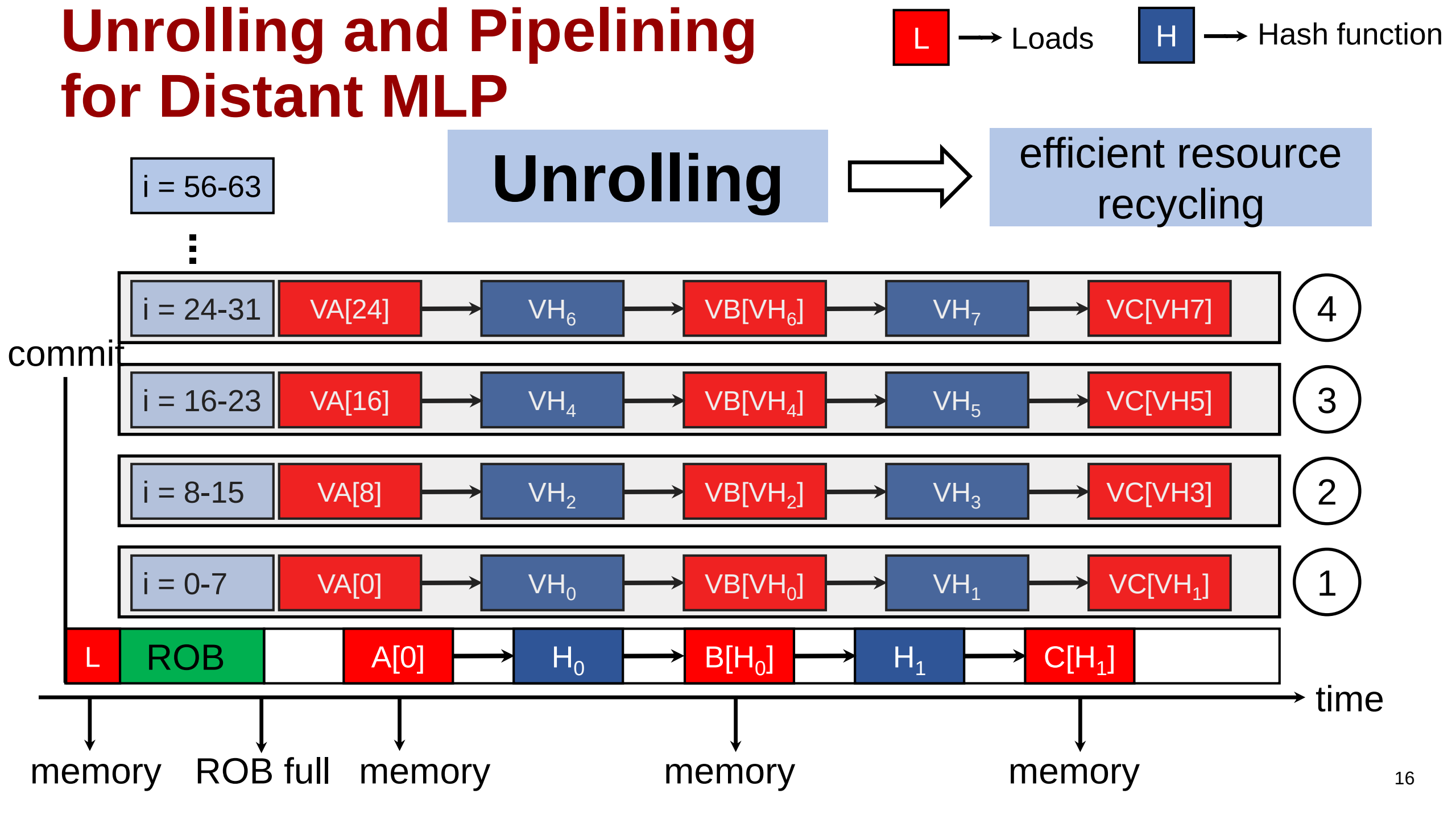

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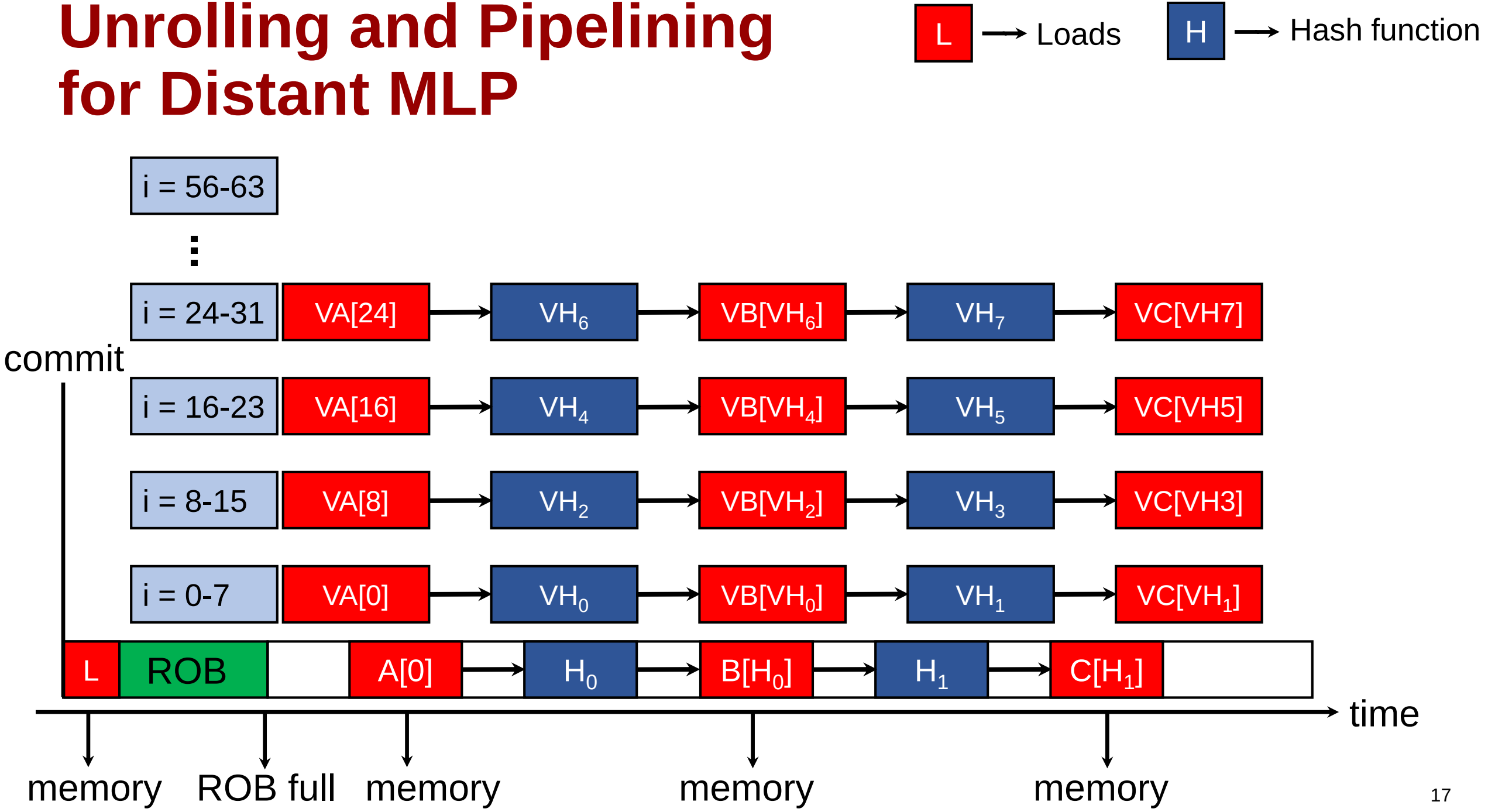

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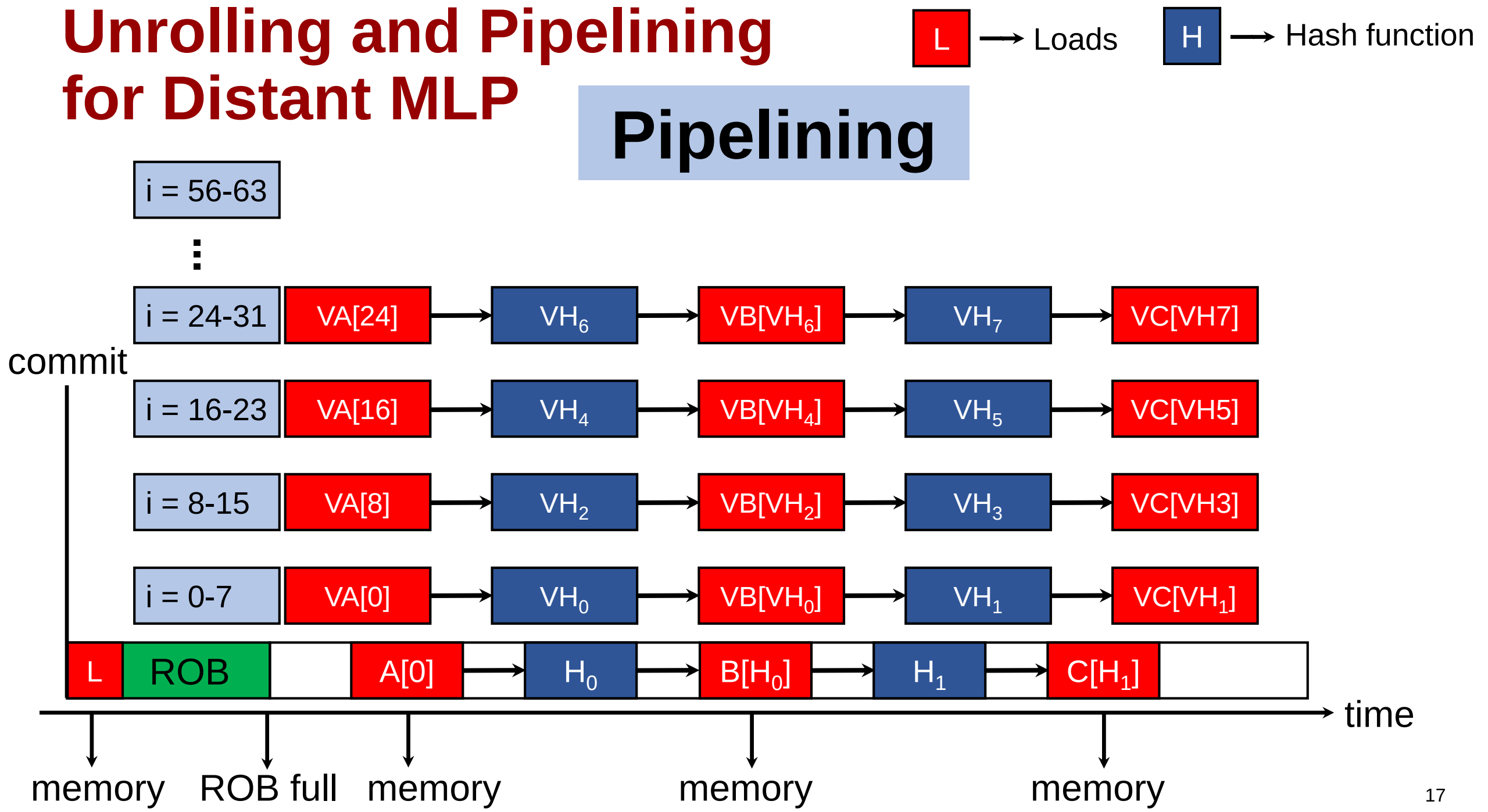

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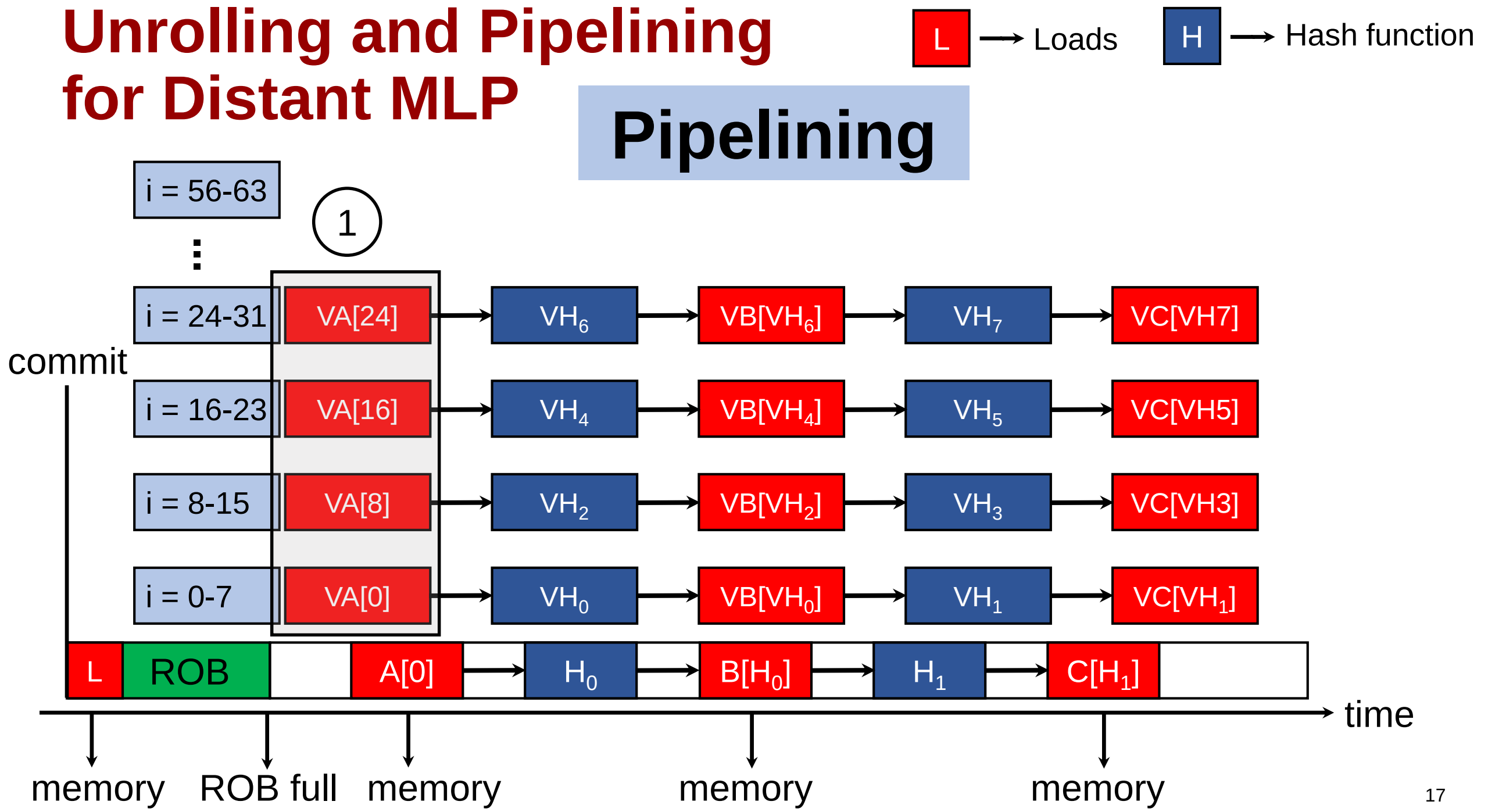

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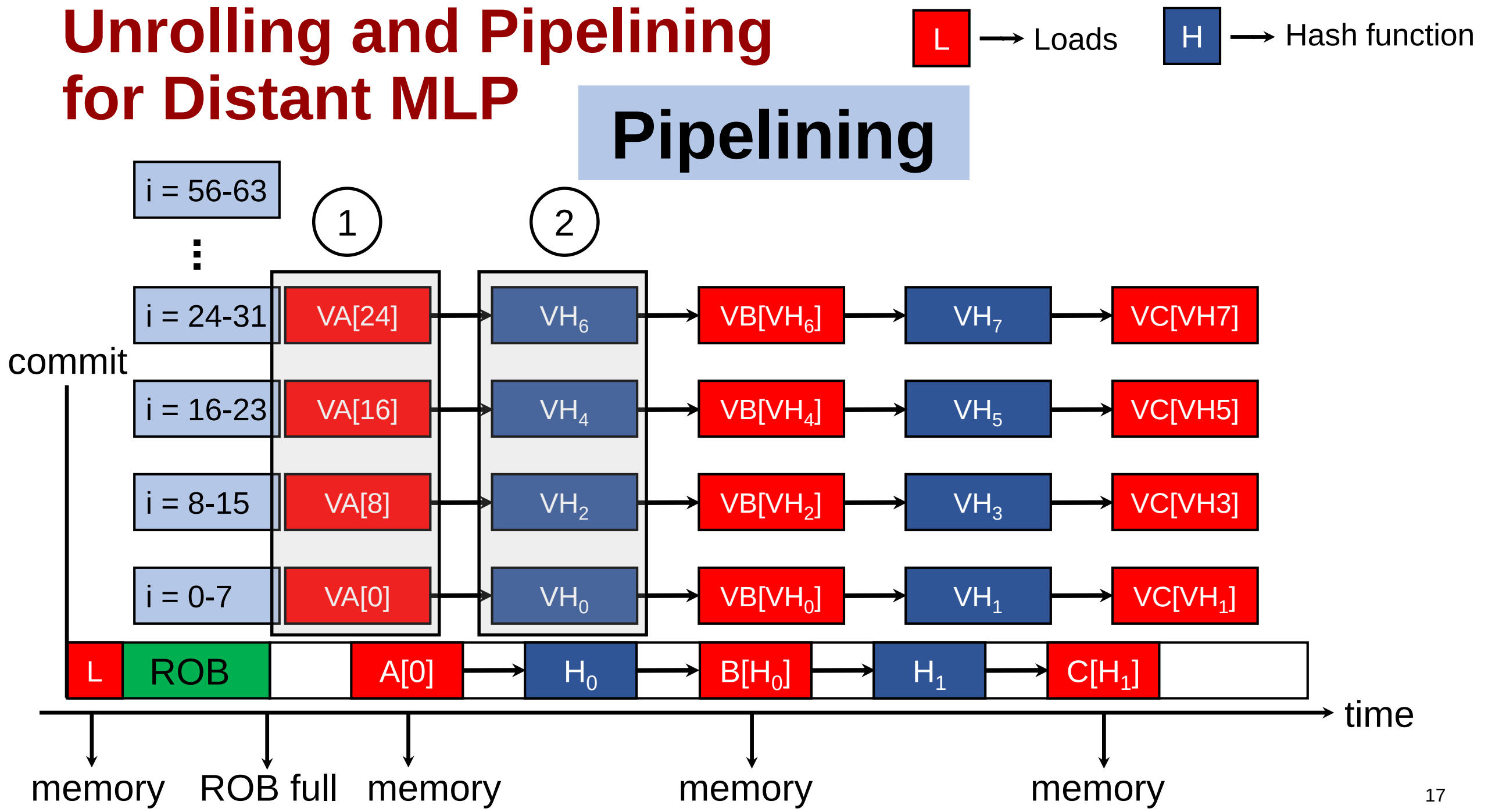

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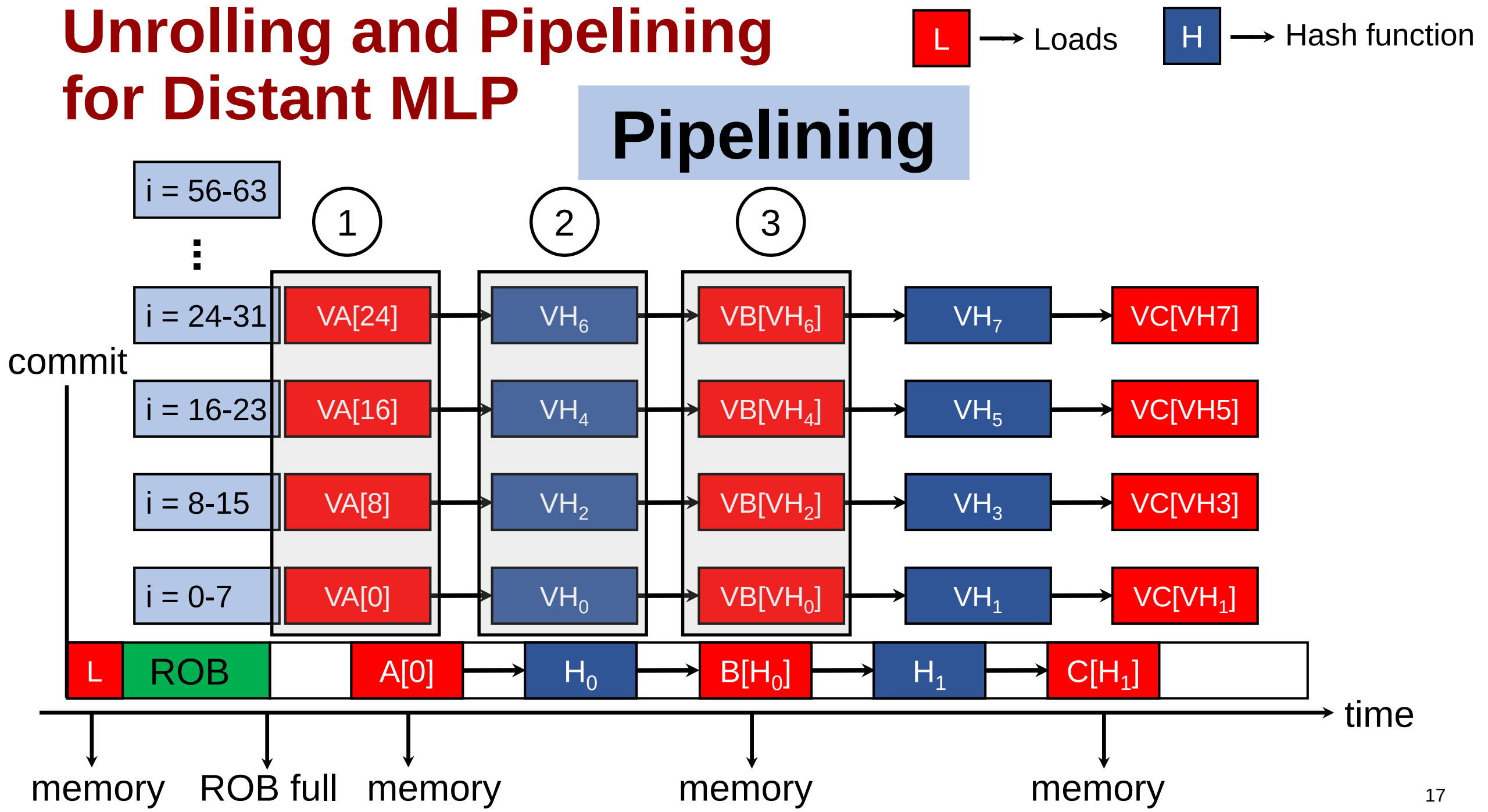

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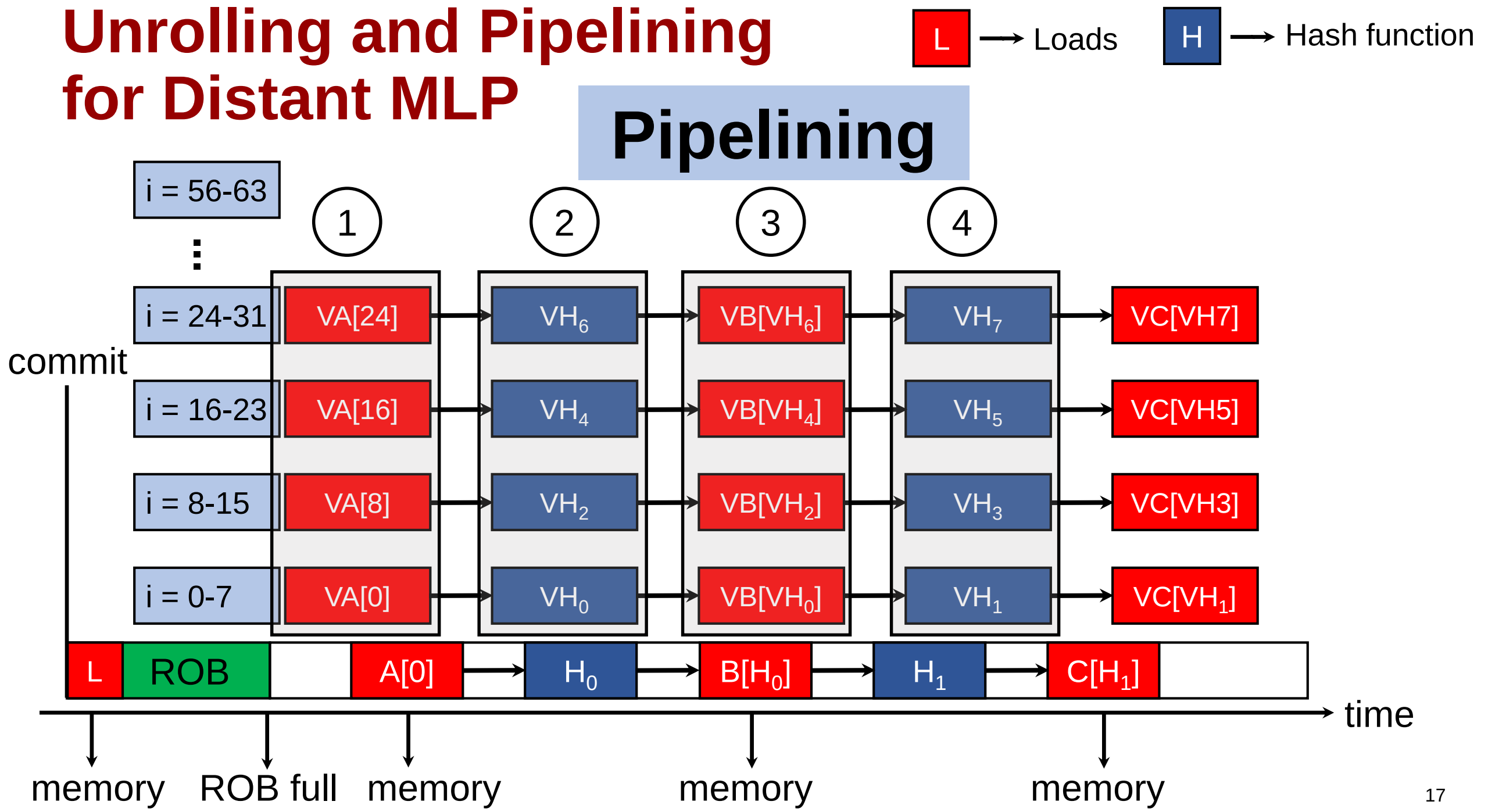

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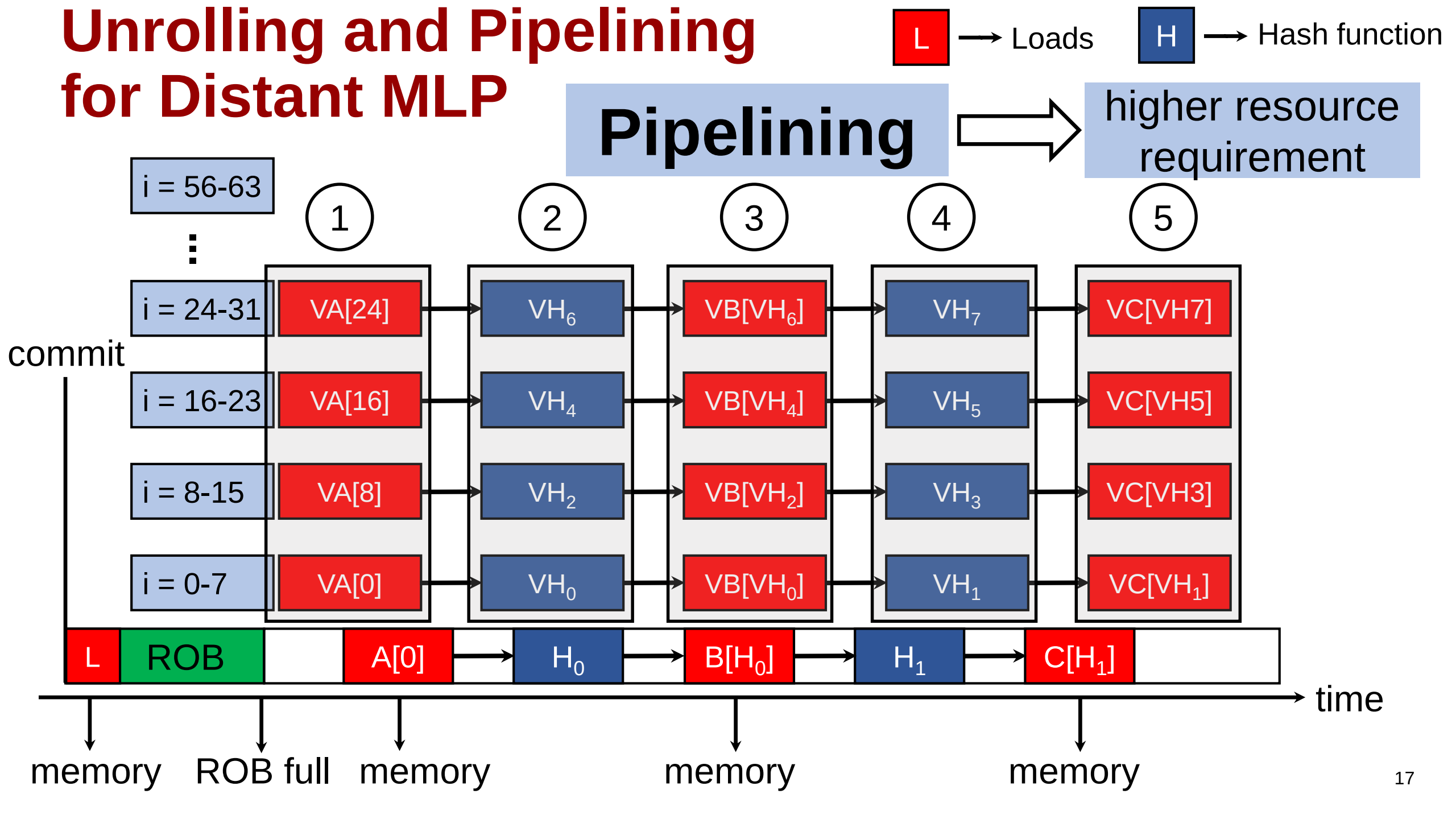
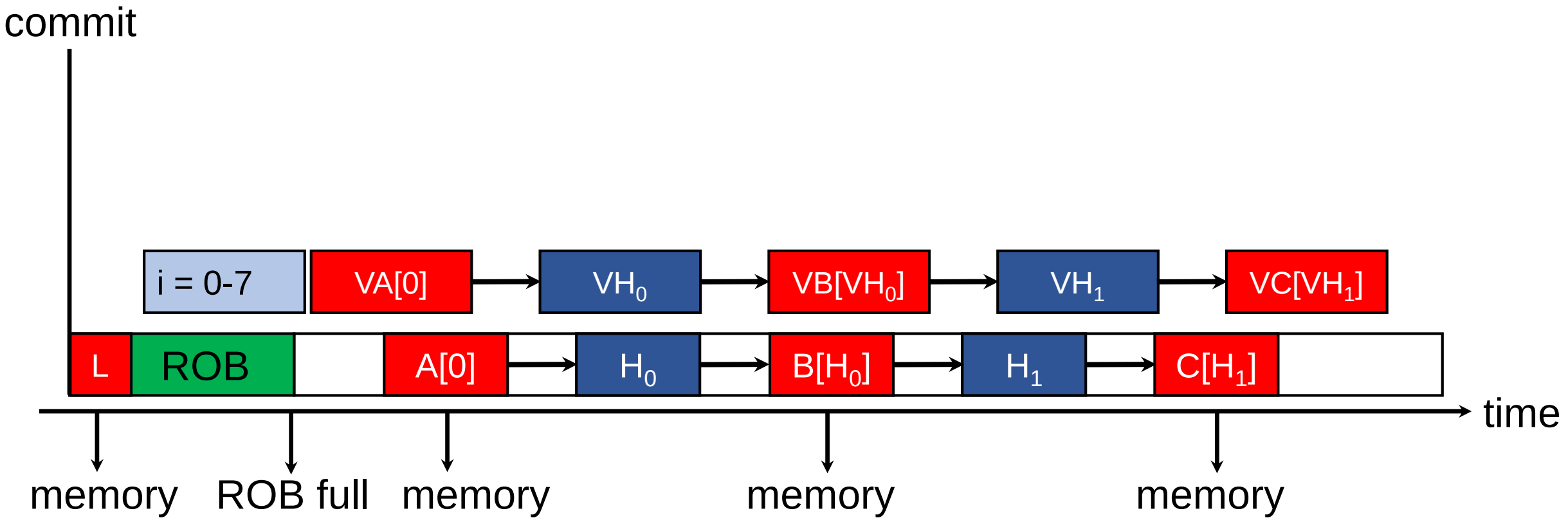


Delayed Termination in Vector Runahead

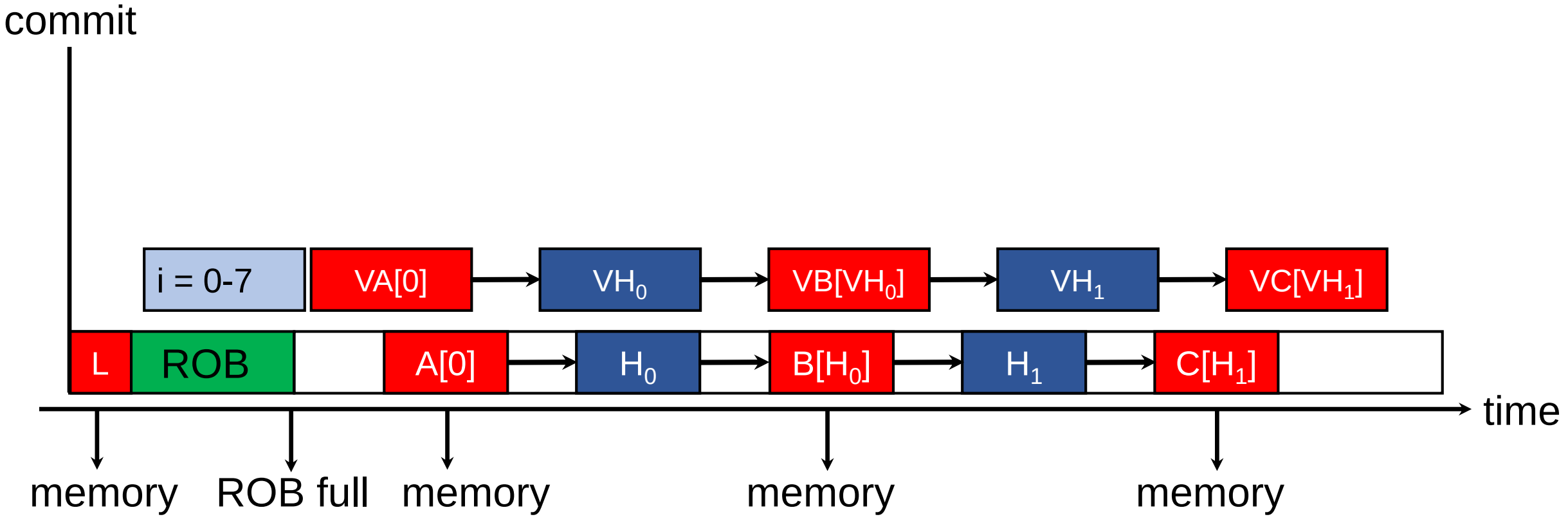
When to terminate runahead mode?



Delayed Termination in Vector Runahead

When to terminate runahead mode?

Last indirect load: Identified with vector taint tracking



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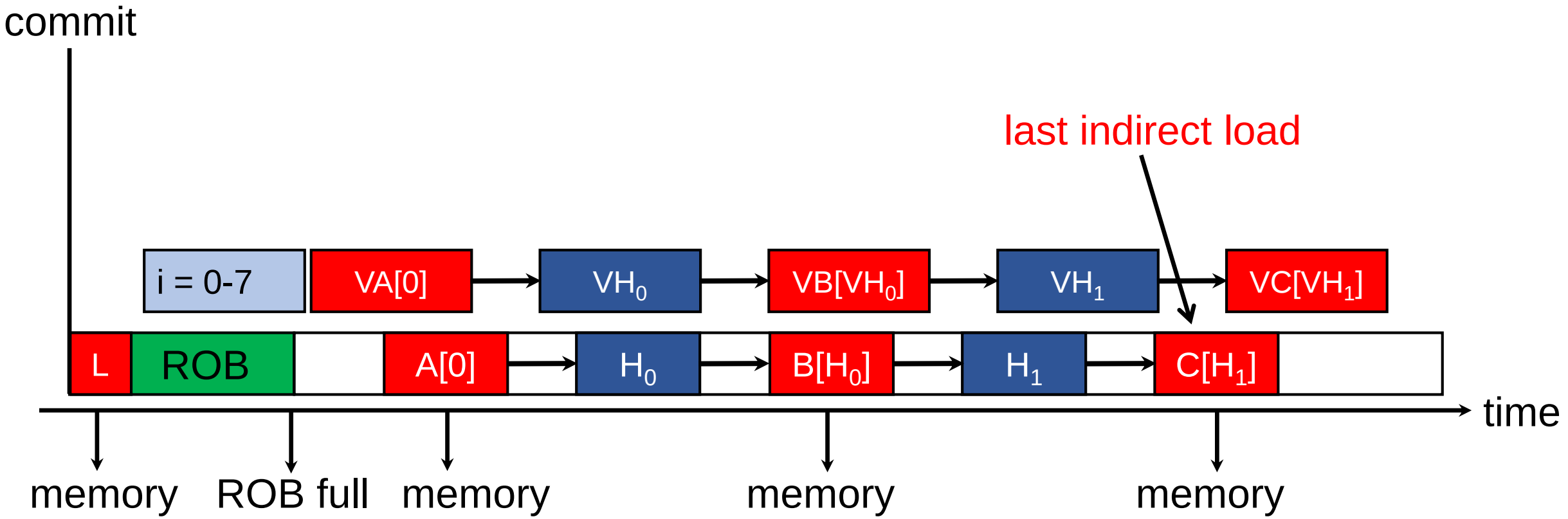
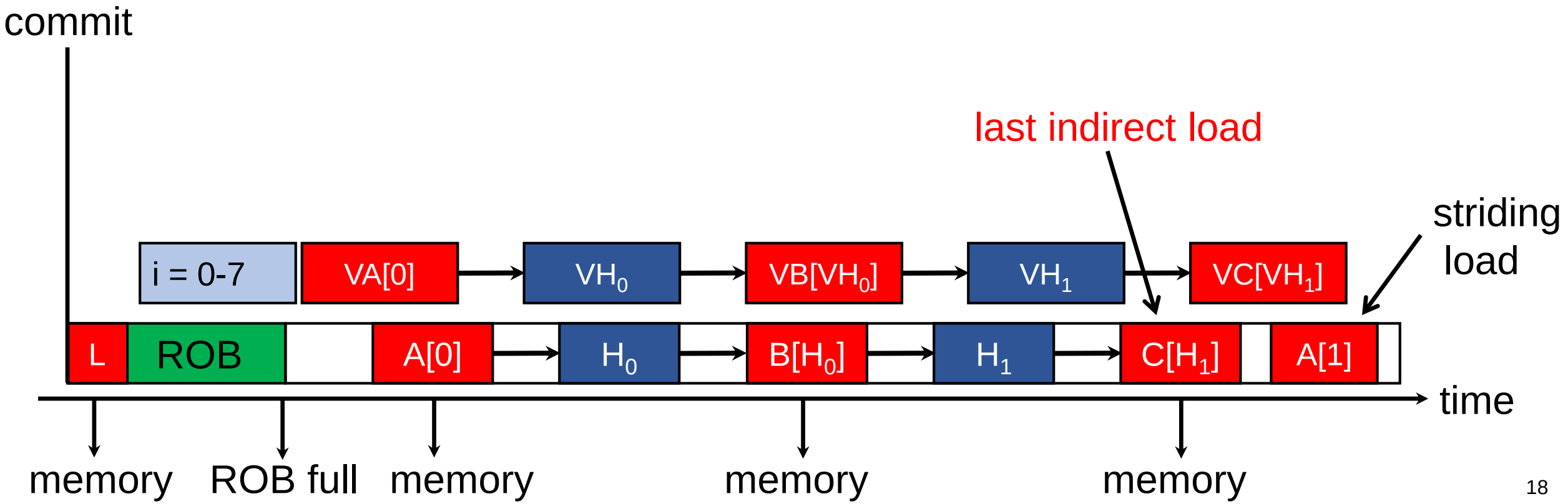


Delayed Termination in Vector Runahead

When to terminate runahead mode?

Last indirect load: Identified with vector taint tracking

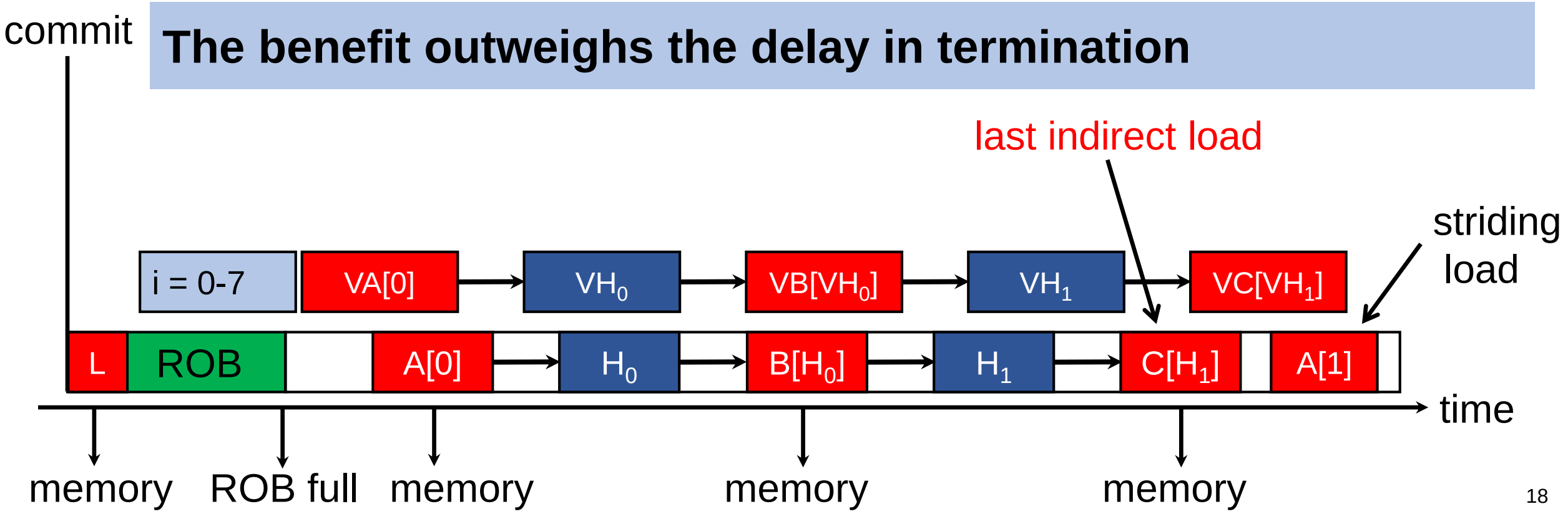


Delayed Termination in Vector Runahead

When to terminate runahead mode?

Last indirect load: Identified with vector taint tracking

The benefit outweighs the delay in termination



Register Renaming in Vector Runahead

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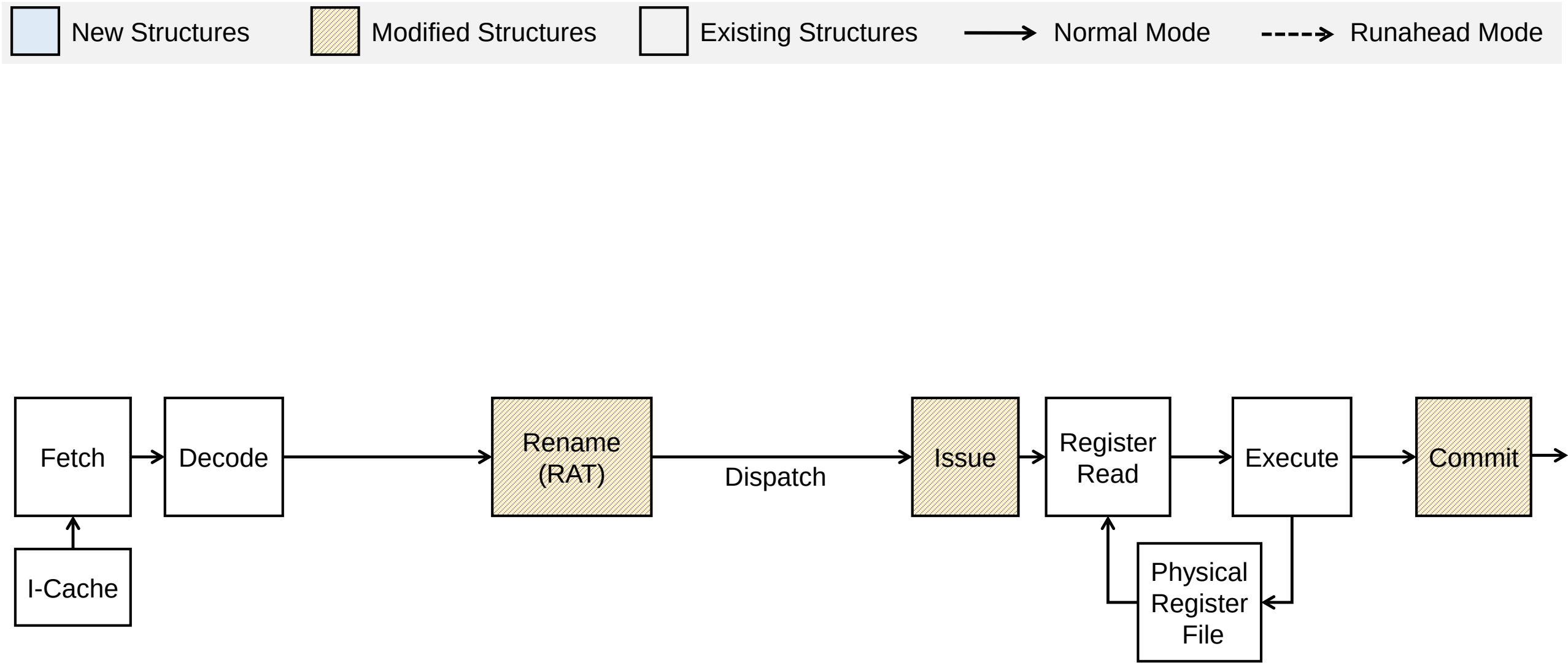
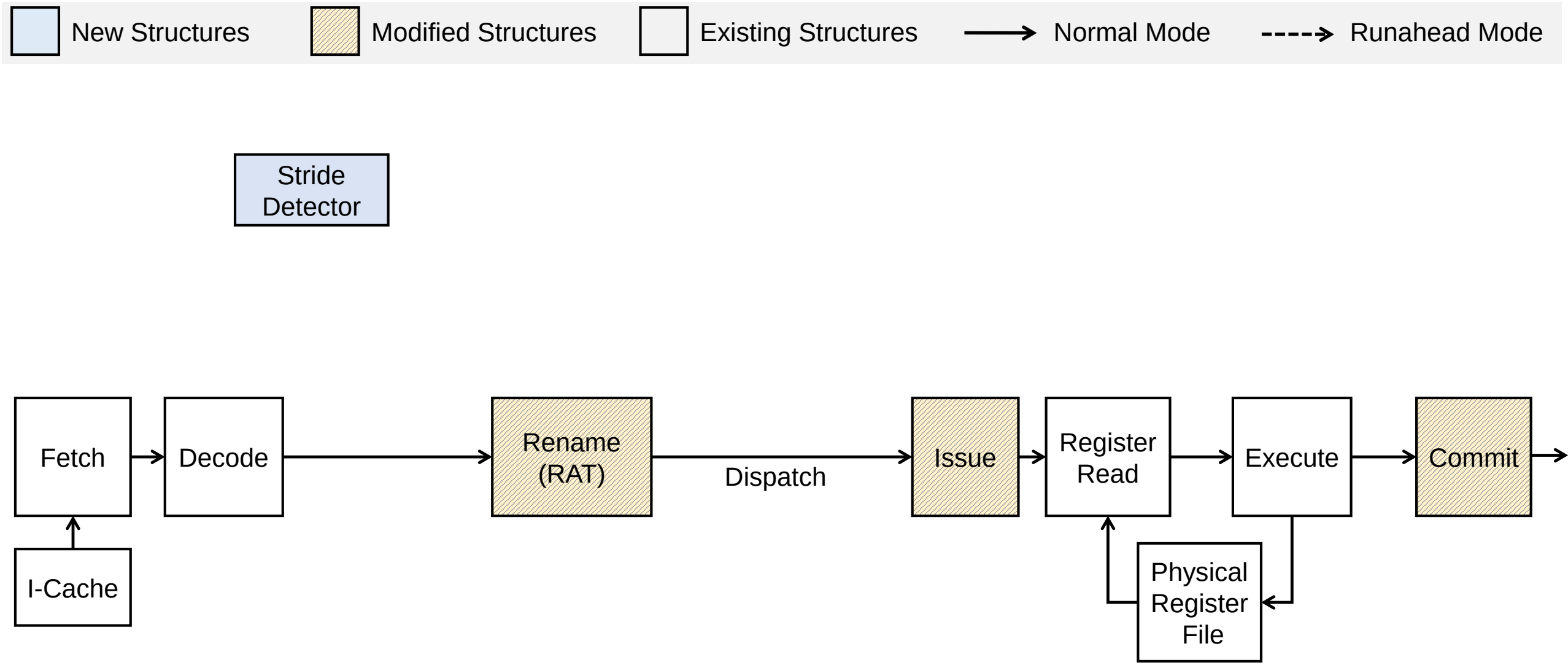
2. **Deallocation:** Like Precise Runahead Using Register Deallocation Queue (RDQ)

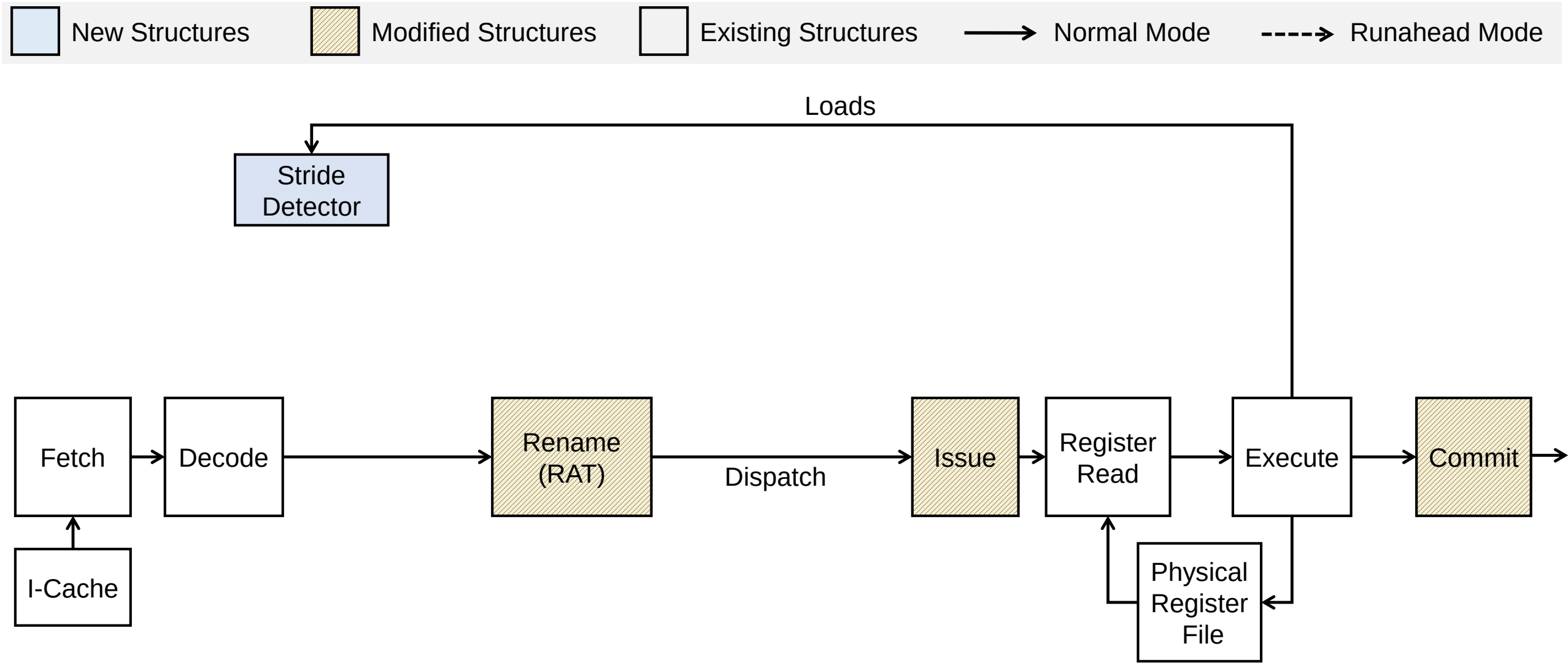
Vector Runahead Microarchitecture



Vector Runahead Microarchitecture



Vector Runahead Microarchitecture



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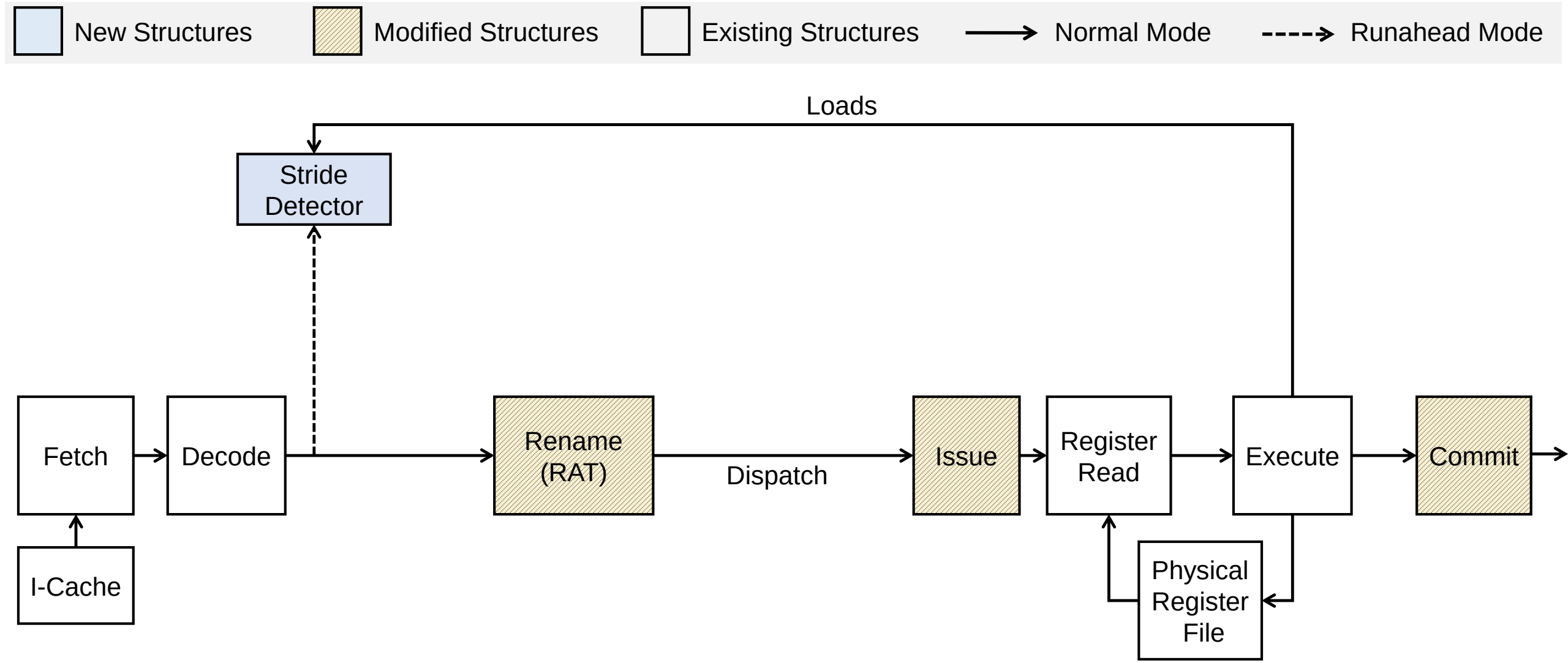

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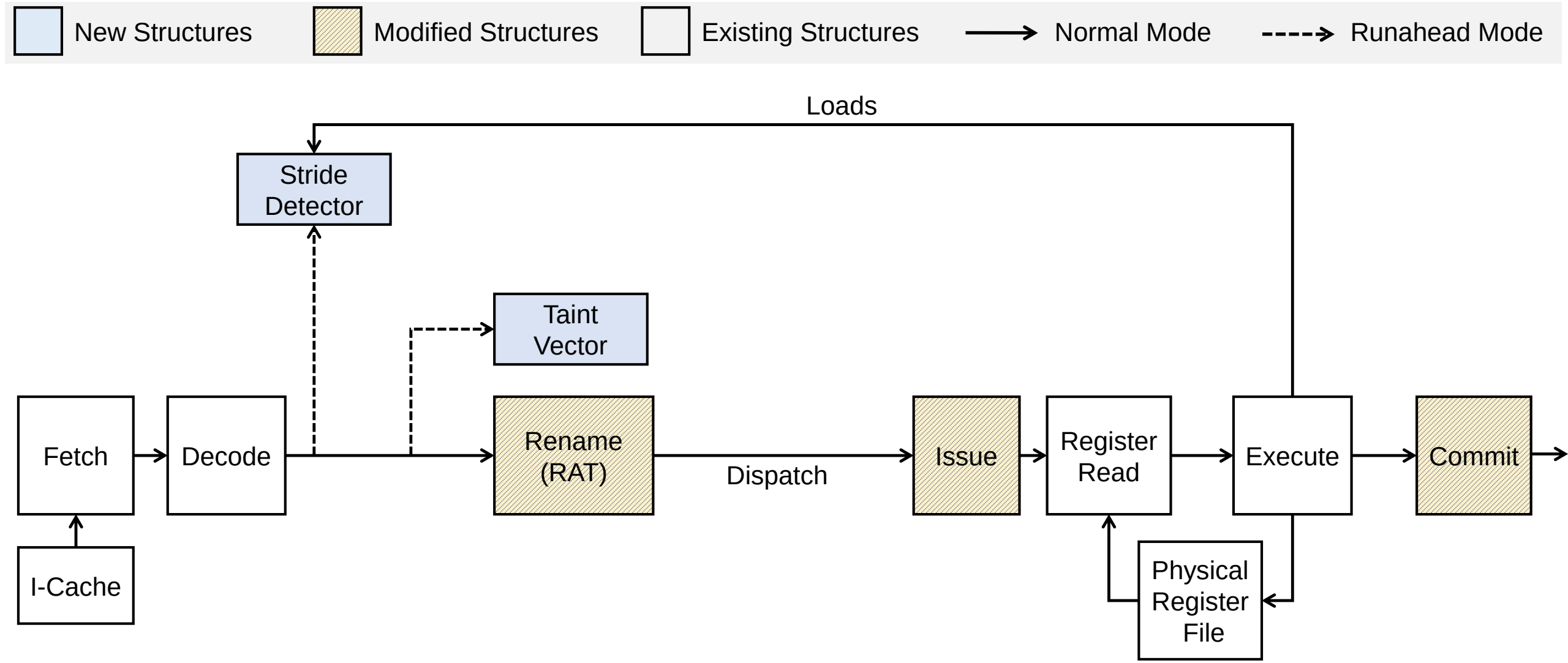

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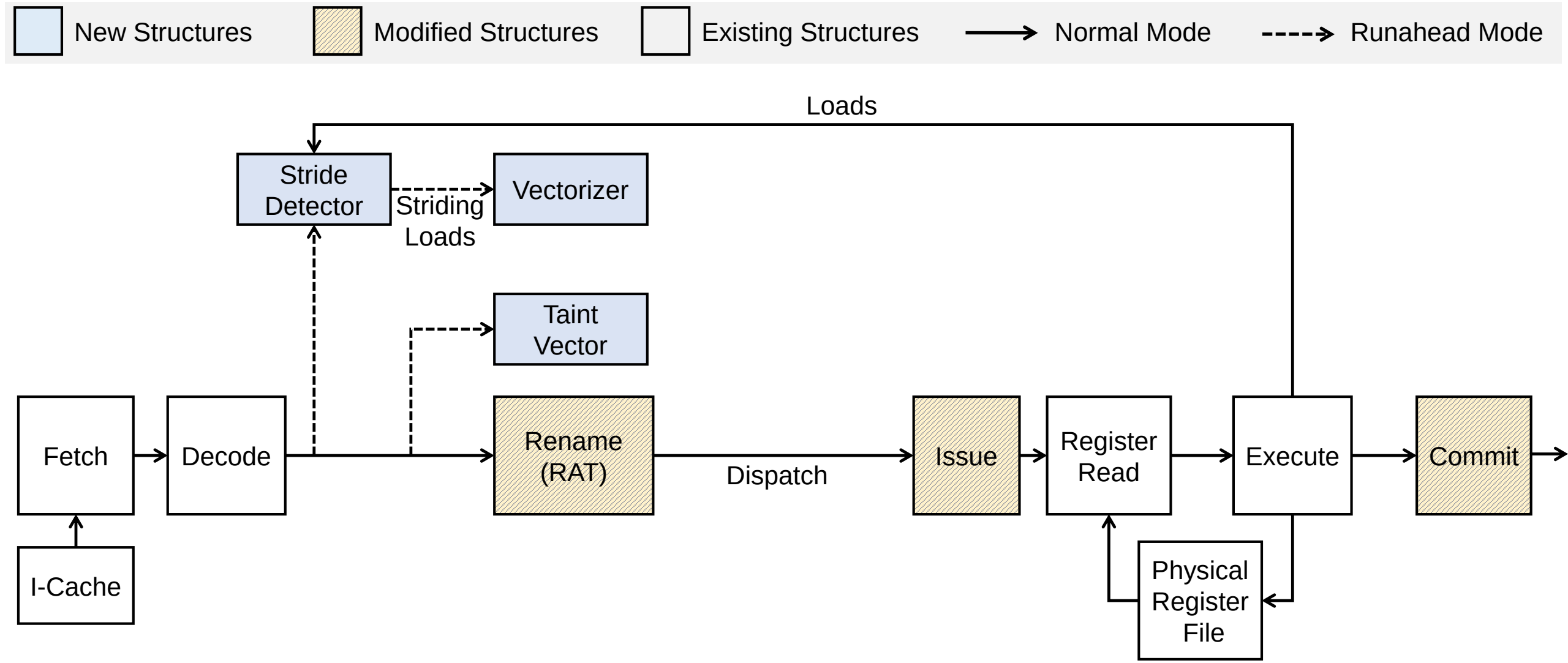

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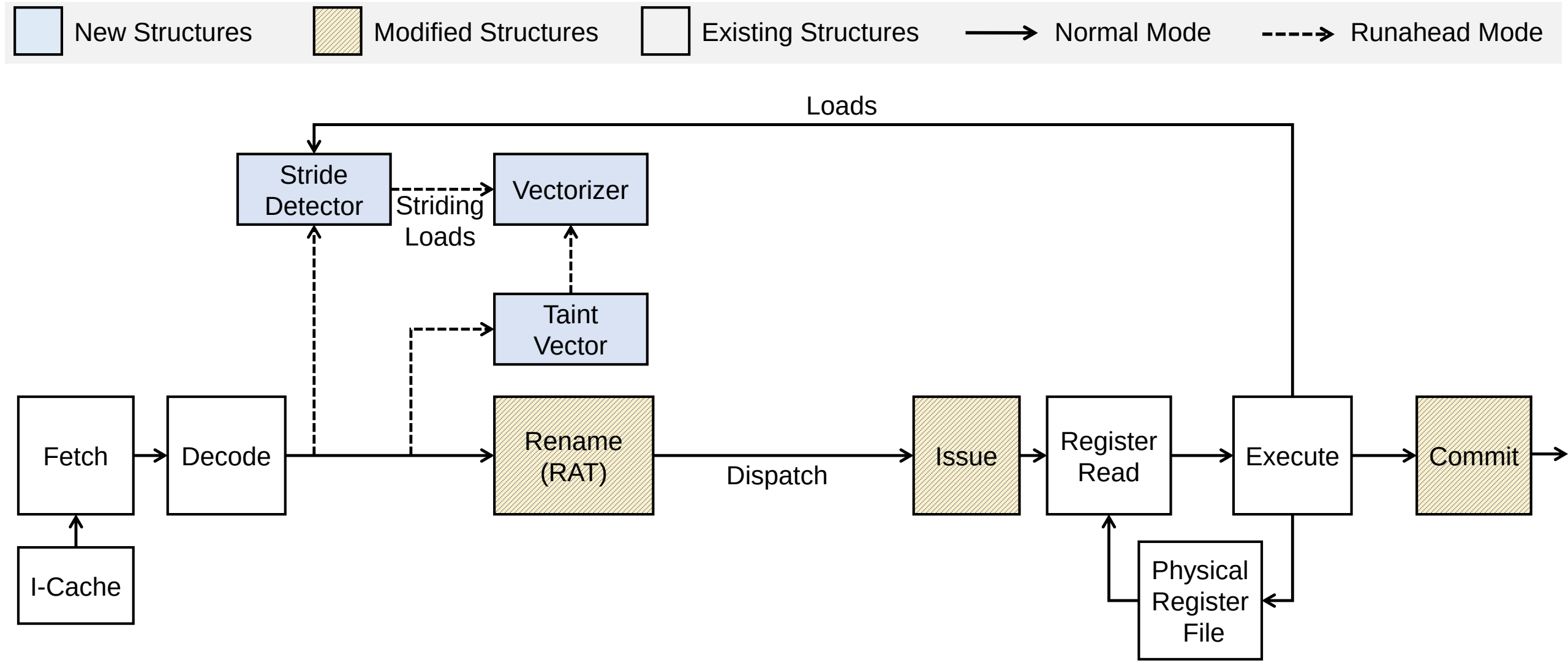

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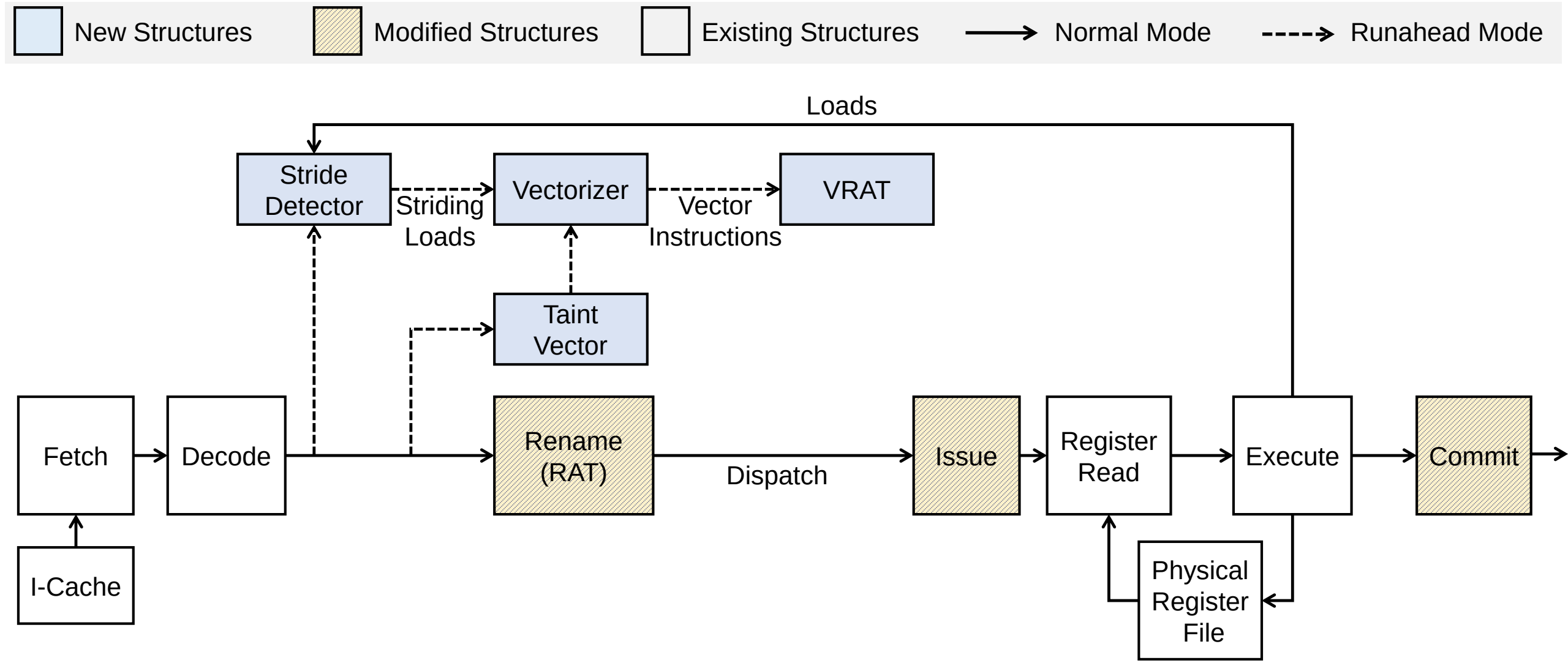

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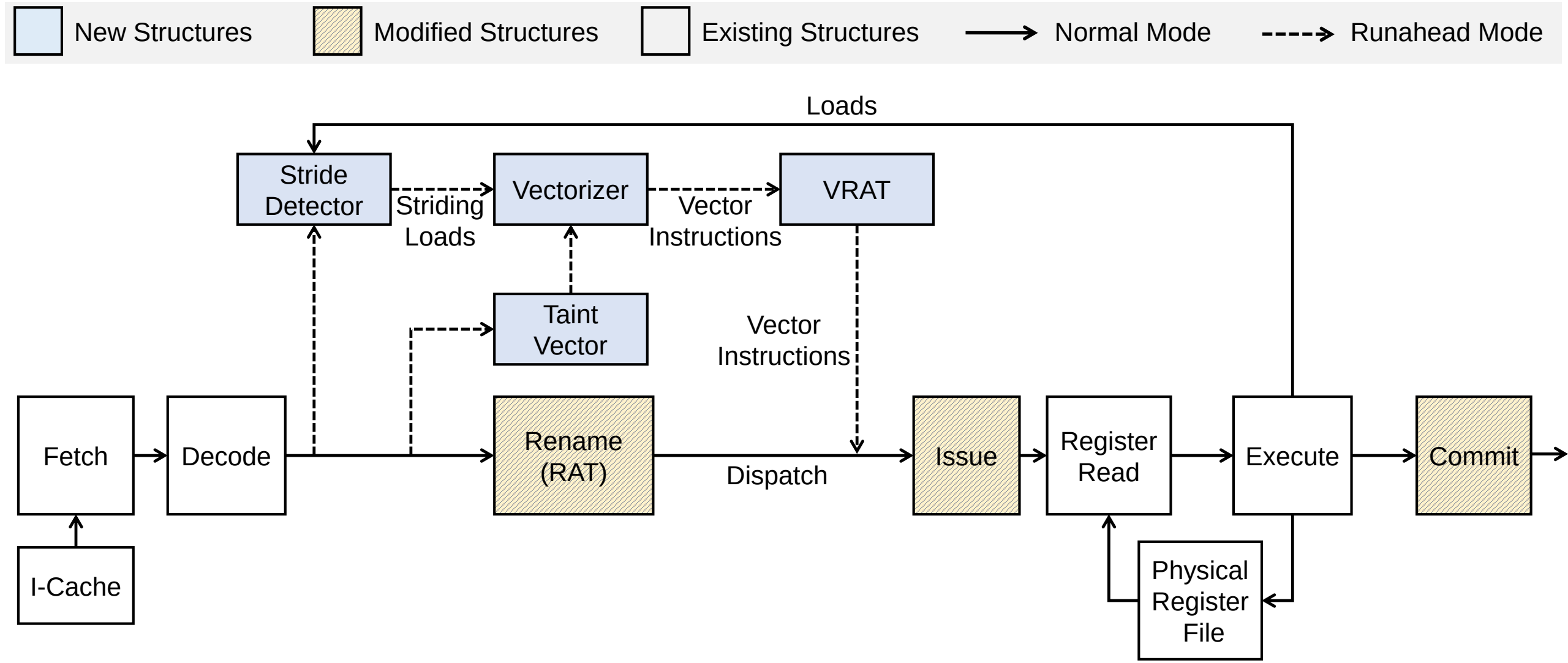

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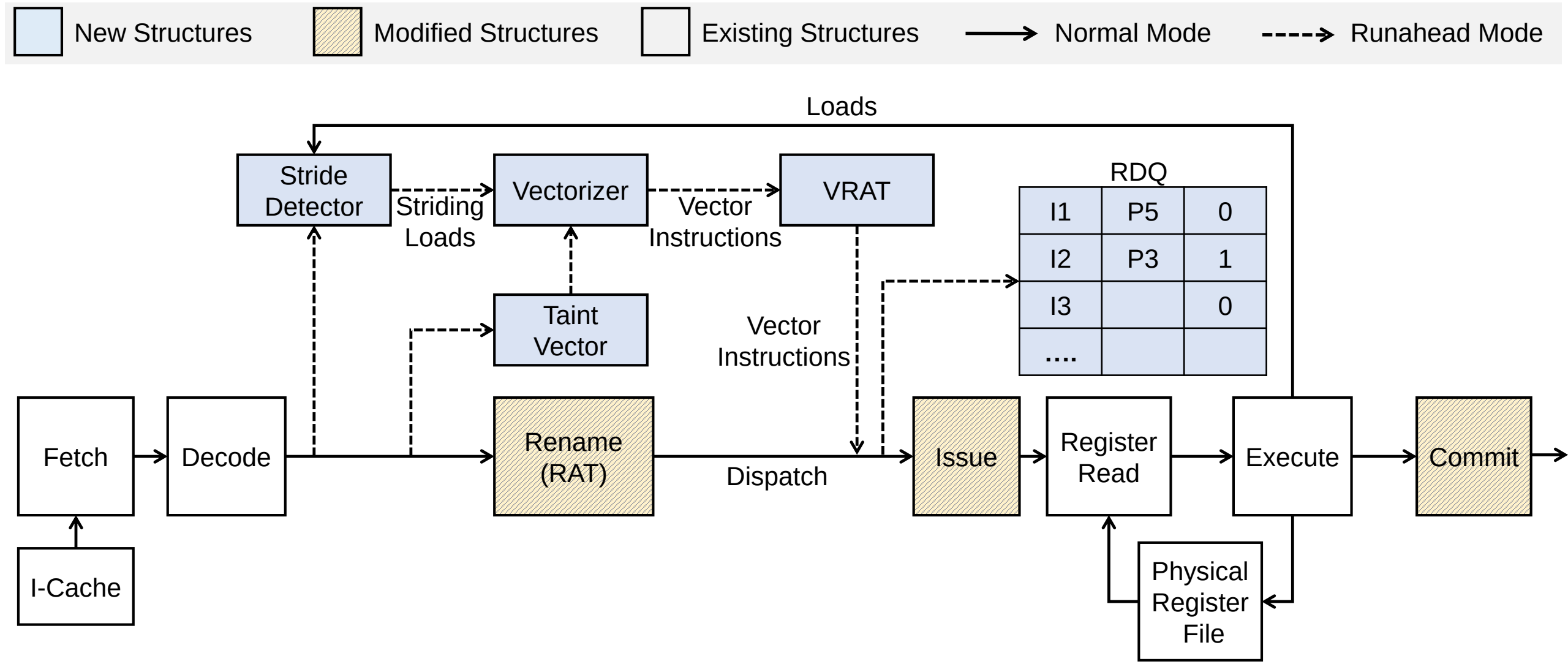

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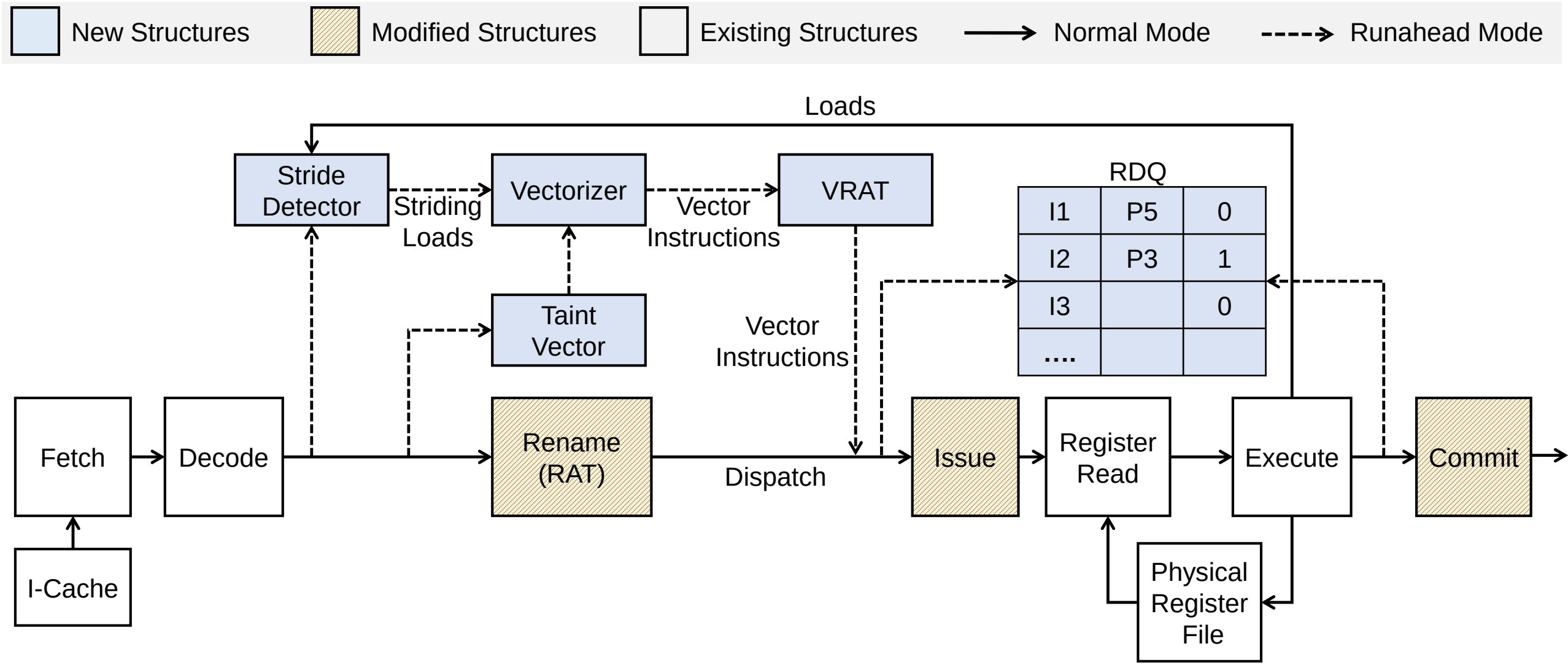

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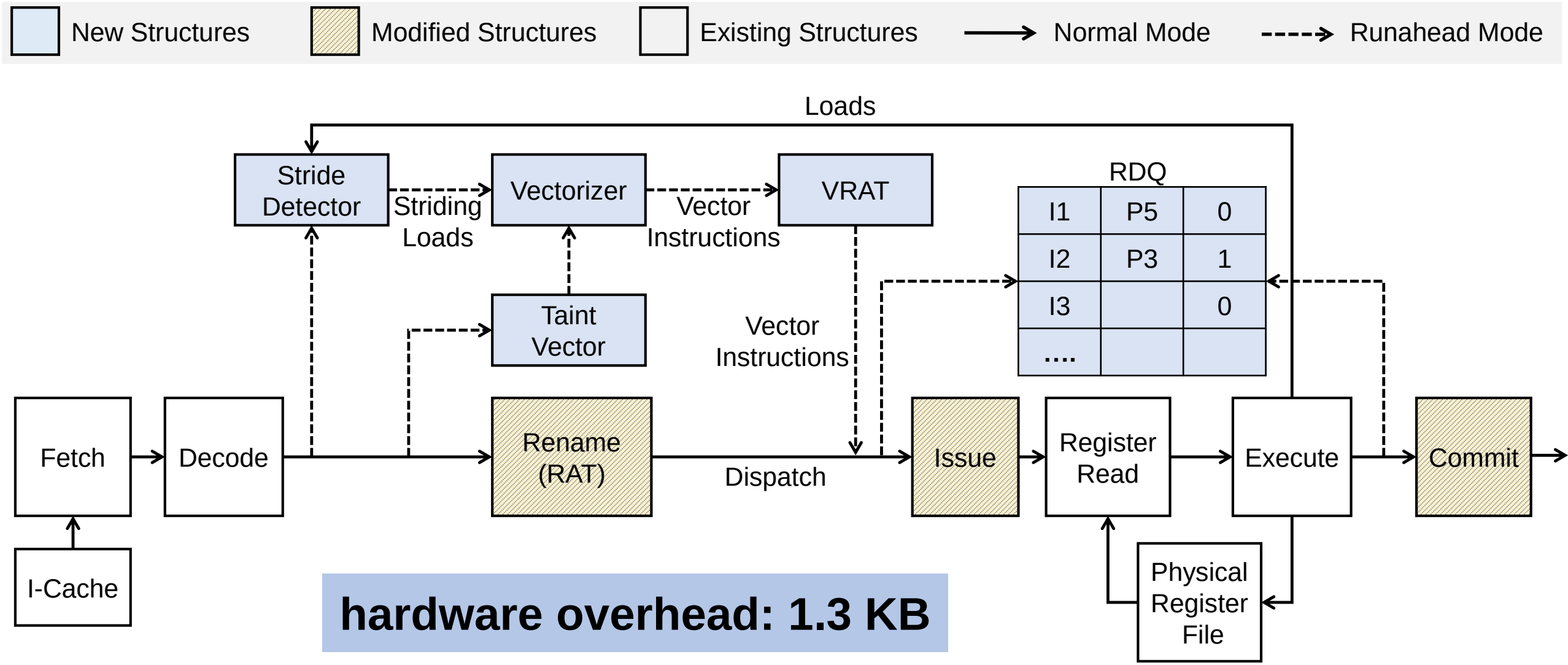

Evaluation

Simulator: Sniper 6.0

Baseline: 3.2 GHz OoO, ROB=224, issue queue=97,
load queue=64, store queue=60, register file: 180 int, 96 vector

Workloads: Benchmarks with complex memory indirection patterns from HPC, graph analytics, and database domains

Aggressive stride prefetcher with 16 streams, MSHR=24

Evaluation

OoO: Baseline out-of-order core

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PRE: Precise runahead execution*

-- Ideal stalling slice table

*[Naithani et al. HPCA'20]

Evaluation

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PRE: Precise runahead execution*

-- Ideal stalling slice table

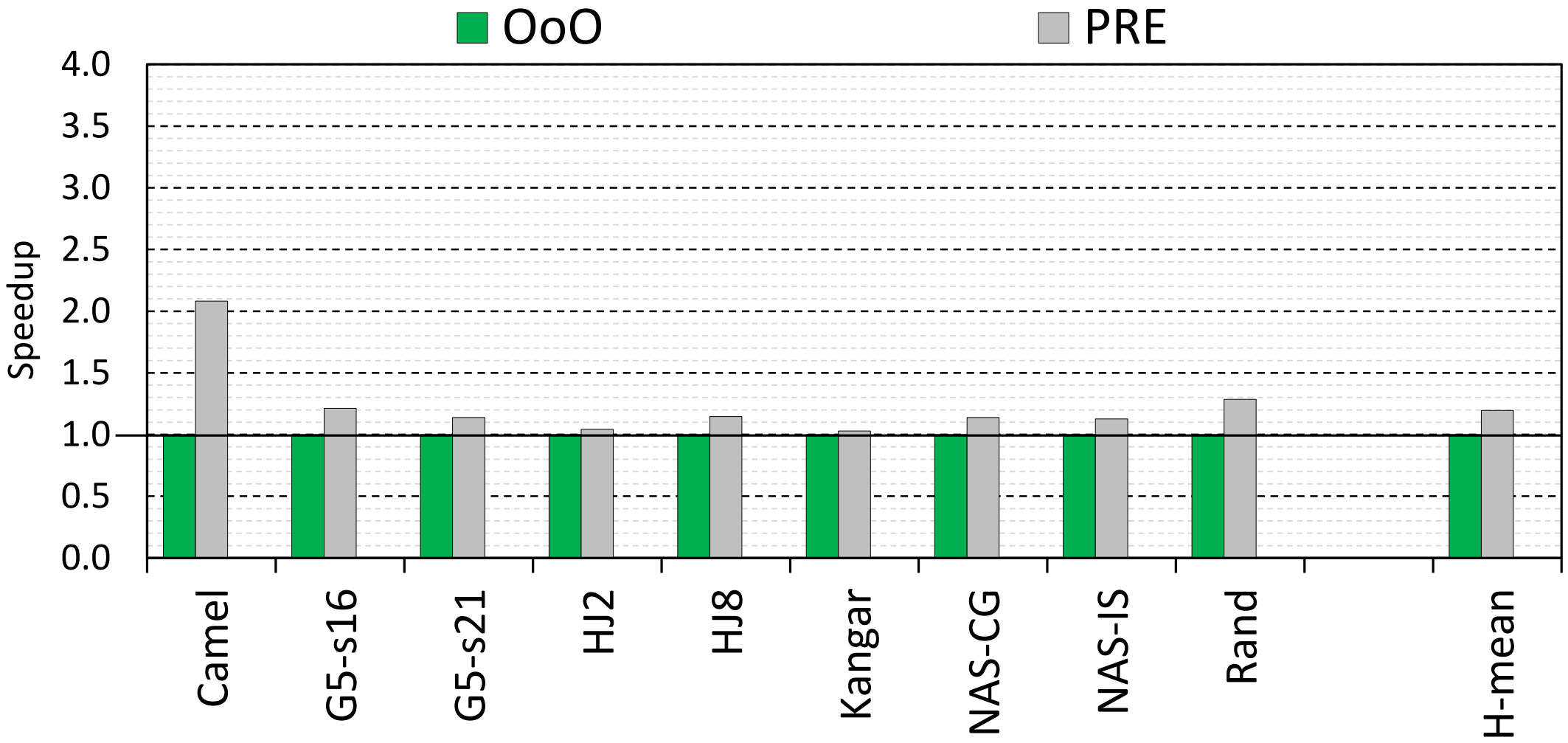
VR: Vector Runahead**

-- Pipelined version: Simultaneously issue eight vector instructions for each scalar instruction

*[Naithani et al. HPCA'20]

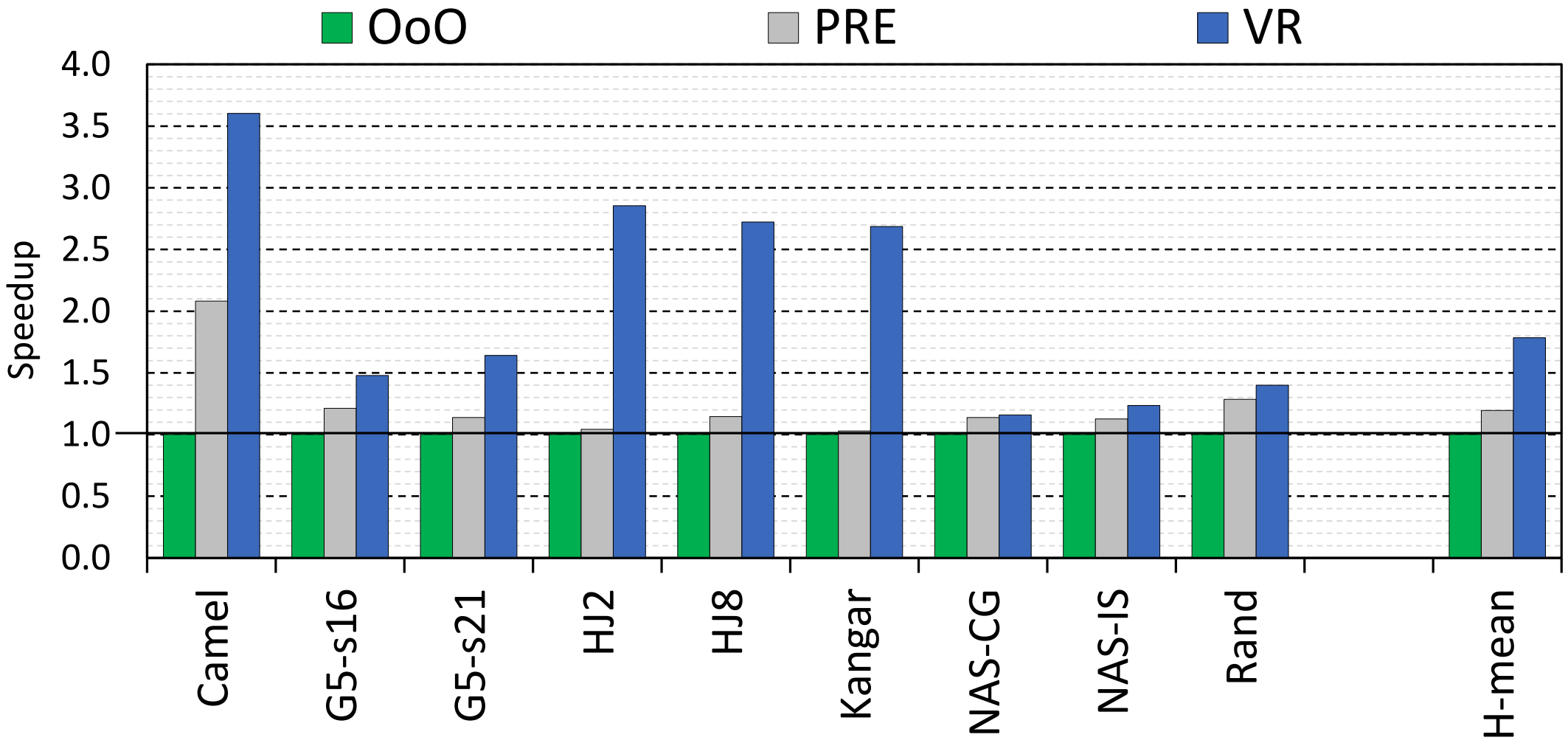
**[Naithani et al. ISCA'21]

Evaluation – Performance



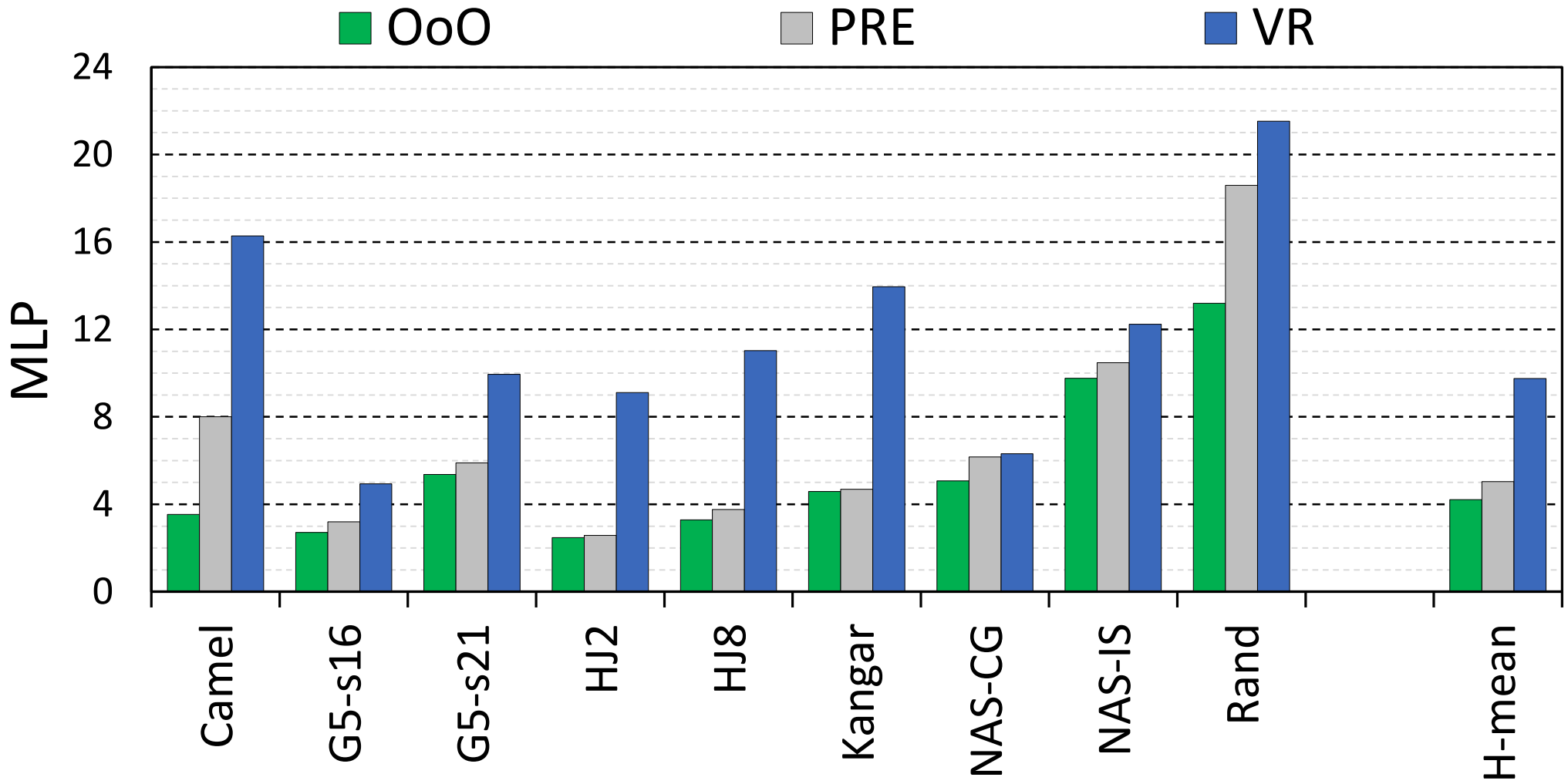
PRE: 1.20x

Evaluation – Performance



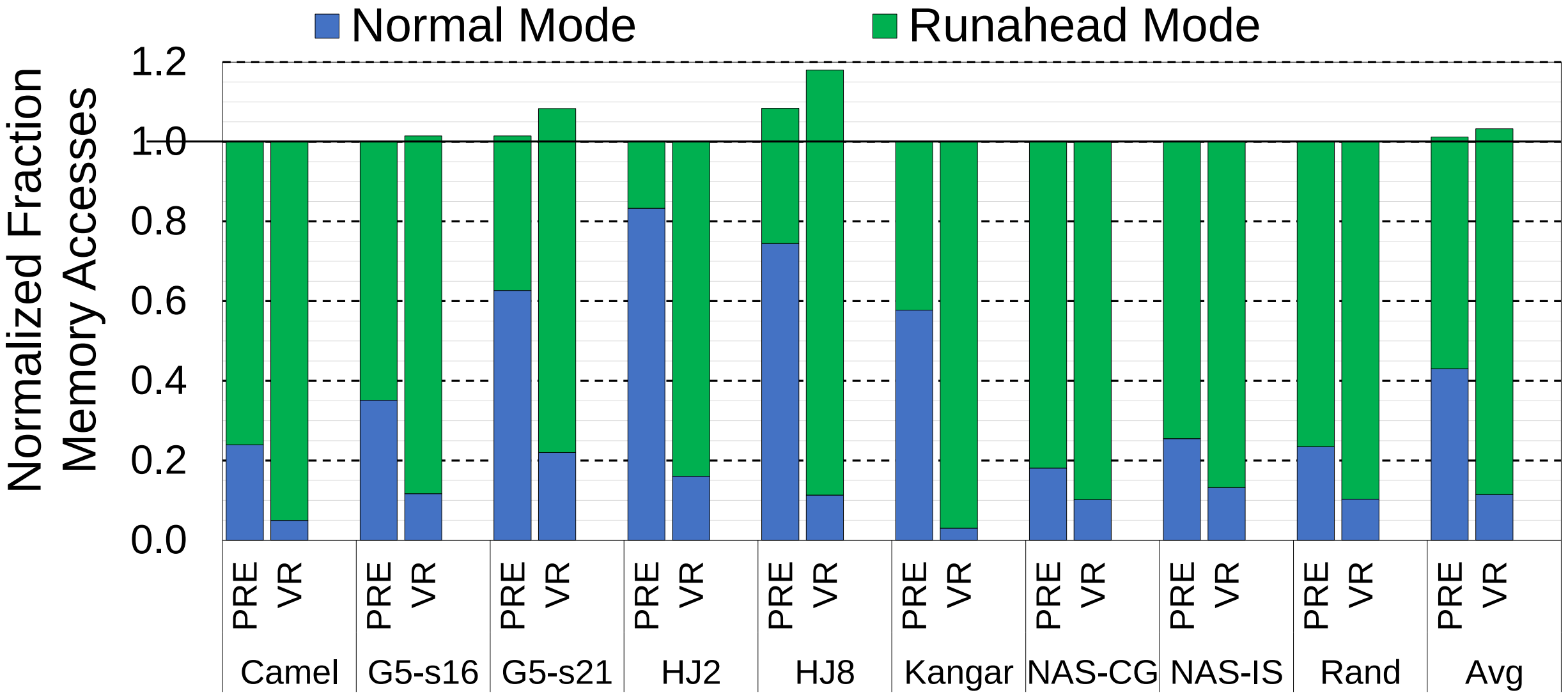
PRE: 1.20x **VR: 1.79x**

Evaluation – Memory-Level Parallelism



OoO: 4.2 **PRE: 5** **VR: 9.8**

Prefetching Coverage



Prefetching Accuracy and Timeliness

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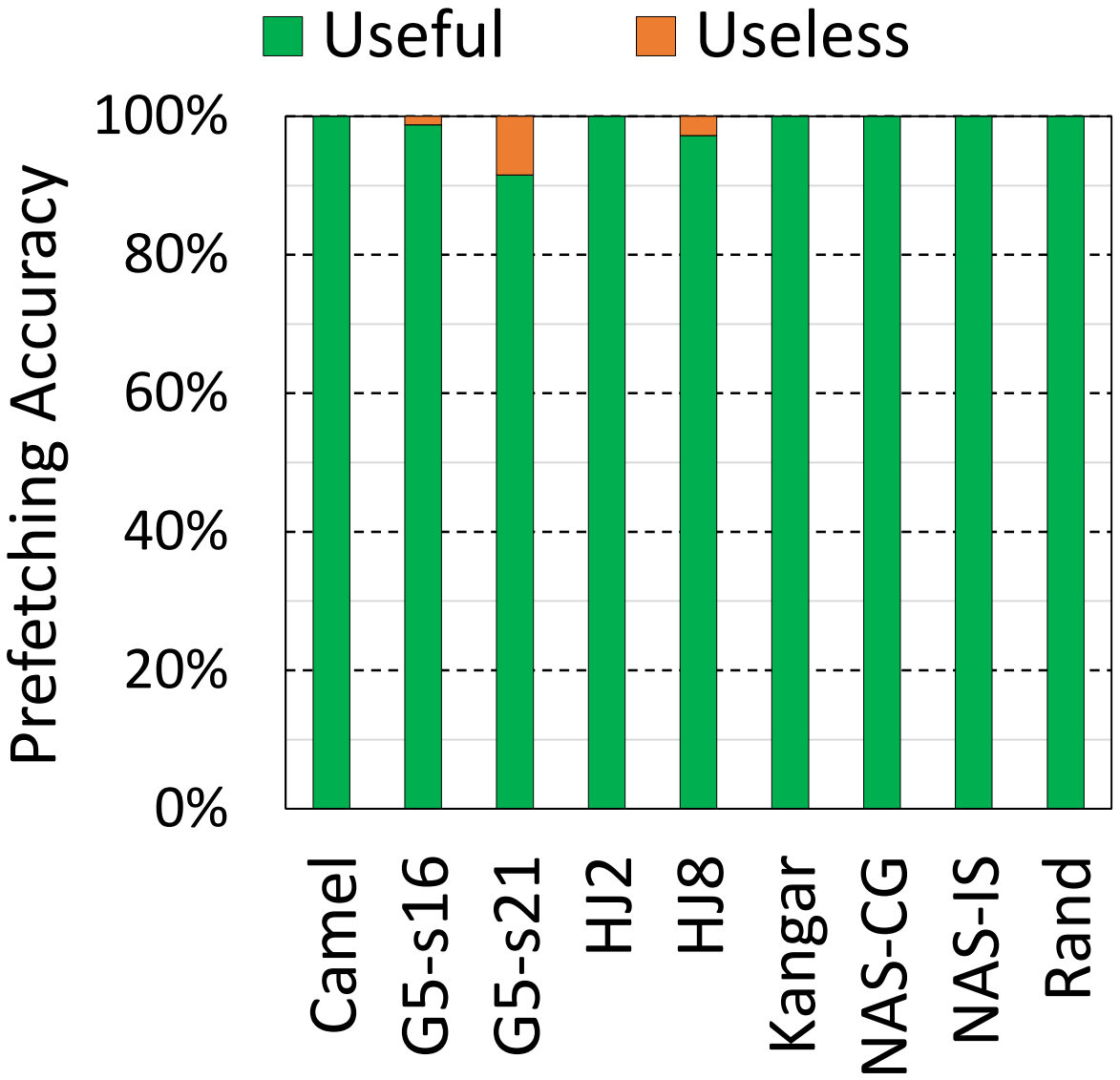

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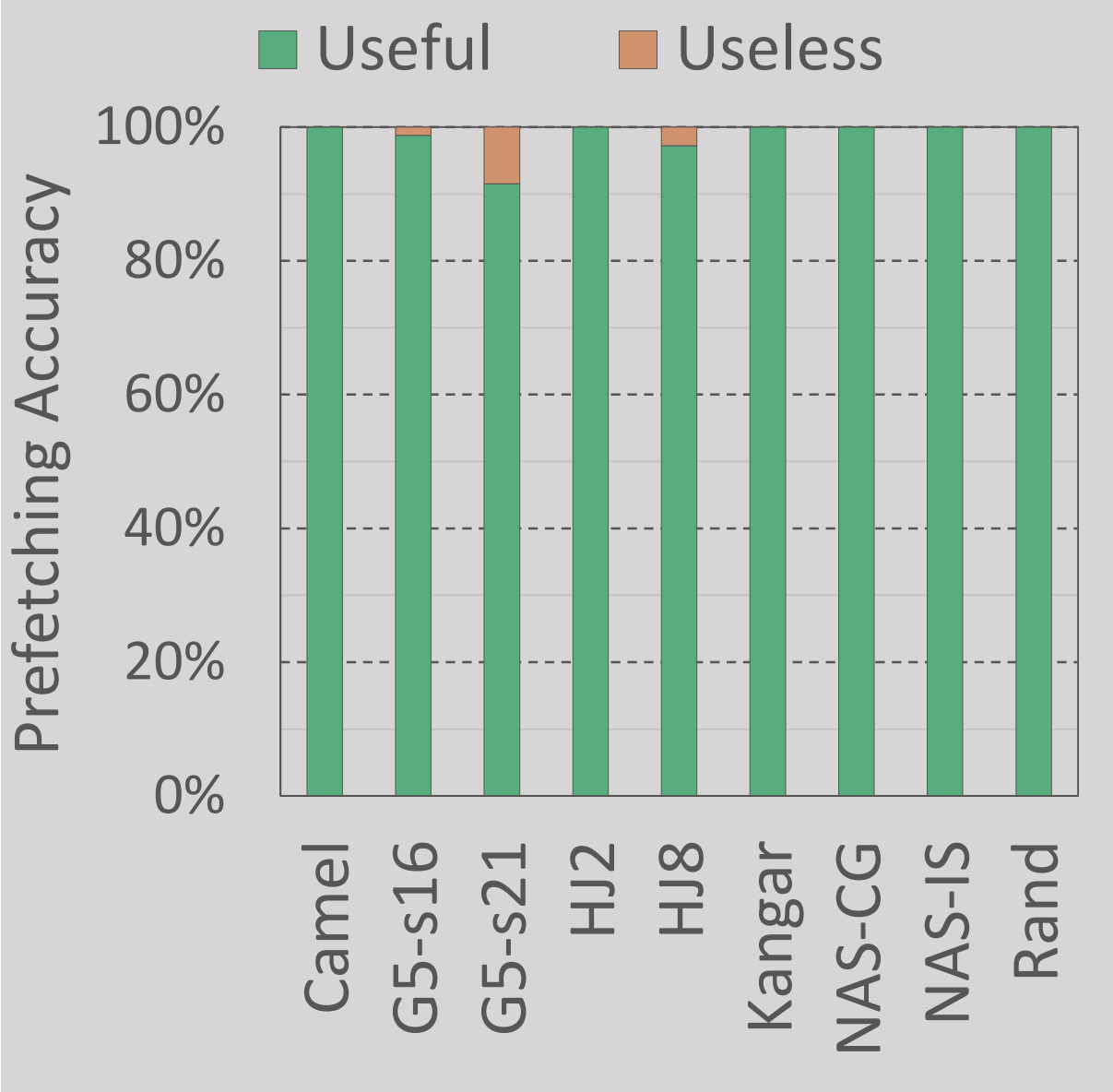

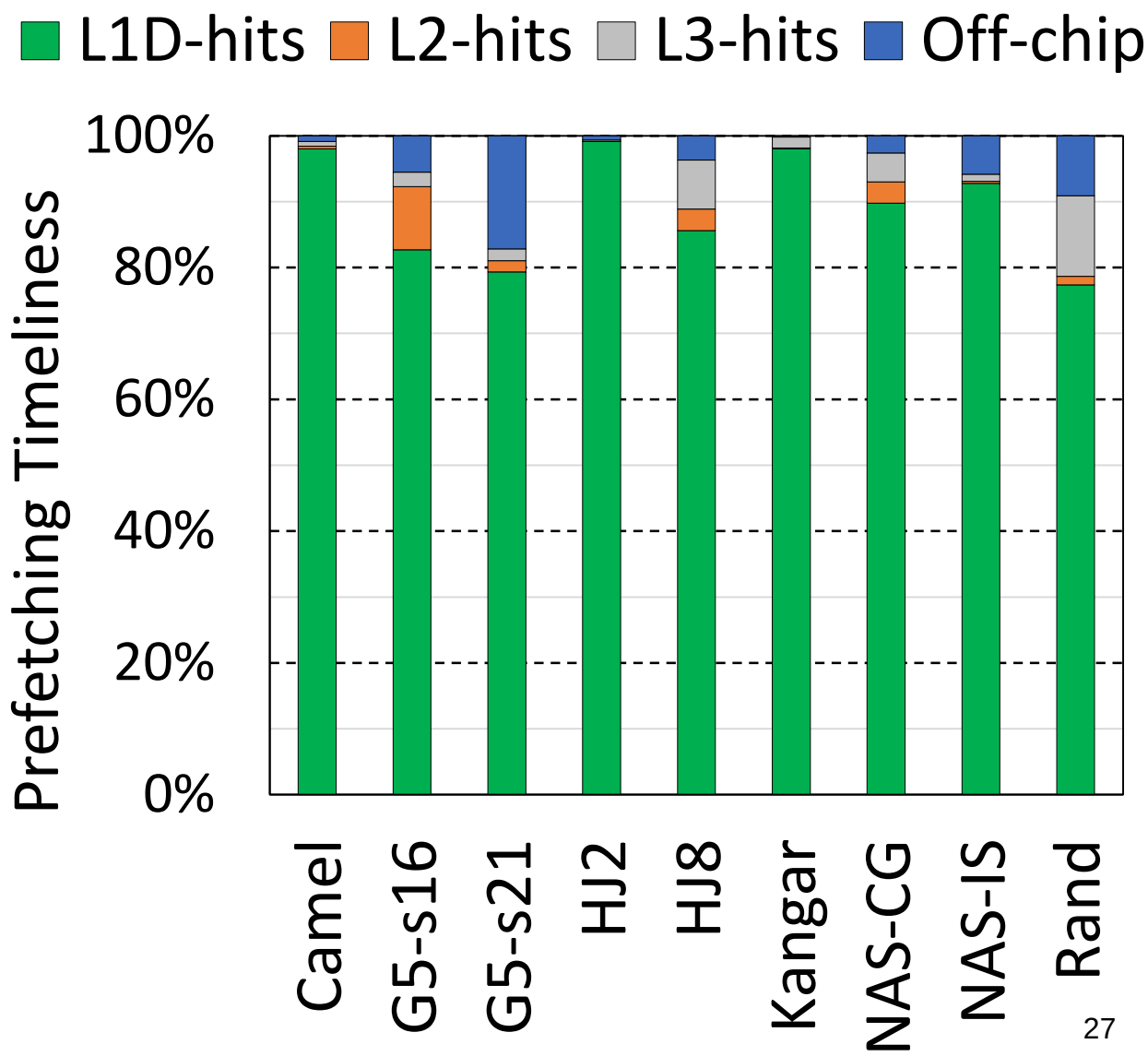

Evaluation – In the Paper

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1. Indirect Memory Prefetcher
   -- IMP 1.19x versus Vector Runahead: 1.79x
   -- Works only for simple single-level indirects

MICRO 2015

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2. Unrolling and pipelining

MICRO 2015

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MICRO 2015

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3. Varying LLC size: Vector Runahead equally effective

4. Varying MSHR entries
   -- Sufficient MSHRs needed for VR's extreme level of MLP

Conclusions

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2. Vector Runahead = Reordered loads + speculative vectorization + delayed termination

3. Increases effective fetch/decode bandwidth

1.79x higher performance by 2.3x higher MLP

Vector Runahead

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Sam Ainsworth (Edinburgh)
Timothy M. Jones (Cambridge)
Lieven Eeckhout (Ghent)

THE UNIVERSITY *of* EDINBURGH

UNIVERSITY OF CAMBRIDGE