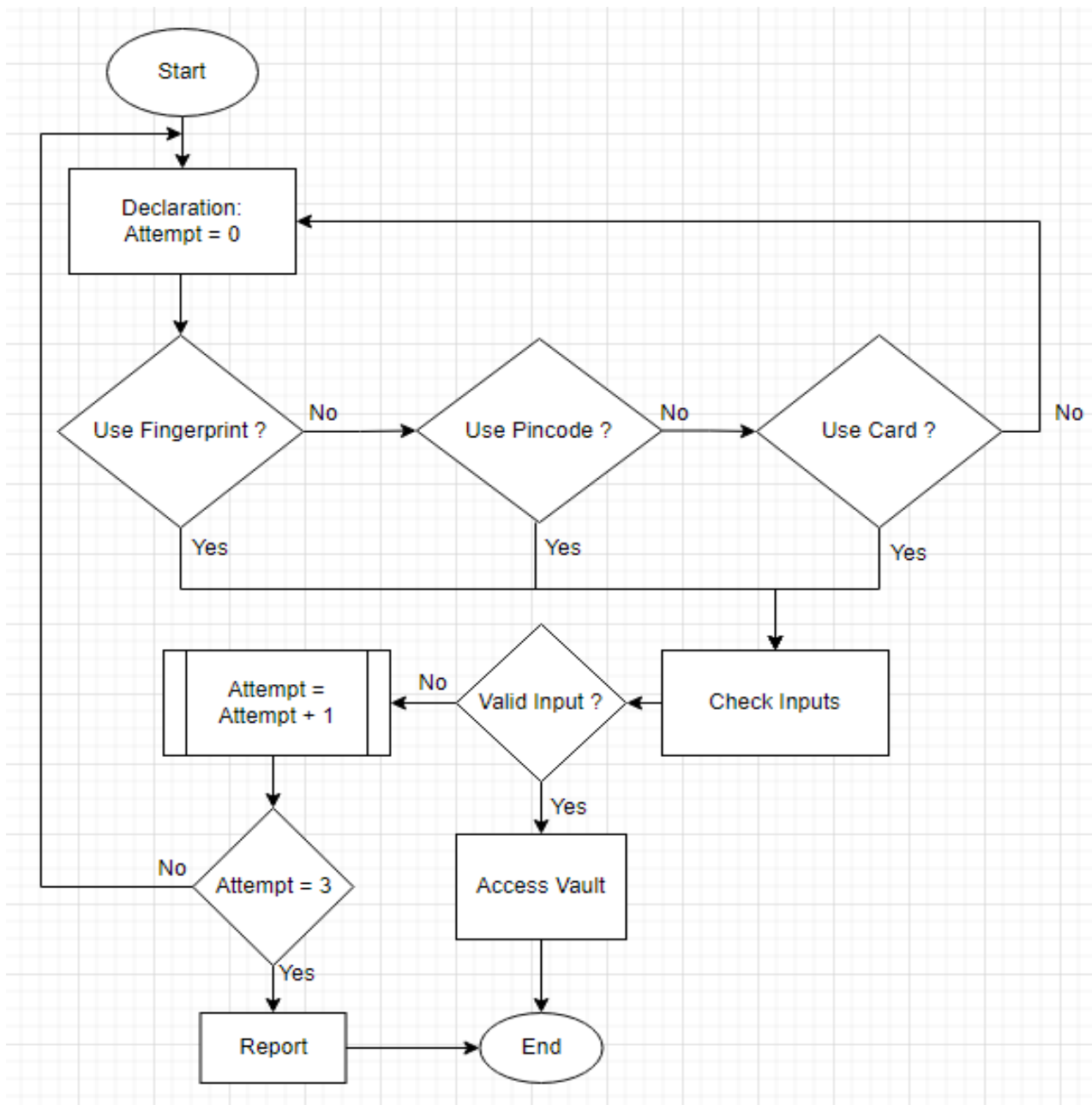


## MIDTERM EXAM (Group 2)

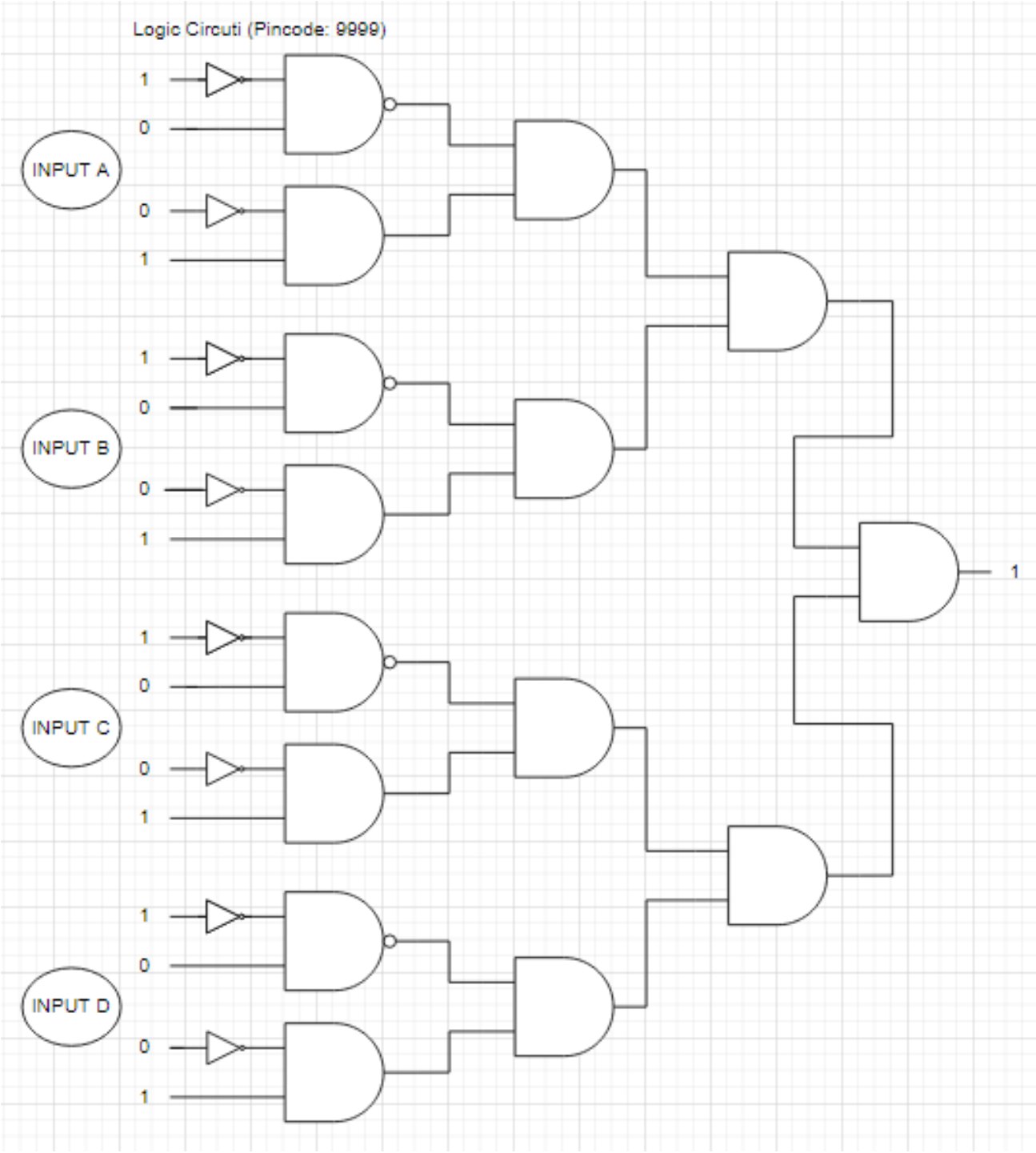
- Manuel, Leomhar
- Monacillo, Sean David Christopher
- Narag, Avor John
- Rilan, Michael Angelo
- Salvador, Nigelle Jarred

### Test 1: Illustration (20 points)

Flowchart Diagram



Logic Circuit Diagram



## Test II. Mapping

Addresses in Hex		Uses
FFFF E000	ROM	SYSTEM PROGRAM
DFFF D800	RAM	VIDEO RAM
D7FF 4000	UNUSED	
3FFF 0400	RAM	USER RAM
03FF 0000	RAM	FAST INSTRUCTIONS

**Test 3: Programming (40 points)**

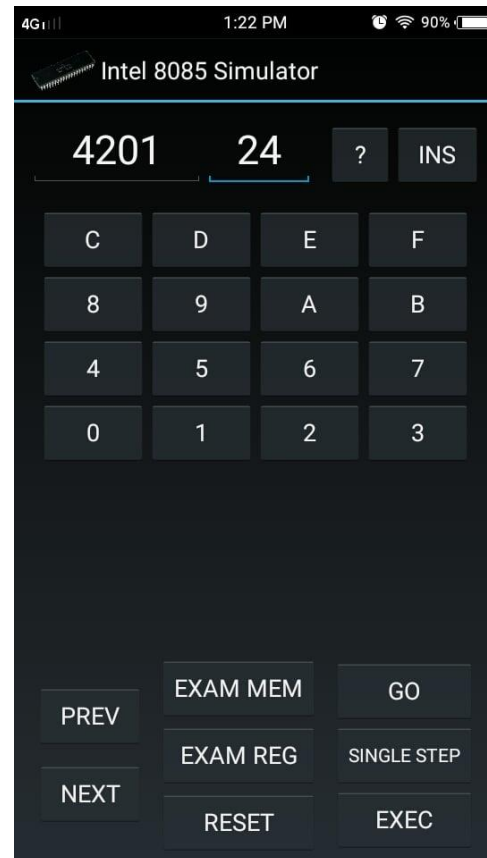
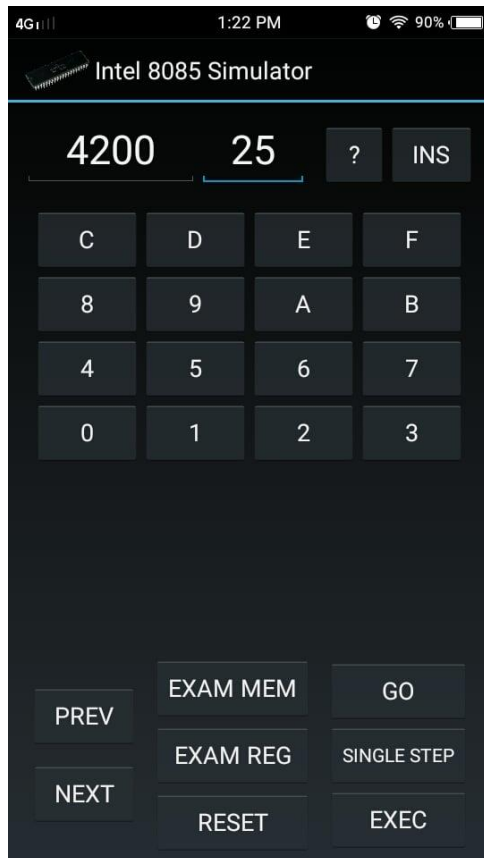
<b>ADDRESS</b>	<b>OPCODE</b>
4100	0E
4101	00
4102	21
4103	00
4104	42
4105	7E
4106	23
4107	86
4108	D2
4109	0C
410A	41
410B	0C
410C	23
410D	77
410E	23
410F	71
4110	21
4111	00
4112	42
4113	7E
4114	23
4115	46

4116	90
4117	D2
4118	1B
4119	41
411A	0C
411B	21
411C	04
411D	42
411E	77
411F	23
4120	71
4121	76

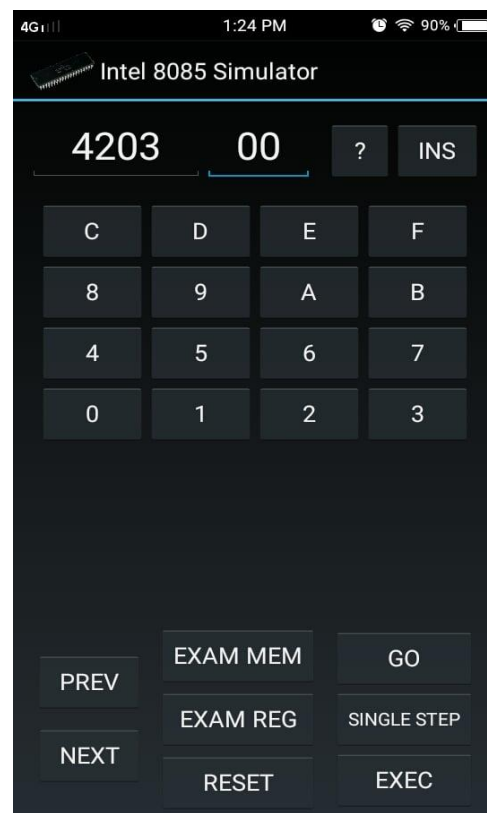
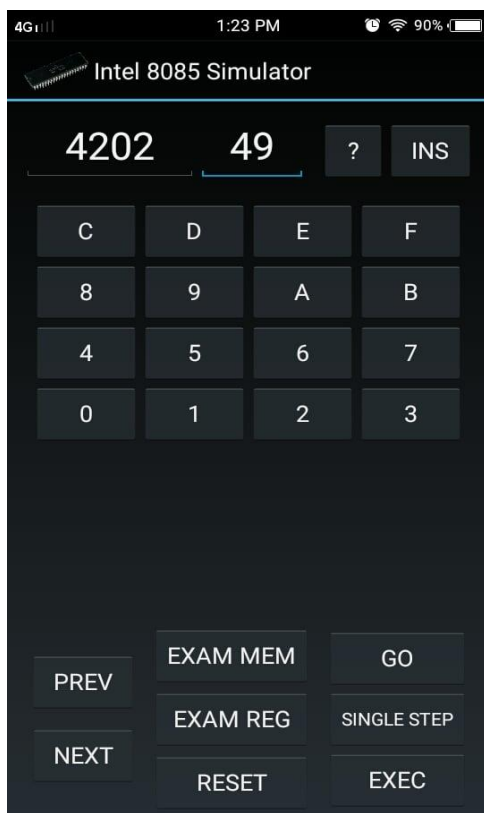
in		out	
4200	25	4202	49
4201	24	4203	00
		4204	01
		4205	00

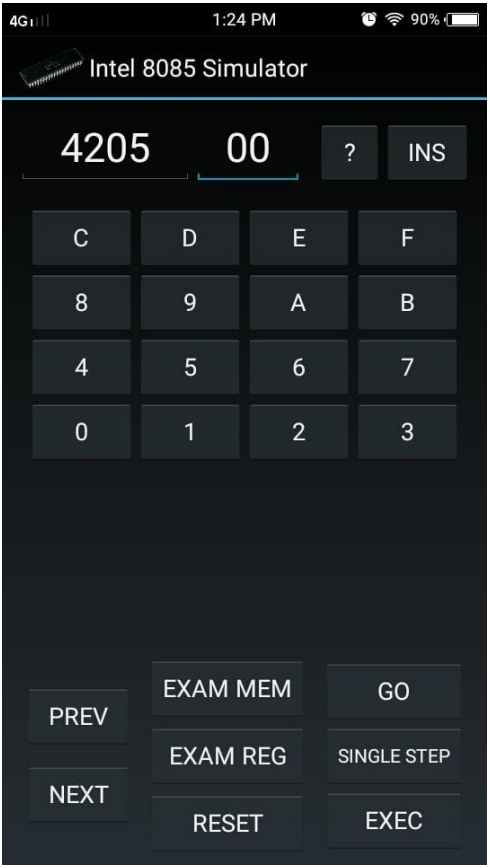
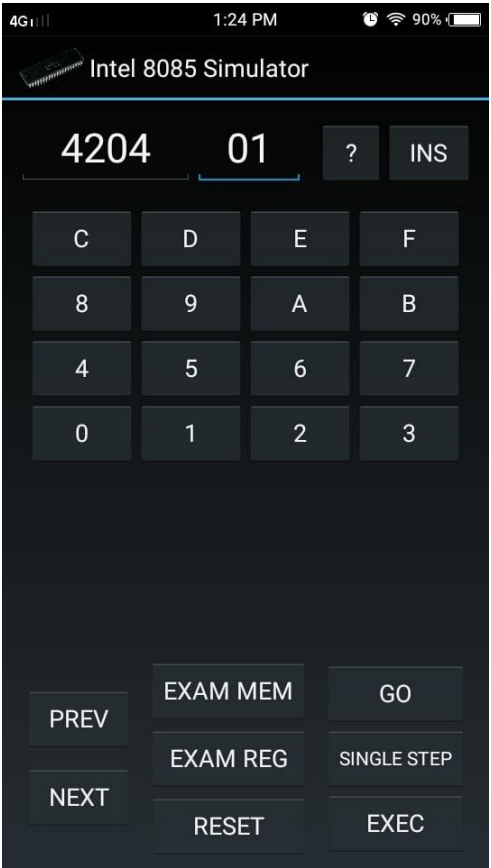
## Screenshots:

In



Out





## Test IV. Addressing

- (a) 512bytes memory chip would have 9 address lines plus the three inputs for decoder chip resulting to 4 unused lines since the data will be stored in 16-bit address 6000H.  
 $2^4 = 16$  image addresses
- (b) The image addresses are: 6000, 6200, 6400, 6600, 6800, 6A00, 6C00, 6E00, 7000, 7200, 7400, 7600, 7800, 7A00, 7C00, 7E00

Table



[illegible]