United International University
Department of Computer Science and Engineering

CSE 313: Computer Architecture

Final Examination, Summer 19 Time: 2 Hours

N.B.Answer all the questions

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1. (a) Consider the block diagram for single-cycle datapath. Point out whether each circuit element is combinational or sequential. Write in your answer script. [2]

   (b) Write down the values of the following control signals for the instruction [2]
   bne $so, $s1, L

   1. RegDst
   2. MemtoReg
   3. ALUSrc
   4. branch

   (c) Modify the block diagram for single-cycle datapath that you have been provided so that it can execute the following instruction. Note that, this instruction writes the memory address (the address, not the value) calculated using given base, $s0 and offset, 4 (format same as load/store) into the register specified as the first operand, $t0. [3]

```
wa $t0, 4($s0)
```

2. Suppose you want to design a processor datapath. You have come up with an idea for a datapath that goes through the following six stages for executing an instruction given with the time required to complete each stage in ps. Note that symbols follow convention. Your friend Ron Weasley has suggested you a single-cycle design. You have successfully implemented that.

IF	ID	RR	EXE	MEM	WB
200	50	75	175	200	100

Table 1: Pipeline Stages

Now answer the following questions.

(a) What will be the execution time of the given code using your implementation? [2]

```
addi $s0, $0, 50
add $s1, $0, $0
loop:
beq $s0, $0, exit
add $s1, $s1, $so
addi $s0, $s0, -1
j loop
exit:
```

(b) What should be the clock period and clock frequency of the processor that employs your design? [2]

(c) Suppose another friend of yours, Hermione Granger, is not happy with the design. She has read about pipelining and is forcing you to implement pipelining in your processor. You have implemented that. Ron always argues with Hermione. He has come up with the following code that poses some challenges to pipelining. What challenge is he talking about? What will be the runtime of the code? Show with timing diagram. [3]

```
add $t0, $s2, $s1
sw $t0, 4($s0)
lw $t2, 8($s0)
sub $t1, $t2, $s1
addi $t3, $t4, 2
```

(d) Hermione laughs at Ron and says that she has a solution to the challenge. She starts teaching you the technique of forwarding. You then implement forwarding into your processor. What will be the runtime of the code in part (c) now? [3]

(e) Ron doesn't give up so easily. He says that the runtime is still not optimal. Luna Lovegood, a maverick friend of yours, now teaches you a technique that will be able to make the runtime optimal. What is the technique? Can you show the use of the technique to make runtime of the code in part (c) optimal? [2]

(f) Luna now has a basic question for you. Do you ever face the challenge you faced in part (c) in single-cycle design? Why or why not? [2]

3. Now that you are done with designing processor, you start designing cache. You have read about direct-mapped cache and decide to implement that. You have decided to design 1 KB cache and your block size is 2 words. Consider that your main memory is byte-addressable and each memory address consists of 32 bits.

(a) How many blocks are there in your cache? [1]

(b) Find the hit rate if you access following memory addresses in the given order. Assume that the cache is initially empty. [4]
6, 11, 31, 1027, 5, 1032, 12, 4

(c) Find the number of offset and tag bits. [1]

(d) Hermione again interferes. She claims that if you expand your block size to 8 words, you will have reduced miss rate than that obtained in part (b). Ron doesn't think so. Find out whether Ron or Hermione is right. [4]

(e) Why is s/he right? Which principle of locality is responsible in this case? [1]

(f) Slytherins use 8 GB memory and their memory is word-addressable. Is their memory size greater than the memory you use? If they use your cache, find out the number of tag bits. [2]

4. Consider the following code. We will parallelize only the nested loop part in this code.

```
int f=a+b-c*d/e;
for(int i=0;i<x;i++){
    for(int j=y;j>0;j--){
        for(int k=0;k<z*z;k++)
            pro*=A[i][j][k];
    }
}
```

(a) Consider that time for a single arithmetic operation is 1 ns. Find the speedup with respect to runtime of the given code for octa-core vs unicore processor system for x=10, y=10 and z=10. [2]

(b) Find the speedup with similar conditions for x=5, y=5 and z=5. [2]

(c) Compare the speedups obtained in part (a) and part (b). What conclusion can you draw? [2]