United International University
Department of CSE
CSE 313: Computer Architecture
Final Examination
Spring 2022

Time: 2 Hours **Full Marks: 40**

Any examinee found adopting unfair means will be expelled from the trimester / program as per UIU disciplinary rules.

[N.B.: Answer all the questions. Assume any data if it is not mentioned explicitly.]

<table>
<tr><td>1.</td><td>a) Modify the block diagram for single-cycle datapath so that it can execute the following instruction “mtr”. Note that, this instruction saves value from an address [address = offset (20) + base ($s0)] onto a temporary register ($t0) .
mtr $t0, 20($s0)
Also write down the control unit values for this instruction.</td><td>[5]</td></tr>
<tr><td></td><td>b) Modify the block diagram for single-cycle datapath so that it can execute the following instructions “jst”. Note that, the job of the given instruction is to save a function address in the PC register and also to save the address of the second next instruction in the $ra register.
jst 1024
Also write down the control unit values for these instructions.</td><td>[5]</td></tr>
<tr><td></td><td>c) What is the use of the PC register in the given block diagram for single-cycle datapath? What are the possible values of the PC register after executing an I- Type instruction? Explain.</td><td>[3]</td></tr>
<tr><td>2.</td><td>Consider a processor that goes through the following six stages while executing an instruction. The duration of each stage (in ps) is given underneath it:
<table>
<tr><td>Instruction Fetch</td><td>Instruction Decode</td><td>Register Read</td><td>ALU Operation</td><td>Memory Access</td><td>Register Write</td></tr>
<tr><td>250</td><td>50</td><td>150</td><td>300</td><td>250</td><td>150</td></tr>
</table>
Also consider the following instruction snippet:
add $s0, $s1, $s2
add $s1, $s2, $s3
sub $t0, $s0, $s1
lw $t2, 20($t1)
add $s4, $t2, $t2
Now answer the following questions:</td><td></td></tr>
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<table>
<tr><td></td><td>a) If basic pipelining is implemented in your processor, how many times faster will the instruction snippet execute (i.e., the speedup factor) compared to a single-cycle implementation? There is no need to include a timing diagram in your answer.</td><td>[5]</td></tr>
<tr><td></td><td>b) Suggest a hardware change that you can implement in your processor to improve the execution time of the instruction snippet. What would be the execution time after this change? Include a timing diagram in your answer.</td><td>[5]</td></tr>
<tr><td></td><td>c) Explain how an optimized compiler can improve the execution time of the instruction snippet further. In your answer, clearly show any changes that might be brought in the given instruction snippet.</td><td>[3]</td></tr>
<tr><td></td><td>d) Suppose you have split the “Memory Access” stage into two separate stages – “Memory Read” and “Memory Write.” Explain why this may cause the processor to stall more.</td><td>[2]</td></tr>
<tr><td>3.</td><td>a) Consider a cache memory of size 2KB and block size having 8 words (1 word = 4 bytes). Determine the miss rate if the following bytes are addressed sequentially.

15, 19, 4097, 4098, 7, 30</td><td>[5]</td></tr>
<tr><td></td><td>b) If we change the block size in Q3(a) to 4 words, find out the miss rate for similar memory address access. Find out the miss rate and explain the principle of locality.</td><td>[5]</td></tr>
<tr><td></td><td>c) Find the number of blocks in the cache and bytes per block for the following example.

<table><tr><td>Tag</td><td>Index</td><td>Offset</td></tr><tr><td>31-13</td><td>12-6</td><td>5-0</td></tr></table></td><td>[2]</td></tr>
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