United International University
Department of Computer Science and Engineering

CSE 313: Computer Architecture

Final Examination Set: A Time: 2 Hours

Instruction: Right side of the page contains the Marks of the questions.
Answer all the parts of the same question together

1. (a) Convert the Decimal Floating Point number 58.75×10^{26} to IEEE 754 standard Single Precision format. Clearly mention size of each part. Use six bit precision for fraction part. [3]

   (b) Write down the IEEE 754 representation of `+Infinity` [1]

   (c) Show a step by step simulation for adding the two Binary Floating Point Number $1.0001101 \times 2^{(110)_2}$ and $100.10011 \times 2^{(100)_2}$ using Floating Point Addition algorithm. Clearly mention name of each step. [4]

   (d) Draw only the components which are used for the Alignment step of Floating Point Addition given at Figure 1:Floating Point Adder [2]

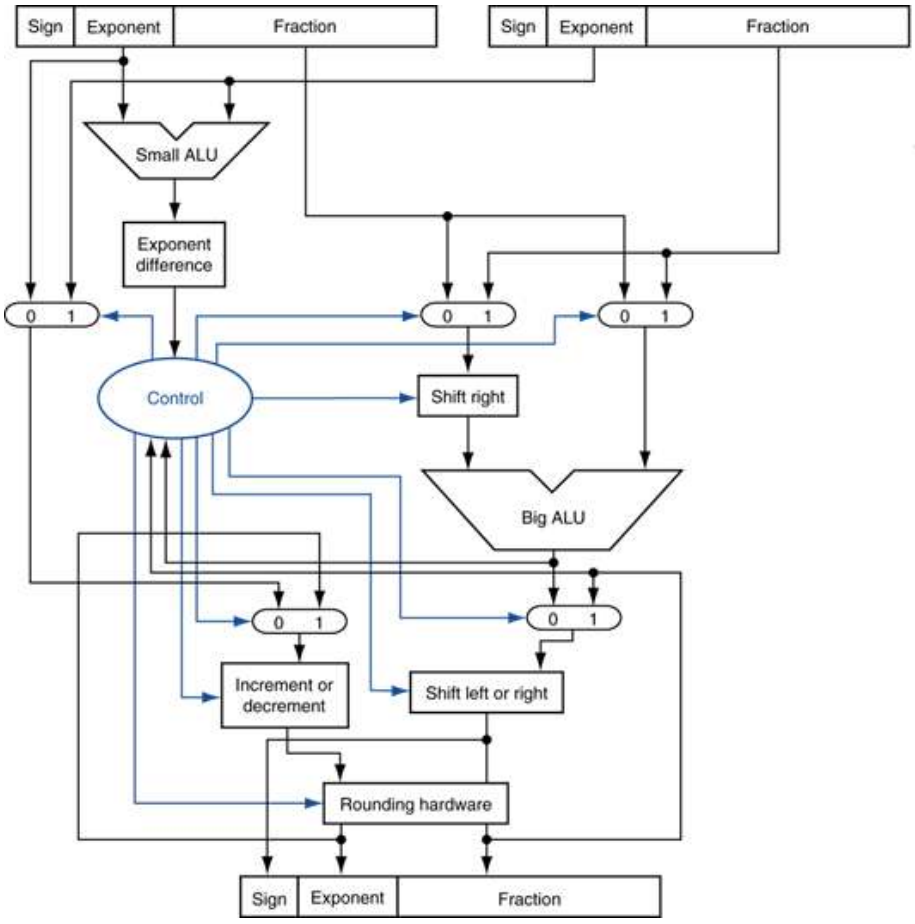

Figure 1: Floating Point Adder

2. Answer any 3 (Three) questions from 2(a)- 2(e)

   (a) Write down the value of the following Control Signals for the instruction `sub $5, $6, $7` [2]
   i) RegWrite, ii) MemWrite, iii) Branch, iv) Zero

(b) Define Sequential and Combinational Logic elements. Give one example of each type. [2]

(c) Write down the function of the following components for MIPS processor - [2]
i) PC register, ii) Instruction Memory iii) Data Memory iv) Multiplexer

(d) Write down whether the following components are Sequential or Combinational - [2]
i) Big ALU, ii) JK Flip Flop, iii) DRAM, iv) SR Latch,
v) Shifter, vi) Half Adder, vii) Program Counter, vii) Cache Memory

(e) Write down the timing diagram for a D flipflop. [2]

3. Draw only the active Datapath for the following instruction `beq $4, $5, 100` [4]
Use the figure at Figure 2:Full Datapath for reference.

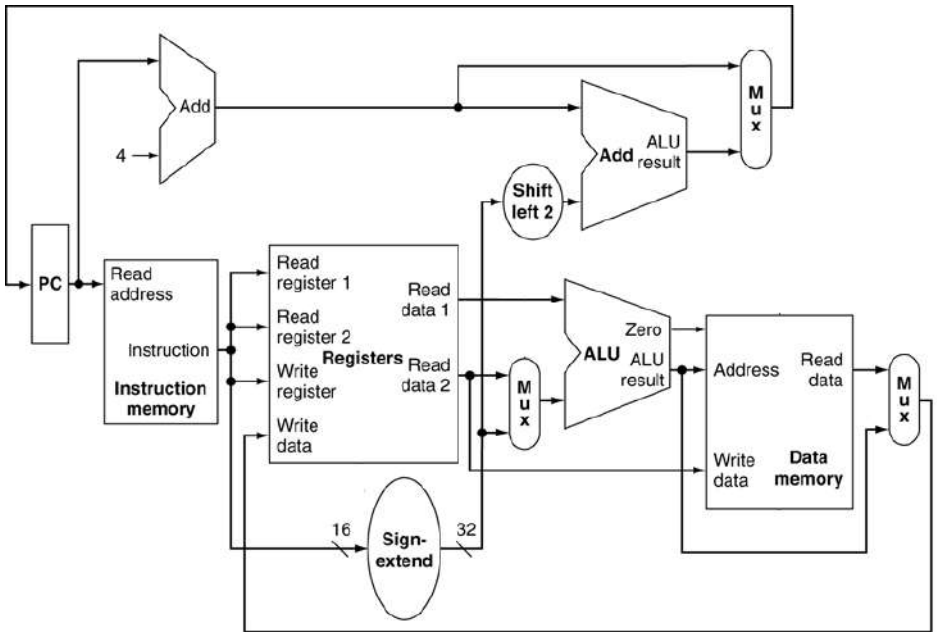

Figure 2: Full Datapath

4. (a) Calculate the performance gain by using a 5 (five) stage pipelined processor over a non-pipelined processor for the following set of instructions with the help of a timing diagram. [4]

```
lw  $5, 100, ($2)
sub $6, $5, $7
sub $5, $2, $3
```

Use the following table for pipeline stage data -

Type	Fetch	Reg Read	ALU Op	Memory Read	Reg Write
sub	100 ps	100 ps	200 ps		100 ps
lw	100 ps	100 ps	200 ps	200 ps	100 ps

(b) Give one example for each type of Pipeline Hazards. [3]

(c) What is Double Data Hazard? Give one example case of Double Data Hazard. [1]

(d) Rewrite the following MIPS code by rescheduling it in such way that minimizes the number of cycles to execute it. Assume the pipelined processor already does not have any forwarding/bypassing enabled. - [2]

```
0000:  add $5, $6, $7
0004:  sub $10, $6, $5
0008:  add $5, $5, $10
0012:  lw  $2, 100($6)
0016:  add $9, $2, $8
0020:  lw  $3, 200($8)
0024:  add $5, $3, $7
0028:  lw  $1, 200($2)
0032:  add $5, $6, $7
0036:  add $5, $1, $7
```

5. (a) Answer Any 3(Three) questions from 5(a)(i) - 5(a)(v) [3]
(i) Write down one example case for Temporal and Spatial locality principle
(ii) Write down two differences between Write Through and Write Back Policy
(iii) Describe the Row Buffer and Synchronous RAM property for Dynamic RAM
(iv) Describe Queuing Delay and Seek Time for Hard Disk with proper examples.
(v) Write down one difference between DDR and QDR Dynamic RAM

(b) Calculate the Average Read Time for the given a Hard Disk Drive of 2kB sector, 7,200 rpm, 2.4ms average seek time, 147MB/s transfer rate, 0.2ms controller overhead, idle disk. [2]

(c) We have a Cache with 10 bit index, 128 bits Data bits per Block, Find the Cache Index where the Memory Byte Address 2000 will be directly mapped into? The address field contains 32 bits. [2]

(d) Calculate the Average Memory Access Time the Direct Mapped Cache attached with a 2 GHz processor. The following properties are found in the specs sheet- [3]
I-Cache Miss Rate 10%,
I-Cache Access Time 10ns,
Instruction Memory Access Time 175 ns,
D-Cache Miss Rate 20%,
D-Cache Miss Penalty 400 cycles,
Memory instructions consists of 25% of the total instructions