United International University (UIU)

Department of Computer Science and Engineering

CSE 1325/225(A) DIGITAL LOGIC DESIGN Final Assignment

Total Marks: 40 Spring 2020

Answer all the Questions

Q1.	Using **J-K flip-flops**, design an arbitrary counter that goes through the sequence 2, 4, 3, 7, 1,0, 5 … and repeat. You have to show (a) the flip-flops' input table, (b) Simplification of flip-flop's input functions using K-Map and (c) Logic diagram.	[4+4+2]

(a) *JK* Flip-Flop

$Q(t)$	$Q(t+1)$	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Q2.	Design a sequential circuit that can recognize the pattern **0010**. Use J-K FF for your design. You must show : (i) State diagram (ii) State table (iii) Flip Flop input functions (iv) K-map minimizations of inputs and output and (v) Circuit diagram.	[2*5=10]

Q3.	(i) Design a 4 bit asynchronous/ripple up counter with a positive edge triggered JK Flip Flop. You have to include an input named "**Count_Up**" in your design. The circuit will work if **Count_Up** =1 and remain unchanged if **Count_Up** = 0. (a) Draw the logic diagram of the circuit (b) Explain the design procedure in your own words shortly.	[2+1]
	(ii) Consider a UIU alarm system with five inputs: fire (F-001), water-tank-full (W-101), burglary (B-100), smoke (S-111) and dust(D-000). For this alarm system an alarm signal (A) is on if any of these events occur and the corresponding three bit output code is shown to denote the incident. For this alarm system: (a) Find out the simplified expression of the alarm signal (A) (b) The design of the encoder system(Output Equations) for the given events. (c) Draw the logic diagram.	[1+2+1]
	(iii) Draw the implementation of the following functions using active high decoders. F1(A, B, C)=$\sum$m(0, 2, 4, 5) F2(X, Y,Z)= $\prod_M$ (1, 2, 6, 7)	[3]

Q4.	(i) Consider a digital system with four binary bits as input and a single bit as output. The binary output is 1 if the number of 1s in the input is less than the number of 0s, otherwise the output is 0. Implement this system using 4x1 MUXs only. You **can't** use any other basic gates i.e AND/OR/NOT gates. (a) Draw the truth table (b) Draw the circuit diagram with necessary input/output labels.	[2+2]
	(ii) Using any number of 3 to 8 active high decoders, implement a 5 to 32 active high decoder. You must draw the circuit diagram for your design and label the decoder pin names and their inputs/outputs carefully.	[3]
	(iii) Implement the following function using one 4x1 MUX and necessary basic gates. $F(A, B, C, D)=\sum m(0, 2, 5, 9, 13)$	[3]