CPUTime = C.C X GET CCT ce=Icxepl



United International University

Department of CSE CSE 313: Computer Architecture Midterm Examination Summer 2022

Time: 1 hour and 45 minutes

Full Marks: 30

[Any examinee found adopting unfair means will be expelled from the trimester / program as per UIU disciplinary rules.]

[N.B.: Answer all the questions. Assume any data if it is not mentioned explicitly.]

[5] 1. a) Suppose, there are three classes of instructions A, B, and C in a particular instruction set architecture with CPIs 1.2, 2, and 2.5 respectively. The number of instructions from each class in two separate programs is as follows:

	Programs	Instruction classes			1c cpl go xi
		A di	В	С	3477 R
_	P1	40 51.2	10	16 -	= cc 7 cp 60v
_ [P2	12	13	40	Sec 7)

If both the programs are run on the same device with a clock frequency of 2GHz, = C.F = ? then find out which program is faster and by how much.

If both the programs are run then find out which program				quency of $2GHz$ $= C.F = ?$, setep
b) Assume that a processor requires the following instru			rate is executin	g a program tha	t ev o
Instructions	FP	INT	L/S	Branch	Cont Since
Instruction count (10 ⁶)	160	110	10	16	1013
CPI	2	1	5	· 2	166 "

If you want to run the program two times faster than now, then how much should you improve the CPI of FP instructions?

Timponed = 1.

2. Consider the following C function that accepts two arguments, an integer array and the length of the array n. This function doubles the value of the positive integers in the array and returns the sum of the updated positive integers. The starting MIPS assembly instruction address is 1000.

```
int pos_sum(int a[], int n) {
 int sum = 0, i = 0;
 while (i < n) {
  if (a[i] > 0) {
   a[i] = 2 * a[i];
   sum += a[i];
  i++;
return sum;
```

```
414
```

Assume that the variable sum corresponds to the register \$s1 and the variable i 0010 wi

- a) Convert the code to the corresponding MIPS assembly instructions.
- [6] [5]
- b) Convert the first 8 lines of your assembly instructions to the corresponding machine code. No need to convert it to binary.
- c) Consider an array A, whose base address is in \$s3. The ISA is double word addressable, that is the memory can contain double words. What will be [2] the corresponding MIPS assembly code for accessing the address of the 9th element of the array, i.e A[9]. (Write in a single line)
- 3. a) Simulate the division algorithm to divide B by A, where A=0100 and B=01001110. Show all the iterations and steps required to complete this division. [3]
 - b) Draw the flowchart of above simulation. [2]

MIPS Machine Codes

Instruction	Opcode	Function Code
add	0	32
sub	0	34
lw	35	
SW	43	
and	0	36
or	0	37
nor	0	39
andi	12	
ori	13	
sll	0	0
srl	0	2
beq	4	
bne	5	
slt	0	42
i	2	
jr	0	8
jal	3	
addi	8	

MIPS Registers

Nume	Register Number		
Szero	0 1 2-3		
Nat			
SOU SOL			
Salt Sa3	4-7		
500 St7	8-15		
Sstt Ss7	16-23		
212 219	24-25		
\$k0.5k1	26-27		
Sgr	28		
SSD	29		
Sir	30		
Sm	31		