United International University
Department of CSE
CSE 313: Computer Architecture
Midterm Examination
Fall 2022

Time: 1 hour and 45 minutes **Full Marks: 30**

[Any examinee found adopting unfair means will be expelled from the trimester/program as per UIU disciplinary rules.]

[N.B.: Answer all the questions. Assume any data if it is not mentioned explicitly.]

1. a) Suppose there are three classes of instructions A, B, and C in a particular instruction set architecture with CPIs 1.2, 2, and 2.5 respectively. The number of instructions from each class in two separate programs is as follows:

Programs	Instruction classes		
	A	B	C
P1	40	10	16
P2	12	13	40

Consider that both programs run on the same device with a clock frequency of 2GHz. Both P1 and P2 both require 400 s to be completed.

(i) Find out the affected and unaffected times for both programs. [2]
(ii) Find the improvement factor for P1 if we get the total program completion time improved by 4x? [3]
(iii) If P2 now has the same execution time as P1 what should be the CPI for instruction class B? [4]

b) Consider a computer program running with the CPU times according to the following table

FP instr.	INT instr.	L\S instr.	Branch instr.	Total time
50s	80s	50s	30s	210s

Assume that the time for INT operation is improved. By how much (in %) the time for INT operation is reduced if the total time is reduced by 20%? [3]

c) Explain Amdahl's law with an example. Also, write in brief about the parameters in Amdahl's law. [2]

2. Consider the following C function (attached below) that accepts three arguments, an integer array and the length of the array size and a variable k. The starting MIPS assembly instruction address is 1600. **Here, the variables x, sum, mul, and j are in address $S0, $S1, $S2 and $S3 respectively.**

```
int superFunc (int array[], int size, int k)
{
     int x = k, sum =0, mul =1;
     while ( x < size-1)
     {
          int j = array[x+1];
          while(j!= array[x])
          {
               mul *= 5;
               j--;
          }
          sum += (mul+j);
          array[x-1] = sum;
          x += 2;
     }
     if(sum < mul )
          return sum;
     else
          return sum + mul ;
}
```

a. Convert the code to the corresponding MIPS assembly instructions. [10]

b. Convert Line number 1620 to 1648 of your assembly instructions to the corresponding machine code. No need to convert it to binary. [4]

c. Consider an array A, whose base address is in $s3. The ISA is double word addressable that is the memory can contain double words. What will be the corresponding MIPS assembly code for loading the address of the 9th element of the array, i.e A[9], increase the value by 6 and Then store the Value to the address of the 4th element of the array, i.e A[4]. [2]

MIPS Machine Codes

Instruction	Opcode	Function Code
add	0	32
sub	0	34
lw	35	
sw	43	
and	0	36
or	0	37
nor	0	39
andi	12	
ori	13	
sll	0	0
srl	0	2
beq	4	
bne	5	
slt	0	42
j	2	
jr	0	8
jal	3	
addi	8	

MIPS Registers

Name	Register Number
$zero	0
$at	1
$v0-$v1	2-3
$a0-$a3	4-7
$t0-$t7	8-15
$s0-$s7	16-23
$t8-$t9	24-25
$k0-$k1	26-27
$gp	28
$sp	29
$fp	30
$ra	31