United International University (UIU)

Dept. of Computer Science & Engineering (CSE)

Mid-Term Exam: Trimester: Summer 2023

Course Code: CSE 4325 Course Title: Microprocessor, Microcontroller and Interfacing

Total Marks: 30 Duration: 1 hour 45 minute(s)

Any examinee found adopting unfair means would be expelled from the trimester/ program as per UIU disciplinary rules.

Question 1: Answer all the questions. (6 Marks)

Transfer of bus control from processor to device takes **100 ns**. Transfer of bus control from device to processor takes **150 ns**.

a.	If one of the input/output devices employs **DMA** in **burst** mode and takes 10000250 ns to transfer 512 bytes of data, what is the data transfer rate of the device in KB/s?	[2]
b.	Suppose, you are transferring 512 bytes of data in both burst mode and cycle stealing mode. For the first half of the bytes, you use burst mode and for the rest half, you use cycle stealing mode. Assume that in cycle stealing mode, data is transferred 2 bytes at a time. How long will it take to transfer a block of 512 bytes? (Use the data transfer rate found from (a))	[4]

Question 2: Answer all the questions. (6 Marks)

a.	Suppose, execution of a signed additional instruction (4F37H + 3012H) occurred, what would be the value of zero flag (ZF), sign flag (SF), parity flag (PF), overflow flag (OF), carry flag(CF) ?	[5]
b.	Name one advantage of using memory segmentation in a microprocessor.	[1]

Question 3: Answer all the questions. (6 Marks)

a.	DS = 34A9H, BX = 8722H, BP = 45E4H To access the physical address in the data segment (DS), what should be the value of I) the segment register if the offset register holds the value of 7B85H. II) the segment register if the offset register holds the value of 45D2H. III) the offset register if the segment register holds the value of 7D92H. **Justify whether your answer is valid or not.**	[3]

b.	RAM[A] has a data bus of 8 bits and RAM[B] has a data bus of 16 bits. Both RAMs have a total memory capacity of 128 MB. What is the address bus width of each RAM?	[3]

Question 4: Answer all the questions. (6 Marks)		
a.	Draw the diagram of a microprocessor with 20-bit address bus and 8-bit data bus interfaced to 28 KB RAM system using the full decoding method. Each RAM chip has a 12-bit address bus and 8-bit data bus. Provide the corresponding address range (starting address and end address) for the system.	[3]
b.	Modify the circuit of (a) to address memory range 50000H – 56FFFH. Draw the diagram as before and provide the modified address range. You need only draw the part of the diagram that goes through any modification.	[3]

Question 5: Answer all the questions. (6 Marks)		
a.	If there are a total of 32 Interrupt types in a microprocessor and the address bus has width of 12 bits, what is the ending address of the interrupt vector table if the starting address is 000H.	[2]
b.	Mention names of some address registers used in 8086 microprocessor. What do stack pointer and instruction pointer point to?	[2]
c	What are the sequence of events that takes place when an interrupt instruction is executed.	[2]