United International University (UIU)

Dept. of Computer Science & Engineering (CSE)

Mid-Term Exam: Trimester: Fall 2022

Course Code: CSE 4325 Course Title: Microprocessor, Microcontroller and Interfacing
Section: (A, B, C, D, E) Total Marks: 30 Duration: 1 hour 45 minute(s)

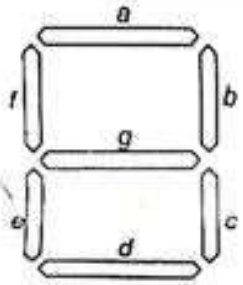
Any examinee found adopting unfair means would be expelled from the trimester/ program as per UIU disciplinary rules.

Question 1: Answer all the questions. **(6 Marks)**

a.	**Draw** the diagram of a 16-bit microprocessor with a 20 bit address bus and 8 bit data bus interfaced to a 112KB RAM system using the full decoding method. Each RAM chip has a 15 bit address bus and 8 bit data bus. **Provide** the corresponding address map for the system.	[3]
b.	**Explain** the operation principle of SRAM and DRAM briefly and state the key differences between them.	[2+1]

Question 2: Answer all the questions. **(6 Marks)**

a. [1+2]



A seven segment LED display (shown in the above figure) is connected to "PORT A" of a microprocessor where LED a, b, c, d, e, f & g are connected sequentially to PA6, PA5, PA4, PA3, PA2, PA1, PA0. **Explain** which type of programmed I/O has to be implemented to show any digit from 0-9 in the seven segment. Also, **determine** the value of data direction register, DDRA and data register, PORTA to show digit "2" in the seven segment display.

b. [2+1]

Suppose, transfer of bus control, from processor to device takes 1000ns and device to processor takes 2000ns. One of the I/O devices has a data transfer rate of 195.3125 KB/sec and employs DMA.

a) If we employ DMA in cycle stealing mode for the first one third of the bytes and burst mode for the rest, how long will it take to transfer a block of 3000 bytes?
b) If the microprocessor does not use the bus for 3.003ms in a span of every 1 minute, then determine the total time it will take to transfer the 3000 bytes in transparent mode. Assume, the DMA employs burst mode when it detects the bus is not used by the processor.

Question 3: Answer all the questions. (6 Marks)		
a.	RAM A and RAM B are both of size 1 MB individually. If RAM A has a data bus of 8 bits and RAM B has a data bus of 16 bits, what should be the size of the address bus for each RAM individually?	[1+1] 5
b.	Suppose execution of a signed additional instruction (7F80H + 6F80H) occurred, what would be the value of Zero flag (ZF), Sign Flag (SF), Parity Flag (PF), Overflow flag (OF).	[4]

Question 4: Answer all the questions. (6 Marks) 0		
a.	An ultrasonic motion detector and a smoke detector are connected to a microprocessor and they send interrupt signals to communicate with the microprocessor. The ISR program of ultrasonic motion detector's IP starts from 02C0H value and the ISR program of smoke detector's IP starts from 3F0H in the memory. **Draw** the Interrupt Vector table of ultrasonic motion and smoke detector. **Also**, determine each detector's interrupt number and **mention** which has the lowest priority.	[3]
b.	**Explain** when the Interrupt type 2 occurs in a system and also **explain** the overall step by step operation of this type of Interrupt.	[2]
c.	**Explain** the function of "IRET" in interrupt service procedure.	[1]

Question 5: Answer all the questions. (6 Marks)		
a.	A microprocessor has a 20 bit address bus and 16 bit data bus. It has a 4KB memory segment. **Explain** what changes have to be applied in the BIU Unit's Adder when converting the logical address to physical address compared to the 8086 microprocessor BIU Unit's adder.	[1] 5
b.	Suppose the address AB2FH: 0164H has an instruction. To execute the instruction, **find** the following: I. value of CS if IP is 9F04H II. value of IP if CS is 9F04H III. last physical address of the segment in which the instruction is saved.	[2+2+1] 4