



**United International University**  
 Department of CSE  
 CSE 3313: Computer Architecture  
 Midterm Examination  
 Spring 2023

**Time: 1 hour and 45  
minutes**

**Full Marks: 30**

[Any examinee found adopting unfair means will be expelled from the trimester / program as per UIU disciplinary rules.]

[N.B.: Answer all the questions. Assume any data if it is not mentioned explicitly.]

1.	<p>a) Alternative compiled code sequences are using same instructions as <b>add</b>, <b>sub</b> and <b>beq</b>. A table is given to show the required number of cycles per instruction (CPI) and the instruction count (IC) on each code sequence.</p> <p>Find out the number of clock cycles and average CPI for all the code sequences.</p> <table><tr><td>Instructions</td><td>add</td><td>sub</td><td>beq</td></tr><tr><td>CPI</td><td>3</td><td>4</td><td>7</td></tr><tr><td>Code sequence 1</td><td>240</td><td>300</td><td>500</td></tr><tr><td>Code Sequence 2</td><td>320</td><td>100</td><td>150</td></tr></table>	Instructions	add	sub	beq	CPI	3	4	7	Code sequence 1	240	300	500	Code Sequence 2	320	100	150	[4]
Instructions	add	sub	beq															
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	<p>b) Consider a computer running a program that requires 400 s, with 90 s spent executing FP instructions, 180 s executed L/S instructions, and 60 s spent executing branch instructions. Find out the affected and unaffected times for Amdahl's law. What is the improvement factor using Amdahl's law if we get the program completion time improved by 4x?</p>	[4]																
	<p>c) What is power wall? Discuss the necessity of multi-core processors.</p>	[2]																
2.	<p>Consider the following C function. The starting MIPS assembly instruction address is 1000. Assume necessary registers.</p>																	

	<pre>int function(int n1, int n2){     int i,s=1;     for(i=n1;i&lt;n2;i++){         if(arr[i]&lt;5){             arr[i]=arr[i]+(s*5);             s=s+i;         }         else         {             s++;         }     }     return s; }</pre>									
	a) Convert the code to the corresponding MIPS assembly instructions.	[6]								
	b) Convert the first 10 lines of your assembly instructions to the corresponding machine code. No need to convert it to binary.	[5]								
	c) Assume we have a new instruction type available in MIPS architecture which is K-type. Only jump instruction can be executed using the K-type MIPS field. Structure of the K-type is given below. Please find the maximum jump address. Explain your answer. <table border="1"><tr><td>op</td><td>rs</td><td>rt</td><td>C/A</td></tr><tr><td>12 bits</td><td>10 bits</td><td>10 bits</td><td>32 bits</td></tr></table>	op	rs	rt	C/A	12 bits	10 bits	10 bits	32 bits	[3]
op	rs	rt	C/A							
12 bits	10 bits	10 bits	32 bits							
3.	a) Assuming 4-bit architecture and using the division algorithm show each step of the division of 11 by 6.	[4]								
	b) Optimized multiplication is better than the normal multiplication algorithm. Why? Explain.	[2]								

## MIPS Machine Codes

Instruction	Opcode	Function Code
add	0	32
sub	0	34
lw	35	
sw	43	
and	0	36
or	0	37
nor	0	39
andi	12	
ori	13	
sll	0	0
srl	0	2
beq	4	
bne	5	
slt	0	42
j	2	
jr	0	8
jal	3	
addi	8	

## MIPS Registers

Name	Register Number
\$zero	0
\$at	1
\$v0-\$v1	2-3
\$a0-\$a3	4-7
\$t0-\$t7	8-15
\$s0-\$s7	16-23
\$t8-\$t9	24-25
\$k0-\$k1	26-27
\$gp	28
\$sp	29
\$fp	30
\$ra	31