



United International University (UIU)

Department of Computer Science and Engineering CSE 1325: DIGITAL LOGIC DESIGN, Final Fall 2021

Total Marks: **40** Duration: 2 hour + 15 min (for uploading)

Section A: Answer any 3 (three) of the Questions from 1 to 4.

1.	Design a clocked sequential circuit that recognizes the 4-bit input sequence 1010 , including overlap such that for input $x = 01010100011010010100$ the corresponding output $Z = 0000101000000100001$. Design the circuit using D Flip-Flops . You have to show the following: i. The state diagram ii. The flip-flop input table iii. The simplified equation(s) for the flip-flop input(s) and the output(s) iv. The final circuit diagram	[2] [2] [2] [2]																	
2.	Design a D Flip-Flop using a JK Flip-Flop and basic gates . You have to show the following i. The conversion table ii. The simplified equation(s) for the flip-flop input(s) iii. The final circuit diagram	[4] [2] [2]																	
3.	A MOD-12 counter counts from 0000 to 1011 . Design the MOD-12 binary ripple counter with positive edge-triggered T Flip-Flops and basic gates . Include an asynchronous RESET signal to reset the circuit to state 0000 (when $RESET = 1$).	[8]																	
4.	Draw the logic diagram of a 4-bit universal shift register, which, based on the two mode-selection (control) inputs S_1 and S_0 can do the following operations. You are free to use any kind of flip-flop and other necessary gates you prefer. <table border="1"> <thead> <tr> <th colspan="2">Mode Control</th> <th rowspan="2">Register Operation</th> </tr> <tr> <th>S_1</th> <th>S_0</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Parallel Load</td> </tr> <tr> <td>0</td> <td>1</td> <td>Shift Left</td> </tr> <tr> <td>1</td> <td>0</td> <td>Shift Right</td> </tr> <tr> <td>1</td> <td>1</td> <td>No Change</td> </tr> </tbody> </table>	Mode Control		Register Operation	S_1	S_0	0	0	Parallel Load	0	1	Shift Left	1	0	Shift Right	1	1	No Change	[8]
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S_1	S_0																		
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Section B: Answer any 2 (two) of the Questions from 5 to 7.

5.	A) Design the following Boolean function using a 3-to-8 line decoder and an OR gate. $F(A, B, C) = A\bar{B} + B\bar{C}$ B) Design a Full Adder circuit of two binary numbers with two bits denoted as A_1A_0 and B_1B_0 and an input carry C_i using two 1-bit full adder circuits block diagram and external basic gates. Here output will be sum = s_1s_0 and output carry C_0 .	[4] [4]
6.	A) Implement the following Boolean function with an 8-to-1-line multiplexer and external basic gates. $F(W, X, Y, Z) = \Pi_M(0, 2, 5, 6, 7, 8, 9, 10)$ B) Design an 8-to-1 -line multiplexer using 2-to-1 line multiplexers only. You need to use the	[4] [4]

	block diagram of the 2 to 1 line multiplexer.	
7.	<p>A) Design a 4-input Priority Encoder with inputs $D_3D_2D_1D_0$. Derive the truth table of the priority encoder where priority is set according to the following sequence of priority from the highest to the lowest $D_1 > D_2 > D_0 > D_3$. Derive the Boolean expressions for outputs and draw the circuit diagram.</p> <p>B) Find the Boolean expressions of the outputs of a Hexadecimal to Binary encoder where inputs are $H_0, H_1, H_2, \dots, H_{15}$ and outputs are A, B, C, D.</p>	<p>[4]</p> <p>[4]</p>

Excitation Tables for different Flip-Flops

Q(t)	Q(t+1)	D	Operation
0	0	0	Reset
0	1	1	Set
1	0	0	Reset
1	1	1	Set

Q(t)	Q(t+1)	J	K	Operation
0	0	0	x	No change/reset
0	1	1	x	Set/complement
1	0	x	1	Reset/complement
1	1	x	0	No change/set

Q(t)	Q(t+1)	T	Operation
0	0	0	No change
0	1	1	Complement
1	0	1	Complement
1	1	0	No change