United International University
Department of CSE
CSE 313: Computer Architecture
Final Examination
Spring 2023

Time: 2 Hours Full Marks: 40

[N.B.: Answer all the questions. Assume any data if it is not mentioned explicitly.]

1. a) You have to modify the block diagram for the single-cycle data path so that it can execute the following instruction 'X'. Also, write the control unit values for this instruction. [5]

X ($s0), $s1, $s2

This instruction adds the values of $s1 and $s2 and saves the result in the memory address specified by the value of $s0. For example, if the value of $s0 is 1000, then the sum of the values $s1 and $s2 will be saved in the memory address 1000. The machine code format for the instruction is given below, where rs, rt, and rd will contain the index numbers of $s1, $s2, and $s0 registers, respectively.

Opcode	rs	rt	rd	shamt	func
31-26	25-21	20-16	15-11	10-6	5-0

b) You have to modify the block diagram for the single-cycle data path so that it can execute the following instruction 'Y'. Also, write the control unit values for this instruction. [5]

Y ($s1)

This instruction loads the program counter (PC) with the memory address specified by the value of $s1. The machine code format for the instruction is the same as in question 1(a), where rs will contain the index number of the $s1 register.

2. Consider a processor that goes through the following six stages while executing an instruction.

Instruction Fetch	Instruction Decode	ALU Operation	Memory Write	Memory Read	Register Write
100 ns	150 ns	250 ns	110 ns	200 ns	150 ns

Also consider the following instruction snippet:

```
add $s7, $s1, $s2
lw  $t4, 20($s7)
sub $t0, $s0, $t4
sw  $t7, 20($s7)
add $t1, $t7, $t3
and $s3,$s4,$zero
```

Now answer the following questions:

a) Determine the number of stalls for data-hazard for the "**lw**" (load word) instruction when we are applying the bypassing method. Explain your answer. [3]

b) A software engineer, Mr. A, believes that the total number of cycles required for a given code snippet with forwarding will be 9 cycles. Do you agree with Mr. A's claim? Please provide an explanation for your answer, including a timing diagram to illustrate the cycle count. [5]

c) Mr. A, again claims that he can eliminate all stalls in the given code snippet by using the code scheduling method. Is it possible to remove all the stalls? Please provide an explanation for your answer, including a timing diagram to illustrate the potential stall removal. [1+4]

d) If we have only one stage Memory in place of Memory Read and Memory Write then the total number of pipeline stages will be five. Will it have any impact your answer in question no. 2 (c)? [2]

3. The address field of a direct-mapped cache is given below

Tag	Offset	Index
63-50	49-32	31-0

(a) Calculate the number of blocks and bytes/blocks. [2]

(b) Calculate the actual size of the cache. [2]

4. Consider a cache memory of size 4KB and block size having 4 words (1 word = 4 bytes). [5]

(a) Determine the miss rate if the following bytes are addressed sequentially.

1, 2, 10, 4097, 4098, 15 .

(b) If we change the block size in (a) to 8 words, find out the miss rate for similar memory address access. Find out the miss rate. [4]

(c) Compare the miss rate in (i) & (ii) and explain the principle of locality. [2]