



United International University
Department of CSE
CSE 313: Computer Architecture
Final Examination
Summer 2022

Time: 2 Hours

Full Marks: 40

Any examinee found adopting unfair means will be expelled from the trimester/program as per UIU disciplinary rules.

[N.B.: Answer all the questions. Assume any data if it is not mentioned explicitly.]

1. a) Modify the block diagram for the single-cycle datapath so that it can execute the following instruction "X". Note that the instruction works with three operands and checks if the value of the second register is less than the value of the third register. If so, set the value of the first register to 1. [5]

The instruction format is given as: X \$s0, \$s1, \$s2

Also write down the control unit values for this instruction.

- b) Modify the block diagram for the single-cycle datapath so that it can execute the following instruction "Y". The instruction jumps to any function called. It first saves the returning address to register 31, then jumps to the target address (the starting address of the function called). [5]

The instruction format is given as: Y 1024

Also write down the control unit values for these instructions.

2. Consider a processor that goes through the following six stages while executing an instruction. The duration of each stage (in ps) is given underneath it:

Instruction Fetch	Instruction Decode	Register Read	ALU Operation	Memory Access	Register Write
250	50	150	300	250	150

- a) Assume that the following code snippet is executed in single cycle datapath. Calculate the execution time of the following code snippet assuming \$s5 = 5, \$s1=0, \$t0=1. [2.5]

```

LOOP:
beq $s5, $zero, EXIT
sll $t0, $t0, 2
lw $s2, $t0($s0)
add $s1, $s1, $s2
addi $s5, $s5, -1
j LOOP
EXIT:

```

IF ID RR ALU MEM RW
250 50 150 300 250 150

Consider the following code snippet.

```

add $s0, $s1, $s2
lw $s1, 16($s0)
sub $s2, $s4, $s6
sw $s7, 12($s0)
add $s2, $s7, $s8

```

IF ID RR ALU MEM RW
250 50 150 300 250 150

add \$s1, \$s2
sub \$s4, \$s6
add \$s7, \$s8

Now answer the following questions:

- b) If basic pipelining is implemented in your processor, calculate the execution time of the instruction snippet with proper timing diagram. [2.5]

- c) Suggest a hardware change that you can implement in your processor to improve the execution time of the instruction snippet. What would be the execution time after this change? Include a timing diagram in your answer. [5]

- d) Explain how an optimized compiler can improve the execution time of the instruction snippet further. In your answer, clearly show any changes that might be brought in the given instruction snippet. [2]

- ✓ 3. a) Consider a cache memory of size 8KB and block size having 8 words (1 word = 4 bytes). Determine the miss rate if the following bytes are addressed sequentially. [5]
21, 64, 2058, 128, 2078

- b) If we change the block size in Q3(a) to 4 words, find out the miss rate for similar memory address access. Find out the miss rate and explain the principle of locality. [5]

- c) Consider a 512KB cache memory with 4 words/block. Determine the actual size of the cache. [2]

4.

Consider the following code. We will parallelize only the nested loop part.

```
sum = x + y + z;
for(int i = 0; i < x; i++) {
    for(int j = y; j > 0; j--) {
        for(int k = 0; k < z; k++) {
            sum += (x + y + z);
        }
    }
}
```

2.5

$$\frac{1}{(1 - \frac{FP}{PR}) + \frac{FP}{PR}} =$$

$$\text{speedup} = \frac{1}{(1 - \frac{2}{16}) \times 2.5} =$$

a) Time for one single arithmetic operation is 2ns. Find the speedup with respect to the runtime of the given code for a hexa-core processor vs a single core processor for $x=4$, $y=4$, and $z=4$. [2]

16

b) Now, again find the speedup for the same code using the value $x=5$, $y=5$, and $z=5$; [2]

c) Compare the speedup obtained in part (a) and in part (b). Is it strong scaling or weak? Give a brief description. [2]

2.5

$$1 + \frac{128}{16} = 5.5$$