United International **University (UIU)**

Department of Computer Science and Engineering

CSE 1325: DIGITAL LOGIC DESIGN, Final Spring 2024

Total Marks: **40** Duration: 2 hours

Answer ALL Questions

1. Design a sequential circuit with two D flip-flops A and B and one input X. When X=0, the state of the circuit remains the same. When X=1, the circuit goes through the state transition from 00 to 10 to 11 to 01, back to 00, and then repeats. [8]

2. A company has called 6 candidates assigning a serial number from 1 to 6 for an interview. On the day of the interview, the interview board wants to call the candidates in the following arbitrary order: 4-1-6-2-5-3-4-... They want you to design a synchronous counter using D flip flops and basic gates. For any unwanted number, assume the next number is 1. You must show:

(i) The state table, [3]
(ii) The optimized input functions, and [3]
(iii) The circuit diagram. [2]

3. Design a four-bit shift register with parallel load using D flip-flops. There are two control inputs: shift and load. When shift = 1 and load = 0, the content of the register is shifted by one position to right. New data are transferred into the register when load = 1 and shift = 0. If both control inputs are equal to 0, the content of the register does not change. If both control inputs are equal to 1, the content of the register toggle. Draw the circuit diagram of your system. [4]

4. Consider an alarm system for the nurses' station of a hospital. There are 5 possible events here: emergency in the ICU (I - 111), emergency in the NICU (N - 100), emergency in the general ward (G - 010), emergency in the post-operative room (O - 001) and emergency in the maternity ward (M - 110). Here, the first letter is the input and the three bits are the output of the system. For example, in I-001, I is the input and 001 is the output. To maintain priority during the occurrence of multiple events at the same time, the priority sequence is: N > I > O > M > G. Design an encoder that can encode the events based on given priority.

You have to answer the followings:
(i) Derive the truth table of the priority encoder including the valid bit. [3]
(ii) Derive the Boolean expressions for all the outputs. [3]
(iii) Draw the logic diagram using basic gates. [2]

5 Mr. Jude Bellingham wants to make a system where 8 inputs will be converted to 3 outputs like the following figure. [4]

(i) What does the following black box imply from a digital logic point of view (Encoder/Decoder)?
(ii) Write the truth table for the black box.
(iii) Write the logical expressions for the three outputs.

6 Implement the following functions using a single decoder: [4]

F1= $\sum_m(0,1,3,4)$

F2= $\prod_M(2,5,6)$

You may assume that the decoder provides active high output.

7 Design a 16:1 MUX using any number of 4:1 MUX. [4]

Excitation Tables for different Flip-Flops

Q(t)	Q(t+1)	D	Operation
0	0	0	Reset
0	1	1	Set
1	0	0	Reset
1	1	1	Set

Q(t)	Q(t+1)	J	K	Operation
0	0	0	x	No change/reset
0	1	1	x	Set/complement
1	0	x	1	Reset/complement
1	1	x	0	No change/set