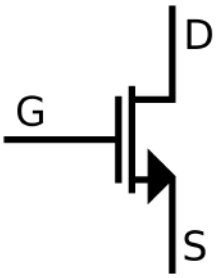
United International University (UIU)
Dept. of Computer Science & Engineering (CSE)
Final-Term Exam: Trimester: Fall 2023

Course Code: EEE 2123; **Course Title:** Electronics
Total Marks: 40; **Duration:** 2 hours

Any examinee found adopting unfair means would be expelled from the trimester/ program as per UIU disciplinary rules.

There are six(6) questions in this paper. Answer all of them.

Q1(a). For the given **NMOS** with $V_t = 1V$, find the **operating region** in each cases : [5x1=5]



Case	V_S	V_G	V_D
a	+1.0	+1.0	+2.0
b	+1.0	+2.5	+2.0
c	+1.0	+2.5	+1.5
d	+1.0	+1.5	0
e	0	+2.5	1.0

Fig 1: Circuit diagram and data table for Q1(a)

Q1(b). Determine the values of $\mathbf{R_D}$ and $\mathbf{R_S}$, so that the transistor operates at $I_D = 0.3mA$ and $V_D = +0.4$ V. The NMOS transistor has $V_t = 1$ V, $\mu_n C_{ox} = 60\ \mu A/V^2$, W/L = 40 [6]

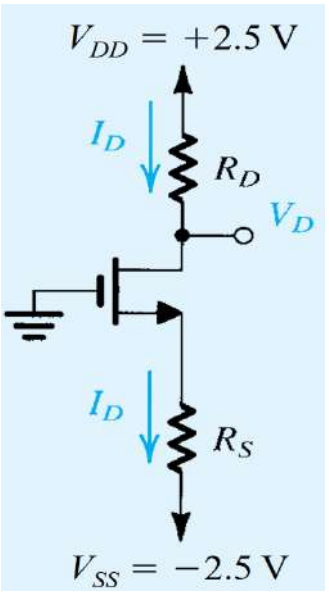


Fig 2: Circuit diagram for Q1(b)

Q2. Analyze the circuit below to determine voltages at all nodes and the currents through all branches. Let, $\mathbf{V_{tn} = 1V}$, $\mathbf{k_n'(W/L) = 1\ mA/V^2}$**.** [6]

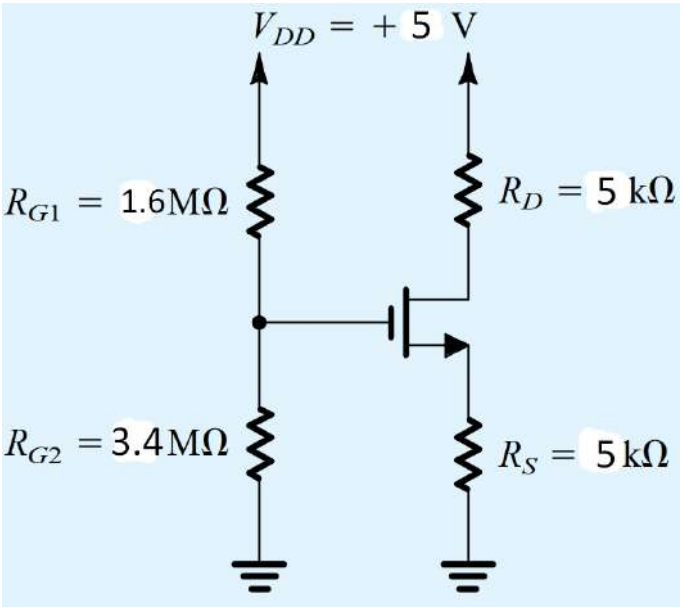


Fig 3: Circuit diagram for Q2

Q3. The transistor shown below is operating at the edge of saturation. Find the values of voltages at all nodes (V_B, V_C, V_E) and the currents through all branches .

Here, β = 100. [4]

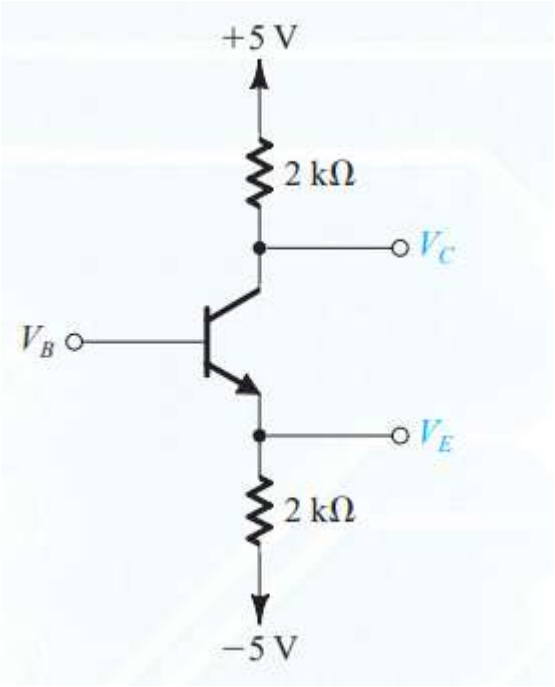


Fig 4: Circuit diagram for Q3

Q4. For the transistor in the following circuit, $\beta = 50$ and $\beta_{forced} = 15$. Analyze the circuit to the value of voltage at all nodes and current through all branches.[5]

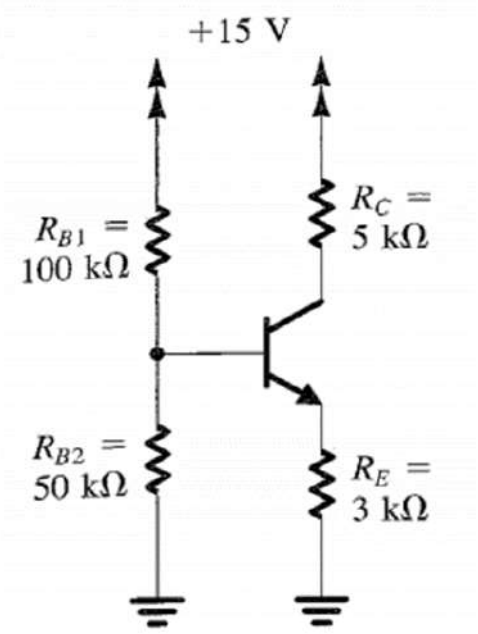


Fig 5: Circuit diagram for Q4

Q5(a). The PMOS network of a random digital system is given below: [4]

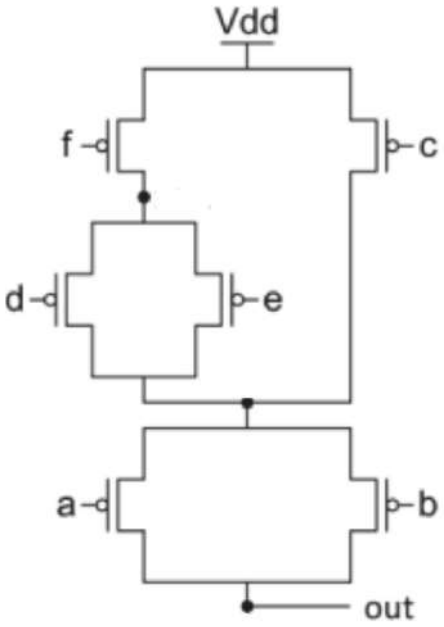


Fig 6: Circuit diagram for Q5(a)

Draw the corresponding NMOS network using the concept of CMOS technology and mention the expression of the output function, V_{out}.

Q5(b). Implement the following logic function " f " in single stage and draw the corresponding circuit diagram: [4]

$$f = A\overline{B} + B(\overline{C} + \overline{CD})$$

Q6. Design an amplifier circuit that can generate the following outputs: [3+3]

(a) $v_0 = 5\int v_i dt + 15\ v_i$

(b) $v_0 = v_1 + \frac{1}{3}\frac{dv_2}{dt} - v_3$ (Here v_1, v_2 and v_3 are three different inputs)

Clearly mention the values of all circuit parameters. Assume that the feedback resistor is 1 kΩ in all cases.