United International University **(UIU)**
Dept. of Computer Science & Engineering **(CSE)**
Final-Term Exam: Trimester: Spring 2024

Course Code: EEE 2123; **Course Title:** Electronics
Total Marks: 40; **Duration:** 2 hours

Any examinee found adopting unfair means would be expelled from the trimester/ program as per UIU disciplinary rules.

There are six(6) questions in this paper. Answer all of them.

Q1(a). The threshold voltage of each MOSFET in the following figure is $V_{tn} = 1$ V. Determine the region of operation of the MOSFET in each circuit. **[4]**

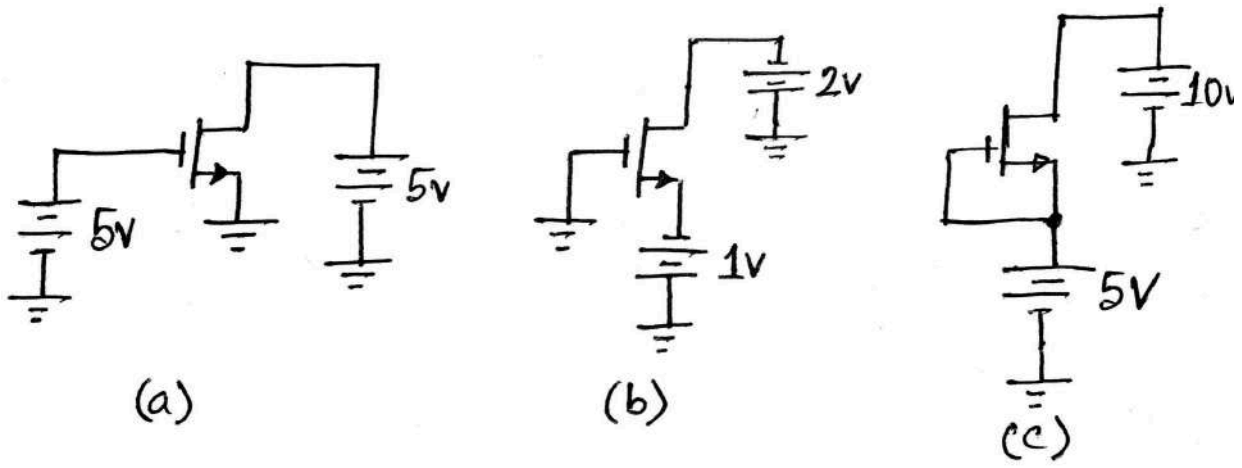

Fig 1: Circuit diagram for Q1(a)

Q1(b). For the circuit in Fig 2, find the value of **R** that results in $V_D = 0.7$ V. The MOSFET has $V_{tn} = 0.4$ V, $\mu_n C_{ox} = 0.5\ mA/V^2$, $W/L = 4$. **[5]**

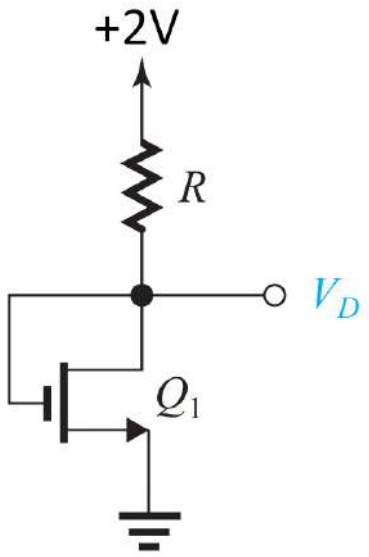

Fig 2: Circuit diagram for Q1(b)

Q2. Design the circuit in Fig. 3 to obtain I = 1 μA, I_D = 0.5 mA, V_S = 2 V, and V_D = 5 V. The NMOS transistor has V_{tn} = 0.5 V, $k'_n(W/L)$ = 4 mA/V^2. **[6]**

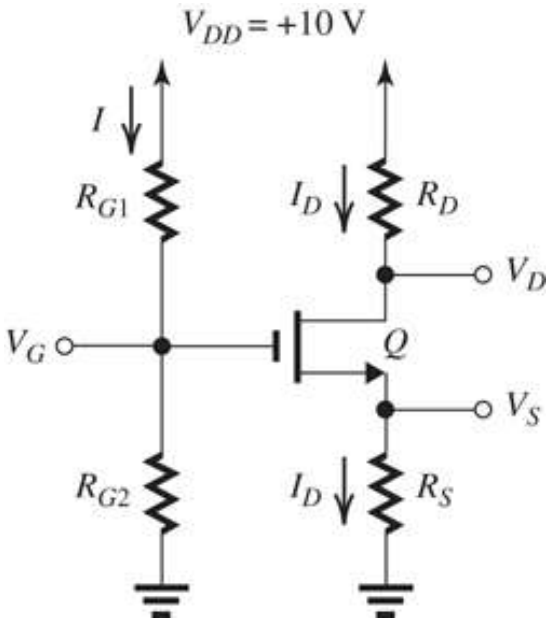

Fig 3: Circuit diagram for Q2

Q3. Determine the voltages at all nodes and current through all branches of circuit in Fig. 4. Given, the current gain, β = 110. **[5]**

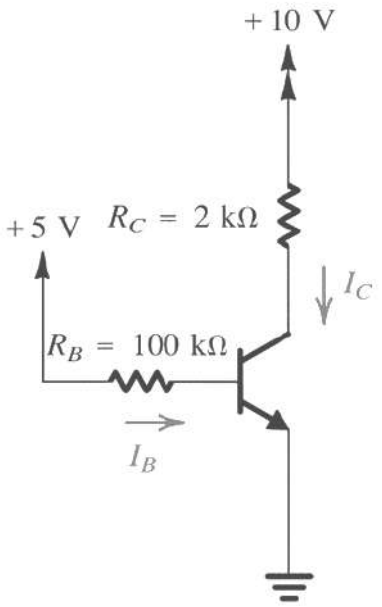

Fig 4: Circuit diagram for Q3

Q4. Find all node voltages and branch currents in the following circuit in Fig. 5. Assume, $R_{B1} = R_{B2} = 50\ k\Omega$ and $\beta=100$. **[6]**

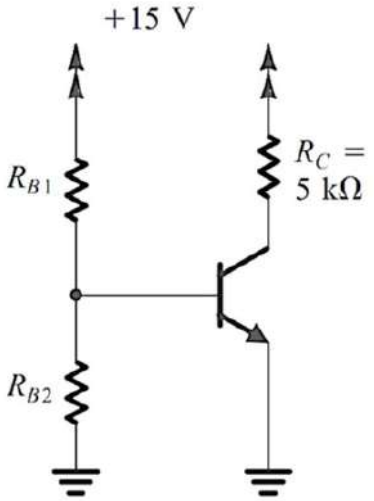

Fig 5: Circuit diagram for Q4

Q5(a). Write the expressions of V_1 and V_0 in terms of A and B in the following diagram in Fig. 6. If A = 0 and B = 1 what will be the values of V_1 and V_0. Clearly show which mosfets will be on and which will remain off. **[4]**

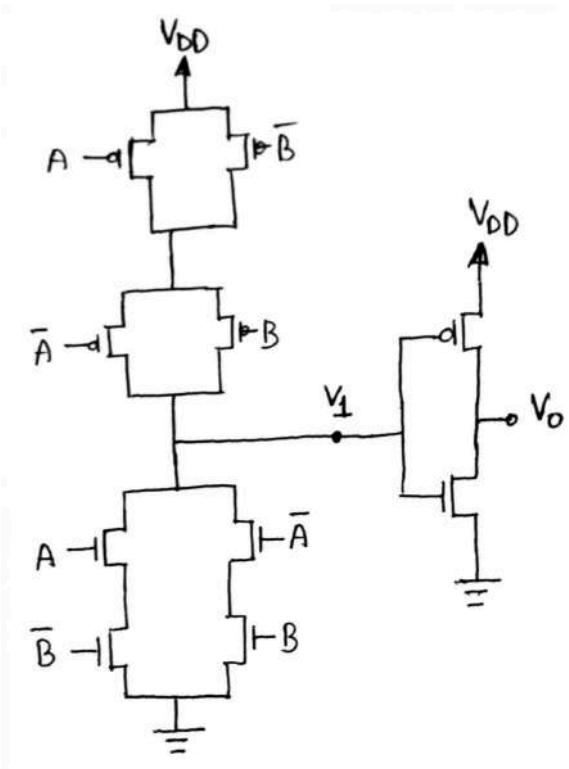

Fig 6: Circuit diagram for Q5(a)

Q5(b). Implement the following logic function " f " in single stage and draw the corresponding circuit diagram: **[4]**

$$f = (\overline{AB}\,C + B\,\overline{CD})$$

Q6. Design an amplifier circuit that can generate the following outputs: **[3+3]**

(a) $v_0 = -7v_i + 5\frac{dv_i}{dt} - \frac{1}{3}\int v_i dt$

(b) $v_0 = 3v_1 - 2v_2 - 8v_3$ (Here v_1, v_2 and v_3 are three different inputs)

Clearly mention the values of all circuit parameters. Assume that the feedback resistor is 1 kΩ in all cases.