United International University (UIU)

Dept. of Computer Science & Engineering (CSE)

Mid-Term Exam Trimester: Fall 2023

Course Code: CSE 4325 Course Title: Microprocessors and Microcontrollers

Total Marks: 30 Duration: 1 hour 45 minute(s)

Any examinee found adopting unfair means would be expelled from the trimester/ program as per UIU disciplinary rules.

Question 1: Answer all the questions. (6 Marks)		
	Transfer of bus control from processor to device takes **100 ns**. Transfer of bus control from device to processor takes **200 ns**.	
a.	If one of the input/output devices employs **DMA** in **burst** mode and takes 10000300 ns to transfer 1536 bytes of data, what is the data transfer rate of the device in KB/s?	[2]
b.	Suppose, you are transferring 1536 bytes of data in both burst mode and cycle stealing mode. For the first **one-third** of the bytes, you use **burst mode** and for the rest **two-third**, you use **cycle stealing mode**. Assume that in cycle stealing mode, data is transferred **4 bytes at a time**. How long will it take to transfer a block of 1536 bytes? (Use the data transfer rate found from (a))	[4]
Question 2: Answer all the questions. (6 Marks)		
a.	Suppose, execution of a signed additional instruction (6BCDH + 5234H) occurred, What would be the value of zero flag (ZF), sign flag (SF), parity flag (PF), overflow flag (OF)?	[4]
b.	Describe in short the four general purpose registers of the 8086 microprocessor.	[2]
Question 3: Answer all the questions. (6 Marks)		
a.	Suppose the address 79E4H : 2A8CH has an instruction. To access this instruction, what should be the value of I) the **segment register** if the offset register holds the value of 5A3CH. II) the **segment register** if the offset register holds the value of 5A2DH. III) the **offset register** if the segment register holds the value of 2679H. **Justify whether your answer is valid or not.**	[3]

b.	RAM[A] has a **data bus** of 32 bits and RAM[B] has an **address bus** of 26 bits. Both RAMs have a total memory capacity of 128 MB. What is the **address bus** width of RAM[A] and **data bus** width of RAM[B]?	[3]

Question 4: Answer all the questions. (6 Marks)

a.	**Draw the diagram** of a microprocessor with a 20-bit address bus and 8-bit data bus interfaced to 28 KB RAM system using the **full decoding method**. Each RAM chip has a 13-bit address bus and 8-bit data bus. Provide the corresponding address range (starting address and end address) for the system.	[3]
b.	Modify the circuit of (a) to address memory range B0000H – B6FFFH. Draw the diagram as before and provide the modified address range. **You need only draw the part of the diagram that goes through any modification.**	[3]

Question 5: Answer all the questions. (6 Marks)

a.	Calculate the memory location of **CS and IP** for the interrupt **INT EH** in the interrupt vector table.	[3]
b.	What is the sequence of events that takes place when a software interrupt instruction is executed?	[2]
c.	Explain the function of **"IRET"** in interrupt service procedure.	[1]