United International University (UIU)
Dept. of Computer Science& Engineering (CSE)

Final Exam. Trimester: Fall 2020

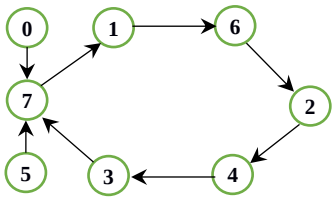
Course Code: CSE 1325, Course Title: DIGITAL LOGIC DESIGN

Total Marks: **25** Duration: 1 hour 15 minutes + 15 minutes (for uploading)

Answer ALL 3 Questions from Q1 to Q3 [3 × 5 = 15]

1. A sequence recognizer is a sequential state machine which takes an input string of bits and generates an output 1 whenever the target sequence has been detected. You have to design a machine where output depends on the present state and the external input (x). Now, design a sequence recognizer for recognizing the sequence 1010 using D flip flop. You have to find the followings. [5]
   a) State diagram.
   b) Flip-flop input table.
   c) K-map minimizations of input and output equations.
   d) Logic diagram.

2. Design an arbitrary synchronous counter circuit using D flip flop that counts according to the sequence given in the given figure. You must show the (i) flip-flop input table, (ii) k-map minimizations of flip-flop input functions and (iii) circuit diagram. [5]



3. A) Design a 4-bit asynchronous Ripple Counter with one control input (A) using negative edge J-K Flip Flops. The counter will count up when A = 1 and will count down when A = 0. [2]
   B) We have a lot of D flip flops at our disposal. Design a 4-bit register using as many D flip flops along with any number of basic gates or combinational functional blocks as needed that can do the following three operations: load, no change and reset. [3]

Answer any 2 Questions from Q4 to Q6 [2 × 5 = 10]

4. [5]
   - You have to build a circuit with 3-bits number (A, B, C) as input and 2-bits number (X, Y) as output.
   - If the total number of ones in the input bit is even then X will be '1' else X will be '0'. For example, if input is "101" then the X will be '1'.
   - If the decimal equivalent of the input is odd then Y will be '1' else Y will be '0'. For example, if the input "101" then Y will be '1'.

   Implement the circuit using a single decoder of your choice and OR gates only.

5. A) We have two digits A (A3 A2 A1 A0) and B (B3 B2 B1 B0) that we need to add. But, we have only 2-bit full adders. Design a circuit to add those two digits using any number of 2-bit full adders as needed. [2]
   B) Implement the function F(A, B, C, D) = ∑(0,3,6,8,12,14,15) using a 4x1 MUX. [3]

6. Consider an UIU alarm system with five inputs: fire (F-001), water-tank-full (W-101), burglary (B-100), smoke (S-111) and dust (D-000). Here, the first letter is the input and the three bits are the output. For example, in “F-001”, F is the input and “001” is the output. To maintain priority during the occurrence of multiple events at the same time, the priority sequence followed is D<W<B<S<F. [5]
   (a) Derive the truth table of the priority encoder.
   (b) Derive the Boolean expressions for all the outputs.