United International University (UIU)
Dept. of Computer Science & Engineering (CSE)
Final-Term Exam: Trimester: Summer 2023

Course Code: EEE 2123; **Course Title:** Electronics
Total Marks: 40; **Duration:** 2 hours

Any examinee found adopting unfair means would be expelled from the trimester/ program as per UIU disciplinary rules.

There are six(6) questions in this paper. Answer all of them.

Q1(a). For the given NMOS , find the **operating region** in each cases : [4x1=4]

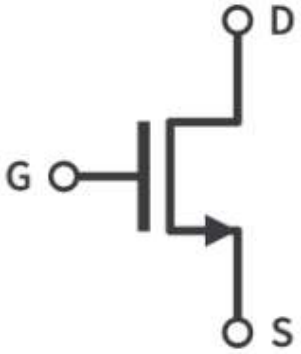

Fig 1: Circuit diagram for Q1(a)

(a) $V_G = 0$ V ,$V_S = -2$V , $V_D = 1$V, $V_t = 1$V
(b) $V_G = 1.5$V ,$V_S = 0$V , $V_D = 0.1$V, $V_t = 1.2$V
(c) $V_G = -2$V ,$V_S = -3$V , $V_D = 5$V, $V_t = 1.5$V
(d) $V_G = 5$V ,$V_S = -1$ V , $V_D = 5$ V, $V_t = 1$V

Q1(b). The MOSFET shown below has $V_{tn} = 1$V , $\mu_n C_{ox} = 0.1$ mA/V^2. Find the values of **W/L** and **R** so that when $v_I = V_{DD} = +5$ V , $r_{DS} = 50\ \Omega$ & $v_o = 50$ mV . [6]

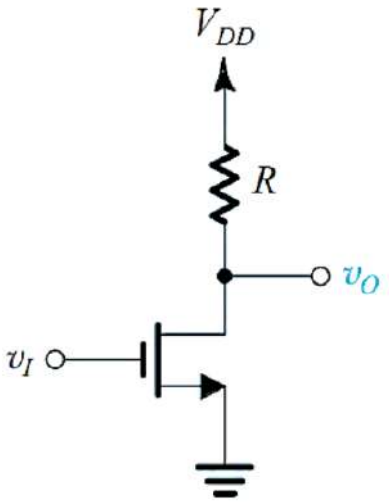

Fig 2: Circuit diagram for Q1(b)

Q2. Analyze the circuit below to determine voltages at all nodes and the currents through all branches.Let, $\mathbf{V_{tn} = 1V}$, $\mathbf{k_n'(W/L) = 1\ mA/V^2}$ **.** [6]

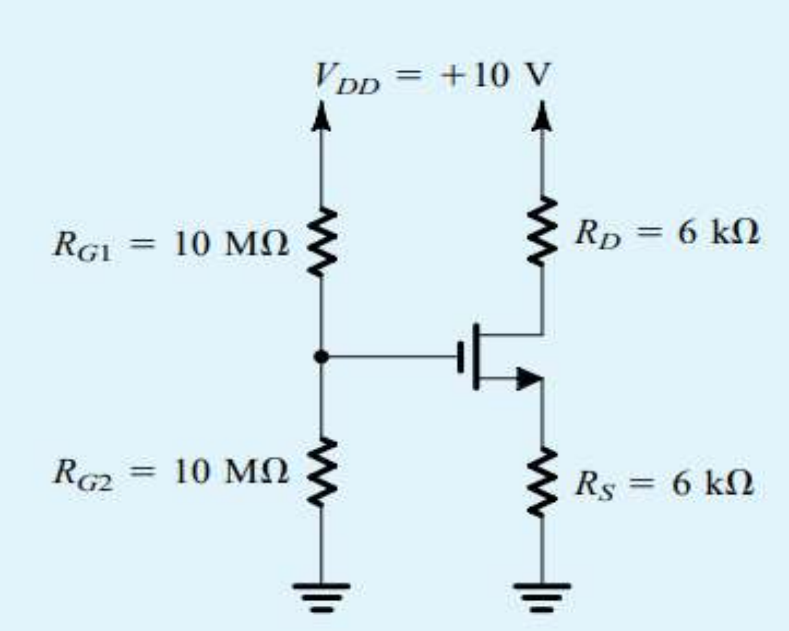

Fig 3: Circuit diagram for Q2

Q3. Determine the voltage at all nodes and current through all branches for the BJT circuit shown below. Here, $R_E + R_C = 8$ kΩ and $0 < R_E < R_C$ [4]

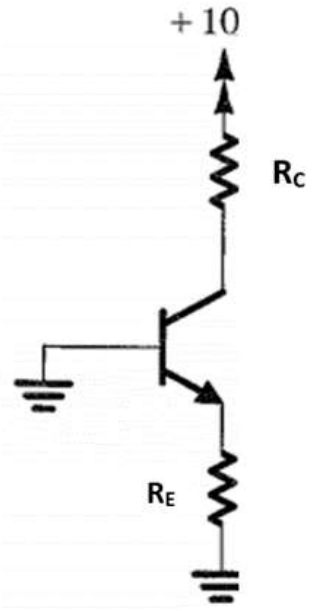

Fig 4: Circuit diagram for Q3

Q4. For the bipolar junction transistor in the following circuit,

R_B=100 kΩ and β_{forced} = 15. Find the value of R_C. Assume silicon diode. [6]

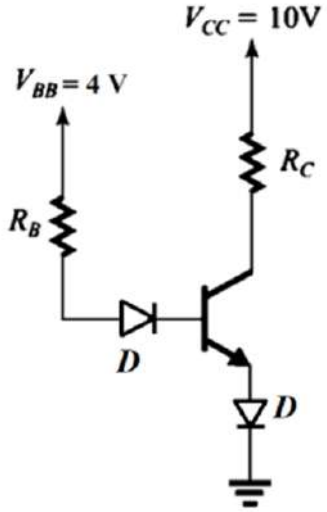

Fig 5: Circuit diagram for Q4

Q5(a). . The PMOS network of a random digital system is given below: [4]

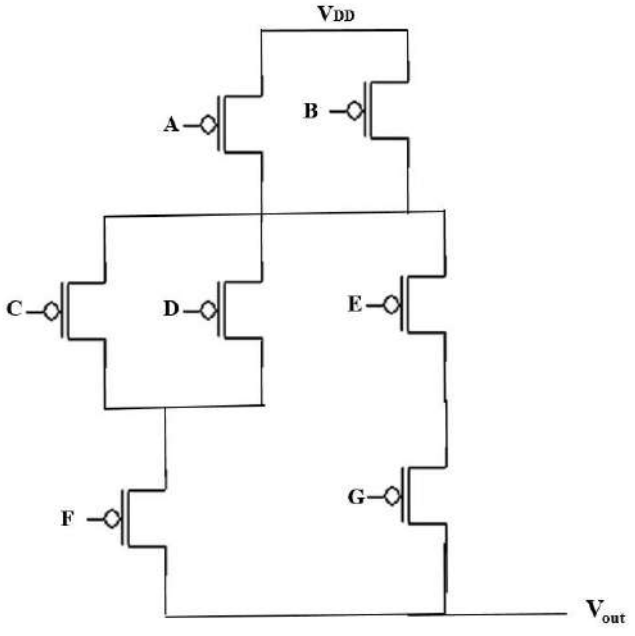

Fig 6: Circuit diagram for Q5(a)

Draw the corresponding NMOS network using the concept of CMOS technology and mention the expression of the output function, V_{out}.

Q5(b). Implement the following logic function " f " in single stage and draw the corresponding circuit diagram: [4]

$$f = (ab + \bar{c})ed + gh$$

Q6. Design an amplifier circuit that can generate the following outputs: [3+3]

(a) $v_0 = 10\ v_i - 5\ \frac{dvi}{dt}$

(b) $v_0 = 5v_1 + 15v_2$ (here, v1 and v2 are two different inputs)

Clearly mention the values of all circuit parameters. Assume that the feedback resistor is 10 kΩ in all cases.