United International University (UIU)

Dept. of Computer Science & Engineering (CSE)

Mid-Term Exam: Trimester: Spring 2023

Course Code: CSE 4325 Course Title: Microprocessors and Microcontrollers
Section: (A, B, C, D) Total Marks: 30 Duration: 1 hour 45 minute(s)
[You have to answer all the five questions]

Any examinee found adopting unfair means would be expelled from the trimester/ program as per UIU disciplinary rules.

Question 1: Answer all the questions.		**(6 Marks)**
a.	Transfer of bus control from processor to device takes 150 ns. But transfer of bus control from device to processor takes 550 ns. I) One of the input-output devices employs DMA in burst mode and takes 13335083 *ns* to transfer 2048 byte of data. What is the data transfer rate of the device? II) Now in the cycle stealing mode, data transfer will begin with one byte at a time and in every consecutive/following cycle, one extra byte will transfer than the previous one. That means, in the first cycle one byte will transfer, in the second cycle two bytes will transfer, in the third cycle three bytes will transfer and, in this manner, data transfer will continue until all the required bytes are transferred. Suppose you need to transfer 7875 bytes of data in this cycle stealing mode. **Calculate** the time required to transfer the data in this mode. ***[Consider the same data transfer rate that you got from the part (I)]*** ***[Hint: Try to build a series of the first n positive integers among the consecutive data transmission cycles]***	[2] [4]
Question 2: Answer all the questions.		**(6 Marks)**
a.	Suppose execution of a signed instruction (8BCD H – 71AB H) occurred. What would be the value of Carry flag (CF), Zero flag (ZF), Sign Flag (SF), Parity Flag (PF), and Overflow flag (OF)?	[5]
b.	Briefly **describe** the four general purpose registers of the 8086 microprocessor.	[1]
Question 3: Answer all the questions.		**(6 Marks)**
a.	Suppose the address 68E2H : 3B9AH has an instruction. To access this instruction, what should be the value of I) the segment register if the offset register holds the value of 4C5AH. II) the segment register if the offset register holds the value of 7D98H. III) the offset register if the segment register holds the value of 26FFH. **Justify** your answer.	[3]
b.	If two consecutive segments have the values of 8600H and 8601H, in total how many physical address slots exist in both of these segments that are not overlapping between both segments?	[3]
Question 4: Answer all the questions.		**(6 Marks)**
a.	**Draw** the diagram of a microprocessor with 20-bit address bus and 8-bit data bus interfaced to 96KB RAM system using the full decoding method. Each RAM chip has a 14-bit address bus and 8-bit data bus. **Provide** the corresponding address range (starting address and end address) for the system.	[4]
b.	**Modify** the circuit of (a) to address memory range A0000H - B7FFFH. **Draw** the diagram as before and provide the modified address range. You need only draw the part of the diagram that goes through any modification.	[2]

Question 5: Answer all the questions. (6 Marks)

a. [3]

Sensor X: Fire Alarm Sensor	**Sensor Y:** Ultrasonic Motion Detector
INT X	INT Y

A fire alarm sensor and an ultrasonic motion detector are connected to a microprocessor. When the sensors detect an input, they send interrupt signals to the microprocessor. The CS and IP values for the start of the ISRs for both interrupts are stored in an interrupt vector table. In the interrupt vector table, the lower byte of CS for the fire alarm sensor is in the physical address 0025AH, and the upper byte of IP for the ultrasonic motion detector is in the physical address 001D5H.

I) **Draw** the interrupt vector table for the sensors showing their memory locations.
II) **Determine** each sensor's interrupt number in hexadecimal.
III) If both sensors send interrupt signals to the microprocessor at the same time, which one will be executed first and why?

b. When does the interrupt type 4 occur in a system? **Explain** the overall step by step operation for this type of interrupt. [2]

c. Why does 8086 reset the interrupt flag (IF) and trap flag (TF) when an interrupt instruction is executed? [1]