United International University (UIU)

Dept. of Computer Science & Engineering (CSE)

Mid-Term Exam Trimester: Spring 2024

Course Code: CSE 4325 Course Title: Microprocessors and Microcontrollers

Total Marks: 30 Duration: 1 hour 30 minute(s)

Any examinee found adopting unfair means would be expelled from the trimester/ program as per UIU disciplinary rules.

Question 1: Answer all the questions. (6 Marks)		
	Transfer of bus control from processor to device takes **300 ns**. Transfer of bus control from device to processor takes **200 ns**.	
a.	If one of the input/output devices employs **DMA** in **cycle stealing** mode and takes **12564000 ns** to transfer **512 bytes** of data. If data is transferred **4 bytes** at a time, what is the data transfer rate of the device in **KB/s**?	[3]
b.	Suppose, you are transferring **8192 bytes** of data. Which mode(**burst mode/cycle stealing mode**) will be faster to transfer this data? Assume that in cycle stealing mode, data is transferred **4 bytes at a time**. ? (Use the data transfer rate found from (a))	[3]
Question 2: Answer all the questions. (6 Marks)		
a.	Suppose, execution of a signed substractional instruction **(8000H - 0001H)** occurred, What would be the value of carry flag (CF), sign flag (SF), parity flag (PF), overflow flag (OF)?	[4]
b.	Proof mathematically, the maximum size of a segment is **64KB** in an 8086 microprocessor.	[2]
Question 3: Answer all the questions. (6 Marks)		
a.	SS = 2526H BX = 0020H BP = 1105H CS = A231H To access the physical address in the **Stack Segment**, what should be the value of I) the **segment register** if the offset register holds the value of 3C5AH. II) the **offset register** if the segment register holds the value of 213AH. **Justify whether your answer is valid or not.** III) Find the first and last physical address of the **Code Segment**.	[3]

b.	RAM[A] has a **data bus** of 16 bits and RAM[B] has an **address bus** of 17 bits. Both RAMs have a total memory capacity of 128 KB. What is the **address bus** width of RAM[A] and **data bus** width of RAM[B]?	[3]

Question 4: Answer all the questions. (6 Marks)

a.	**Draw the diagram** of a microprocessor with a 20-bit address bus and 8-bit data bus interfaced to 8 KB RAM system using the **full decoding method**. Each RAM chip has a 11-bit address bus and 8-bit data bus. Draw the circuit to address memory range **58000H – 59FFFH**. Provide the **address mapping** as well.	[6]

Question 5: Answer all the questions. (6 Marks)

a.	In the interrupt vector table, the **upper byte of CS** for the ultrasonic motion detector is in the physical address **0036BH**, and the **upper byte of IP** for the fire alarm sensor is in the physical address **001E5H**. **I)** Determine each sensor's interrupt number in hexadecimal. **II)** If both sensors send interrupt signals to the microprocessor at the same time, which one will be executed first and why?	[4]
b.	If there are a total **128** interrupts in an **8086** microprocessor then what will be the size of the **interrupt vector table**?	[2]