United International University
Department of Computer Science and Engineering

CSE 313: Computer Architecture

Final Examination Time: 2 Hours Date:

Name: ID:

Answer all five questions

Submit the question paper with the answer script

---

1. (a) Calculate the value of $1.11001_2 \times 2^{-1} + 1.00011_2 \times 2^2$ using the binary addition formula with result upto 6 significant binary bits. Mention the value at each step of the operation. [3]

   (b) Show the representation of the result from Q1(a) to a **double precision** IEEE 754 standard floating point variable. Clearly mention all the parts of the IEEE 754 standard [3]

   (c) Mention the **single precision** floating point representation of the value 0 and **infinity** using IEEE 754 standard. [2]

2. (a) Mention **one** difference between Sequential and Combinational logic elements. Give one example of each type. [2]

   (b) Write down the function of the following control signals from the Figure 1- [2]
   i. RegWrite, ii. MemRead, iii. MemWrite, iv. MemToReg

   (c) Modify the following diagram at Figure 1 to incorporate **Jump** instructions. (Check the question for Figure 1) [2]

   (d) Draw the datapath for **R Type** instructions in MIPS over the Figure 1 (Check the question for Figure 1) [2]

3. (a) Calculate the total time needed for executing the following instructions in a pipelined MIPS processor **without** any forwarding unit. Draw the timing diagram. [5]

```
sub $2,  $1, $0
and $12, $2, $6
or  $13, $6, $2
lw  $2,  200($5)
add $14, $2, $2
sw  $15, 100($2)
```

Fetch	Decode	Execution	Memory	Write Back
100 ps	150 ps	100 ps	200 ps	50ps

Table 1: Pipeline Data

   (b) Define Double Data Hazard. Explain one example of Double Data hazard using the values of Forwarding Units. [3]

4. (a) Explain the usage of Hierarchical Memory units to gain benefits from Spatial and Temporal locality principles. [2]

   (b) Calculate the Average Disk Access time for a hard disk that has 512kB sector, 7,200rpm, 1ms average seek time, 300MB/s transfer rate, 0.2ms controller overhead, idle disk. [2]

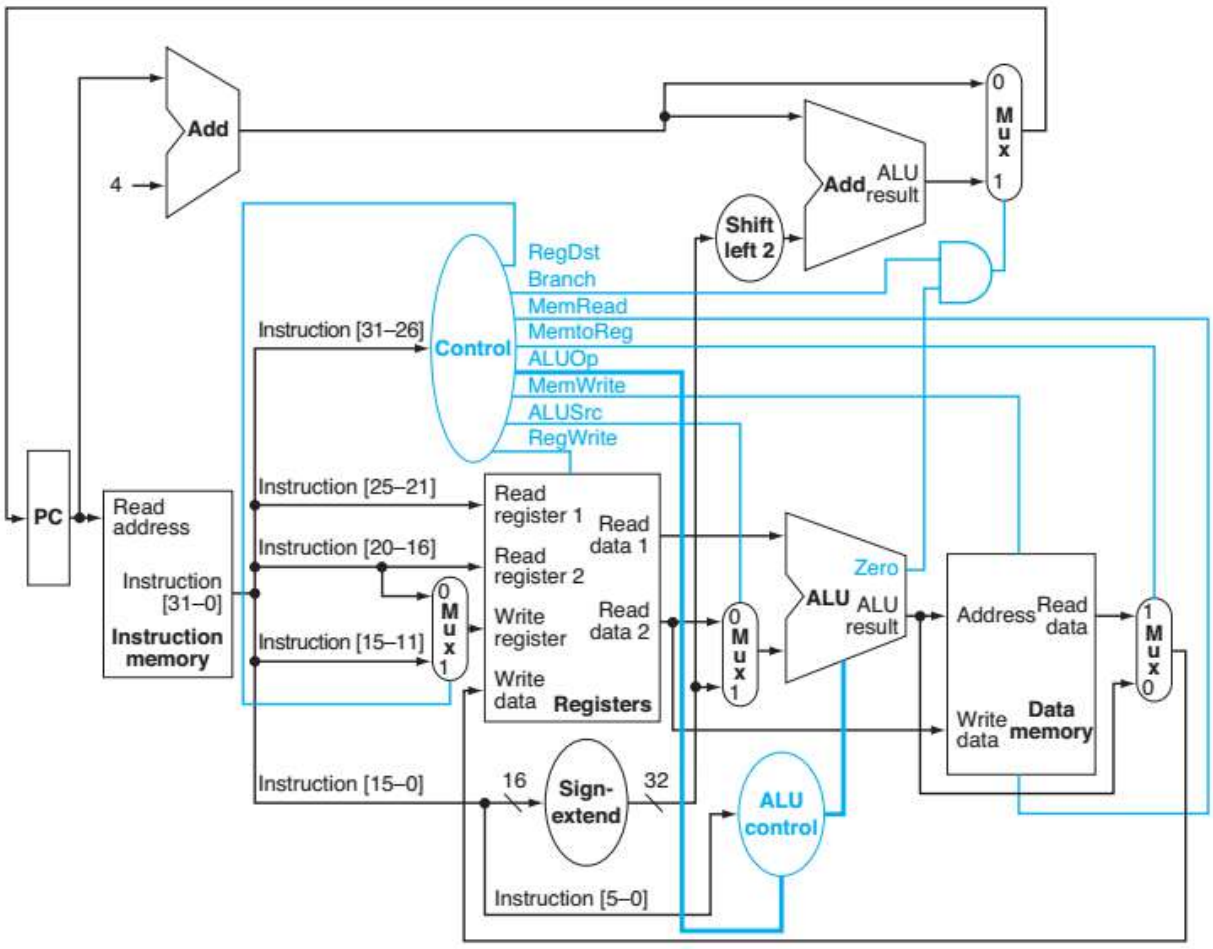

Figure 1: Non Pipelined Processor

(c) The initial state of a 2-way set associative Cache with 8 blocks is given as following - [4]

index 0	index 1	index 2	index 3
mem[0] -	mem[1] mem[5]	- -	- -

Determine hit/miss for the following memory references if **LRU** is used as replacement policy with proper diagrams. Memory reference sequence is 8, 4, 0, 4, 9, 5, 0, 9

5. (a) Suppose a processor with 4 Ghz clock rate has base CPI of 2. L1 cache miss rate is 5%. L2 cache miss rate is 2% and access time is 50 ns. Main memory access time is 400 ns. Calculate the performance gain by using both L1 & L2 cache over using L1 cache only. [2]

(b) Calculate the **Single Error Correction** Hamming code for the following data bits - 1101 1101 0100 [2]

(c) A computer system has 4 GB of main memory and a virtual address space equal to 16 GB. Each page is 8 KB long. Calculate the number of bits needed for Physical Page Number (PPN) and Virtual Page Number (VPN) [2]

(d) Define TLB. Explain the usage of TLB in Address Translation. [2]