United International University

Department of CSE
CSE 313: Computer Architecture
Midterm Examination
Summer 2021

Time: 1 Hour **Full Marks: 20**

[Any examinee found adopting unfair means will be expelled from the trimester / program as per UIU disciplinary rules.]

[N.B.: Answer all the questions. Assume any data if it is not mentioned explicitly.]

1. A program executes in 350 milliseconds on a computer, of which 75 milliseconds is spent on Arithmetic operations, 75 milliseconds on Conditional operations and 35 milliseconds on Branch Operations, and rest of the time in other overheads. Find out the time affected and unaffected. [4]

   Suppose we are trying to improve the run time by using a better ALU that only improves the time for Arithmetic operations and Branch operations. Determine if we can get 2 (two) times overall better performance only by changing the ALU or not.

2.
```
int add_numbers (int n)
{
      int x = 2;

      for (i = 0; i! = 5; i++)
      {
         x = x + i;

         if(x<5)
             x = x - 10;
         x++;
      }
      return x;
}
```

Assume that the variables n, x and i are in $a0, $s0 and $s1 accordingly.

a) Write the MIPS code for the C function mentioned above. Include the code for storing and restoring the spilling registers in stack. [5]

b) Suppose the code of the function starts at byte address 1000. Write the corresponding machine code for your answer in question 2 (a). No need to convert into binary, just mention the field-wise decimal values in a table. [**Take help from the tables on the next page for the address of the registers**] [5]

c) We know that J type instructions are for unconditional jumps. In J type MIPS instruction fields, what is the maximum value of the jump possible? Give brief description. [2]

3. Use optimized multiplication algorithm to multiply two binary numbers A by B, where A = 0101 and B = 1011. Show all the steps required to complete this multiplication. [4]

MIPS Machine Codes

Instruction	Opcode	Function Code
add	0	32
sub	0	34
lw	35	
sw	43	
and	0	36
or	0	37
nor	0	39
andi	12	
ori	13	
sll	0	0
srl	0	2
beq	4	
bne	5	
slt	0	42
j	2	
jr	0	8
jal	3	
addi	8	

MIPS Registers

Name	Register Number
$zero	0
$at	1
$v0-$v1	2-3
$a0-$a3	4-7
$t0-$t7	8-15
$s0-$s7	16-23
$t8-$t9	24-25
$k0-$k1	26-27
$gp	28
$sp	29
$fp	30
$ra	31