United International University
Department of CSE
CSE 313: Computer Architecture
Final Examination
Fall 2022

Time: 2 Hours Full Marks: 40

[N.B.: Answer all the questions. Assume any data if it is not mentioned explicitly.]

1. a) Mr. X is trying to figure out the exact instruction to complete the conversion from C code to assembly language. He wants to execute the instruction in a single-cycle data path. However, he is using MIPS architecture where NOT instruction is not available. Can you help him to figure out the solution so that he can modify the block diagram for a single-cycle data path? Please write the control unit values as well. [5]

Here is the C code he is trying to execute.

a=b'

b) Modify the block diagram for the single-cycle data path to execute the instruction **'jr'**. Also, find the control unit values. [5]

c) For instruction **'bne'**, find the possible values that can be obtained in the PC register. [3]

2. Consider a processor that goes through the following six stages while executing an instruction.

Instruction Fetch	Instruction Decode	Register Read	ALU Operation	Memory Access	Register Write
100 ns	150 ns	200 ns	250 ns	200 ns	150 ns

Also consider the following instruction snippet:

```
add $s0, $s1, $s2
add $s1, $s0, $s3
sub $t0, $s0, $s1
sw  $t0, 20($s7)
add $t1, $t0, $t3
sub $t2, $s6, $s7
add $s4, $t0, $t2
```

Now answer the following questions:

a) If basic pipelining is implemented in your processor, how many times faster will the instruction snippet execute (i.e., the speedup factor) compared to a single-cycle implementation? There is no need to include a timing diagram in your answer. [5]

b) Suggest a hardware change that you can implement in your processor to improve the execution time of the instruction snippet. What would be the execution time after this change? Include a timing diagram in your answer. [5]

c) Explain how an optimized compiler can improve the execution time of the instruction snippet further. In your answer, clearly show any changes that might be brought in the given instruction snippet. [4]

3. Consider, you have decided to design a 1 KB cache and your block size is 2 words. Consider that your main memory is byte-addressable and each memory address consists of 16 bits.

(a) Find the number of offset and tag bits. [2]

(b) Find the hit rate if you access the following memory addresses in the given order. Assume that the cache is initially empty. [3]

6, 11, 31, 1027, 5, 1032, 12, 4

(c) Now consider that the cache memory is modified such that the size of the tag field becomes 4 bits and the number of cache blocks becomes 256. Determine the new number of words per block from this and then find the miss rate for the accessing the memory addresses in 4(b). [3]

4. Consider a 512 KB cache with an offset of 18. The memory address field of the cache consists of 64 bits.

(a) Calculate the size of the tag field. [2]

(b) Calculate the actual size of the cache. [3]