



United International University  
Department of CSE  
CSE 313: Computer Architecture  
Midterm Examination  
Fall 2021

Time: 1 Hour and 45 minutes

Full Marks: 30

[N.B.: Answer all the questions. Assume any data if it is not mentioned explicitly.]

1. a) Alternative compiled code sequences are using same instructions as **add**, **sub** and **beq**. [4]  
A table is given to show their required number of cycles per instruction(CPI) and the instruction count(IC) on each code sequences.

Find out the number of clock cycles and average CPI for all the code sequences.

Instruction	add	sub	beq
CPI for each	3	4	7
Code sequence 1 IC	240	300	500
Code sequence 2 IC	320	100	150

- b) Consider a computer running a program that requires 400 s, with 90 s spent executing FP instructions, 180 s executed L/S instructions, and 60 s spent executing branch instructions. Find out affected and unaffected time for Amdahl's law. What is the improvement factor using Amdahl's law if we get the program completion time improved by 4x? [4]

- c) What is the power wall? Please explain briefly. [2]

2. Consider the following C function that accepts two arguments, *higher* and *lower*, calculates the sum of all values stored between the *higher* and *lower* indexes of the array *arr*, and returns the result.

```
int func(int higher, int lower){
    int current = lower;
    int sum = 0;
    while(current <= higher){
        sum = sum + arr[current];
        current++;
    }
    return sum;
}
```

Given that the variable *current* corresponds to the register \$s0, *sum* to \$s1, *arr* to \$s2, and the starting address of the instructions in memory is 2400.

a) Write down the output of passing the code above through a MIPS **compiler**. [5]

b) Write down the output of passing the code above through a MIPS **assembler**. [5]

c) Suppose you want to **call the function above from the main function**. What assembly operation would you use? Explain the functionality of this operation. [3]

d) Suppose a MIPS architect has designed a new **branch** instruction of the following format: [2]

op (6 bits)	rs (8 bits)	rt (8 bits)	address (10 bits)
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What will be highest possible value of address in the corresponding MIPS **assembly** code?

3. Use division algorithm to divide B by A, where A = 0111 and B = 1101. Show all the steps required to complete this division. [5]

#### MIPS Machine Codes

Instruction	Opcode	Function Code
add	0	32
sub	0	34
lw	35	
sw	43	
and	0	36
or	0	37
nor	0	39
andi	12	
ori	13	
sll	0	0
srl	0	2
beq	4	
bne	5	
slt	0	42
j	2	
jr	0	8
jal	3	
addi	8	