United International University (UIU)

Dept. of Computer Science & Engineering (CSE)

Midterm: Fall - 2023

Course: CSI 426 || Simulation and Modeling

Marks: 30, Time: 1 hour 45 Minutes

Figures in the right-hand margin indicate full marks.

Any examinee found adopting unfair means will be expelled from the trimester/ program as per UIU disciplinary rules.

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1. *(a)* In the Buffon's Needle experiment, the following graph was derived for a specific setup. The equation of the curve $f(x) = \frac{4}{3}\cos(\theta)$. Now, calculate the probability of intersection *p(hit)*. **[3]**

   (b) Suppose you have opened a new ATM booth at UIU and it's getting a great response from your friends. But the machine can serve only one customer at a time. So, sometimes there is a long queue in front of the booth. Consider the following sequence of events. The arrival times for the students are given, along with the times they will need to get served.

Customer Name	Arrival time	Service Time
P	*3*	2
Q	*5*	3
R	*9*	5
S	*11*	4
T	*17*	4
U	*18*	3
V	*19*	1

[2]

[4]

2. (a) Design an ALU with two selection variables, S_1 and S_0, that generates the following operations. Find the equations of X, Y and Z. *[Do not draw any diagram]* **[5]**

S_1	S_0	C_{IN}	FUNCTION
0	0	X	A **or** B
0	1	X	A **and** B
1	0	0	$A + 1$
1	0	1	A
1	1	0	$A - B$
1	1	1	$A - B - 1$

(b) Let us assume you have two 4-bit numbers A and B. You have performed subtraction(A-B) and the condition of the status bits was as follows: **[2]**

i) S = 1, V = 0, Z = 0

ii) S = 0, V = 1, Z = 0

Write the relation between two numbers A and B

3.

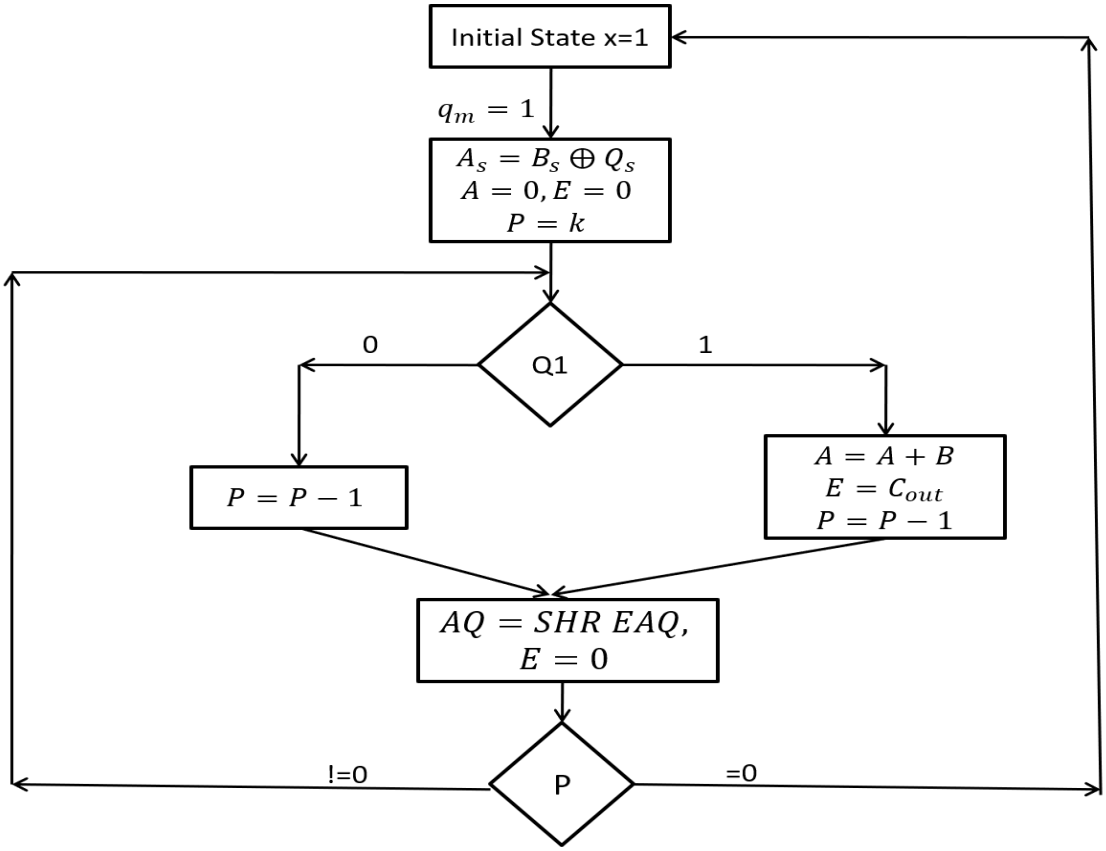

Figure 1: Flowchart for Multiplication (Question 3-a)

(a) Suppose you are implementing Multiplication according to the flowchart shown in **Figure 1**. While multiplying, in order to store necessary inputs and outputs, consider taking these 4-bit registers: *A, B(Multiplicand), Q(Multiplier),* and *P(Number of remaining bits to multiply),* along with these flip-flops: A_s, *E*. **[4]**

Now, for this configuration, simulate the multiplication process (showing every step) for these 4-bit positive binary numbers: *1101(Multiplicand)* and *1010(Multiplier).*

(b) Suppose you are implementing the state diagram shown in **Figure 2** using the *Sequence Register and Decoder* Method. Find the necessary equations for all the flip-flops to be used in this method. **[4]**

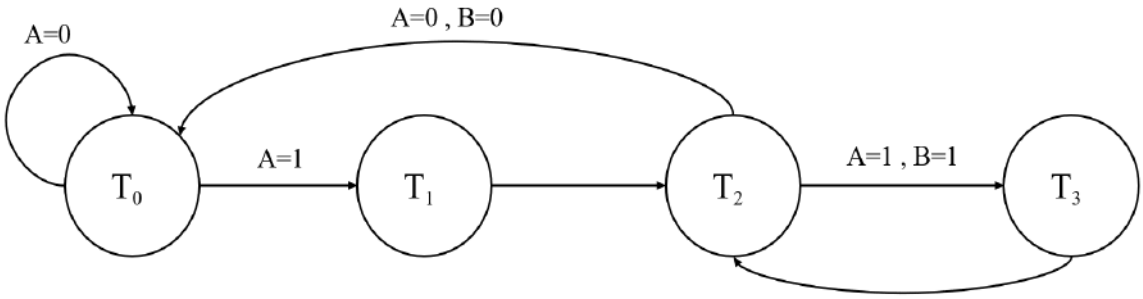

Figure 2: State Diagram for Question 3-b

(c) Imagine a new startup company BDtel is designing a Multiplication Control Logic Unit for 16-bit binary numbers. Their simple design uses 16-bit registers with the following configuration of the components:

Information Regarding Control Organization	
No. of States in the State Diagram	128
No. of Flip-flops used for this State Diagram	128

Soon they realized that their design uses a large number of components, which will make it expensive and big in size. To reduce both the cost and the size, they consulted with you. Would you advise them to make any changes in the design? If yes, what are the changes and why? If not, why not?

4. We have the algorithm for the addition-subtraction problem of signed numbers in **Figure 3**. The list of control signals **(Table 2)** to be generated and the required ALU **(Table 1)** operation signals are also given here. Determine the functions of each control signal. Mention the actions of each state. [*You do not need to draw the flowchart or state diagram.]* **[4]**

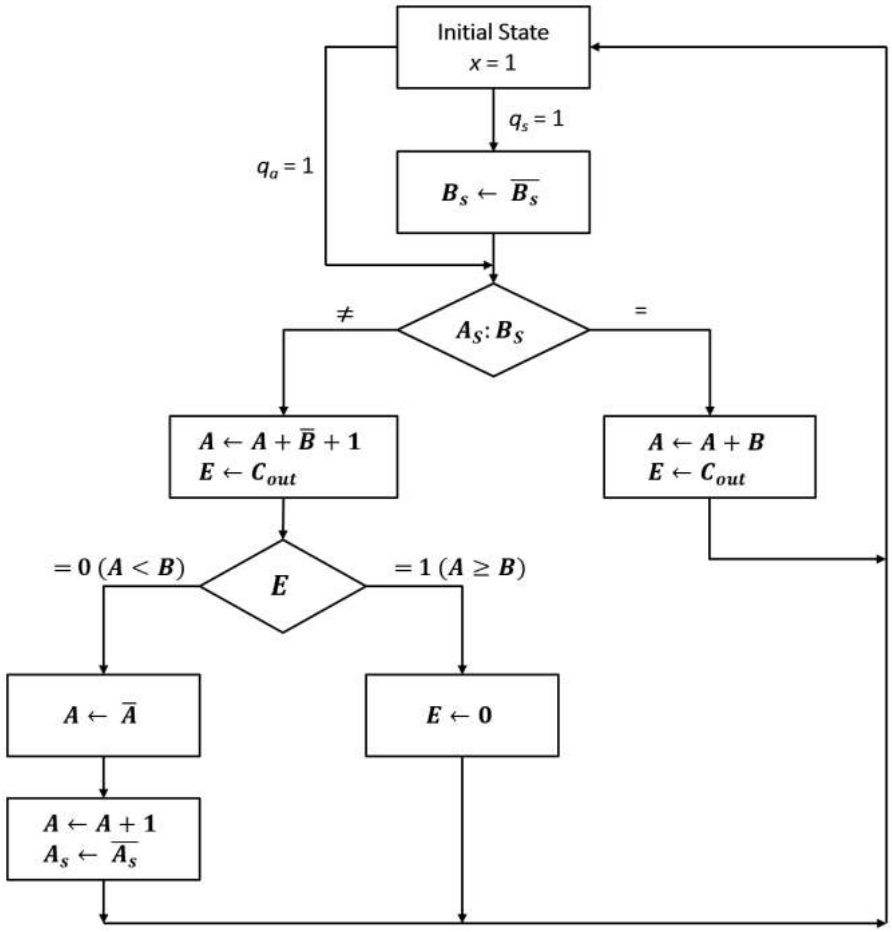

Figure 3: Flowchart for Addition-Subtraction (Question 4)

Table 1 ALU Specification

S_2	S_1	S_0	C_{in}	*Operation*
0	1	1	0	A + 1
0	1	0	0	A + B
1	1	0	0	$\bar{A}$
1	0	1	0	A - B

Table 2 Control Signals

Control Signals
x (Initial State)
S_2
S_1
S_0
C_{in}
L (Load A and E)
p (Complement B_s)
q (Complement As)
r (Reset E)