United International University

Department of Computer Science and Engineering

EEE 2123 : Electronics

Final Exam : Spring 2023 Time: 2 hours Marks: 40

There are five questions here. Answer **all of them.**

1. (a) The threshold voltage of each MOSFET in the following figure is V_t= 0.4 V. Determine the region of operation of the MOSFET in each circuit. [4]

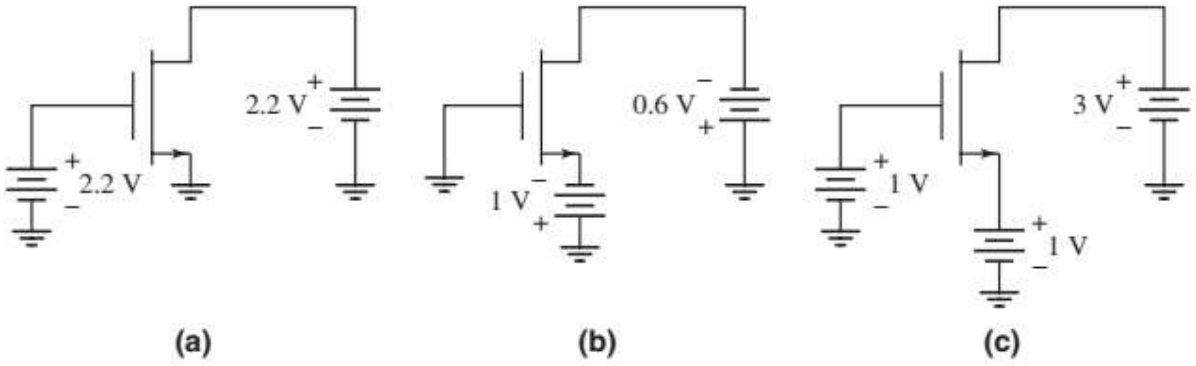

Figure 1: Circuit diagram for Q-1(a)

(b) For the n-MOS in the following circuit, the parameters are V_t = 0.4 V, k'_n= 120 μ A/V^2, and W/L = 25. Find out V_{GS}, V_{DS} and I_D. [6]

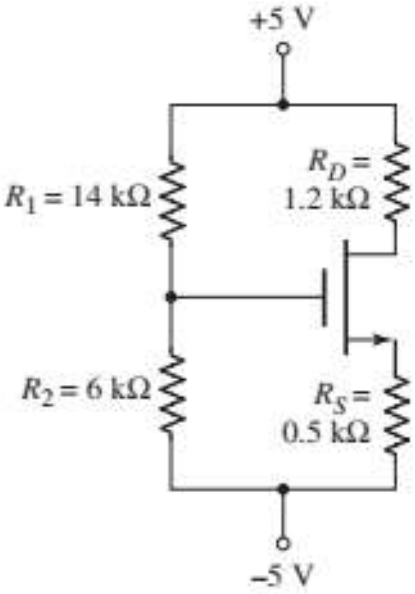

Figure 2: Circuit diagram for Q-1(b)

(c) For a particular NMOS, V_G, V_t and V_S are +2 V, 1 V and -2 V respectively. With proper calculation, find out the operating region if the drain terminal is shorted with the source. [4]

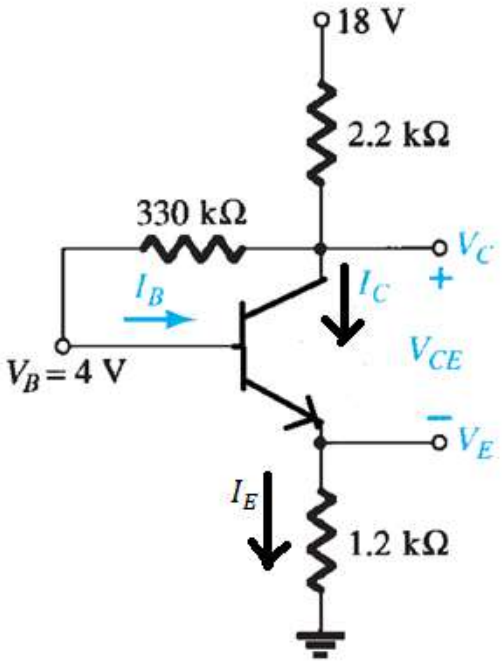

Figure 3: Circuit diagram for Q-2(a)

2. (a) Given $V_B = 4$ V for the network of the following figure, determine $V_E, V_C, I_C, I_B, I_C, I_E$ and β. [7]

   (b) Find the value of V_0 from the following figure. [4]

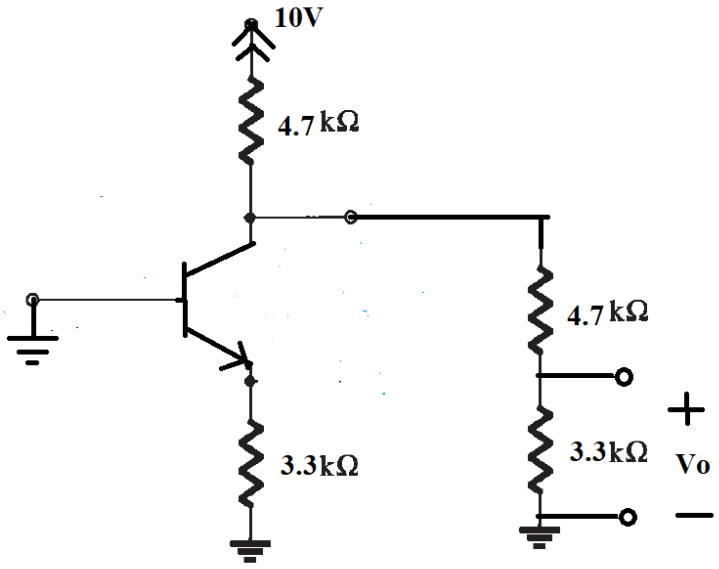

Figure 4: Circuit diagram for Q-2(b)

3. Can you replace a resistor with a MOSFET? If yes, give explanation with proper characteristic curve. [The characteristic curve should be properly labelled] [4]

4. Consider the following Boolean function:

$$A = [(a' + b + c')d + e'f']g + h'$$

(a) Obtain the complementary function using the concept of De Morgan's theorem. [2]

(b) Draw only the **NMOS** representation of the function obtained in (a) using the concept of CMOS technology. [3]

5. Design an amplifier circuit that can generate the following outputs:

(a) $v_0 = 0$ where input v_i is a sine wave. [3]

(b) $v_0 = 15\int v_i dt - 10\frac{dv_i}{dt}$ [3]

Clearly mention the values of all circuit parameters in the diagram. Assume the value of capacitor to be 10 μF in all cases.