



# United International University (UIU)

Department of Computer Science and Engineering  
CSE 225: DIGITAL LOGIC DESIGN, Midterm Fall 2018

Total Marks: 40

Duration: 2 hour

## Section A: Answer both of the Questions, 1 and 2.

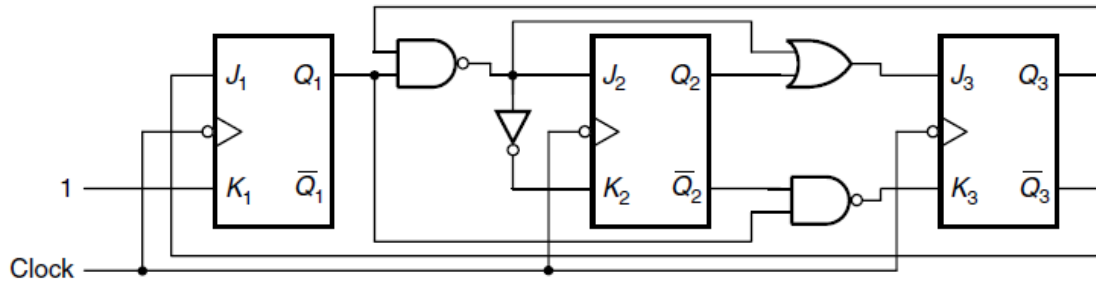
1.	<p>For the given state diagram, find out (a) the flip-flops' input table, (b) equations and (c) the logic diagram when <b>J-K flip-flops</b> are being used</p>	<table border="1"> <caption>(a) JK Flip-Flop</caption> <thead> <tr> <th><math>Q(t)</math></th><th><math>Q(t+1)</math></th><th>J</th><th>K</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>0</td><td>X</td></tr> <tr> <td>0</td><td>1</td><td>1</td><td>X</td></tr> <tr> <td>1</td><td>0</td><td>X</td><td>1</td></tr> <tr> <td>1</td><td>1</td><td>X</td><td>0</td></tr> </tbody> </table>	$Q(t)$	$Q(t+1)$	J	K	0	0	0	X	0	1	1	X	1	0	X	1	1	1	X	0	[3+ 3+ 2]
$Q(t)$	$Q(t+1)$	J	K																				
0	0	0	X																				
0	1	1	X																				
1	0	X	1																				
1	1	X	0																				
2.	<p>Using <b>D flip-flops</b>, design a synchronous counter that goes through the sequence, 7, 4, 3, 6, 1, 2 ... and repeat. You have to show (a) the flip-flops' input table, (b) equations and (c) the logic diagram.</p>		[3+ 3+ 2]																				

## Section B: Answer any two of the Questions from 4, 5 and 6.

3.	<p>A) An electronic game uses an array of seven LEDs (light-emitting diodes) to display the results of a random roll of a die. Use a 3-to-8-line decoder and OR gates to map the 3-bit combinations on inputs <math>X_2</math>, <math>X_1</math>, and <math>X_0</math> for values 1 through 6 to the outputs <b>a</b> through <b>g</b>. Input combinations 000 and 111 are don't-cares.</p> <p>B) Construct a 1-bit full adder using two 1-bit half adders.</p>	[6]
4.	<p>A) Implement the following Boolean function F with an 8-to-1 line multiplexer and necessary basic logic gates.</p> $F(A, B, C, D) = \sum m(0, 2, 4, 5, 7, 9, 10, 11, 15)$ <p>B) Design a 3-to-8 active low decoder using 2-to-4 active low decoder. Label the decoder pin names and their inputs/outputs carefully.</p>	[5] [3]
5.	<p>A) Design an 8-to-1 multiplexer using 4-to-1 multiplexer and 2-to-1 multiplexer.</p> <p>B) Design an Octal-to-Binary encoder. Show the function table and the equations only.</p> <p>C) Design a 6-bit full adder using multiple 2-bit full adders. Show the diagram only.</p>	[3] [3] [2]

**Section C: Answer any one Question from 7 and 8.**

6. A) What sequence should be repeated for the sequential circuit of the following Figure for the following initial state  $Q_3Q_2Q_1$ : 001? [6]



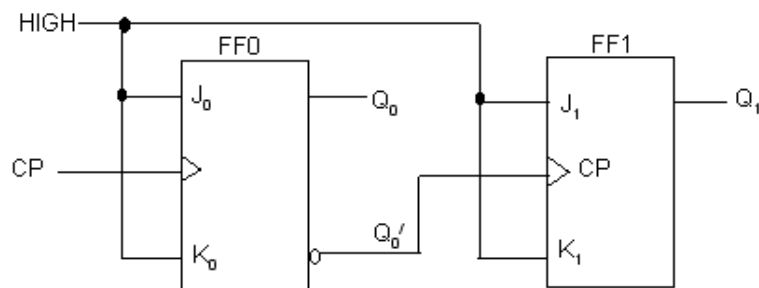
- B) Draw the diagram of a master-slave flip-flop using D flip-flops. [2]

7. A) Design a 4 bit register which can do the following operations based on the two control INPUTS X and Y as given below: [5]

X	Y	Operation
0	0	Right Shift
0	1	Parallel Load
1	0	1's complement
1	1	Left Shift

You can use any kind of flip-flops and other necessary gates as required. Draw a neat logic diagram of your solution.

- B) Following is a logic diagram for an asynchronous ripple counter. [3]



Now, if the FF1 is replaced with a flip-flop that has negative edge triggered clock, the circuit will behave in a different way. Find out the sequence it will show in  $Q_1Q_0$  for that situation.