United International University
Department of Computer Science and Engineering

CSE-3313: Computer Architecture
Final Examination: Spring 2024
Total Marks: 40 Time: 2 hours

Any examinee found adopting unfair means will be expelled from the trimester / program as per UIU disciplinary rules.

Answer all questions. Numbers to the right of the questions denote their marks.

1. (a) You have to modify the block diagram for the single-cycle data path so that it can execute the following instruction **'rma'**. Also, write the control unit values for this instruction: **rma $t1, $s2, 1016**. This instruction will read the values of the source register(**rs**), multiply the value by 4, and pass the result to the ALU unit. The value in the given memory address will be the other operand of the ALU unit. The ALU performs an addition operation between the operands and the result is stored in the register **rt**. The machine code format for the instruction is given below table-2, where rs, rt will contain the index numbers of $t1 and $s2 registers, respectively. [5]

op	rs	rt	C/A
6 bits	5 bits	5 bits	16 bits

Table 1: machine code format of instruction **rma**

(b) Modify the block diagram for a single-cycle data path so that it can execute the following instruction **'jt $s0, $s1, 2000'**. Note that, the job of the given instruction is to jump to the given address if the value of the first source register(**$s0**) is greater than the second source register(**$s1**). Write down the control unit values as well. [5]

2. Consider a processor that goes through the following seven stages while executing an instruction

Instruction Fetch (IF)	150 ns
Instruction Decode (ID)	120 ns
Register Read (RR)	100 ns
Execution (EXE)	250 ns
Memory Read (MEMR)	180 ns
Memory Write (MEMW)	220 ns
Write Back (WB)	200 ns

Table 2: Seven stages pipeline

(a) Find out the total time for the given code below in a single cycle method. [2]

Listing 1: Code for 2(a)

```
1     addi $t0, $zero, 0
2     addi $s1, $zero, 1
3
4     LOOP:
5     beq $s1, 6, ENDLOOP
6     add $t0, $t0, $s1
7     addi $s1, $s1, 1
8     j LOOP
9
10    ENDLOOP:
11    sub $s0, $s2, $s3
```

(b) Implement the basic pipeline method and find out the total time using a timing diagram. [5]

(c) If we want to reduce the stalls, what method we should apply? Justify your answer with a timing diagram. [5]

Listing 2: Code for 2(b) and 2(c) and 2(d)

```
lw $t0, 8($s1)
sw $t0, 20($s1)
add $s2, $s2, $s0
addi $s0, $s2, 4
ori $t1, $t3, 1
```

(d) Find the optimal solution without a timing diagram. Can we remove all the stalls? Explain. [3]

3. (a) CPU has clock rate of 0.5 GHz and a 1KB direct mapped cache with 4 words data block. CPU generates 16 bits address. Memory is byte-addressable.

index	V	D	tag	data
0	0	?	?	-
0	0	?	?	-
...	-	-	-	-
...	-	-	-	-
$2^n - 1$	-	-	-	-

Table 3: Direct mapped cache

i. Calculate the actual size of the cache. [3]

ii. Find the hit rate if you access the following memory addresses in the given order. Assume that the cache is initially empty.
400, 918, 1426, 122, 410, 916 [4]

iii. If hit time is 2 clock cycles and miss penalty 60 clock cycles, then calculate the average memory access time. [2]

(b) Data block size in cache is 8 words and there are 4 cache blocks. Memory is byte-addressable.

i. How many 32 bits integers can be stored in a cache block.

ii. Find out the miss rate for the following code. **Initially, the array arr is not in the cache and i is in the register.** [2+4]

```
int main()
{
    int arr[64];
    for(int i=0;i<64;i++)  arr[i]=i;
    for(int i=63;i>0;i--)  printf("%d ",a[i]);
}
```