



United International University (UIU)
Dept. of Computer Science & Engineering (CSE)
Mid-Term Exam, Trimester: Fall 2023

Course Code: CSE 113/EEE 2113; **Course Title:** Electrical Circuits

Total Marks: 30; **Duration:** 1 hour 45 minute(s)

Any examinee found adopting unfair means would be expelled from the trimester/ program as per UIU disciplinary rules.

Question 1: Answer all the questions.

(8 Marks)

The charge flowing in a resistive load is shown in **Figure 1**. Based on the figure, answer the following questions:

[4+2
+2]

- i) Sketch the corresponding current clearly.
- ii) If the voltage across the load is 5V at $t = 3.5s$, what power will the load absorb at that time? Also, determine the resistance of this load.

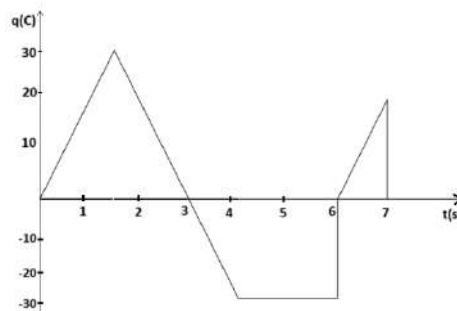


Figure 1.

Question 2: Answer all the questions.

(8 Marks)

For the circuit shown in **Figure 2**, answer the following questions:

[2+3
+3]

- i) Apply KCL at Node A and write the current equation. Then, find the value of I_3 .
- ii) Apply KVL for the first loop (I_1) and find the value of I_1 .
- iii) Apply KVL in the second loop (I_2) and write the equation. Then find the value of V_x as indicated in the circuit.

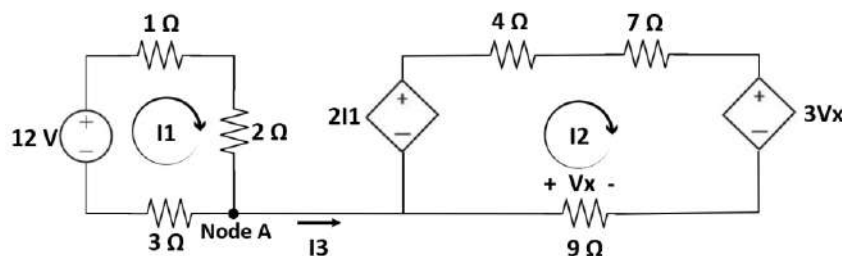


Figure 2.

Question 3: Answer all the questions

(6 Marks)

Answer the following questions for the circuit shown in **Figure 3 (a-b)**:

[3+3]

- i) Find R_{ab} for the circuit shown in **Figure 3(a)**.
- ii) Determine each current (i_1, i_2, i_3, i_4) in the circuit shown in **Figure 3(b)**.

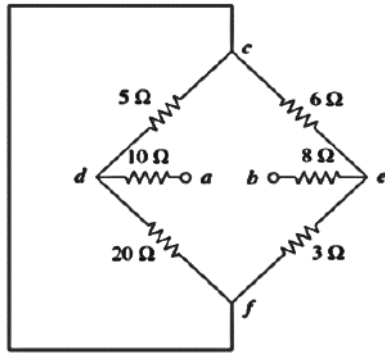


Figure 3(a)

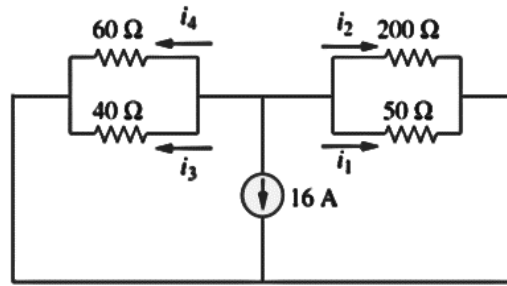


Figure 3(b)

Question 4: Answer all the questions.

(4 Marks)

For the circuit shown in **Figure 4**, determine i_o and v_o using **mesh analysis**.

[2+2]

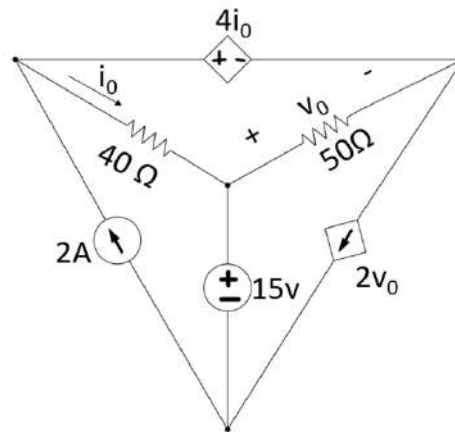


Figure 4.

Question 5: Answer all the questions.

(4 Marks)

Let's assume the V_x node voltage is 20V in the circuit shown in **Figure 5**. Now, answer the following questions using **node analysis**:

[2+2]

- Calculate all the other node voltages in the circuit using node analysis.
- Determine the power supplied or absorbed by the source(s) in the circuit.

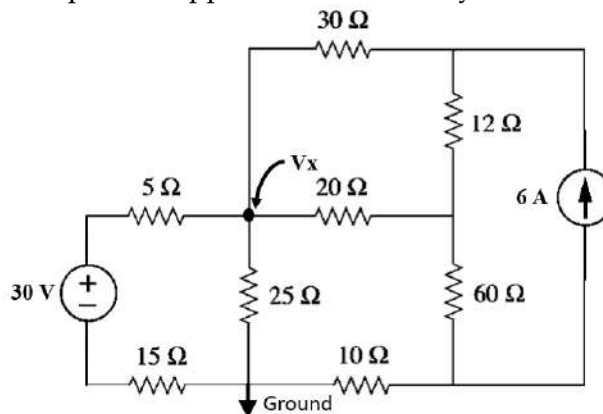


Figure 5.