United International University (UIU)

Dept. of Computer Science & Engineering (CSE)

Mid-Term Exam::Trimester::Fall 2019

Course Code: CSE 425 Course Title: Microprocessor, Microcontroller and Interfacing
Sec: (A, B, C) Total Marks: 30 Duration: 1hr 45 minutes

Question 1: Answer all the questions. (12 Marks)

a. Draw detail block diagram of Direct memory access (DMA) controller interfacing with microprocessor 8086 showing different buses. [2]

b. Explain the value of the Status flags of the 8086 microprocessor after executing the second instruction (shown below). [2]

1st instruction: `MOV BL, DAH`
2nd instruction: `ADD BL, 9FH`

c. Suppose, keyboard is connected with the PORT A and printer is connected with PORT B of the microcomputer system (see table 1). **Standard I/O technique** is used for input and output operation. Write down the **instruction** in assembly language to read value from the keyboard, increment the value by 3 (three) and then print the value using the printer. [2]

PORT name	Input / Output device
PORT A	Keyboard
PORT B	Printer

Table: 1

d. Explain each software interrupt instruction in two to four sentences: INT 3, INTO. What is the purpose of the Interrupt Vector Table? Explain in one to two sentences. [2+1]

e. Consider a microcomputer system in which transfer of BUS control (DMA request processing) from the microprocessor to DMA device takes 5×10^{10} picosecond and DMA device to the microprocessor (DMA bus release) takes 3×10^{7} nanosecond. One of the I/O devices has data transfer rate of 23 MB/sec and employs DMA. Calculate the time (in second) DMA takes to transfer a block of 2 GB of data using **burst mode**. Show the corresponding data transfer operation using a **sequence diagram**. Suppose, data are transferred two byte in one cycle. (1 picosecond $=1 \times 10^{-9}$ millisecond) [2+1]

Question 2: Answer all the questions. (18 Marks)

a. Draw the diagram of 8-bit microprocessor with 24-bit address bus interfaced with 512 KB RAM using the **Linear Decoding technique**. Each RAM chip has 16-bit address bus and 8-bit data bus. [2.5+ 1.5+ 1]
Suppose there are **n** number of addresses in a RAM chip then write down the **1st, 7th, (n−8) th** address for accessing **3rd** and **6th** RAM chip by the microprocessor. What is the maximum memory capacity, which could be interfaced with the microprocessor under this configuration using the Linear Decoding technique? (Show necessary calculation)

b. Draw the diagram of the 16-bit microprocessor with 20-bit address bus interfaced with 80 KB RAM using the **Full Decoding technique** (use optimum decoder size). Each RAM chip has 12-bit address bus and 16-bit data bus. [2.5+ 1.5+ 1]
Suppose there is **n** number of addresses in a RAM chip then write down the **4th, 1023th** and **(n−1) th** address for accessing **0th** and **32th** RAM chip by the microprocessor. What is the maximum memory capacity, which could be interfaced with the microprocessor under this configuration using the Full Decoding technique? (Show necessary calculation)

c. Suppose you need to implement, a **matrix keyboard** (3*2) interfacing with the microprocessor through 82C55 peripheral interface Port A and Port C. Additionally, a **matrix led** (2*2) interfaced with Port A and Port B. [3+1]

i. Draw the corresponding connection diagram between the **matrix keyboard**, **matrix led** and 82C55 based on the above-mentioned configuration.

ii. Write down the appropriate **command byte A** for 82C55 command register in **figure 1** to implement the above-mentioned configuration.

d. "In **linear decoding**, the address map of the microprocessor is contiguous and it is not sparsely distributed". [3]
Do you agree or disagree with this statement? Explain and justify your opinion with an example in three to five sentences.

e. Draw the block diagram of DRAM. [1]

[redacted]