FPCVT Project Status (01/21/2021 - 04:15:23)			
Project File:	FPCVT.xise	**Parser Errors:**	No Errors
Module Name:	FPCVT	**Implementation State:**	Placed and Routed
Target Device:	xc6slx16-3csg324	• **Errors:**	No Errors
Product Version:	ISE 14.7	• **Warnings:**	No Warnings
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary [-]				
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	0	18,224	0%	
Number of Slice LUTs	50	9,112	1%	
Number used as logic	50	9,112	1%	
Number using O6 output only	34			
Number using O5 output only	12			
Number using O5 and O6	4			
Number used as ROM	0			
Number used as Memory	0	2,176	0%	
Number of occupied Slices	23	2,278	1%	
Number of MUXCYs used	16	4,556	1%	
Number of LUT Flip Flop pairs used	50			
Number with an unused Flip Flop	50	50	100%	
Number with an unused LUT	0	50	0%	
Number of fully used LUT-FF pairs	0	50	0%	
Number of slice register sites lost to control set restrictions	0	18,224	0%	
Number of bonded IOBs	22	232	9%	
Number of RAMB16BWERs	0	32	0%	
Number of RAMB8BWERs	0	64	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	0	16	0%	
Number of DCM/DCM_CLKGENs	0	4	0%	
Number of ILOGIC2/ISERDES2s	0	248	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	248	0%	
Number of OLOGIC2/OSERDES2s	0	248	0%	
Number of BSCANs	0	4	0%	
Number of BUFHs	0	128	0%	

Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	32	0%	
Number of ICAPs	0	1	0%	
Number of MCBs	0	2	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	2	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	3.09			

Performance Summary			[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:			

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Thu Jan 21 04:14:57 2021	0	0	0
Translation Report	Current	Thu Jan 21 04:15:03 2021	0	0	0
Map Report	Current	Thu Jan 21 04:15:10 2021	0	0	6 Infos (0 new)
Place and Route Report	Current	Thu Jan 21 04:15:17 2021	0	0	2 Infos (0 new)
Power Report					
Post-PAR Static Timing Report	Current	Thu Jan 21 04:15:21 2021	0	0	4 Infos (0 new)
Bitgen Report	Out of Date	Mon Jan 18 03:11:17 2021	0	0	0

Secondary Reports			[-]
Report Name	**Status**	**Generated**	
ISIM Simulator Log	Out of Date	Thu Jan 21 04:14:42 2021	
WebTalk Report	Out of Date	Mon Jan 18 03:11:18 2021	
WebTalk Log File	Out of Date	Mon Jan 18 03:11:19 2021	

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