

vending_machine Project Status (01/23/2021 - 06:32:15)			
<b>Project File:</b>	vending_machine.xise	<b>Parser Errors:</b>	No Errors
<b>Module Name:</b>	vending_machine	<b>Implementation State:</b>	Programming File Generated
<b>Target Device:</b>	xc6slx16-3csg324	<b>• Errors:</b>	No Errors
<b>Product Version:</b>	ISE 14.7	<b>• Warnings:</b>	<a href="#">1 Warning (1 new)</a>
<b>Design Goal:</b>	Balanced	<b>• Routing Results:</b>	<a href="#">All Signals Completely Routed</a>
<b>Design Strategy:</b>	<a href="#">Xilinx Default (unlocked)</a>	<b>• Timing Constraints:</b>	<a href="#">All Constraints Met</a>
<b>Environment:</b>	<a href="#">System Settings</a>	<b>• Final Timing Score:</b>	0 <a href="#">(Timing Report)</a>

Device Utilization Summary <span>[+]</span>				
Slice Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Registers	112	18,224	1%	
Number used as Flip Flops	112			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	173	9,112	1%	
Number used as logic	173	9,112	1%	
Number using O6 output only	156			
Number using O5 output only	0			
Number using O5 and O6	17			
Number used as ROM	0			
Number used as Memory	0	2,176	0%	
Number of occupied Slices	59	2,278	2%	
Number of MUXCYs used	4	4,556	1%	
Number of LUT Flip Flop pairs used	184			
Number with an unused Flip Flop	73	184	39%	
Number with an unused LUT	11	184	5%	
Number of fully used LUT-FF pairs	100	184	54%	
Number of unique control sets	7			
Number of slice register sites lost to control set restrictions	24	18,224	1%	
Number of bonded <a href="#">IOBs</a>	17	232	7%	
Number of RAMB16BWERs	0	32	0%	
Number of RAMB8BWERs	0	64	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	1	16	6%	
Number used as BUFGs	1			
Number used as BUFGMUX	0			

Number of DCM/DCM_CLKGENs	0	4	0%	
Number of ILOGIC2/ISERDES2s	0	248	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	248	0%	
Number of OLOGIC2/OSERDES2s	0	248	0%	
Number of BSCANs	0	4	0%	
Number of BUFHs	0	128	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	32	0%	
Number of ICAPs	0	1	0%	
Number of MCBs	0	2	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	2	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	5.17			

Performance Summary				<a href="#">[-]</a>
<b>Final Timing Score:</b>	0 (Setup: 0, Hold: 0)		<b>Pinout Data:</b>	<a href="#">Pinout Report</a>
<b>Routing Results:</b>	<a href="#">All Signals Completely Routed</a>		<b>Clock Data:</b>	<a href="#">Clock Report</a>
<b>Timing Constraints:</b>	<a href="#">All Constraints Met</a>			

Detailed Reports						<a href="#">[-]</a>
Report Name	Status	Generated	Errors	Warnings	Infos	
<a href="#">Synthesis Report</a>	Current	Sat Jan 23 06:13:56 2021	0	<a href="#">1 Warning (1 new)</a>	<a href="#">1 Info (1 new)</a>	
<a href="#">Translation Report</a>	Current	Sat Jan 23 06:14:08 2021	0	0	0	
<a href="#">Map Report</a>	Current	Sat Jan 23 06:14:16 2021	0	0	<a href="#">6 Infos (0 new)</a>	
<a href="#">Place and Route Report</a>	Current	Sat Jan 23 06:14:24 2021	0	0	<a href="#">3 Infos (0 new)</a>	
Power Report						
<a href="#">Post-PAR Static Timing Report</a>	Current	Sat Jan 23 06:14:28 2021	0	0	<a href="#">4 Infos (0 new)</a>	
<a href="#">Bitgen Report</a>	Current	Sat Jan 23 06:32:14 2021	0	0	0	

Secondary Reports			<a href="#">[-]</a>
Report Name	Status	Generated	
<a href="#">ISIM Simulator Log</a>	Current	Sat Jan 23 06:34:52 2021	
<a href="#">WebTalk Report</a>	Current	Sat Jan 23 06:32:15 2021	

<a href="#">WebTalk Log File</a>	Current	Sat Jan 23 06:32:15 2021
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**Date Generated:** 01/23/2021 - 06:35:03