parking_meter Project Status (03/13/2021 - 11:29:06)			
Project File:	parking_meter.xise	**Parser Errors:**	No Errors
Module Name:	parking_meter	**Implementation State:**	Programming File Generated
Target Device:	xc6slx16-3csg324	• **Errors:**	No Errors
Product Version:	ISE 14.7	• **Warnings:**	No Warnings
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary [-]				
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	96	18,224	1%	
Number used as Flip Flops	96			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	1,140	9,112	12%	
Number used as logic	1,132	9,112	12%	
Number using O6 output only	980			
Number using O5 output only	61			
Number using O5 and O6	91			
Number used as ROM	0			
Number used as Memory	0	2,176	0%	
Number used exclusively as route-thrus	8			
Number with same-slice register load	1			
Number with same-slice carry load	7			
Number with other load	0			
Number of occupied Slices	397	2,278	17%	
Number of MUXCYs used	324	4,556	7%	
Number of LUT Flip Flop pairs used	1,156			
Number with an unused Flip Flop	1,070	1,156	92%	
Number with an unused LUT	16	1,156	1%	
Number of fully used LUT-FF pairs	70	1,156	6%	
Number of unique control sets	8			
Number of slice register sites lost to control set restrictions	24	18,224	1%	
Number of bonded IOBs	35	232	15%	
Number of RAMB16BWERs	0	32	0%	
Number of RAMB8BWERs	0	64	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	

Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	1	16	6%	
Number used as BUFGs	1			
Number used as BUFGMUX	0			
Number of DCM/DCM_CLKGENs	0	4	0%	
Number of ILOGIC2/ISERDES2s	0	248	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	248	0%	
Number of OLOGIC2/OSERDES2s	0	248	0%	
Number of BSCANs	0	4	0%	
Number of BUFHs	0	128	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	32	0%	
Number of ICAPs	0	1	0%	
Number of MCBs	0	2	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	2	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	4.70			

Performance Summary			[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Sat Mar 13 11:22:16 2021	0	0	8 Infos (0 new)
Translation Report	Current	Sat Mar 13 11:28:23 2021	0	0	0
Map Report	Current	Sat Mar 13 11:28:40 2021	0	0	6 Infos (6 new)
Place and Route Report	Current	Sat Mar 13 11:28:50 2021	0	0	3 Infos (3 new)
Power Report					
Post-PAR Static Timing Report	Current	Sat Mar 13 11:28:55 2021	0	0	4 Infos (4 new)
Bitgen Report	Current	Sat Mar 13 11:29:05 2021	0	0	0

Report Name	Status	Generated
ISIM Simulator Log	Current	Sat Mar 13 11:29:45 2021
WebTalk Report	Current	Sat Mar 13 11:29:06 2021
WebTalk Log File	Current	Sat Mar 13 11:29:06 2021

Date Generated: 03/13/2021 - 11:29:57