

clock_gen Project Status (01/21/2021 - 22:39:16)			
Project File:	clock_gen.xise	Parser Errors:	No Errors
Module Name:	clock_gen	Implementation State:	Placed and Routed
Target Device:	xc6slx16-3csg324	• Errors:	No Errors
Product Version:	ISE 14.7	• Warnings:	No Warnings
Design Goal:	Balanced	• Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	All Constraints Met
Environment:	System Settings	• Final Timing Score:	0 (Timing Report)

Device Utilization Summary [+]				
Slice Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Registers	19	18,224	1%	
Number used as Flip Flops	19			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	15	9,112	1%	
Number used as logic	15	9,112	1%	
Number using O6 output only	9			
Number using O5 output only	0			
Number using O5 and O6	6			
Number used as ROM	0			
Number used as Memory	0	2,176	0%	
Number of occupied Slices	8	2,278	1%	
Number of MUXCYs used	0	4,556	0%	
Number of LUT Flip Flop pairs used	16			
Number with an unused Flip Flop	2	16	12%	
Number with an unused LUT	1	16	6%	
Number of fully used LUT-FF pairs	13	16	81%	
Number of unique control sets	3			
Number of slice register sites lost to control set restrictions	13	18,224	1%	
Number of bonded IOBs	16	232	6%	
Number of RAMB16BWERs	0	32	0%	
Number of RAMB8BWERs	0	64	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	1	16	6%	
Number used as BUFGs	1			

Number used as BUFGMUX	0			
Number of DCM/DCM_CLKGENs	0	4	0%	
Number of ILOGIC2/ISERDES2s	0	248	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	248	0%	
Number of OLOGIC2/OSERDES2s	0	248	0%	
Number of BSCANs	0	4	0%	
Number of BUFHs	0	128	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	32	0%	
Number of ICAPs	0	1	0%	
Number of MCBs	0	2	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	2	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	4.39			

Performance Summary				[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	Pinout Data:	Pinout Report	
Routing Results:	All Signals Completely Routed	Clock Data:	Clock Report	
Timing Constraints:	All Constraints Met			

Detailed Reports						[-]
Report Name	Status	Generated	Errors	Warnings	Infos	
Synthesis Report	Current	Thu Jan 21 22:38:42 2021	0	0	4 Infos (4 new)	
Translation Report	Current	Thu Jan 21 22:38:54 2021	0	0	0	
Map Report	Current	Thu Jan 21 22:39:02 2021	0	0	6 Infos (0 new)	
Place and Route Report	Current	Thu Jan 21 22:39:08 2021	0	0	3 Infos (0 new)	
Power Report						
Post-PAR Static Timing Report	Current	Thu Jan 21 22:39:13 2021	0	0	4 Infos (0 new)	
Bitgen Report						

Secondary Reports			[-]
Report Name	Status	Generated	
ISIM Simulator Log	Out of Date	Thu Jan 21 22:38:31 2021	

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