vending_machine Project Status (01/23/2021 - 06:32:15)			
Project File:	vending_machine.xise	**Parser Errors:**	No Errors
Module Name:	vending_machine	**Implementation State:**	Programming File Generated
Target Device:	xc6slx16-3csg324	• **Errors:**	No Errors
Product Version:	ISE 14.7	• **Warnings:**	1 Warning (1 new)
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary [-]				
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	112	18,224	1%	
Number used as Flip Flops	112			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	173	9,112	1%	
Number used as logic	173	9,112	1%	
Number using O6 output only	156			
Number using O5 output only	0			
Number using O5 and O6	17			
Number used as ROM	0			
Number used as Memory	0	2,176	0%	
Number of occupied Slices	59	2,278	2%	
Number of MUXCYs used	4	4,556	1%	
Number of LUT Flip Flop pairs used	184			
Number with an unused Flip Flop	73	184	39%	
Number with an unused LUT	11	184	5%	
Number of fully used LUT-FF pairs	100	184	54%	
Number of unique control sets	7			
Number of slice register sites lost to control set restrictions	24	18,224	1%	
Number of bonded IOBs	17	232	7%	
Number of RAMB16BWERs	0	32	0%	
Number of RAMB8BWERs	0	64	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	1	16	6%	
Number used as BUFGs	1			
Number used as BUFGMUX	0			

Number of DCM/DCM_CLKGENs	0	4	0%	
Number of ILOGIC2/ISERDES2s	0	248	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	248	0%	
Number of OLOGIC2/OSERDES2s	0	248	0%	
Number of BSCANs	0	4	0%	
Number of BUFHs	0	128	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	32	0%	
Number of ICAPs	0	1	0%	
Number of MCBs	0	2	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	2	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	5.17			

Performance Summary			[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Sat Jan 23 06:13:56 2021	0	1 Warning (1 new)	1 Info (1 new)
Translation Report	Current	Sat Jan 23 06:14:08 2021	0	0	0
Map Report	Current	Sat Jan 23 06:14:16 2021	0	0	6 Infos (0 new)
Place and Route Report	Current	Sat Jan 23 06:14:24 2021	0	0	3 Infos (0 new)
Power Report					
Post-PAR Static Timing Report	Current	Sat Jan 23 06:14:28 2021	0	0	4 Infos (0 new)
Bitgen Report	Current	Sat Jan 23 06:32:14 2021	0	0	0

Secondary Reports			[-]
Report Name	**Status**	**Generated**	
ISIM Simulator Log	Current	Sat Jan 23 06:34:52 2021	
WebTalk Report	Current	Sat Jan 23 06:32:15 2021	

WebTalk Log File	Current	Sat Jan 23 06:32:15 2021

Date Generated: 01/23/2021 - 06:35:03