# Design of Common Source Amplifier and Current Reference with TSMC 0.18μm Process

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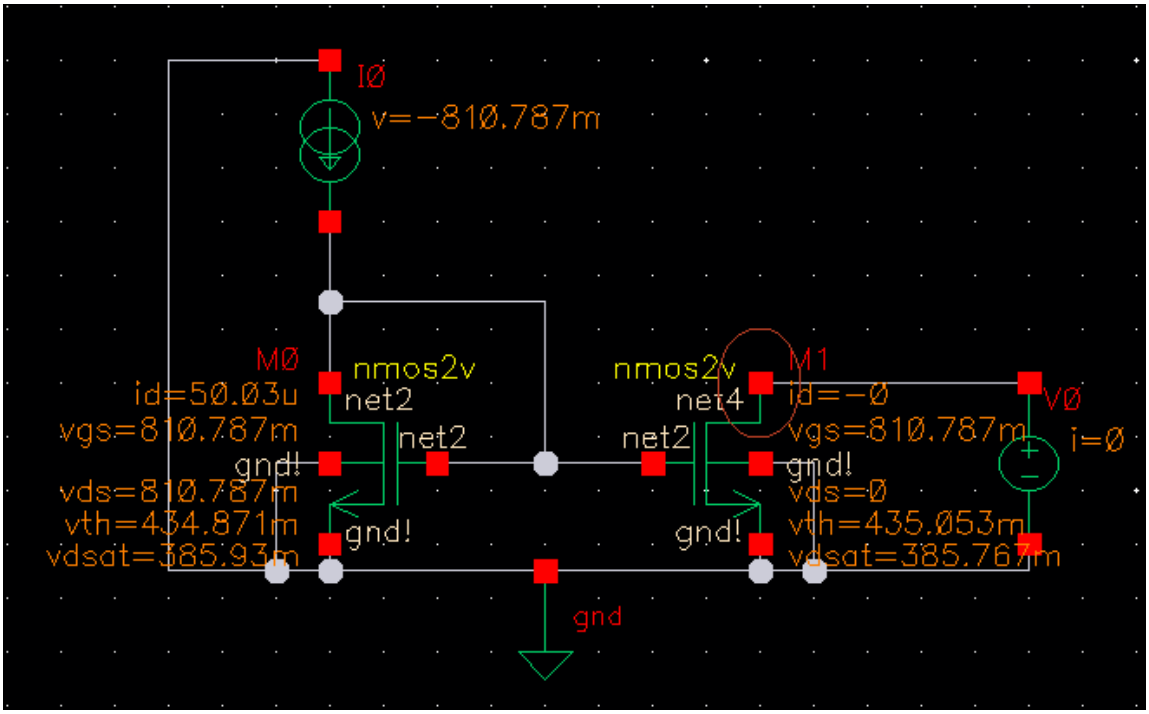
# Introduction:

The purpose of this document is to show experience in design problems, after being given certain specifications, showing how I can then design circuits to meet function as required. The three circuits I focus on here are Current Mirror with an ideal current source, a Common Source Amplifier with a resistive load and a Common Source Amplifier then with an active load, all of which are very common and useful designs in industry. All designs are done in Cadence.

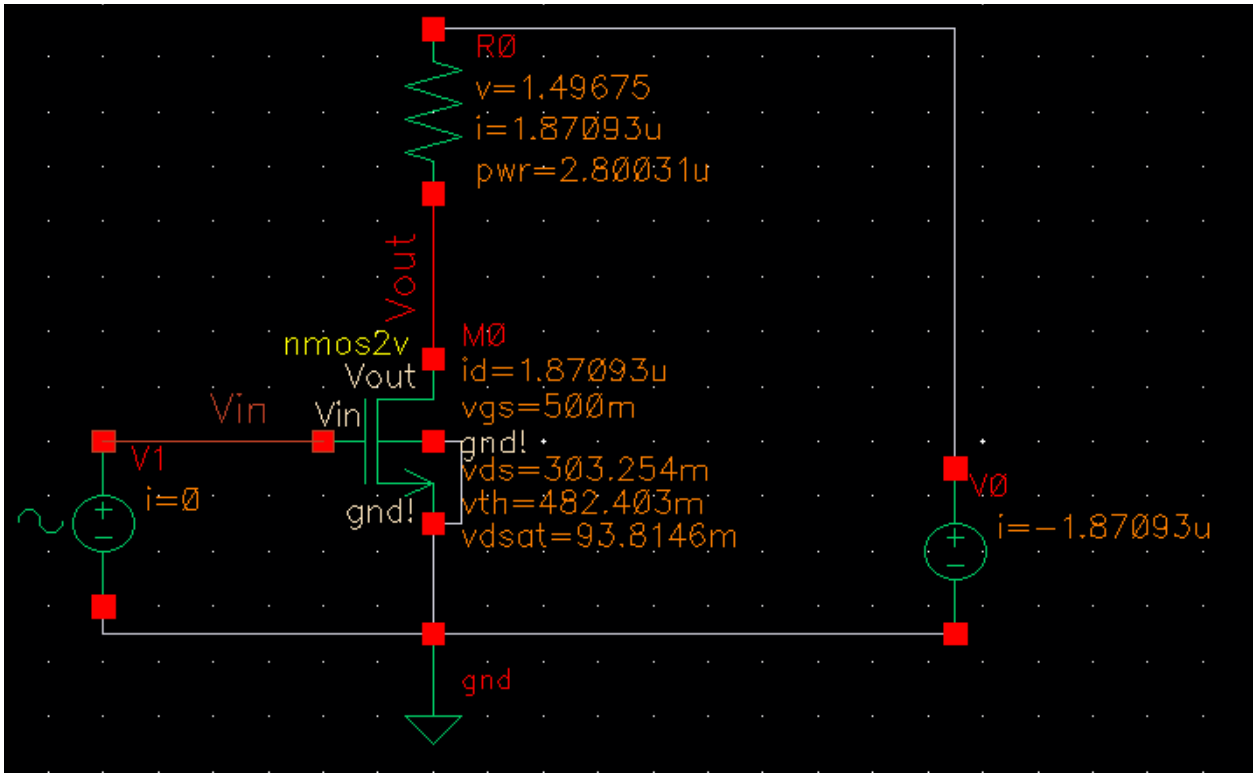
# Design and Procedure:

| MOSFET Current Mirror with Ideal Current Source | | |
|---|---|---|
| | SPEC | Achieved |
| Output Current | 150 µA | 150 µA |
| Output Impedance at 0.45V $V_{DS}$ | 250 KΩ ± 10% | 243.5 KΩ |
| Temperature | 0°C to 80°C | 0°C to 80°C+* |
| * Note: No visible degradation trends of the output current nearing 80°C suggesting that this design can be operated at higher temperatures at user's own risk. | | |



The most important factor in this first design meant an understanding of the necessary W/L ratios to meet the given specifications. I set up a ratio between the (W/L)'s of the two MOSFETs to get a 3 to 1 output current increase. Using the equation $I_d = (1/2)(k'n)(W/L)(V_{gs} - V_{th})^2$ , for each MOSFET makes it evident that the W/L ratio is what we need to focus on to achieve our specifications. Here, almost every variable is set besides the (W/L), hence making the W/L ratio what we can and had to mess around with. Another consideration in our design was why the MOSFETs were chosen to be so large. Our reasoning was to have satiability in our I/V curve for the device (as well as a steady saturation region) instead of having a delta slope in saturation.

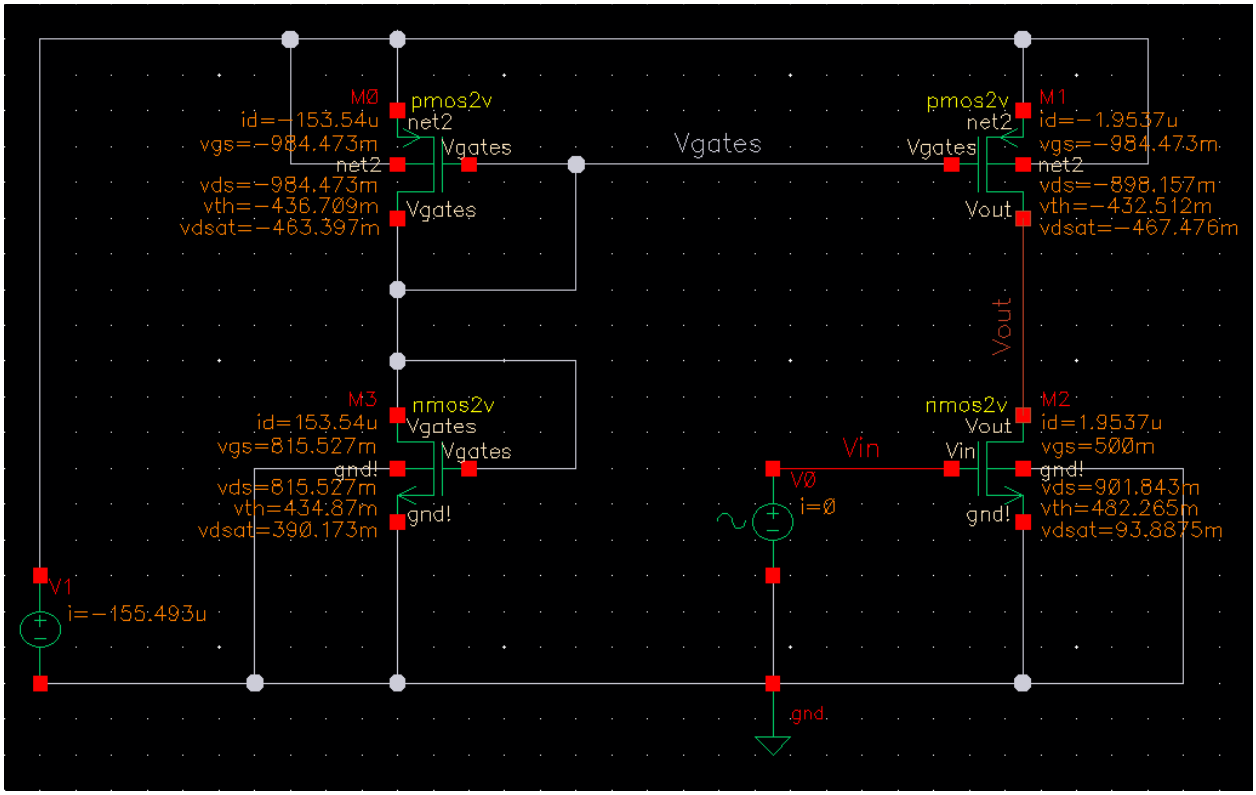
| MOSFET Common-Source Amplifier with Resistive Load | | |
|---|---|---|
| | SPEC | Achieved |
| Power | Less than 0.5 mW | 3.366 µW |
| Gain | At least 20V/V | 22.1V/V |




For the common source amplifier with a resistive load, in order to achieve optimal performance I had to find common ground between the Vin DC bias, the (W/L) ratio of the MOSFET device, and the resistance of the $R_d$ Resistor. To ensure my design functioned at the optimal level I ran a 3 variable Parametric Analysis which generated over 700 data points, this then gave us our optimal balance between the aforementioned parameters. An important part of this design was figuring out the proper ranges in which to find the optimal design values.

Eventually I came to the conclusion that .5 V to .55 V for the DC bias, 1 µm to 10 µm for W in (W/L) with L set to 1 µm, and 500 KΩ to 1000 KΩ for $R_d$ gave us the best results.

| MOSFET Common-Source Amplifier with Active Load | | |
|---|---|---|
| | SPEC | Achieved |
| Power | Less than 0.5 mW | 279.88 µW |
| Gain | At least 20V/V | 260V/V |




Finally for the common source amplifier with an active load I combined the designs developed in the previous parts and used them to achieve the goal of amplifying a signal with an attached active load. Also a design that is very practical in industry. The most difficult part of this design was using PMOS technology and then implementing it in a way congruent to how the NMOS designs were implemented previously. Since active loads are not constant I couldn't make any assumptions as to what its current operating impedance was at any one time. After the initial design I used Parametric Analysis to optimize multiple variables at once, which gave me the values I needed to reach the given specifications.

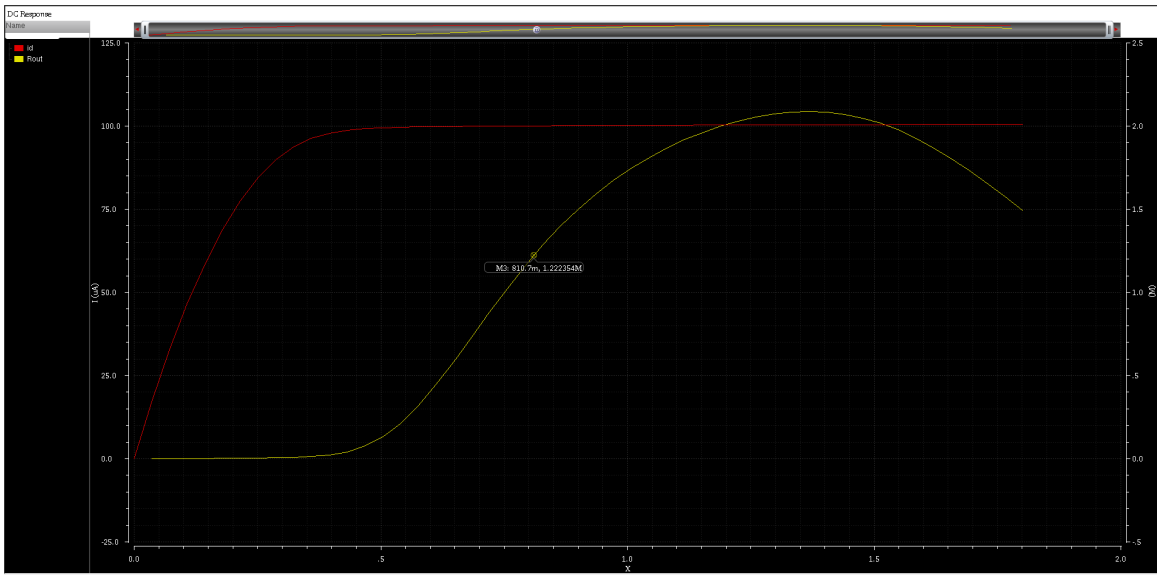
# Simulation Results and Analysis:

## Die Area(s):

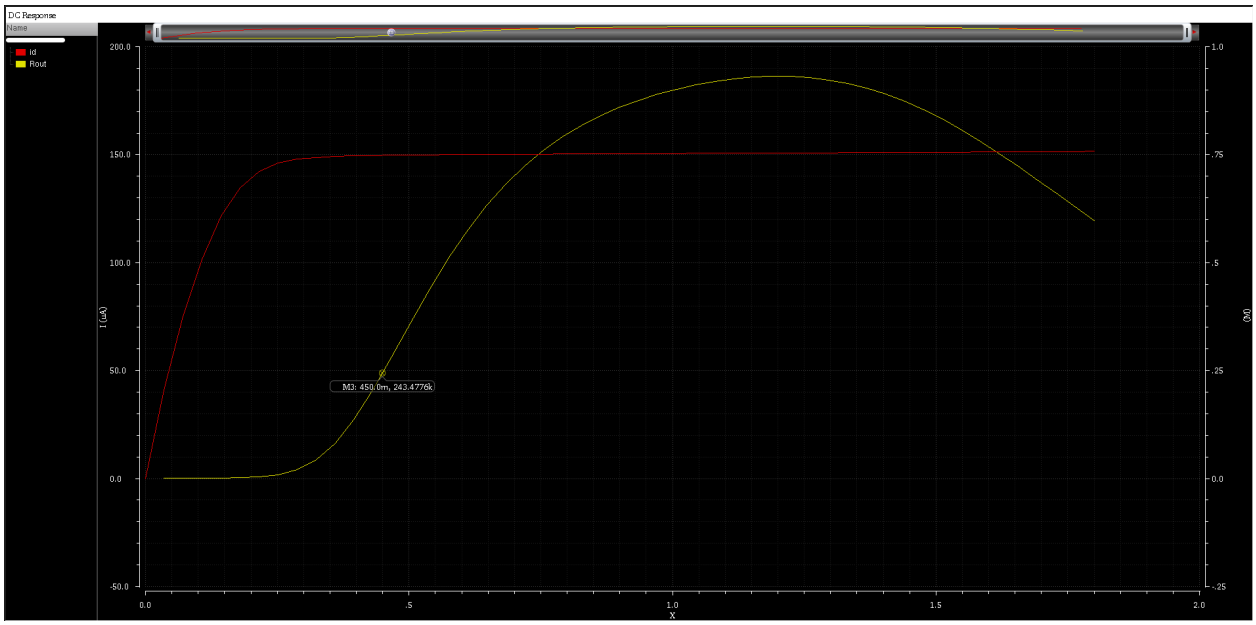
| Device | W or R | L |
|---|---|---|
| **MOSFET Current Mirror with Ideal Current Source** | | |
| M0 | 60 µm | 10 µm |
| M1 | 180 µm | 10 µm |
| Total Die Area | 2.4 $mm^2$ | - - - |
| **MOSFET Common-Source Amplifier with Resistive Load** | | |
| M0 | 2 µm | 1 µm |
| R0 | 800 KΩ | - - - |
| Total Die Area | 802 $\mu m^2$ | - - - |
| **MOSFET Common-Source Amplifier with Active Load** | | |
| M0 | 180 µm | 10 µm |
| M1 | 2.34 µm | 10 µm |
| M2 | 2 µm | 1 µm |
| M3 | 60 µm | 10 µm |
| Total Die Area | 2.425 $mm^2$ | - - - |

## MOSFET Current Mirror with Ideal Current Source:

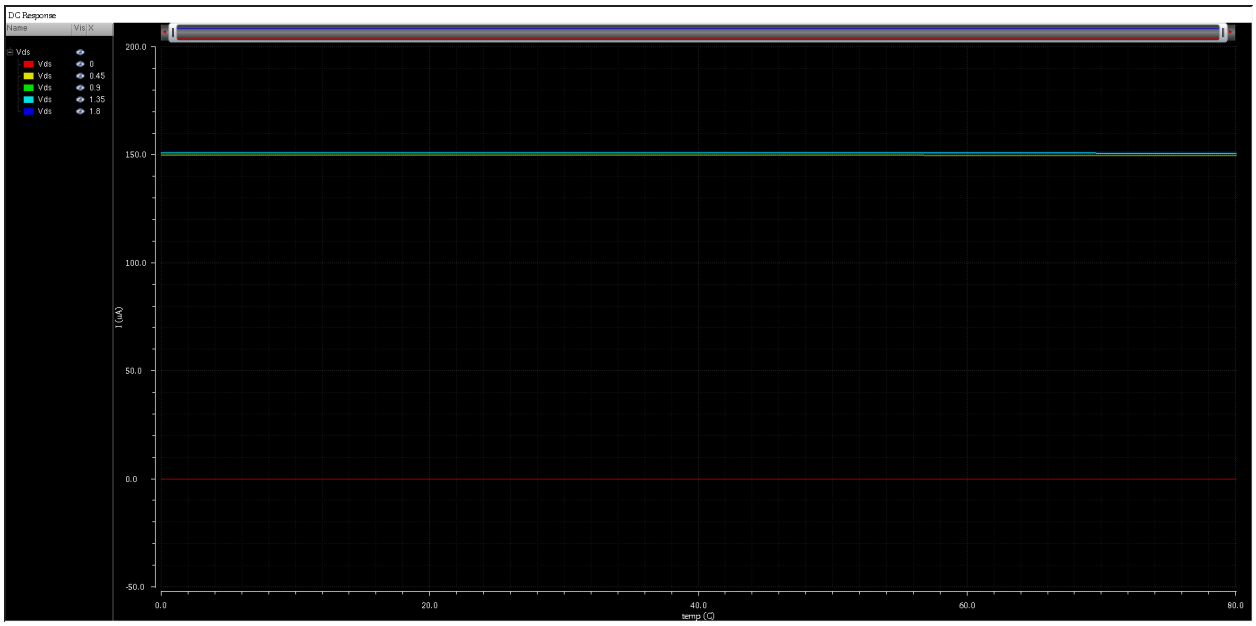
After the initial design of this device to have an $I_d$ ratio of 2 to 1 in the first experiment of the design specifications we then found that it generated an acceptable I/V curve which was stable, next I was able to generate a reasonable Rout impedance graph. The below plot has a marker at 810.7 mV & 1.2 MΩ, is DC Op point.



For the following specifications a Current Mirror, which has an $I_d$ ratio of 3 to 1, I was able to develop a design that operated within the specifications. The graph below shows, that as soon as the circuit is in saturation, there is a relatively constant $I_d$ of 150 µA and output impedance within 10% of 250 KΩ at .45 V (245.5 KΩ at this voltage, which is less than 1% from the ideal impedance and hence acceptable).




In the final part of the specifications, I tested the design from 0°C to 80°C to see if our output current experienced degradation as temperature increased. I observed that this design showed no signs of degradation. This suggests that my design has the option to operate in increased temperatures as long as component life is considered in testing prior to use.



The Current Mirror as a whole, I concluded that I would recommend this design because it was stable and furthermore could operate in a variety of temperatures. That said the die area is pretty large, this being the only hindrance. However if I reduced size, ie channel length, then the saturation current becomes less stable (not a flat line anymore), instead more of a linear increasing function. This is harmful if stable current in saturation is desired, no matter what that voltage is above saturation. Since my circuit operates correctly regardless of temperature changes and operates in a stable manner in saturation mode it is perfect for reliable operation.

## MOSFET Common-Source Amplifier with Resistive Load:

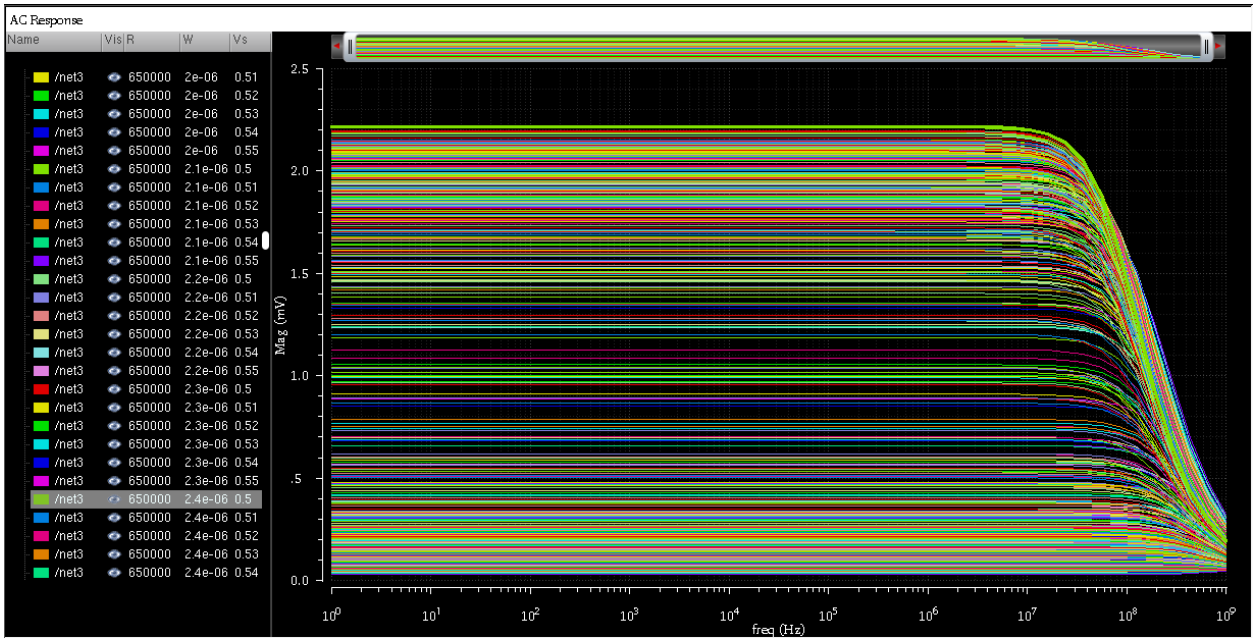
For my design, the main equations we utilized in order to achieve the right balance given the number of variables I had are as follows:

$I_d = (1/2)(k'n)(W/L)(V_{gs} - V_{th})^2$

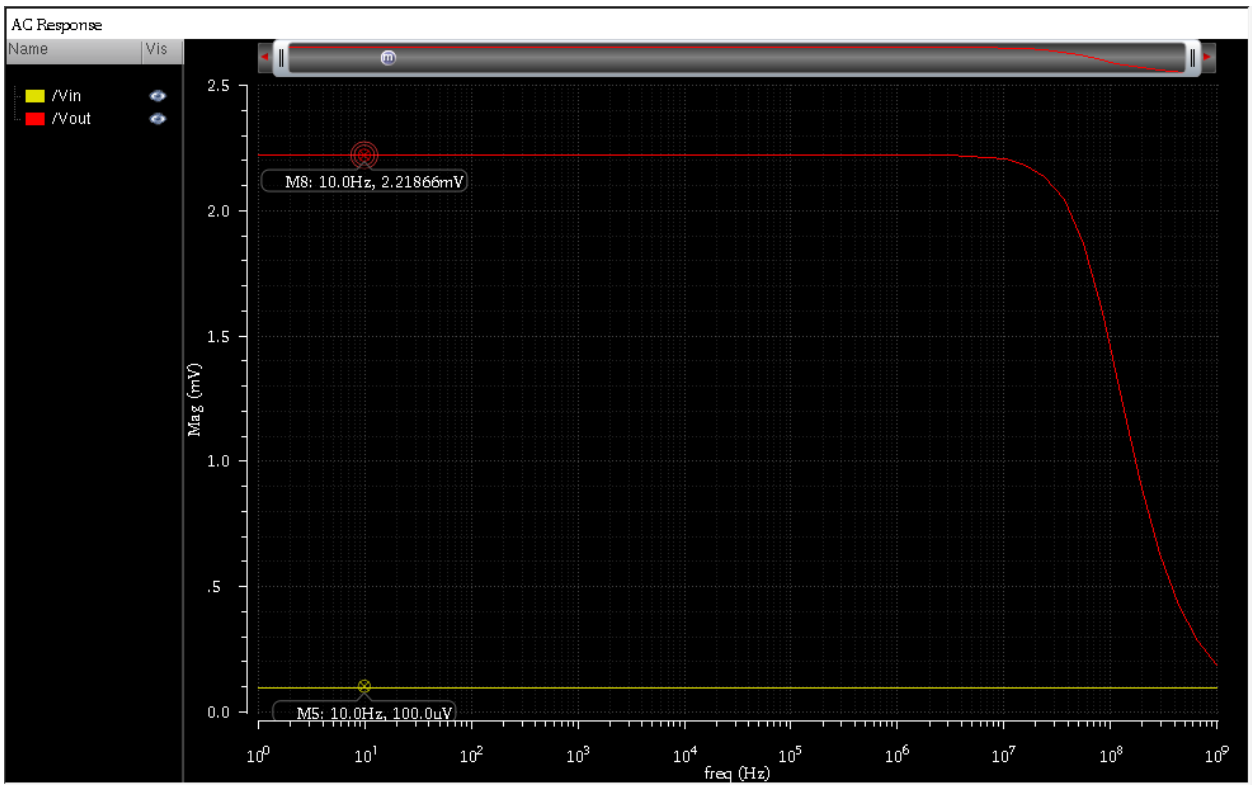
$A_v$ (gain) = gm * $R_{out}$ = $(2I_d/V_{sat})$ * $(V_R/I_d)$  $V_R$ being voltage across $R_d$

$V_R = R_d * I_d$

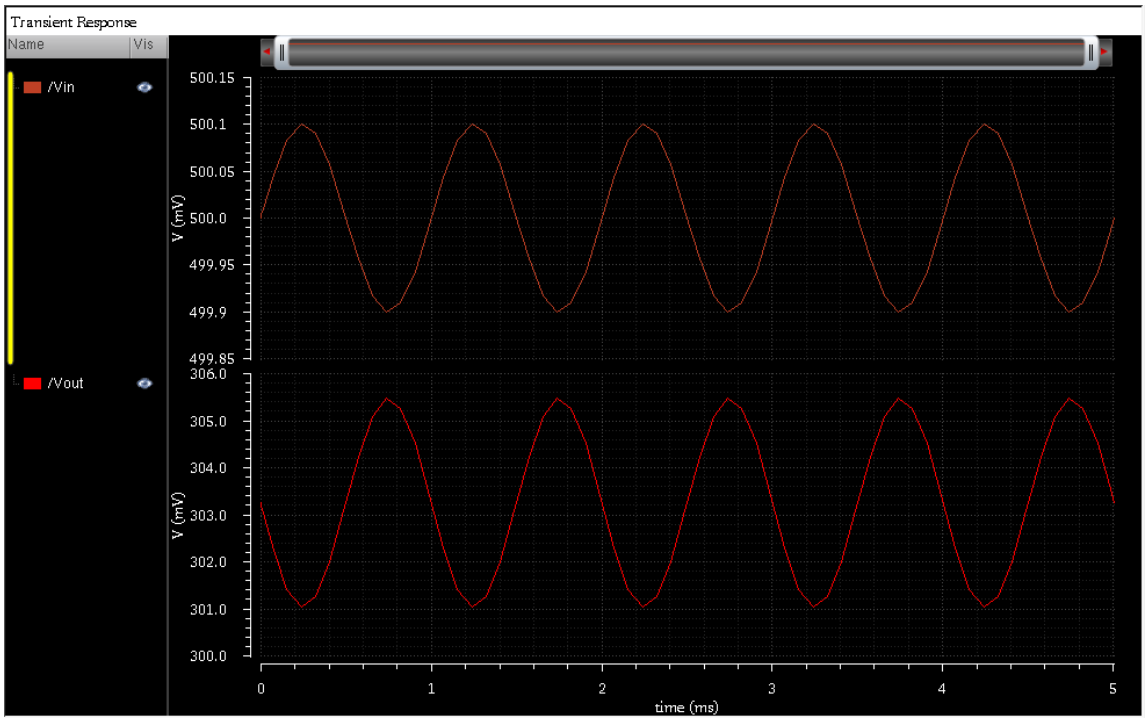
With the above formulas combined with what our DC Vin bias needed to be, I used Parametric Analysis to solve for ideal values what the DC bias, (W/L) ratio, and $R_d$ should be. The following graph shows over 700 data points we gathered help to optimize the design. These values fill make use of the hand calculation formulas aforementioned.

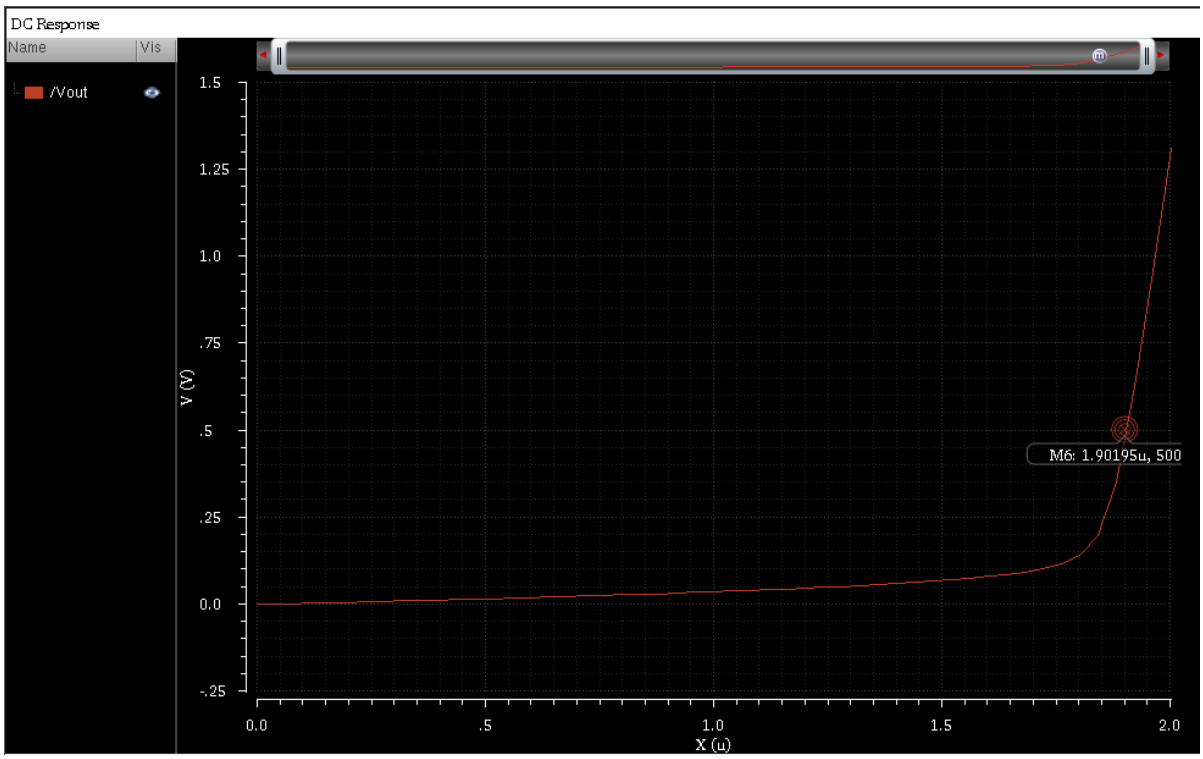



The final specification of the DC bias was .5 V, the (W/L) being (2 µm /1 µm), and $R_d$ being 800 KΩ; I achieved a AC gain of 22.1V/V (see below).

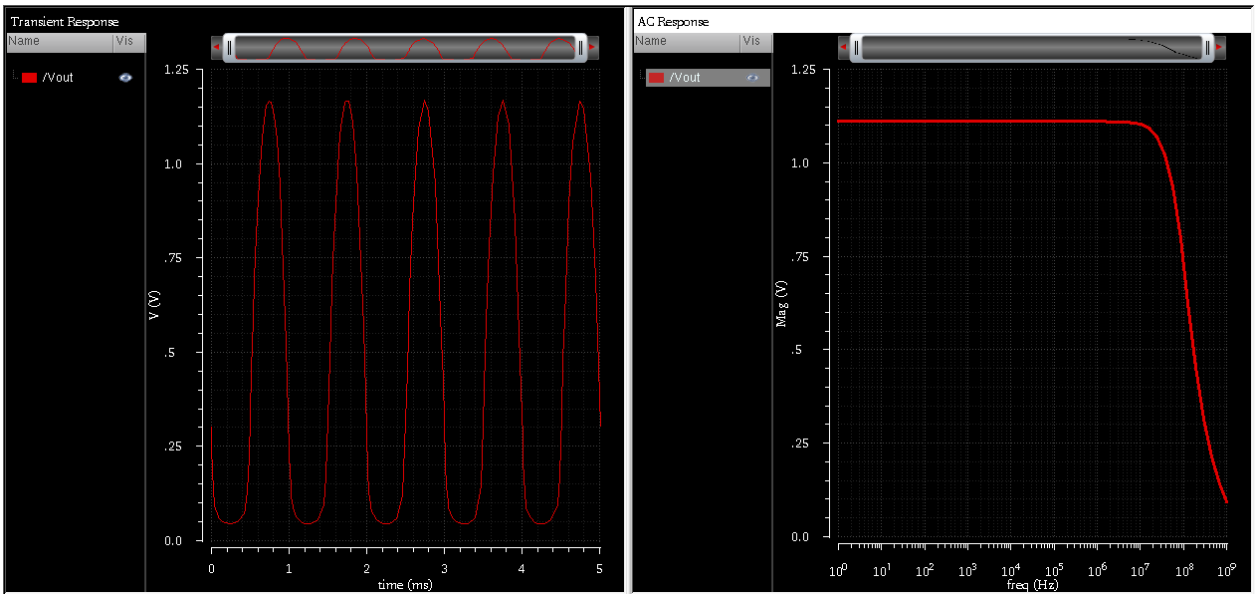



After further tests on this design, I got transient (Vout vs Vin) and DC (Ids vs Vout) graphs respectively. Here there is a 180 degree phase shift as well as log behavior.

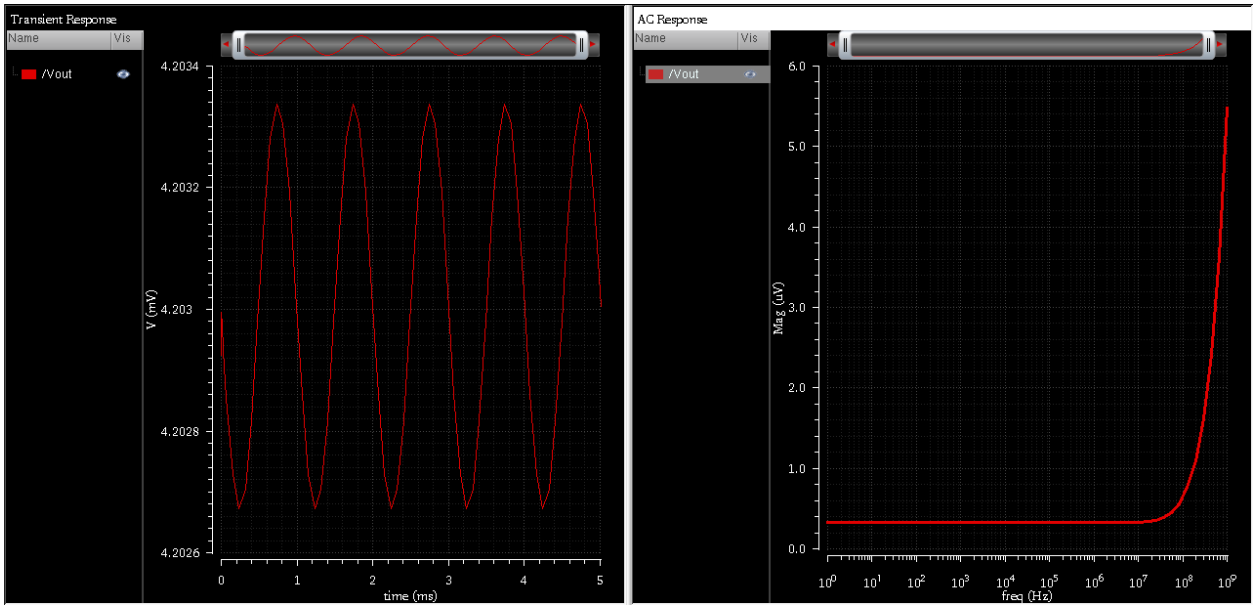




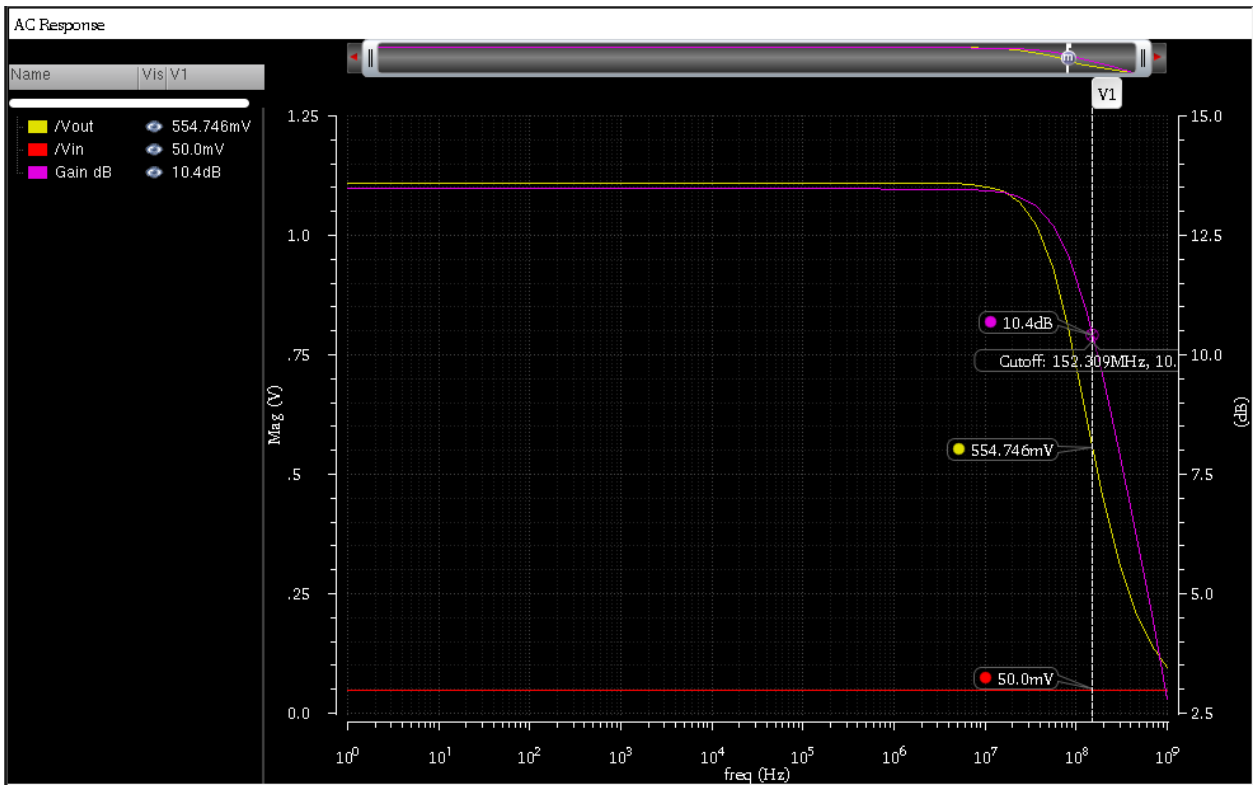

Initially I was using a 100uV bias, however when I used a 50 mV peak to peak voltage swing for Vin with a .5V DC bias, it results in the below transient and AC graphs (respectively). Here the AC gain increases from 22.1V/V to about 11500V/V and the transient response experiences a significant increase in value as well. This is because the increase to the voltage swings from 100µV to 50mV, is about a 500 times greater. In the resulting AC gain is affected in a somewhat linear way as well. Multiplying the original gain (22.1V/V) by 500 I get 11050V/V, which is close to the roundabout gain we can see from the graph of about 11500V/V.

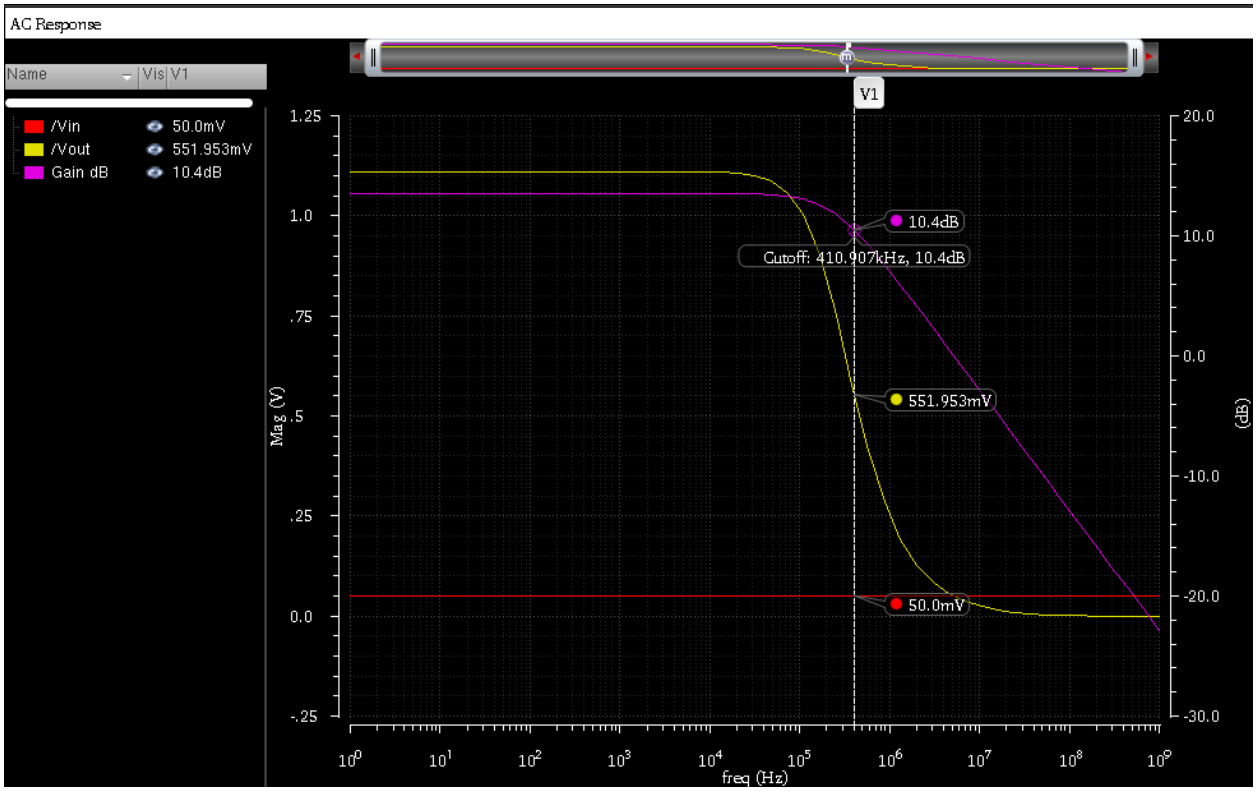


When a 2KΩ load is placed on Vout, then the transient and AC results can be seen below. Here it is evident that the AC gain is null due to the equally null raw transient voltage values.



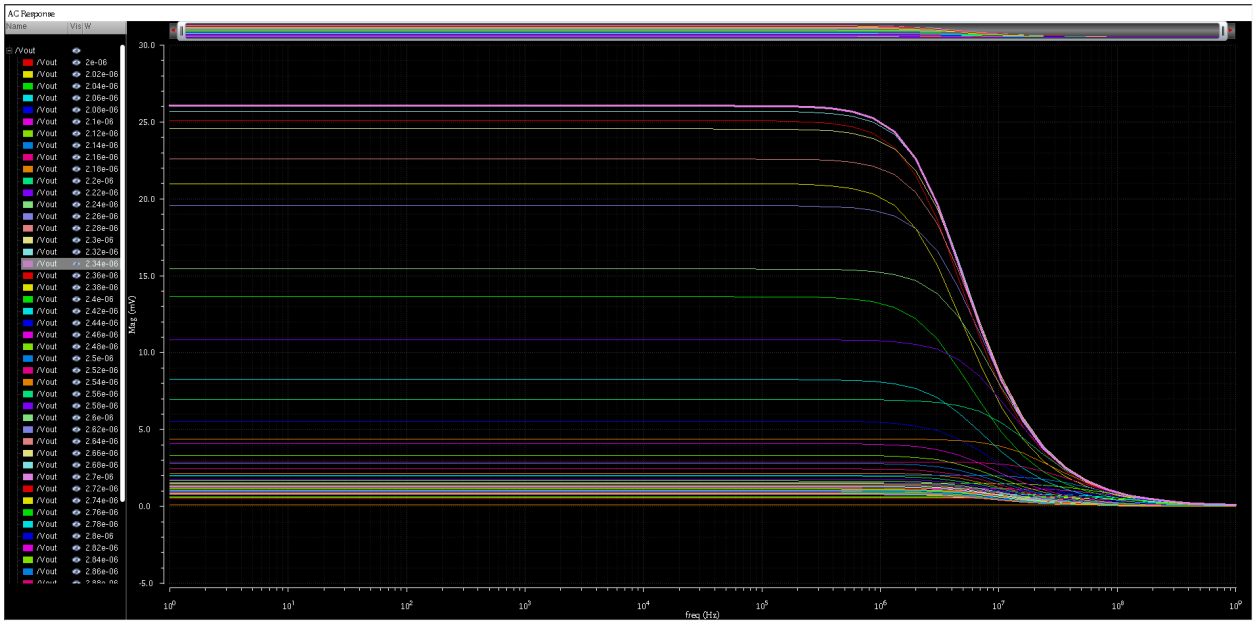

After observing cutoff frequencies, or when the signal loses 3dB of its peak power, I was able to see how this design reacts without any load, and how a 1pF capacitive load affects it. From these graphs (see below), the gain-bandwidth product of the design without a load is 152 MHz * 10.4 dB which is $1.5808 * 10^9$, and the gain-bandwidth product of the 1pF load circuit is 410.9 KHz * 10.4 dB which is $4.27 * 10^6$. Another insight these graphs provide is that when there is no load, the peak decibel value is kept through a longer range of the higher frequencies however, when it reaches the cutoff frequency, the decibel values fall a lot faster than that of the design with the capacitive load.


AC Response
Name
Vis
V1
/Vout
554.746mV
/Vin
50.0mV
Gain dB
10.4dB
V1
1.25
1.0
.75
.5
.25
0.0
Mag (V)
15.0
12.5
10.0
7.5
5.0
2.5
(dB)
10.4dB
Cutoff: 152.309MHz, 10.
554.746mV
50.0mV
$10^0$ $10^1$ $10^2$ $10^3$ $10^4$ $10^5$ $10^6$ $10^7$ $10^8$ $10^9$
freq (Hz)


AC Response
Name
Vis
V1
/Vin
50.0mV
/Vout
551.953mV
Gain dB
10.4dB
V1
1.25
1.0
.75
.5
.25
0.0
-.25
Mag (V)
20.0
10.0
0.0
-10.0
-20.0
-30.0
(dB)
10.4dB
Cutoff: 410.907kHz, 10.4dB
551.953mV
50.0mV
$10^0$ $10^1$ $10^2$ $10^3$ $10^4$ $10^5$ $10^6$ $10^7$ $10^8$ $10^9$
freq (Hz)

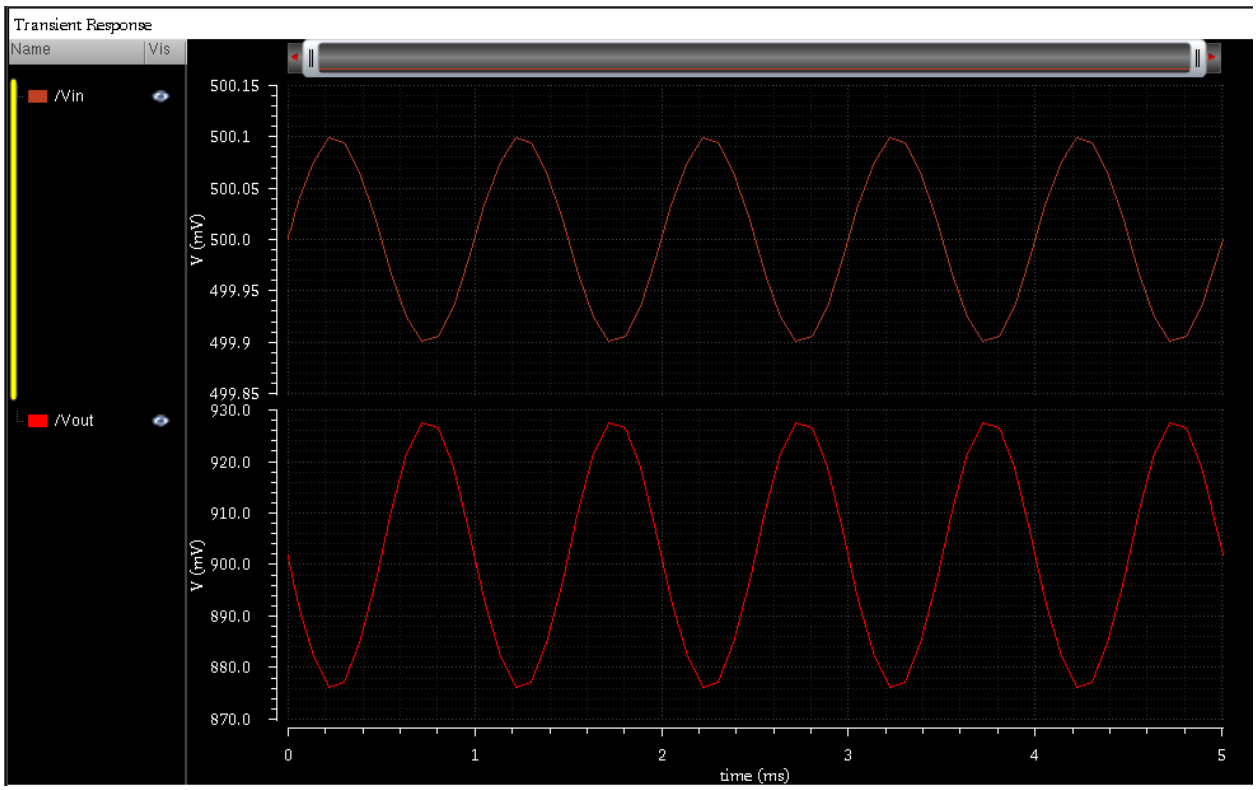
## MOSFET Common-Source Amplifier with Active Load:

To find out the proper values for this design we used a similar Parametric Analysis that resulted in an optimization graph seen below. Here, I chose values that would provide the best gain achievable (which stayed within the design specifications). The result was a gain of 260V/V, better exemplified in the second graph below.

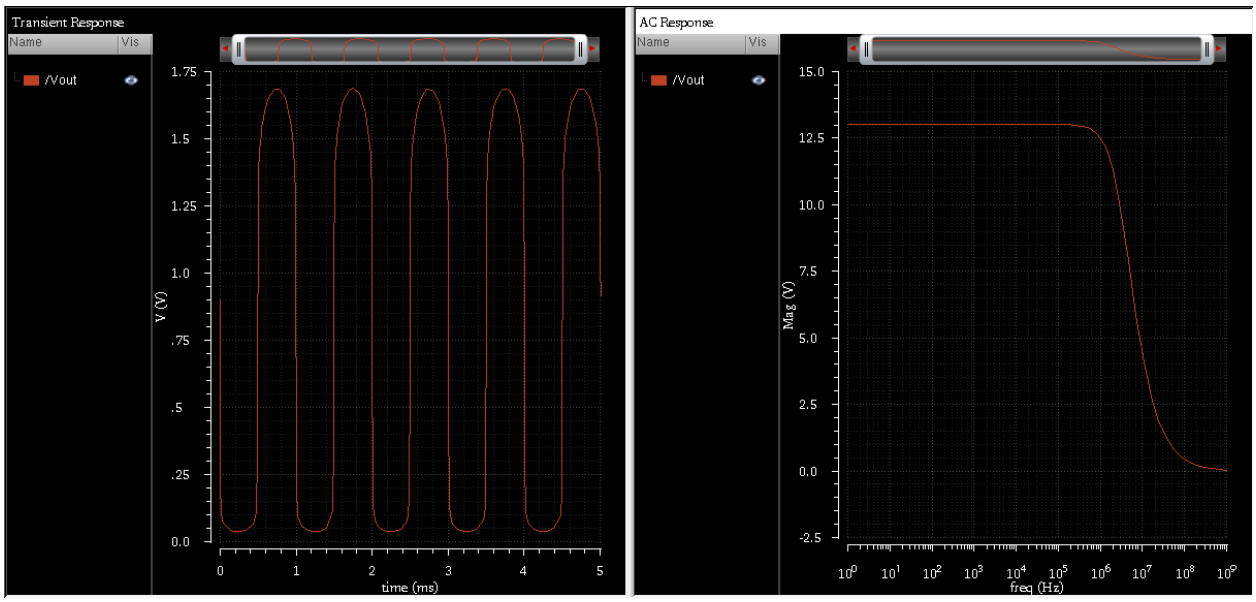




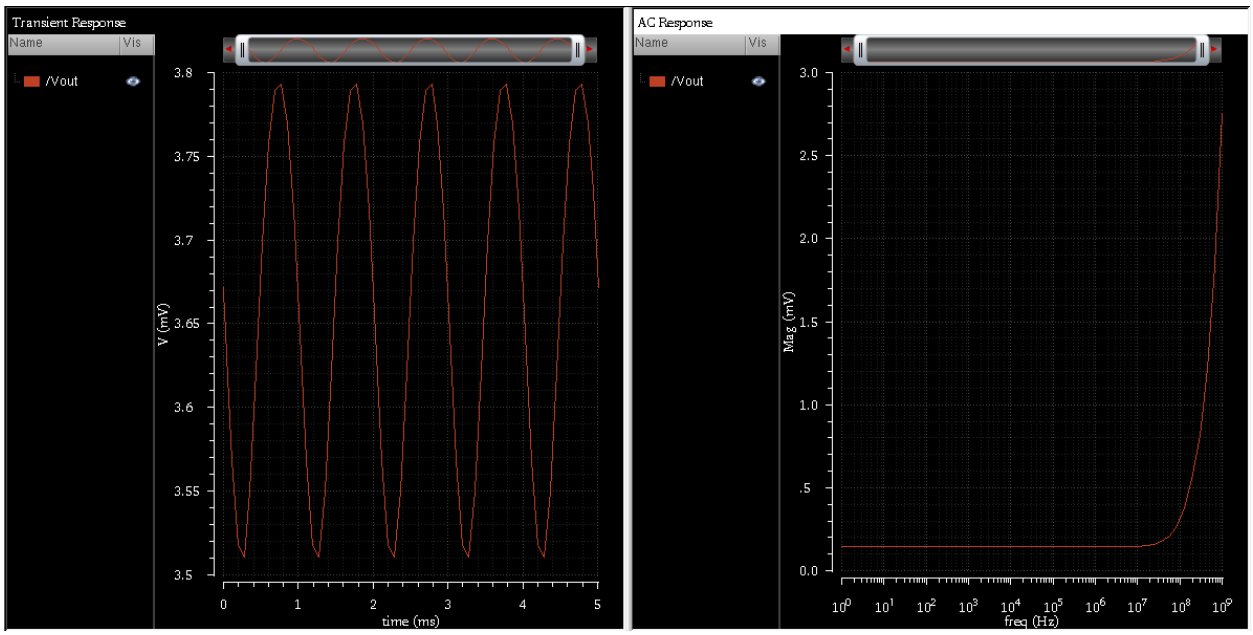
Transient (Vout vs Vin) Graph



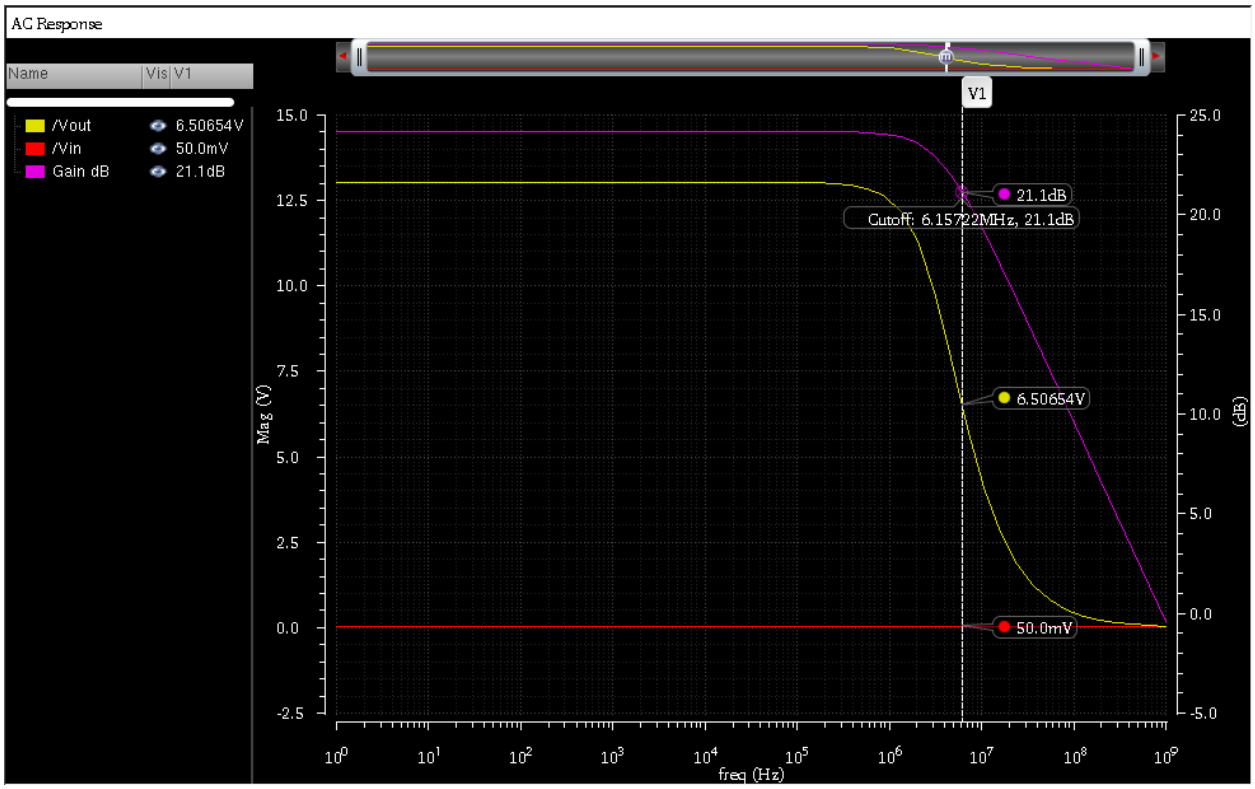

A 50mV peak-to-peak Vin signal with .5V DC bias gives the following result (graph below). For similar reasoning as the last design gain increase, multiplying the past value attained by the previous gain 26mV (260V/V) with the 500 times greater oscillation, the new result is 13V. This is close to the exact value returned from the AC analysis and this also suggests this amplifier is a linear system.

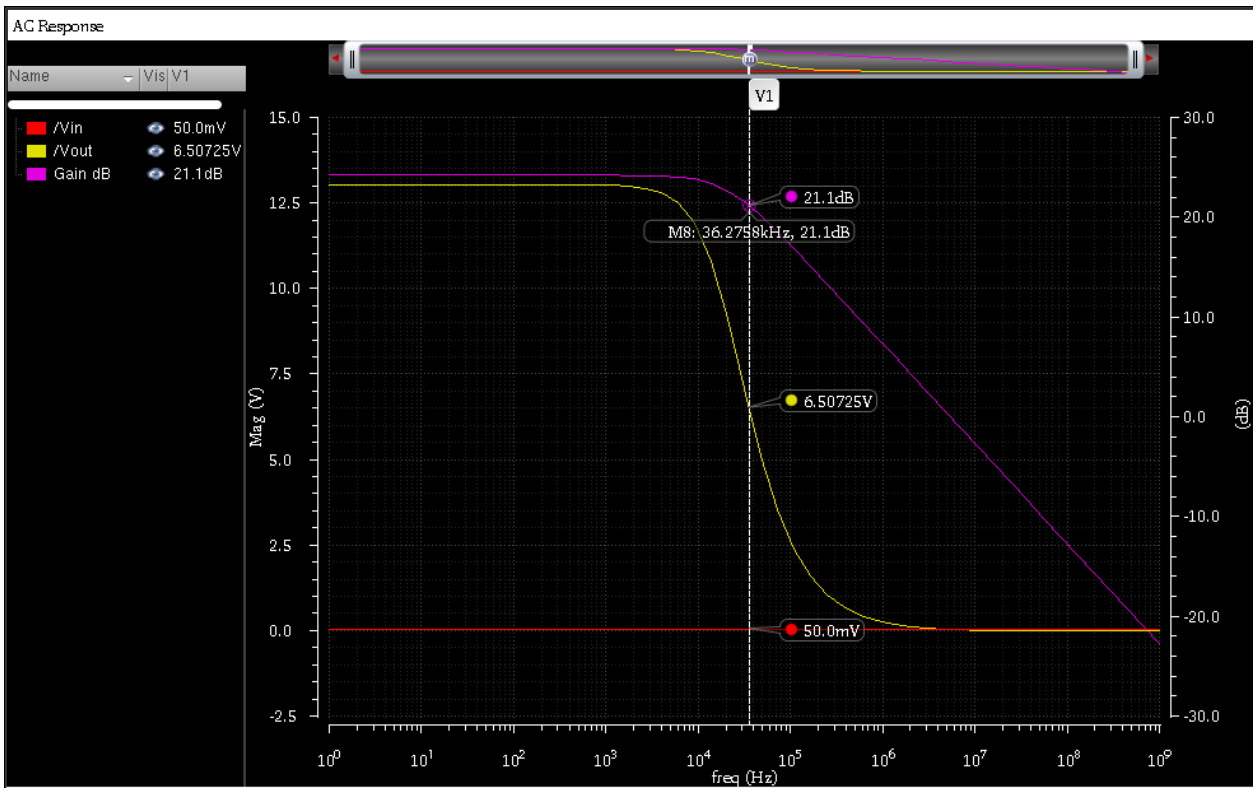



After adding a 2 KΩ load to the output, we see the same massive output degradation.




Now, when looking at the how the gain is affected with capacitive loads, this design behaves very similarly to the way the previous design behaved. The first graph (below) is the one without a load (with a GBW of around 129.913 * $10^6$) and the second is the one with the capacitive load (with a GBW of around 765.402 * $10^3$).






# Conclusion:

Through this report I demonstrated that when given specifications I can design several circuits to meet those requirements and provide an in depth analysis to best predict how this circuit would behave if taken to production. Thank you for reading if you have made it this far!