Aalto University
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Automated Analysis of Weak Memory Models

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ABSTRACT OF MASTER'S THESIS

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Artem YUSHKOVSKIY

Abbreviations

LI	Lorem Ipsum
ABC	Quisque et mi lacus, nec porta ante.
DEF	Proin pellentesque accumsan laoreet

Contents

Chapter 1

Introduction

Most modern computer systems contain large parts that operate concurrently. Though system parallelising can improve its performance drastically, it opens numerous of problems connected to correctness, robustness and reliability, which makes the concurrent program design one of the most difficult problems of programming [1].

Traditionally, studies related to concurrent programming concern on more fundamental theoretical questions of designing race-free and lock-free parallel algorithms, asynchronous data structures and synchronisation primitives of a programming language. Unfortunately, when it comes to the real-world concurrent programs, the algorithmic level of abstraction is not enough for guaranteeing their properties of correctness and reliability. The reasons of this fact lie in the code optimisations that both compiler and hardware perform in order to increase performance as much as possible. For instance, Figure 1.1 provides simple example of unexpected state '`(0:EAX=0 /\ 1:EAX=0)`' reachable in x86 machines (such little examples that illustrate specific behaviours of a WMM are called *litmus tests*). This behaviour is caused by write buffers used by all processors in x86 architecture. These buffers cache writes to shared variables, so that the writes to shared memory does not become visible by other processes immediately. In the example, the write '`MOV [x],1`' performed in the process `P0` stores value `1` into the shared variable `[x]` in the write buffer of process `P0`. Meanwhile, the write cache of the process `P1` may not have updated version of the variable `[x]`, neither may have the main memory, so that the read '`MOV EBX,[x]`' performed in the process `P1` may read the initial value `0`, even if this variable has been already updated in another thread. More presice description of x86-TSO memory model is given in Chapter 2.3.1.

{ x=0; y=0; }	
P0	P1
MOV [x],1 MOV EAX,[y]	MOV [y],1 MOV EAX,[x]
exists (0:EAX=0 /\ 1:EAX=0)	
x86-TSO: allow	

Figure 1.1: *Litmus test of memory operations reordering allowed by the x86-TSO weak memory model*

The first memory model for concurrent systems was formulated by Leslie Lamport back in 1979 [2]. This memory model, called the *sequential consistency (SC) model*, allows only those executions (interleavings) that produce the same result as if the operations had been executed by single process. This means that the order of operations executed by a process is strictly defined by the program it executes. The SC model does requires the write to a shared variable performed in one process to become visible by all other processes not instantly, but simultaneously. This means each process communicates to the shared memory directly, without local buffering. Another important requirement of SC memory model is that it forbids memory operations reordering within single process (the order is strictly defined by the program).

The SC model is considered to be the strong memory model in the sence that it provides strong guarantees regarding the ordering and caused effect of memory operations. Different relaxations of this model lead to the class of *weak memory models (WMM)*. WMMs serve as set of guarantees made by designers of execution environment (hardware, programming language, compiler, database, operation system, etc.) to programmers on which behaviours of their concurrent code they may expect.

Although weak memory studies is rather young research area, there exist frameworks and tools for exploring WMMs and examining simple programs with respect to the them. The state-of-the-art tool is `diy` (for *do it yourself*), developed by the researchers from INRIA institute, France, and University of Cambridge, UK, and firstly released back in 2010. It is the sofware suite for designing and testing weak memory models, it consists of the litmus tests generators `diy7`, `diycross7` and `diyone7`, the litmus tests concrete executor `litmus7` that runs tests on a physical machine while collecting its behaviours, and the weak memory models simulator `herd7` that implements reachability analysis for capturing states allowed by the

WMM. The latter tool uses systematic exhaustive search in a state space, which may be inefficient when analysing real-world programs, therefore more sophisticated search techniques should be applied for this problem.

One possible approach is to use an efficient implementation of an SMT-solver (a SAT-solver extended by satisfiability modulo theories) [3]. This approach allows to capture symbolically the semantics of both the program and the weak memory model while encoding it into a single SMT-formula. Most modern SMT-solvers are efficient enough to be able to operate the state space of size ??? [CITATION-?].

In the work [3], the SMT-based approach was defined for analysing the portability of a program from one hardware architechture to another, which is defined as “an execution that is consistent with the target but inconsistent with the source memory model". Although encoding the control-flow and the data-flow of a program into an SMT-formula seems to be a trivial problem of symbolic execution, encoding of the weak memory model is more tedious. The reason is that some relations of WMMs are defined as mutually-recursive and need to be linearised in order to be encoded into an equivalent logical formula.

Current thesis aims to improve the proof-of-concept tool `PORTHOS` firstly introduced in April 2017 in the work [3] by extending the input language, which currently represents the minimum subset of C, and revising the general architecture of the tool in order to enhance performance, reliability and mantainability.

1.1 Thesis structure

The Chapter 2 gives more detailed description of the weak memory models analysis and provides description of memory models for some common architectures (x86, ARM and POWER, Sparc, ???). Chapter ...

Chapter 2

Weak Memory Models

Over the last decades, the problem of formalisation of the weak memory models has been developed significantly. Research of WMM aimes, firstly, to formalise the weak memory models and provide systematic, sound and complete formal approach of defining WMMs in order to be able to verify systems with respect to them. //the cat language here.

Secondly, researchers work on extracting the formal hardware memory models from existing implementations of from their specifications, that are written in natural language and thus suffer from ambiguities and incompletenesses. Over last decade the memory models have been extracted for most mainstream multiprocessor architectures, such as x86-TSO (*Total Store Order*) model for x86 architecture formalised in 2009 [4], SPARC-TSO for Sparc architecture **?!?!?!**, much more relaxed memory model ??? for Power and ARM architectures defined in ??? [5], Alpha (???). Moreover, in 2005 <who?Milner> started the work on developing the weak memory model for C++ language, which was introduced in C++11 (?) standard **???** (//todo: C11 MM [6]). The memory model for Java that is based on the *happens-before* principle was introduced in JVM??? in ??<year>.

Thirdly, important research direction targets the problem of verifying (or at least finding bugs in) existing software systems with respect to weak memory models. In this <area> the notable works <are on> defining the Linux kernel memory model <that is being actively developing these days **kernel_wmm_1**>. Distributed databases <also need the wmm, see transaction consistency [7]>

2.1 The event-based program representation

The classical approach to model the concurrent programs is to use the *global time*, a single order of interleavings of all actions happened in different threads. However these models are easy to understand, it may be hard to consider *all* possible states, number of which is exponentially large. Another way to do this is to to use non-deterministic models, one of which is the program representation based on *memory events*. The idea in this class of models is based on the fact that the behaviour of a concurrent system is defined only by the interleavings of shared-memory operations, while being independant from the order of local computation events. These models may be further restricted by constraints of a weak memory model, adding *relations* to the memory events.

The event-based program model represents the directed graph (*event-graph*), where vertices represent *events*, and edges represent *relations* over the events. An event is something, that, after being executed, changes the state of an abstract machine executing the concurrent program. An *execution* (trace, run) of a given program is an order of events. An execution is considered to be *valid* if the memory events follow a single global timeline, i.e., can be embedded in a single partial order allowed by the memory model restrictions [8]. An execution to be checked on validity is called the *candidate execution*.

Below we describe some basic types of events and relations.

2.1.1 Events

A *memory event* $e_m \in \mathbb{E}$ represents the fact of access to the memory. Since memory is the crucial low-level resource shared by multiple processes, most relations are defined over memory events. The processes can access a shared memory location (denoted by l_i, for *location*), or a local one (denoted by r_i, for *register*). A memory event is specified by its direction with respect to the shared variable, its location $\texttt{loc}(e_m)$, its processor label $\texttt{proc}(e_m)$, and a unique event label $\texttt{id}(e_m)$ [8]. The set of memory events $\mathbb{M}$ is devided into write events $\mathbb{W}$ (that write values to shared-memory locations) and read events $\mathbb{R}$ (that read values stored in shared-memory locations). We add a restriction that each memory event uses at most one shared location, so that the write event $e_m = write(l_1, l_2)$ that writes value from shared location l_2 to the shared location l_1 is represented as two consequent events $e'_m = \texttt{load}(r_1 \leftarrow l_2)$; $e''_m = \texttt{store}(l_1 \leftarrow r_1)$.

A *computation event* $e_c \in \mathbb{C} \subseteq \mathbb{E}$, represents a low-level assembly computation operation performed solely on local-memory arguments. An example of computation event may be the event $e_c = r_3 \leftarrow add(r_1, r_2)$ that writes the sum of values stored in registers r_1 and r_2 to the register r_3. The *control-flow* instructions (conditional and unconditional jumps) are encoded to the model directly, without additional events, as the *po*-relation (for *program order*; see Chapter 2.1.2 for detailed definition of relations).

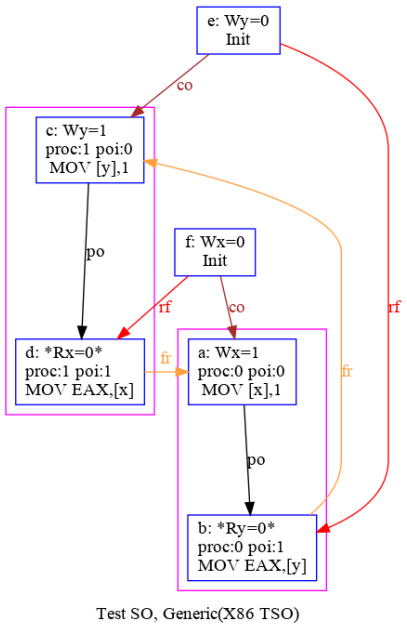
The third class of events is *barrier events*, events caused by the synchronisation instructions (called *fences*). Barrier events do not perform any computation or memory value transfer, instead, they add new relations to the model that restrict the set of allowed behaviours. Technically, a fence may either serve as a synchronisation barrier, or flush local memory caches, etc.

2.1.2 Relations

The basic relation in the event-based program model is the po-relation $\subset \mathbb{E} \times \mathbb{E}$ (*program-order*), which represents the total order of memory events *within single process*, which never relates events from different processes. Thus, if a program specifies the memory instruction i_2 to follow immideately the memory instruction i_2, then there exist an edge $e_1 \xrightarrow{\text{po}} e_2$ in the event-graph where event e_1 is caused by the instruction i_1 and e_2 is caused by the instruction i_2. This relation encodes the control-flow of the program into the event-graph.

The data-flow of a program is encoded by the *communication relations*: the rf-relation $\subset \mathbb{W} \times \mathbb{R}$ (*read-from* relation) that maps a write to a read reading its value, the co-relation $\subset \mathbb{W} \times \mathbb{W}$ (*coherence order*, sometimes called ws-relation for *write serialisation*) defines the total order on writes to the same location across all processes, and the fr-relation $\subset \mathbb{R} \times \mathbb{W}$ (*from-read order*) that maps a read to possible writes preceding the current write event.

Figure 2.1.2 illustrates the candidate execution for the Example 1.1, that reaches the state `(0:EAX=0 /\ 1:EAX=0)` within x86-TSO memory model (the picture is generated by the `herd7` tool, version 7.47).



Test SO, Generic(X86 TSO)

2.2 The CAT language

the CAT language [ref to Jade's paper] (hard part: to decipher the Alglave's paper).

the event representation

2.3 Some known WMM

2.3.1 x86-TSO

// exmaple with reordering // ex. with // Rev-29 Example 7-6. Stores Are Transitively Visible.

There is a barrier instruction `mfence` that may be used for flushing the buffers into the main memory.

briefly known hw memory models: X86-TSO, Alpha, POWER, – ref to Jade; language memory models: Java, C++; library-level kernel memory model, ref to github with tests

Relationship between different models `http://wiki.expertiza.ncsu.edu/index.php/CSC/ECE_506_Spring_2013/10c_ks`

Chapter 3

Implementation

This chapter describes the architecture of the tool `mousquitaires` ...
language: java

3.1 Program Requirements

- stability (tests)
- scalability (new features of language, new models, new tasks for a program)
- transparency
- efficiency

3.2 Program Components

Big view

3.3 C11 to YTree parser

below: mostly mock text.

- The language-dependent syntax tree: - for now it's the C subset language which I called 'Cmin'; as a base, I used the C11 grammar from ANTLR github repository, then I simplified it a lot, cutting off many unnecessary C syntax features and making it more convenient for parsing. When developing the Cmin language, I kept in mind C elements that are necessary for processing the linux kernel code, though for now not the whole grammar element described in file 'Cmin.g4' are being implemented; - later I am

going to add the litmus grammar as well; - in future, it will be not a problem to add any new C-like language;

- The language-independent abstract syntax tree (aliased 'Ytree', where 'Y' resembles branching of the tree): - all tree nodes in my code are prefixed with 'Y', see tentative (yet almost complete) class hierarchy in picture 'YEntity.png'; - this AST contains very basic language elements according to the C execution model (statements and expressions); - converting the language-dependent syntax tree to the language-independent syntax tree is performed by Visitor pattern (e.g., for Cmin->Ytree conversion is made by 'CminToYtreeConverterVisitor') - minor changes are performed by converting to ytree representation: desugaring the target code, etc.

3.4 YTree to XGraph event converter

- Then, the AST is being interpreted and converted to event-based representation (aliased 'Xrepr' for eXecution representation): - more low-level code representation (or high-level assembly); - I try to keep this representation close to the one you described in your papers: basic load & store events, branching events, fence events; - this representation is being implementing these days, I've just started doing it (see current class hierarchy in the picture 'XEntity.png');

- After we acquired the event-based representation, we can perform some modifications/simplifications/optimisations on it (separately, allowing user to manage them): - converting to SSA form as one of necessary steps before encoding; - (more? – I'm not thinking about it yet);

3.4.1 Loop unrolling

The original program encoded into the `XGraph` represents a *flow graph*, a connected cyclic directed graph with single source node `[ENTRY]` (usually for convenience all leaves are connected to the sink node `[EXIT]`). The cycles are caused by low-level jump instructions, obtained from non-linear high-level control-flow statements (such as `while`, `do-while`, `for`, etc.). However, the cyclic flow graph cannot be encoded into SMT formula since ... //TODO:REFERENCE.

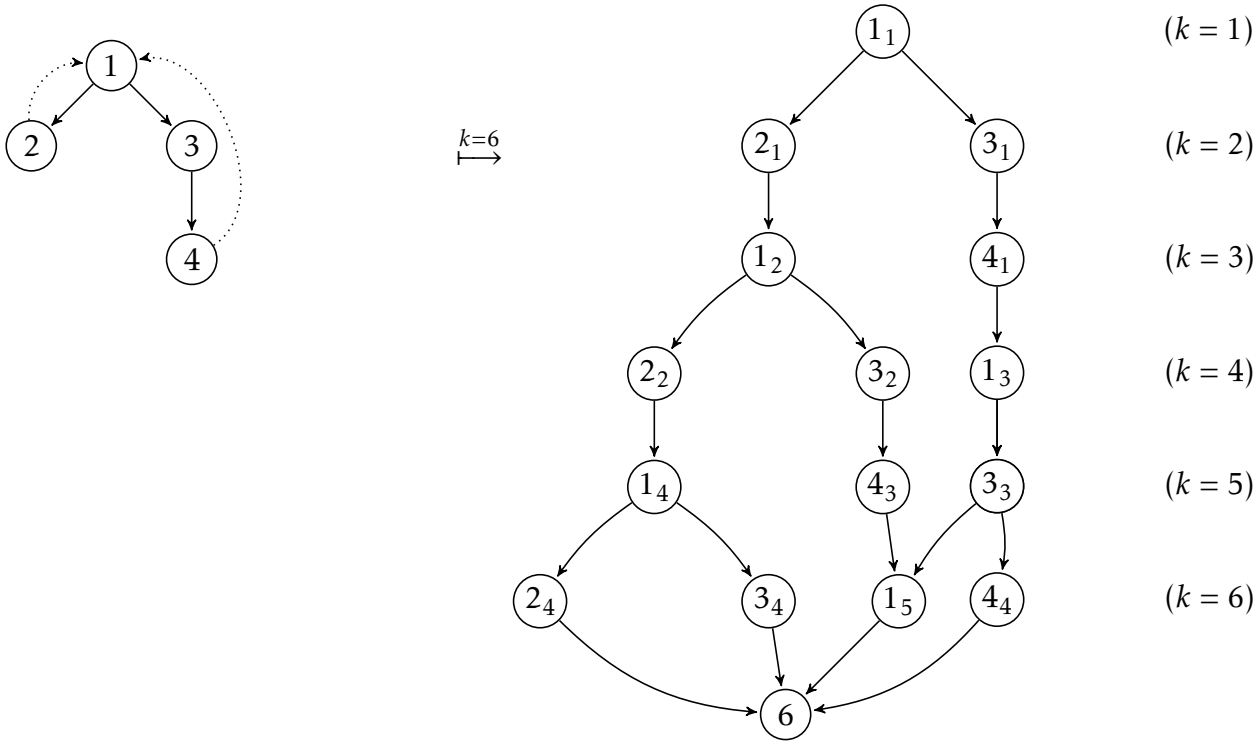


Figure 3.1: *Example of the flow graph from the Figure* **??**, *unwinded up to the bound* $k = 6$

3.5 XGraph to ZFormula (SMT) encoder

- Then, this modified event-representation is being encoded to SMT formula and sent to the solver.

3.6 Optimisations

... performed on each stage

Chapter 4

Evaluation

4.1 Comparison with PORTHOS

4.1.1 Unique Features

4.1.2 Performance

4.2 Comparison with HERD

4.2.1 Unique Features

4.2.2 Performance

Chapter 5

Summary

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