Features	UART (RS232)	SPI	I2C
Full Form	Universal Asynchronous Receiver/Transmitter	Serial Peripheral Interface	Inter-Integrated Circuit
Interface Diagram	TxD RxD RxD TxD (Device-1) (Device-2) UART Interface Diagram	MISO MOSI SCK CS CS (Slave-2) MISO MOSI SCK CS CS (Slave-2)	SDA SCL (Master-1) SDA SCL SDA SCL (Slave-1) SDA SCL (Slave-2) SCL (Slave-2) SCL (Slave-2) SCL (Slave-2)
Pin Designations	TxD: Transmit Data RxD: Receive Data	SCLK: Serial Clock MOSI: Master Output, Slave Input MISO: Master Input, Slave Output SS: Slave Select	SDA: Serial Data SCL: Serial Clock
Data rate	As this is is asynchronous communication, data rate between two devices wanting to communicate should be set to equal value. Maximum data rate supported is about 230 Kbps to 460kbps.	Maximum data rate limit is not specified in SPI interface. Usually supports about 10 Mbps to 20 Mbps	I2C supports 100 kbps, 40 kbps, 3.4 Mbps. Some var also supports 10 Kbps and Mbps.
Distance	Lower about 50 feet	highest	Higher
Type of communication	Asynchronous	Synchronous	Synchronous
Number of masters	Not Application	One	One or more than One

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Clock	No Common Clock signal is used. Both the devices will use there independent clocks.	There is one common serial clock signal between master and slave devices.	There is common clock signal between multiple masters and multiple slaves.
Hardware complexity	lesser	less	more
Protocol	For 8 bits of data one start bit and one stop bit is used.	Each company or manufacturers have got their own specific protocols to communicate with peripherals. Hence one needs to read datasheet to know read/write protocol for SPI communication to be established. For example we would like SPI communication between microcontroller and EPROM. Here one need to go through read/write operational diagram in the EPROM data sheet.	It uses start and stop bits. It uses ACK bit for each 8 bits of data which indicates whether data has been received or not. Figure depicts the data communication protocol.
Software addressing	As this is one to one connection between two devices, addressing is not needed.	Slave select lines are used to address any particular slave connected with the master. There will be 'n' slave select lines on master device for 'n' slaves.	There will be multiple slaves and multiple masters and all masters can communicate with all the slaves. Upto 27 slave devices can be connected/addressed in the I2C interface circuit.

Features	UART (RS232)	SPI	12C
Advantages	• It is simple communication and most popular which is available due to UART support in almost all the devices with 9 pin connector. It is also referred as RS232 interface.	*It is simple protocol and hence so not require processing overheads. *Supports full duplex communication. *Due to separate use of CS lines, same kind of multiple chips can be used in the circuit design. *SPI uses push-pull and hence higher data rates and longer ranges are possible. *SPI uses less power compare to I2C	*Due to open collector design, limited slew rates can be achieved. *More than one masters can be used in the electronic circuit design. *Needs fewer i.e. only 2 wires for communication. *I2C addressing is simple which does not require any CS lines used in SPI and it is easy to add extra devices on the bus. *It uses open collector bus concept. Hence there is bus voltage flexibity on the interface bus. *Uses flow control.
Disadvantages	They are suitable for communication between only two devices. It supports fixed data rate agreed upon between devices initially before communication otherwise data will be garbled.	As number of slave increases, number of CS lines increases, this results in hardware complexity as number of pins required will increase. To add a device in SPI requires one to add extra CS line and changes in software for particular device addressing is concerned. Master and slave relationship can not be changed as usually done in I2C interface. No flow control available in SPI.	*Increases complexity of the circuit when number of slaves and masters increases. *I2C interface is half duplex. *Requires software stack to control the protocol and hence it needs some processing overheads on microcontroller/microprocessor.