LVDS & M-LVDS
Overview

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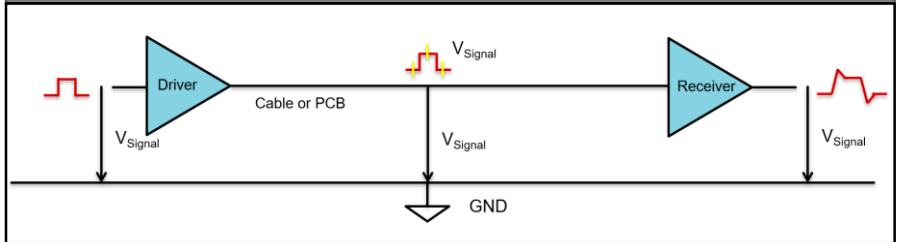
Product Marketing Engineer
Nov. 8th , 2023

Agenda

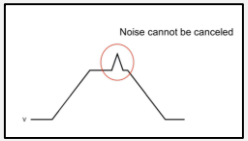
- Overview of Differential Signaling
- LVDS TIA/EIA-644 Introduction
- M-LVDS TIA/EIA-899 Introduction
- TI Portfolio Selection
- Design Considerations
- Resources

Single Ended vs Differential Signaling

Single Ended

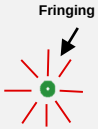


Ex) CMOS, TTL, GTL, ECL, RS-232, etc
Voltages referenced from signal to ground (5V, 3.3V, 1.8V)

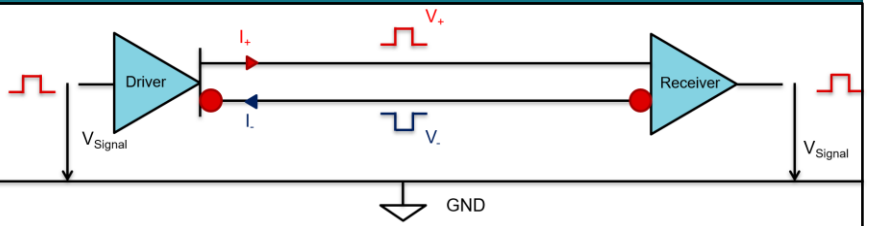


Advantages
+ Simple implementation

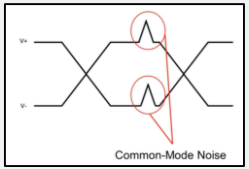
Disadvantages
- Vulnerable to noise
- Doesn't allow ground potential differences
- Generates EMI
- Limited by speed and distance



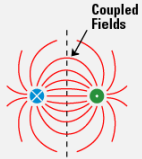
Differential



Ex) LVDS, M-LVDS, RS-422, RS-485, PECL, etc
Voltages referenced from V+ to V-

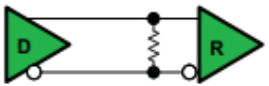
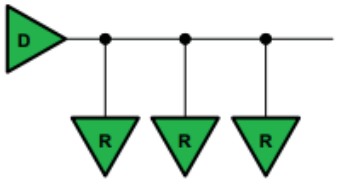
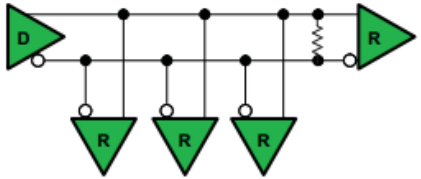
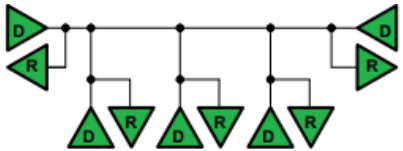
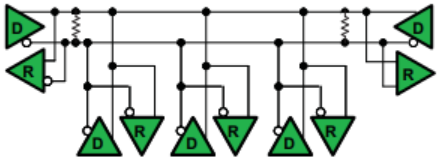


Advantages
+ Noise Rejection
+ Allows ground potential differences
+ Minimal EMI emission
+ Allows high speed and long distance



Disadvantages
- Twisted Pair Cable Required

Modes of Operation

	Single Ended	Differential	Example Application
Point-to-Point			Board to Board control and data signaling Ex) LVDS, RS-422, CML, LVPECL
Multidrop			Clock and data distribution, backplane Ex) M-LVDS, RS-485, CAN
Multipoint			Bidirectional clock, control and data transmission, backplane Ex) M-LVDS, RS-485, CAN

Differential Data Transmission Standards

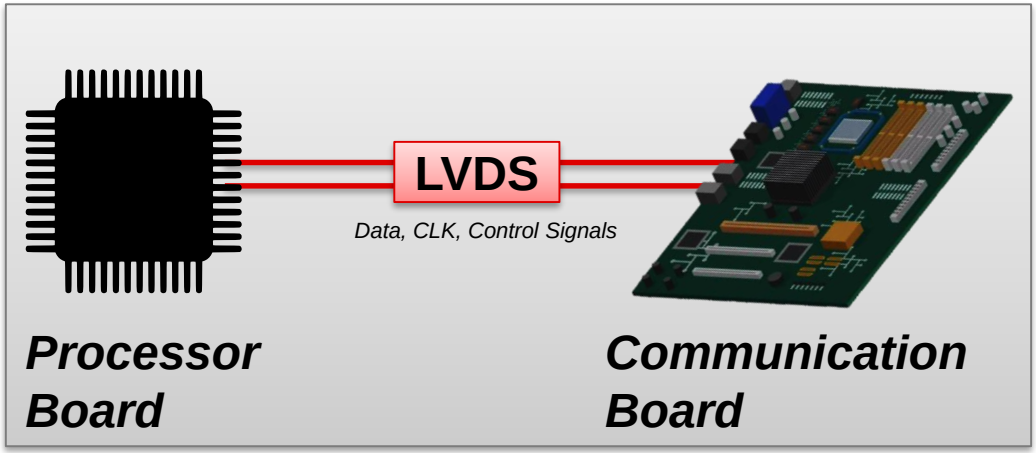
	LVDS	LVPECL	RS-422	CML	M-LVDS	RS-485	CAN
Industry Standard	TIA/EIA-644-A	N/A	TIA/EIA-422-B	N/A	TIA/EIA-899-A	TIA/EIA-485-A	ISO 11898
Bus Topology	Point to Point Multidrop	Point to Point	Point to Point Multidrop	Point to Point	Point to Point Multidrop Multipoint	Point to Point Multidrop Multipoint	Point to Point Multidrop Multipoint
Number of Drivers	1	1	1	-	≤ 32	≤ 32 - 256 (UL)	≤ 30
Number of Receivers	≤ 10	1	≤ 10	-	≤ 32	≤ 32	≤ 30
Maximum Data Rate	**≤ 3.125 Gbps**	≤ 10 Gbps	≤ 40 Mbps	≤ 10 Gbps	**≤ 500 Mbps**	50 Mbps	1 Mbps
Maximum Cable Length (m)	**10**	-	1200	1	**30**	1200	400
Vcc (v)	**1.8, 2.5, 3.3, 5**	3.3	3.3, 5	-	3.3	3.3, 5	3.3, 5
Power Consumption	**Very Low**	Medium	High	Low	**Low**	High	High
OSI Model Layers	Physical	Physical	Physical	Physical	Physical	Physical	Physical + Datalink
DRIVER CHARACTERISTICS							
Load Resistance (Ω)	100	50	100 - 130	50	50	60	Zo
Offset Voltage Vos (V)	1.125 - 1.375	2	±3	Vcc – 0.2V	0.3 - 2.1	-1 - 3	-
Differential Output Voltage (V)	250 - 450	800	±2	400	580 - 650	1.5 - 5	-
Driver Current Load (mA)	2.5 - 4.5	15	-	-	9 - 13	~40	~50
RECEIVER CHARACTERISTICS							
Input Voltage Range (V)	0 - 2.4	2.5 / 3.3	-10 - 10	-	-1.4 - 3.8	-7 - 12	-2 - 7
Input Threshold (mV)	±100	±200	-	-	±50	±200	-
Vcm (V)	±1	Varies	±7	-	±2	±6	-

SLAA067C - Comparing Bus Solutions

LVDS Introduction

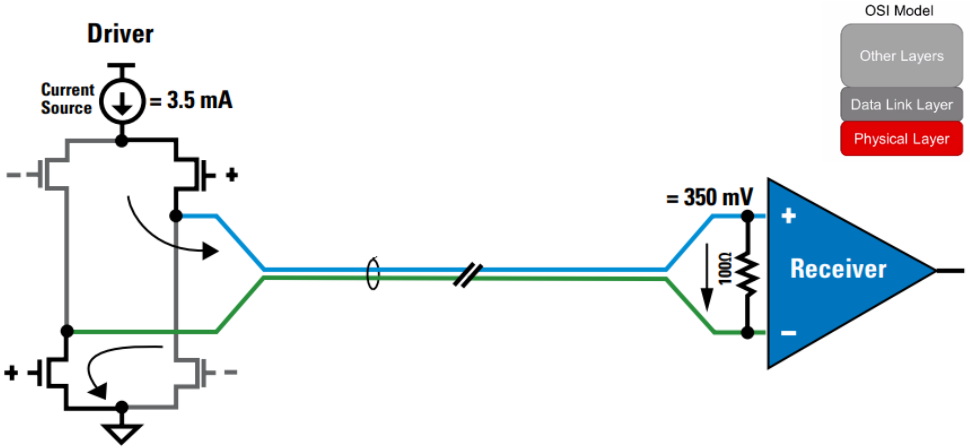
What is LVDS?

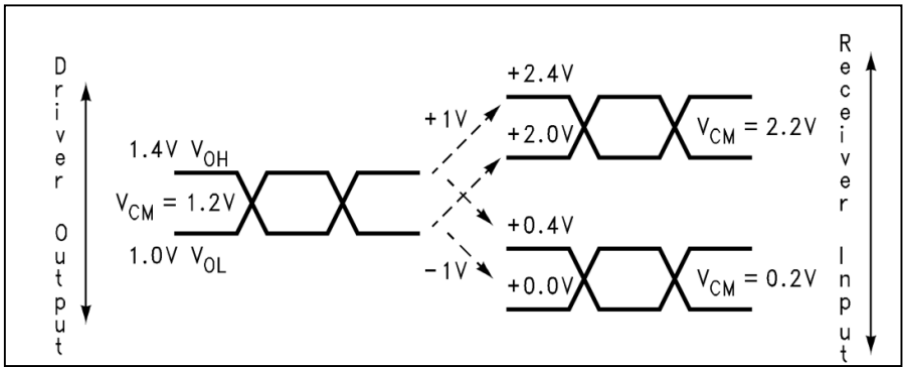
- TIA/EIA-644, Low Voltage Differential Signaling
- High speed general purpose digital interface
- Benefits: **Data Rate & Distance**, **Low Power**, **Low EMI**



	LVDS
Industry Standard	TIA/EIA-644-A
Bus Topology	Point to Point Multidrop
Number of Drivers	1
Number of Receivers	≤ 10
Maximum Data Rate	≤ 3.125 Gbps
Maximum Cable Length	15m
Vcc	1.8V, 2.5V, 3.3V, 5V
Power Consumption	Very Low

LVDS | TIA/EIA-644 Electrical Spec

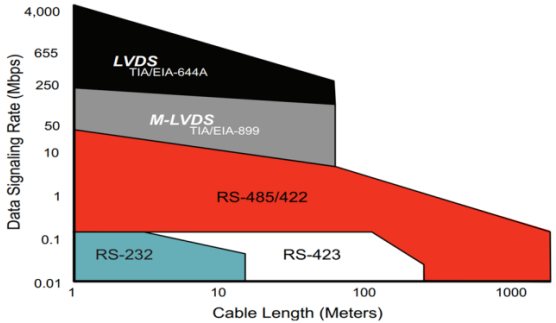




- Typical driver V_{CM} is 1.2V, and typical receiver common mode range is 0.2V to 2.2V
- ±1V receiver ground shift tolerance
- ±100mV receiver threshold
- Driver output is 350mV so plenty of margin

LVDS | Why is it used?

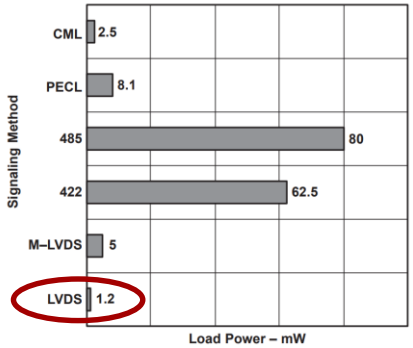
Data Rate & Distance

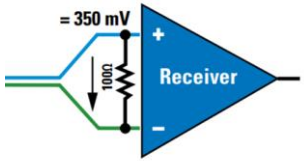


- Up to 3.125Gbps depending on:
  - ✓ Cable quality
  - ✓ PCB layout
  - ✓ Distance
- Up to 10-15m depending on:
  - ✓ Data rate
  - ✓ Tolerable signal distortion
  - ✓ Common mode noise
  - ✓ Tolerable jitter

SLAA844 - How Far, How Fast LVDS?

Low Power



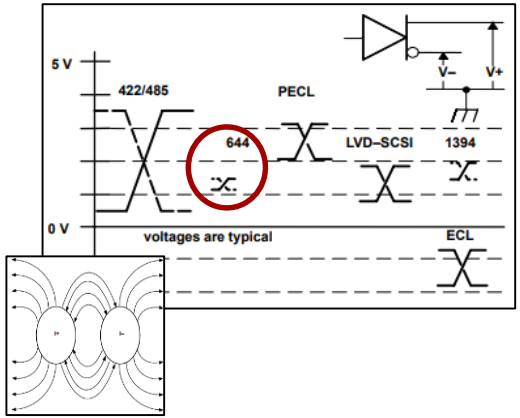


$$P_d = \frac{V_{diff}^2}{R} = \frac{(350mV)^2}{100\Omega} = \mathbf{1.225mW}$$

- Over 30x less power than RS-422

SNLA156 - LVDS High Speed with mW Power

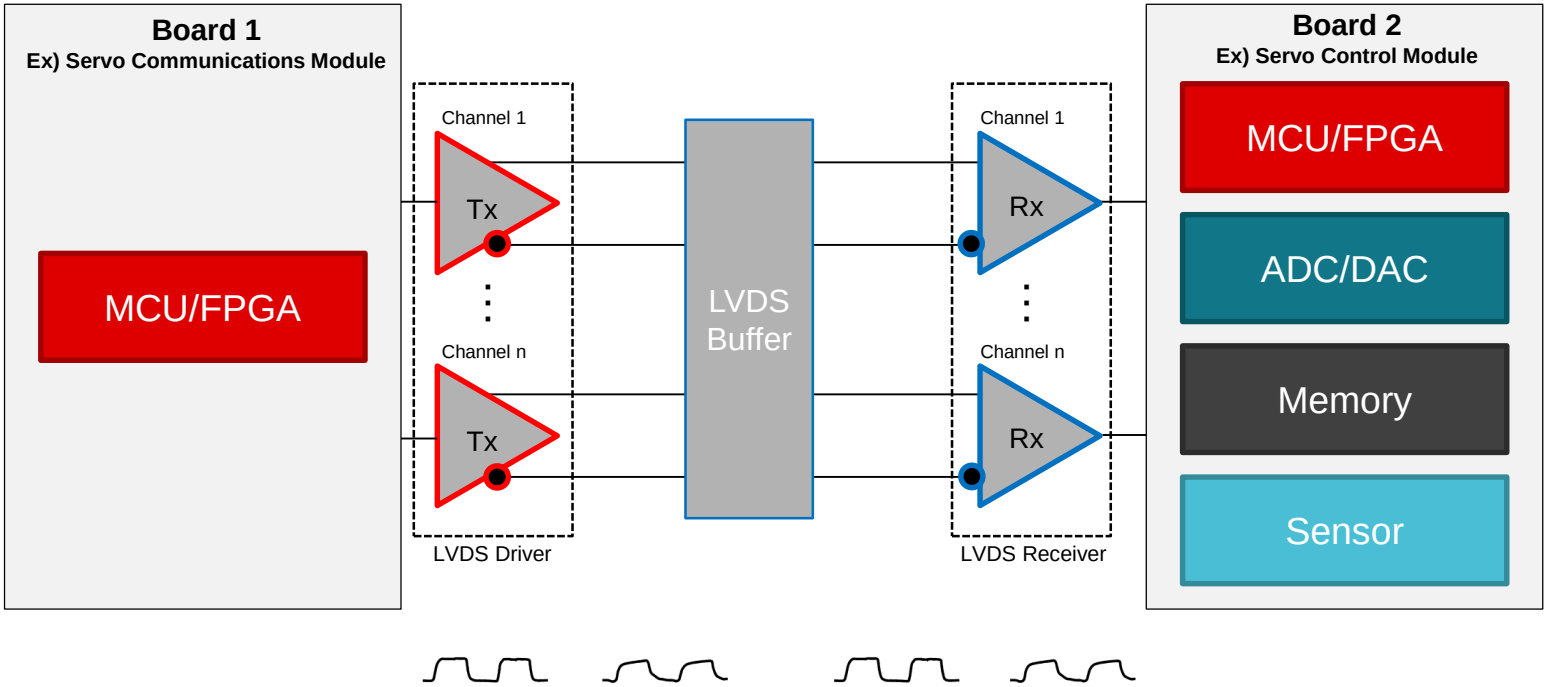
Low EMI



- EMI increases with rate and amplitude of the change in current
- LVDS manages to reduce EMI even at high signaling rates due to the very small 450mV max voltage swing

SLLA030C - Reducing EMI with LVDS

LVDS | How is it used?



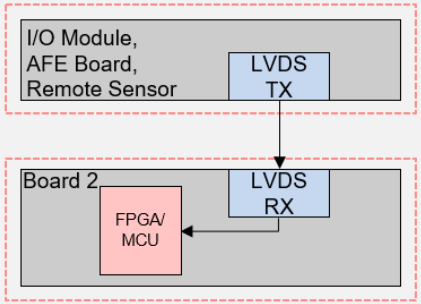
LVDS | Example Use Cases

Industrial
Automotive
Personal Electronics

Interface I/O Module/AFE and FPGA/MCU

Interfacing with I/O modules and sensors typically require high data rates over long cable. This is achieved through LVDS.

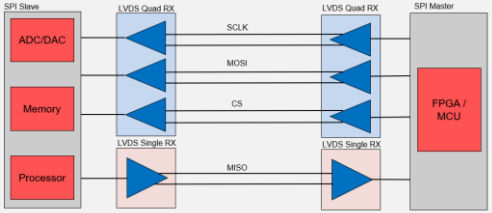
Key End Equipment
- Digital Cockpit Controller
- Multi-Mode Radar
- HEV/EV Wireless Charging
- ATE Tester
- Ultrasound Scanner
- Oscilloscope & Spectrum Analyzer
- Robotic Controller
- Machine Vision Camera



SPI/UART over LVDS

Transmitting SE SPI signals over long distances distorts signal integrity due to external noise and cross talk. Implementing SPI over LVDS improves noise immunity, propagation delay, ground shift and more enabling long distance SPI transmission.

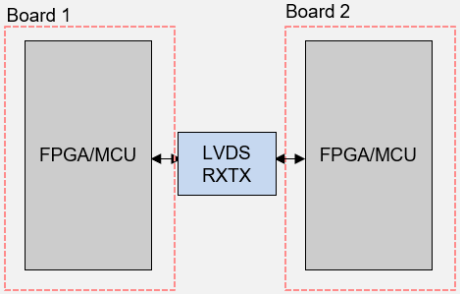
Key End Equipment
- Automotive Traction Invertor
- Elevator & Traction Inverter
- LED Wall



Interface between FPGA/MCUs

Provides high noise immunity for board to board communication at high signaling rates.

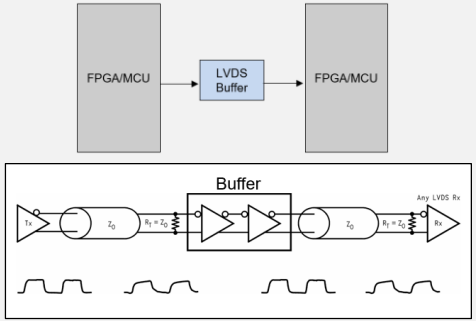
Key End Equipment
- Set Top Box & DVR
- Automated Sorting Equipment
- Ultrasound & CT Scanners
- Multifunction Printer (MFP)
- Oscilloscope & Spectrum Analyzer
- AC Drive Control Module
- LED Wall



Extending LVDS Reach with Buffers

Buffers are utilized to repeat LVDS signals. This enables designers to extend the reach of high speed links and hide the effect of transmission line stubs

Key End Equipment
- Ultrasound Scanner
- Field Instrumentation
- PLC Controller
- Datacenter Switch

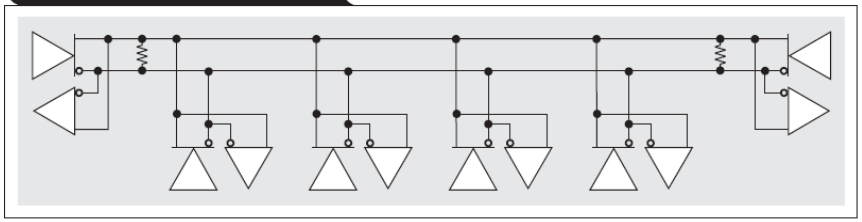


M-LVDS Introduction

M-LVDS | TIA/EIA-899 Electrical Spec

- Multipoint-LVDS for multipoint networks
  - Point-to-Point for extended reach
  - 32 total drivers and receivers on one bus
  - Requires 100Ω termination at both ends of differential pair
  - Physical layer only

Figure 1. Multipoint configuration

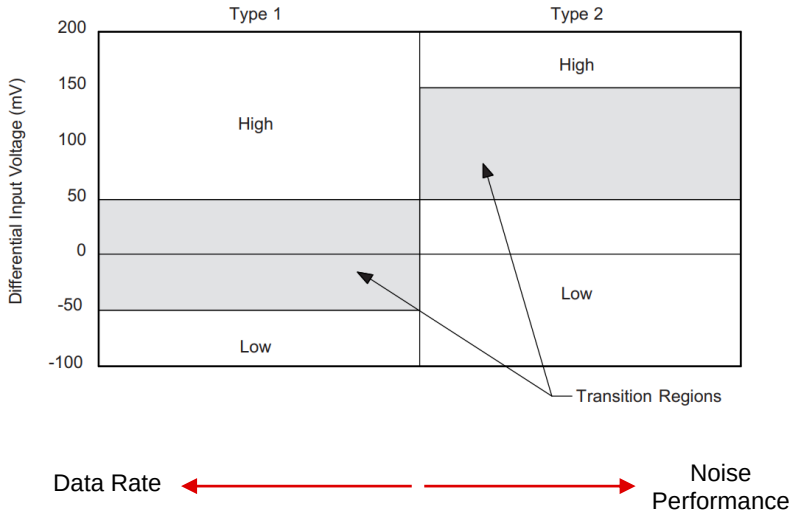


Parameter	LVDS	M-LVDS
Nominal Driver Current (mA)	3.5	11.3 mA
Nominal Driver Load (Ω)	100	50
Receiver Sensitivity (mV)	±100	±50
Input Common Mode Voltage Range (V)	0 to 2.4	-1.4 to 3.8
Number of Transceivers on Bus	1	Up to 32

M-LVDS | Failsafe Receivers

Two different receivers for open input fault condition

RECEIVER TYPE	OUTPUT LOW	OUTPUT HIGH
Type 1	$-2.4\ V \le V_{ID} \le -0.05\ V$	$0.05\ V \le V_{ID} \le 2.4\ V$
Type 2	$-2.4\ V \le V_{ID} \le 0.05\ V$	$0.15\ V \le V_{ID} \le 2.4\ V$



- **Type 1 Receiver:**
  - Useful for maximizing signal speed such as data or clock lines

Vid	Output
≤ -50mV	Low
≥ 50mV	High
-50mV ≤ Vid ≤ 50mV	Indeterminate

- **Type 2 Receiver:**
  - Under open-circuit conditions, output will be low
  - Useful for lower speed applications such as control lines

Vid	Output
≤ 50mV	Low
≥ 150mV	High
50mV ≤ Vid ≤ 150mV	Indeterminate

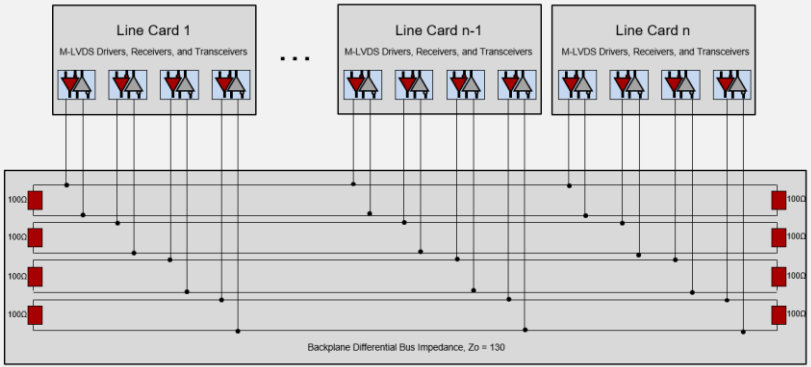
M-LVDS | Example Use Cases

Backplane Data, Clock, & Control Distribution

M-LVDS Enables a high throughput backplane (200Mbps / 100MHz) with excellent signal integrity, minimal EMI and power. These systems can use multi-drop or multipoint distribution of clock, data and control signals

Key End Equipment

- Wireless BBU
- Industrial PC
- Programmable Logic Controller
- Condition Monitoring Module

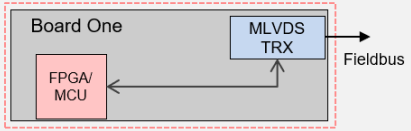


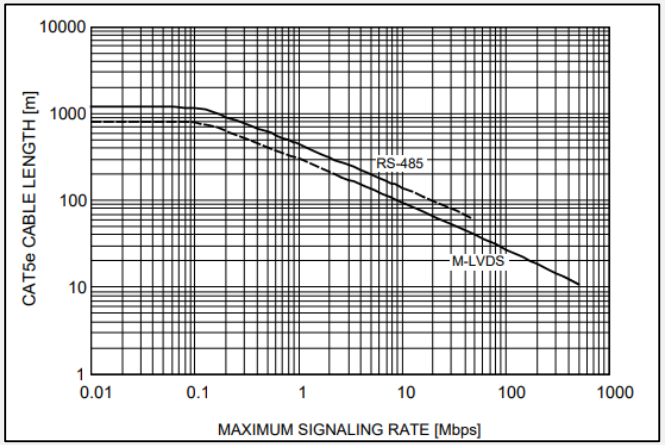
Point-to-Point Long Cable Transmission

The benefit of M-LVDS increased driver current can be extended to point-to-point applications. These systems typically require some or all of the following: long reach, low power, high speed, high noise immunity. M-LVDS is capable of transmitting up to 500Mbps at short distances and 1000m at slow speeds.

Key End Equipment

- Intra-DC Interconnect
- Multifunction Relay
- Vacuum robot
- Professional Video Camera
- Surgical Equipment

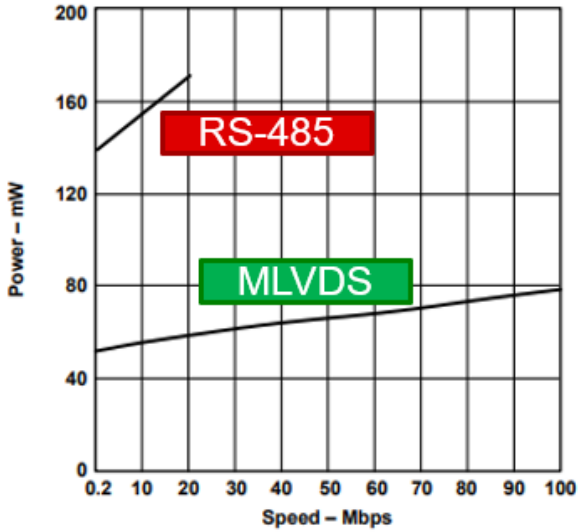




M-LVDS | A Highspeed Alternative to RS-485

M-LVDS Benefits: Lower Prop Delay, Power, & EMI

Parameter	RS-485	M-LVDS
V_{OD} [V]	1.5 to 5.0	0.48 to 0.65
I_{DD} [mA]	28 to 93	9 to 13
I_{OS} [mA]	<250	<43
t_{RISE} / t_{FALL} Typ [ns]	5 to 50	1 to 5
Data Rate Max [Mb/s]	40	250
V_{ID} [V]	0.4 to 5.0	0.1 to 2.4
V_{ICM} [V]	-5.0 to 12.0	-1.4 to 3.8



SLLA106 - TIA/EIA-485 and M-LVDS, Power and Speed Comparison

RS-422/485 to LVDS/MLVDS P2P Guide

LVDS	RS422	Description
SN65LVDS31	AM26LS31	Quad driver, 4-line enabling scheme
SN65LVDS32	AM26LS32	Quad receiver, 4-line enabling scheme
SN65LVDS3486	MC3486	Quad receiver, 2-line enabling scheme
SN65LVDS3487	MC3487	Quad driver, 2-line enabling scheme
SN65LVDS9637	uA9637	Dual receiver
SN65LVDS9638	uA9638	Dual driver
SN65LVDS050	SN75C1167	Dual drivers/receivers with enabling scheme
SN65LVDS051	SN75C1168	Dual drivers/receivers

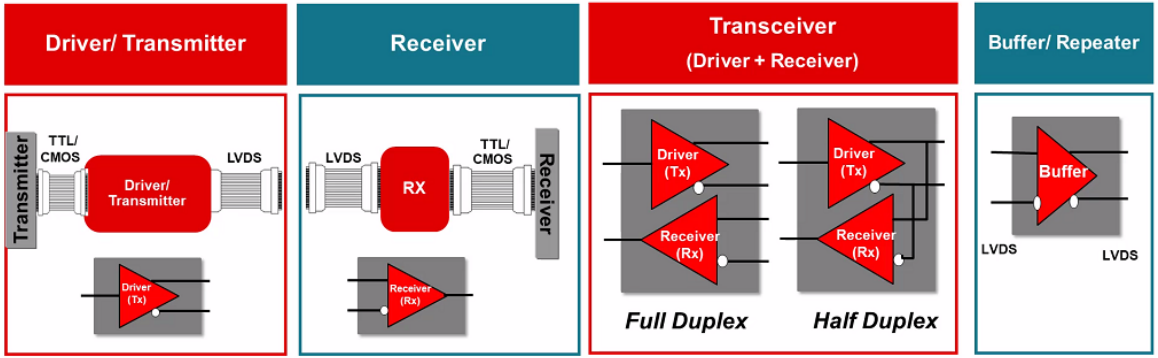
MLVDS	RS485	Description
SN65LVDS179	SN75LBC179	Single driver/receiver
SN65LVDS180	SN75LBC180	Single driver/receiver with enabling scheme
SN65LVDM176	SN75LBC176	Single Transceiver with enabling

Considerations

- Transmission Length – Ensure distance and signaling rate do not exceed maximum limit (MLVDS ~50m | LVDS ~10m)
- Cabling – Cat5 Acceptable
- Termination – 100Ohm Termination Required
- Electrical Characteristics – Ensure max ground potential shift is acceptable (±1V LVDS | ±2V MLVDS), Backplane loading <32 nodes MLVDS

SLLA031A - Using an LVDS Receiver with TIA/EIA–422 Data

LVDS, M-LVDS | Portfolio

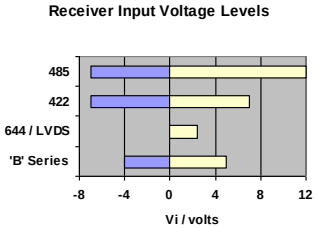


Standard	LVDS (DS90LVxx | SN65LVDSxx)				MLVDS (DS91Mxx | SN65MLVDxx)			
Function	Driver	Receiver	Transceiver	Buffer	Driver	Receiver	Transceiver	Buffer
Input Signal	LVCMOS, LVTTL	LVDS	LVDS, LVCMOS, LVTTL	LVDS	LVCMOS, LVTTL	M-LVDS	M-LVDS, LVCMOS, LVTTL	MLVDS
Output Signal	LVDS	LVCMOS, LVTTL	LVDS, LVCMOS, LVTTL	LVDS	M-LVDS	LVCMOS, LVTTL	M-LVDS, LVCMOS, LVTTL	MLVDS
Vcc (V)	5, 3.3, 2.5	5, 3.3, 2.5, 1.8	3.3	3.3	3.3	3.3	3.3	3.3
Max Signaling Rate (Mbps)	630	600	500	800	250	250	250	250
Max Channels	16	16	2	4	4	4	8	8
Features	Extended Vcm, High ESD, Integrated Termination, Fanout Buffering				Type 1&2 Rx, Half/Full Duplex			

LVDS, M-LVDS | Feature Spotlight

Extended Common Mode

-4 to 5V Receiver Common Mode Range



Data Transmission:

1. *over Longer Distances*
2. *In Noisier Environments*

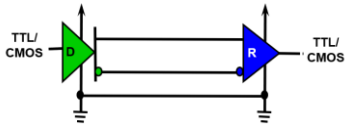
Supported Products:

SN65LVDS3x

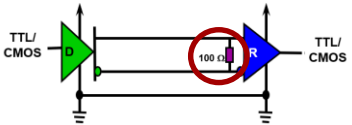
Integrated Termination Resistors

Space and Cost Savings

Standard LVDS Receiver



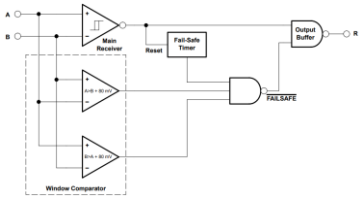
Integrated Termination



DS90LTx, SN65LVDTx

Receiver Failsafe

Maintains receiver output when valid input is not present

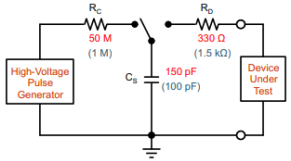


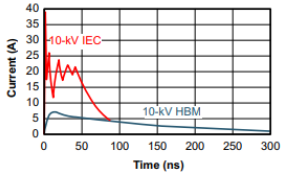
SLLA082B - Active Fail-Safe in TI's LVDS Receivers

SN65LVDS3x

High ESD

7kV+ HBM ESD

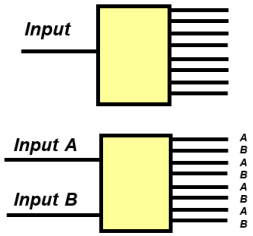




DS90LV048/7, SN65LVDS3x

Fanout Buffering

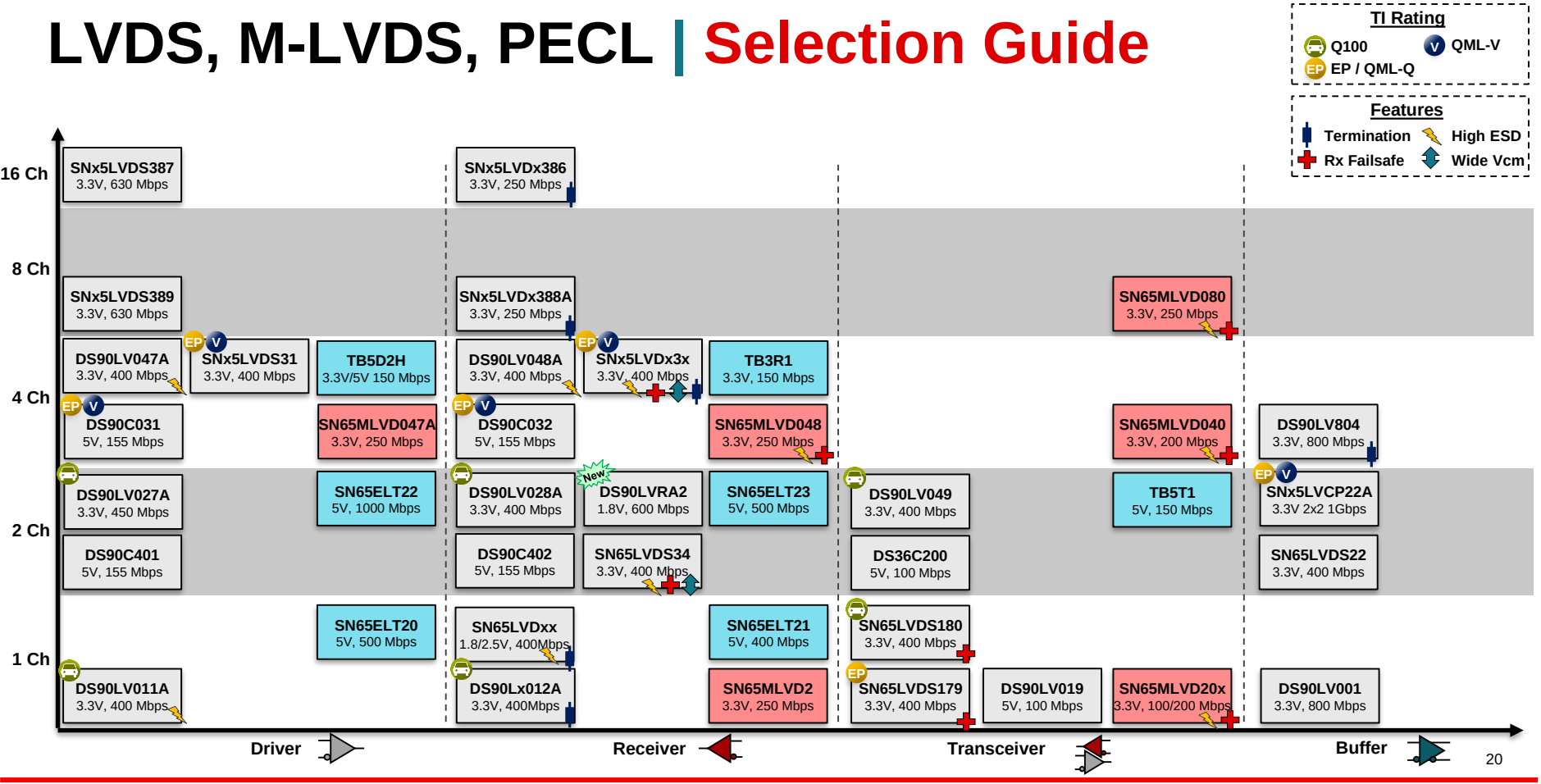
Clock and Data Distribution



1 : 4/8/9/10/16
2 : 2

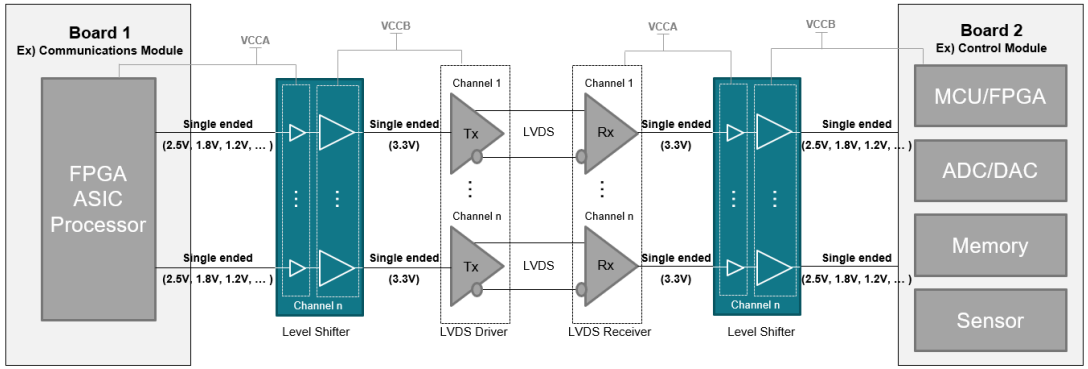
DS90LV110, SN65MLVD12x, DS92CK16, DS10BR254 SN65LVDS117

LVDS, M-LVDS, PECL | Selection Guide



LVDS PECL MLVDS

Enabling LVDS for low power FPGAs/Processors



Channel	LVDS Driver	LVDS Receiver	Level Shifter (3.3V / 5V)
1	DS90LV011A	DS90LV012A	SN74AXC1T45 / SN74LXC1T45
2	DS90LV027A	DS90LV28A	SN74AXC2T245 / SN74LXC2T245
4	DS90LV047A	DS90LV048A	SN74AXC4T245 / SN74LXC4T245
8	SN65LVDS388A	SN65LVDS389A	SN74AXC8T245 / SN74LXC8T245

Enable low voltage I/O (0.65 - 3.3V with AXC and 1.1 - 5.5V with LXC)

Advantages:
- Simple implementation
- Interface across wide voltage range (0.65 – 5V)

Disadvantages:
- Data rate limited by level translator
- Increased component count (level shifter + decoupling caps)
- Larger footprint

NEW

1.8V LVDS family

DS90LVRA2 – 1.8V, dual channel LVDS receiver

SNLA307 - How to Support 1.8-V Signals Using a 3.3-V LVDS Driver/Receiver + Level-Shifter

LVDS | Packaging

1 Channel
(Driver/Receiver)

(D)

SOIC – 8 Pin
3.91mm x 4.9mm (19mm²)

(DBV)

SOT-23 – 5 Pin
1.6mm x 2.9mm (5mm²)

(RSE)

UQFN – 10 Pin
2.0mm x 1.5mm (3mm²)

SO | QFN

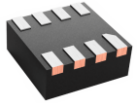
2 Channel
(Driver/Receiver)

(D)

SOIC – 8 Pin
3.91mm x 4.9mm (19mm²)

(DGK)

VSSOP – 8 Pin
3.0mm x 3.0mm (9mm²)

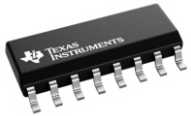


(DQF)

WSON – 8 Pin
2.0mm x 2.0mm (4mm²)

SO | SON

4 Channel
(Driver/Receiver)



(D)

SOIC – 16 Pin
3.91mm x 9.9mm (59mm²)

(PW)

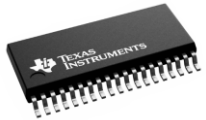
TSSOP – 24 Pin
4.4mm x 7.8mm (34mm²)

(PW)

TSSOP – 16 Pin
4.4mm x 5.0mm (22mm²)

SO

8 Channel &
16 Channel



(DBT)

TSSOP – 38 Pin
4.4mm x 9.7mm (43mm²)

(DGG)

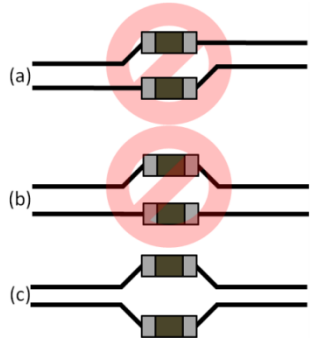
TSSOP – 64 Pin
8.1mm x 17mm (138mm²)

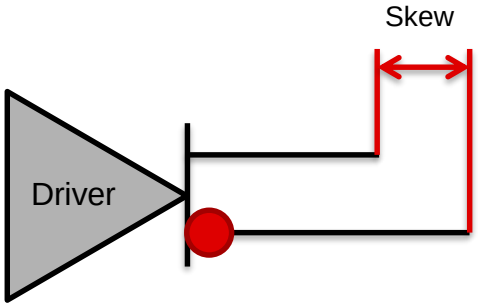
SO

Time/Size

Design Considerations

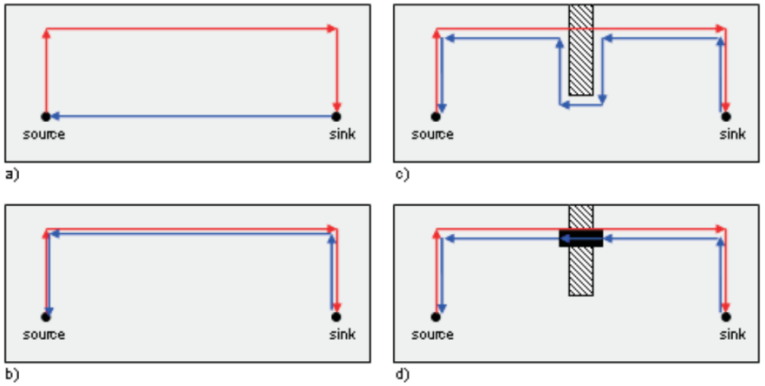
LVDS | Design considerations

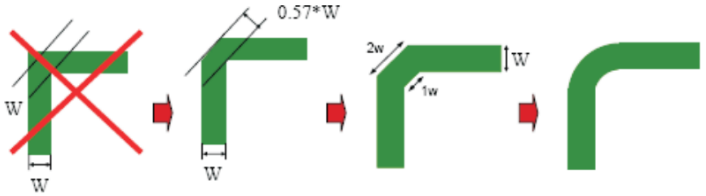




- PCB traces should be 100Ω (±5%) differential impedance
- Maintain equal length on traces to minimize intra-pair skew
- Maintain distance and symmetry between traces
- Minimize trace length lengths
- Minimize use of vias (<2 recommended)

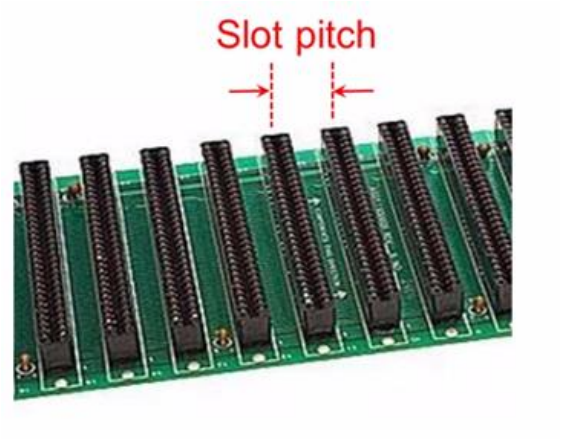
LVDS | Design considerations

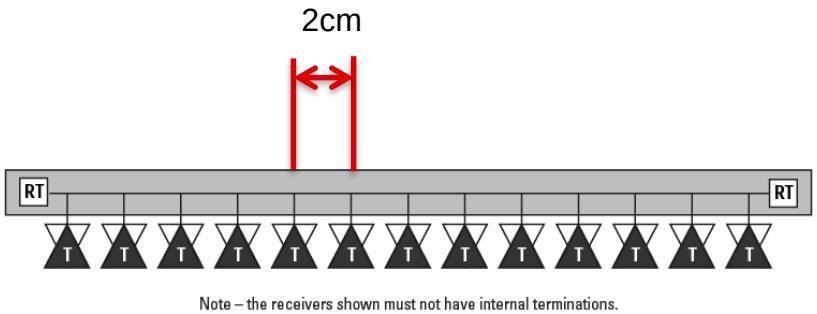




- Use a continuous ground plane underneath the traces
  - Avoid routing over plane splits/voids
  - Place stitching caps across split if unavoidable
- Avoid right angle turns
- Don’t route traces near edge of PCB
- Keep impedance matched across entire length
- Do not route near oscillators or switching regulators

M-LVDS | Design considerations



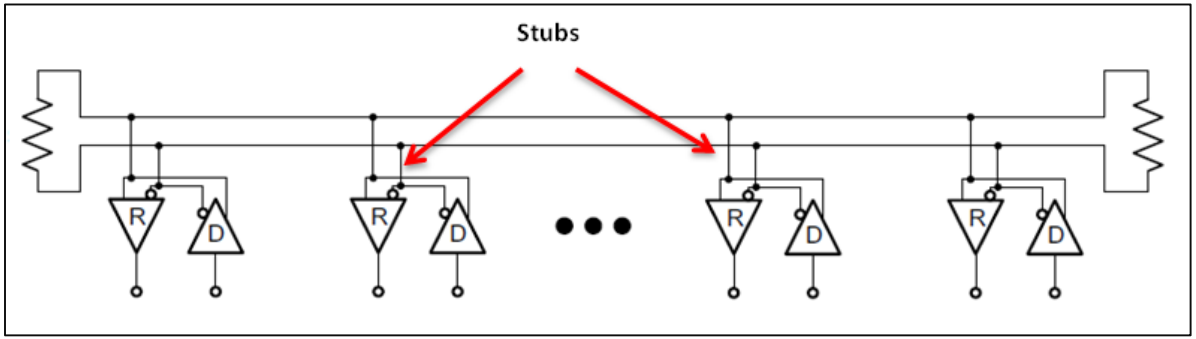


Note – the receivers shown must not have internal terminations.

- Evenly space loads
  - 2cm typical
  - Helps to evenly distribute the loading
- The amount of transceivers depends on how well the system is designed
  - PCB layout
  - Line impedance control
  - Proper termination
  - Stub length
  - Typically, 30 nodes at >200Mbps if well optimized

Stubs

- Terminations only on both edges of the bus
- Lines and connectors connecting boards to backplane create stubs



Guidelines for stubs

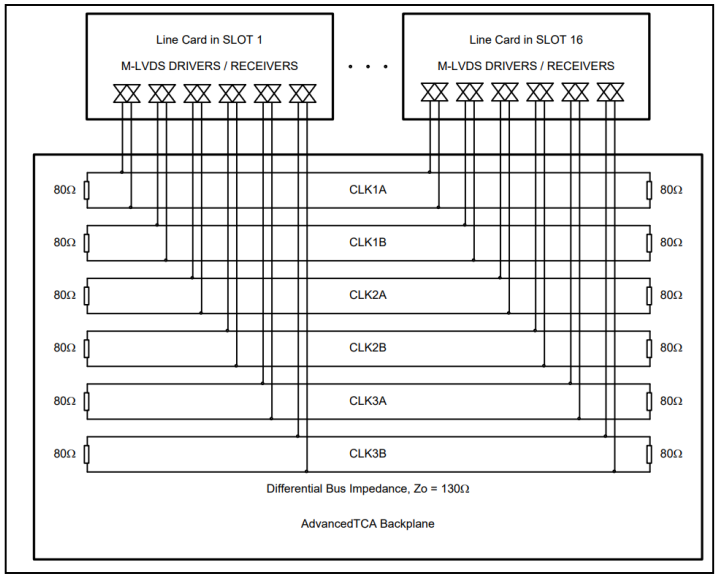
- Minimize length of the stubs to minimize their effect
- How short?
  - Depends on transition time (t_R, t_F)
- Keep t_P in stubs < 30% t_R/t_F
- The shorter the better!
  - Recommended < 1”
  - Shortening to ½” → increase noise margin 50%
- Test points → unintended stubs

Example:

- t_R/t_F (min) = 1.5 ns from datasheet
  → Stub Length < 0.5 ns
- For FR-4 (~1ns / 6”)
  → Stub Length < 3”

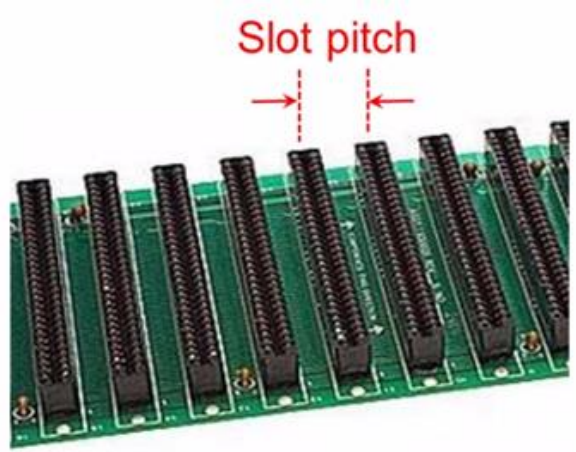
Selecting line characteristic impedance

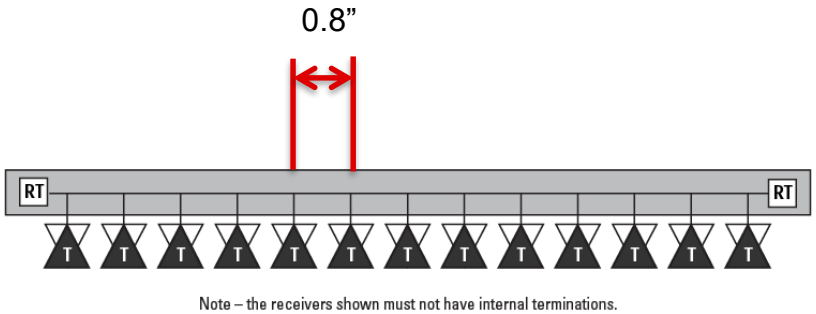
- Plug-in boards on the backplane create loading on the bus
  - Due to capacitance of stubs, transceiver I/Os, connectors, vias, etc.
  - Lowers the effective characteristic impedance of the bus
- Select Z_O to be higher than 100Ω
  - So that effective Z_O > 80 Ω
- Z_O = 130 was found to work well for heavily-loaded backplanes
- Terminations value should match effective Z_O of the line
  - To reduce reflections



Slots arrangement

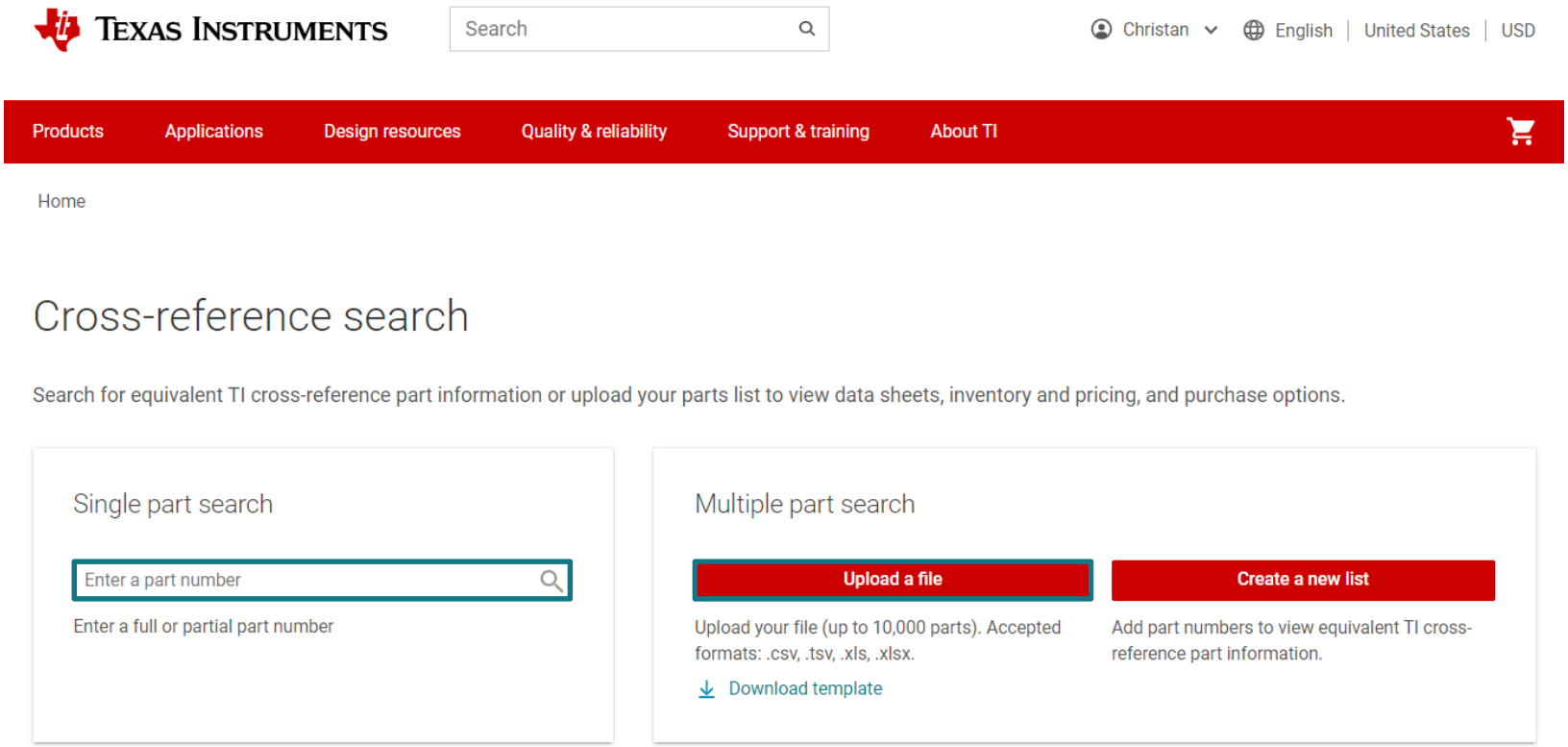
- Evenly space loads
  - 2cm typical
  - Helps to evenly distribute the loading
- The amount of transceivers depends on how well the system is designed
  - PCB layout
  - Line impedance control
  - Proper termination
  - Stub length
  - Typically, 30 nodes at >200Mbps if well optimized
- Slot pitch of 0.8” works well with ZO of 130 Ω



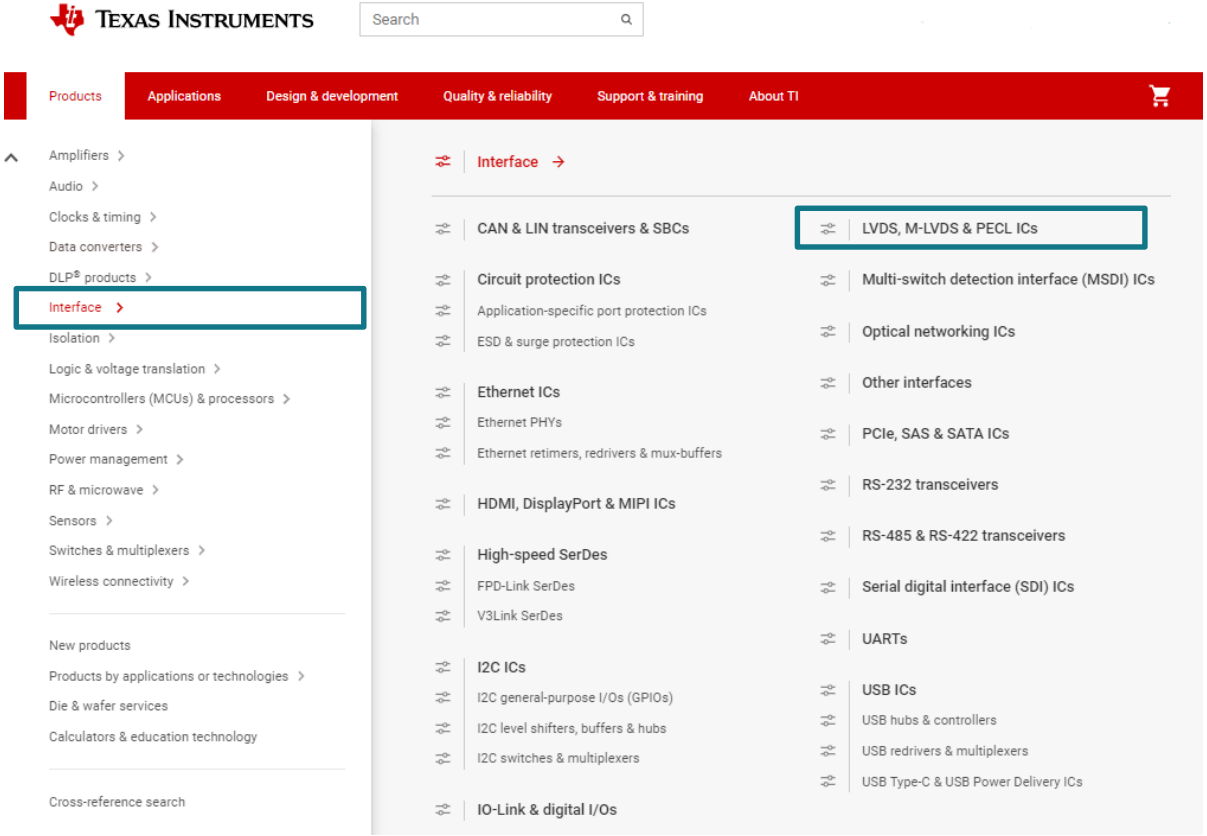


Note – the receivers shown must not have internal terminations.

Cross Reference Tool - https://www.ti.com/cross-reference-search



Where to find more Information - https://www.ti.com/LVDS



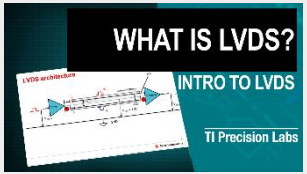
Solution-focused LVDS Content

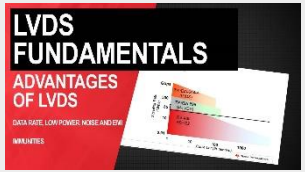
Getting Started with LVDS

LVDS Owners Manual

LVDS Application & Data Handbook

The **LVDS Fundamentals & Precision Labs** training series





Concepts made easy to understand

Type	Content Title
TI Reference Design(s)	• Transmitting SPI Signals Over LVDS Interface
Technical blog content or white paper	• High-Speed Layout Guidelines • Interface Different Logic with LVDS • Support 1.8V using 3.3V LVDS • MLVDS Clock & Data Distribution • LVDS for Noise Reduction in Motor Drives • LVDS in LED Walls • LVDS in Ultrasound • Introduction to M-LVDS • The top 5 questions when using M-LVDS in backplane applications
Selection and design tools and models	• M-LVDS evaluation module

Online support

Q&A

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