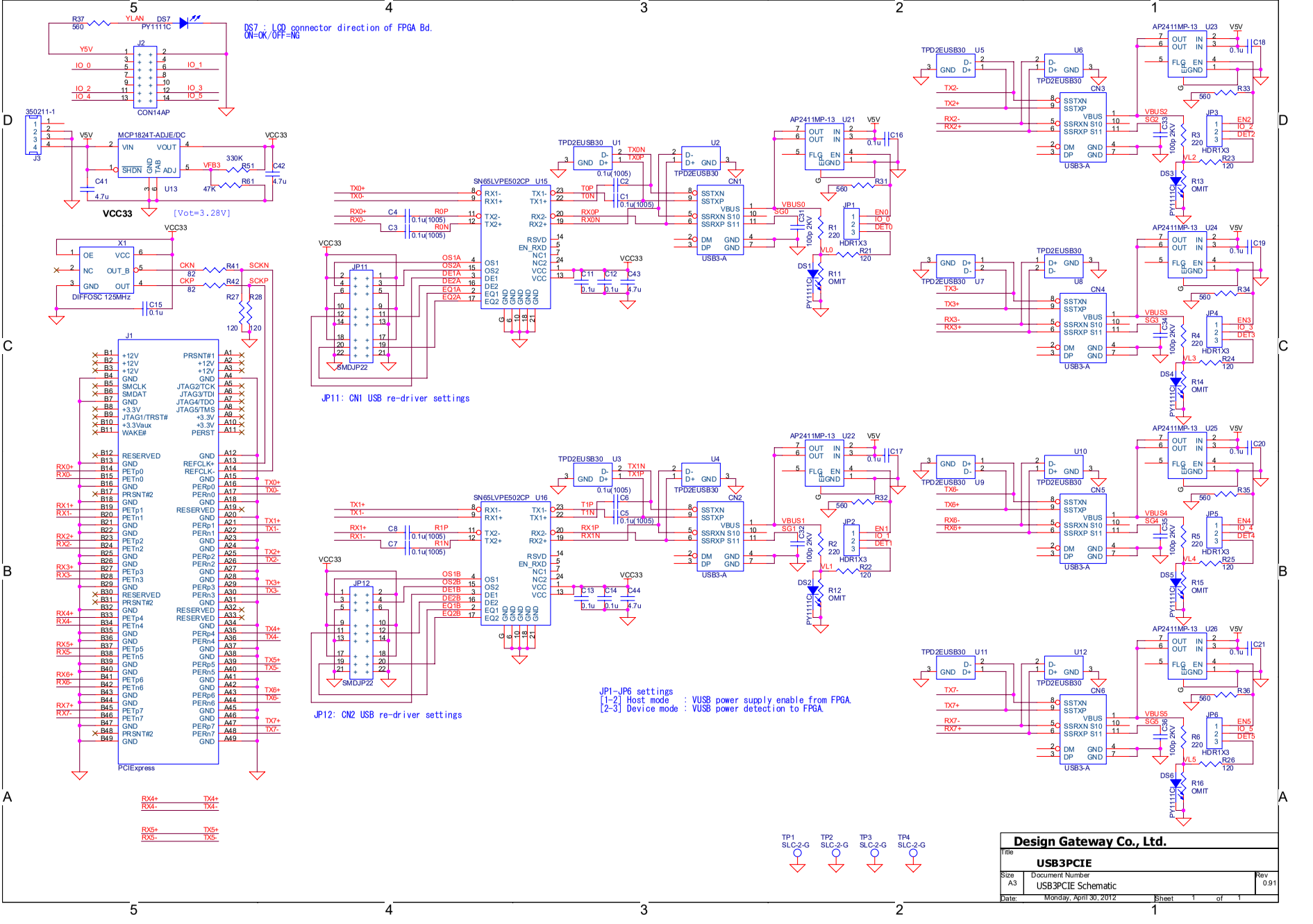
DS7 : LCD connector direction of FPGA Bd.
ON=OK/OFF=NG
R37 560
YLAN
DS7
PY1111C
J2
CON14AP
Y5V
IO_0
IO_1
IO_2
IO_3
IO_4
IO_5
J3
350211-1
V5V
MCP1824T-ADJE/DC
VIN
VOUT
SHDN
GND
TAB
ADJ
U13
VCC33
[Vot=3.28V]
C41 4.7u
VFB3
330K R51
47K R61
C42 4.7u
X1
OE
VCC
NC
OUT_B
GND
OUT
DIFFOSC 125MHz
C15 0.1u
CKN
CKP
82
R41
R42
SCKN
SCKP
R27
R28
120
J1
PCIExpress
+12V
GND
SMCLK
SMDAT
+3.3V
JTAG1/TRST#
+3.3Vaux
WAKE#
RESERVED
PETp0
PETn0
PRSNT#2
PETp1
PETn1
PETp2
PETn2
PETp3
PETn3
PETp4
PETn4
PETp5
PETn5
PETp6
PETn6
PETp7
PETn7
PRSNT#1
JTAG2/TCK
JTAG3/TDI
JTAG4/TDO
JTAG5/TMS
+3.3V
PERST
REFCLK+
REFCLK-
PERp0
PERn0
PERp1
PERn1
PERp2
PERn2
PERp3
PERn3
PERp4
PERn4
PERp5
PERn5
PERp6
PERn6
PERp7
PERn7
RX0+
RX0-
RX1+
RX1-
RX2+
RX2-
RX3+
RX3-
RX4+
RX4-
RX5+
RX5-
RX6+
RX6-
RX7+
RX7-
TX0+
TX0-
TX1+
TX1-
TX2+
TX2-
TX3+
TX3-
TX4+
TX4-
TX5+
TX5-
TX6+
TX6-
TX7+
TX7-
SN65LVPE502CP U15
SN65LVPE502CP U16
RX1-
RX1+
TX1-
TX1+
TX2-
TX2+
RX2-
RX2+
RSVD
EN_RXD
NC1
NC2
VCC
OS1
OS2
DE1
DE2
EQ1
EQ2
GND
TPD2EUSB30 U1
TPD2EUSB30 U2
TPD2EUSB30 U3
TPD2EUSB30 U4
TPD2EUSB30 U5
TPD2EUSB30 U6
TPD2EUSB30 U7
TPD2EUSB30 U8
TPD2EUSB30 U9
TPD2EUSB30 U10
TPD2EUSB30 U11
TPD2EUSB30 U12
D-
D+
GND
SSTXN
SSTXP
VBUS
SSRXN S10
SSRXP S11
DM
DP
USB3-A
CN1
CN2
CN3
CN4
CN5
CN6
TX0N
TX0P
RX0P
RX0N
TX1N
TX1P
RX1P
RX1N
C1 0.1u(1005)
C2 0.1u(1005)
C3 0.1u(1005)
C4 0.1u(1005)
C5 0.1u(1005)
C6 0.1u(1005)
C7 0.1u(1005)
C8 0.1u(1005)
R0P
R0N
R1P
R1N
VBUS0
VBUS1
VBUS2
VBUS3
VBUS4
VBUS5
SG0
SG1
SG2
SG3
SG4
SG5
C31 100p 2KV
C32 100p 2KV
C33 100p 2KV
C34 100p 2KV
C35 100p 2KV
C36 100p 2KV
R1 220
R2 220
R3 220
R4 220
R5 220
R6 220
HDR1X3
JP1
JP2
JP3
JP4
JP5
JP6
EN0
IO_0
DET0
EN1
IO_1
DET1
EN2
IO_2
DET2
EN3
IO_3
DET3
EN4
IO_4
DET4
EN5
IO_5
DET5
VL0
VL1
VL2
VL3
VL4
VL5
R21 120
R22 120
R23 120
R24 120
R25 120
R26 120
DS1
DS2
DS3
DS4
DS5
DS6
R11 OMIT
R12 OMIT
R13 OMIT
R14 OMIT
R15 OMIT
R16 OMIT
AP2411MP-13 U21
AP2411MP-13 U22
AP2411MP-13 U23
AP2411MP-13 U24
AP2411MP-13 U25
AP2411MP-13 U26
OUT
IN
FLG
EN
EGND
C16 0.1u
C17 0.1u
C18 0.1u
C19 0.1u
C20 0.1u
C21 0.1u
R31 560
R32 560
R33 560
R34 560
R35 560
R36 560
JP11
JP12
SMDJP22
OS1A
OS2A
DE1A
DE2A
EQ1A
EQ2A
OS1B
OS2B
DE1B
DE2B
EQ1B
EQ2B
C11 0.1u
C12 0.1u
C43 4.7u
C13 0.1u
C14 0.1u
C44 4.7u
JP11: CN1 USB re-driver settings
JP12: CN2 USB re-driver settings
JP1-JP6 settings
[1-2] Host mode : VUSB power supply enable from FPGA.
[2-3] Device mode : VUSB power detection to FPGA.
TP1 SLC-2-G
TP2 SLC-2-G
TP3 SLC-2-G
TP4 SLC-2-G
Design Gateway Co., Ltd.
Title
USB3PCIE
Size A3
Document Number
USB3PCIE Schematic
Rev 0.91
Date: Monday, April 30, 2012
Sheet 1 of 1