Data Sheet

VT6212 / VT6212L

PCI USB 2.0 Controller

Revision 1.10
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REVISION HISTORY

Document Release	Date	Revision	Initials
1.0	6/5/03	Initial external release	EY
1.01	2/27/04	Updated cover page Updated copyright page Changed pins 104, 103, 57, 58, 59, 97 to NC Updated pin-out diagram Updated pin list Updated pin descriptions	JW
1.02	10/21/04	Added figure 4, lead-free mechanical specification diagram	JW
1.03	12/21/04	Specified PCI 2.2 bus support	JW
1.04	4/19/05	Registers updated f0rx41[4], f0rx42[1-0], f0rx48[5], f0rx4B[0], f2rx41[4], f2rx48[5], f2rx49[7-5], f2rx4A, f2rx4B[5, 3-0], f2rx51	JW
1.05	11/16/05	Modified legal page Changed pins 60, 63, 64 and 102 to NC Updated pin-out diagram Updated pin list Updated pin descriptions	SV
1.06	12/7/05	Updated pin information	SV
1.07	8/18/06	Updated Figure 3, Figure 4, Figure 5 and Figure 6 in package mechanical specifications Updated legal page	TL
1.08	9/21/06	Updated Revision ID Code	TL
1.09	11/17/06	Updated Revision ID Code Modified power specifications in Table 5	TL
1.10	3/16/07	Updated mechanical specification diagram	JY

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VT6212 / VT6212L

PCI USB 2.0
4-Port Host Controller

USB 2.0 UHCI / EHCI Host Controller for the PCI 2.2 Bus

PRODUCT FEATURES

- **USB 2.0**
  - Compliant with Universal Serial Bus Specification Revision 2.0
  - Compliant with Enhanced Host Controller Interface Specification Revision 1.0
  - Compliant with Universal Host Controller Interface Specification Revision 1.1
  - PCI multi-function device consists of two UHCI Host Controllers for full/low-speed signaling and one EHCI Host Controller core for high-speed signaling
  - 4 downstream facing ports in the root hub with integrated physical layer transceivers shared by UHCI and EHCI Host Controllers
  - Supports PCI-Bus Power Management Interface Specification release 1.1
  - Legacy support for all downstream facing ports
  - 4 DMA engines with pipelined control for USB data transfer bandwidth improvement
  - Dynamic clock stop control for power consumption reduction
- **Serial EEPROM Support for Boot Register Update**
- **Cardbus Mode Support**
- **2.5V Power Supply with 5V Tolerant Inputs**
- **0.22µm, Low Power CMOS Process**
- **128-Pin PQFP (VT6212) and 128-Pin LQFP (VT6212L) Packages Available**
- **Schematics and PCB Reference Designs Available**
- **System Clock Using 24 MHz Crystal**
- **Support for PCI Mobile Design Guide**

OVERVIEW

The VT6212 / VT6212L USB 2.0 UHCI and EHCI Host Controller for the PCI 2.2 Bus provides higher bandwidth (480 Mbps) and is backward compatible with USB 1.1. It implements Universal Serial Bus Specification Revision 2.0 and is compliant with UHCI 1.1 and EHCI 1.0 with a 32-bit PCI host bus interface. The VT6212 / VT6212L adopts 4 DMA engines with pipelined control for USB data transfer bandwidth improvement and dynamic clock stop control for power consumption reduction.

The VT6212 / VT6212L supports 4 downstream facing ports with 1.5 (low-speed), 12 (full-speed) and 480 (high-speed) Mbps transaction capability. The Root Hub is integrated with physical-layer transceivers shared by UHCI (for full/low-speed) and EHCI (for high-speed) Host Controllers. The VT6212 / VT6212L also supports PCI-Bus Power Management Interface Specification 1.1 and has legacy support for all downstream facing ports.

The VT6212 / VT6212L is ready to provide a PCI 4-port USB2.0 peripheral-interface to satisfy the needs of desktops, mobile systems, and other host platforms. Support for the VT6212 / VT6212L is built into Microsoft Windows XP and Windows 2000. Win98SE and WinME drivers are provided by VIA.

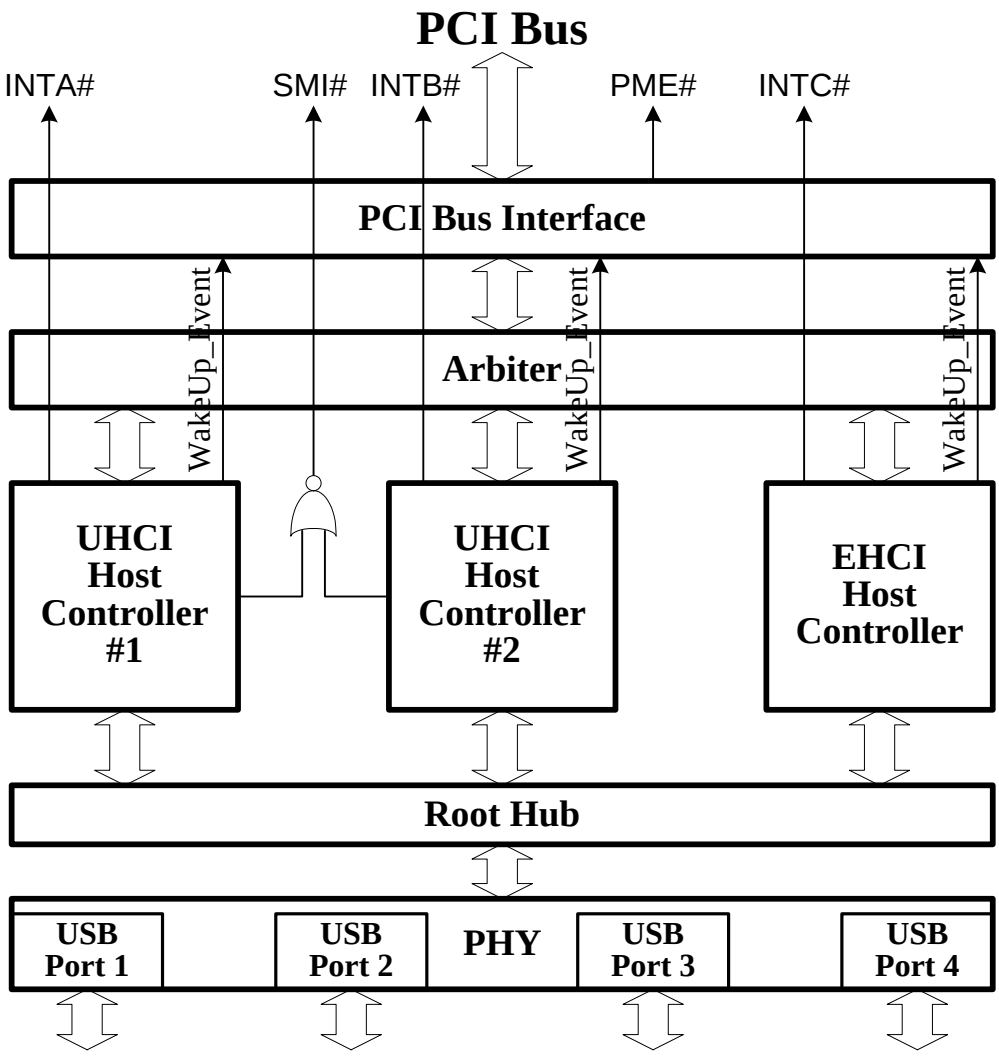


Figure 1. VT6212 / VT6212L Chip Block Diagram

PINOUTS

Pin Diagram

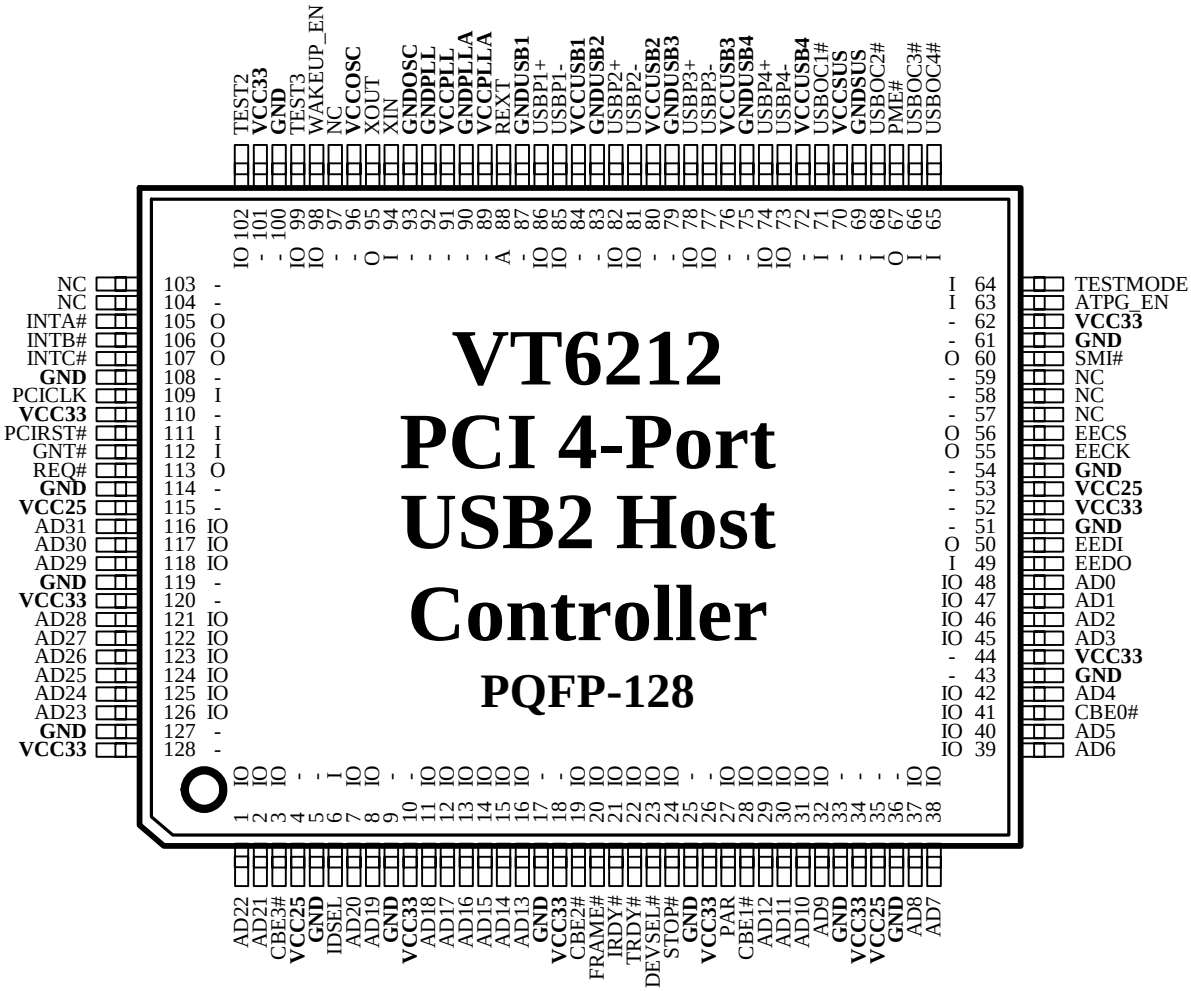


Figure 2. VT6212 (PQFP) / VT6212L (LQFP) Pin Diagram (Top View)

Pin List

Table 1. VT6212 / VT6212L Pin List (Alphabetical Order)

Pin	Typ	PU	Pin Name	Pin	Typ	PU	Pin Name	Pin	Typ	PU	Pin Name	Pin	Typ	PU	Pin Name
48	IO		AD0	63	I	PD	ATPG_EN	**93**	**P**		**GNDOSC**	86	IO		USBP1+
47	IO		AD1	41	IO		CBE0#	**92**	**P**		**GNDPLL**	81	IO		USBP2–
46	IO		AD2	28	IO		CBE1#	**90**	**P**		**GNDPLLA**	82	IO		USBP2+
45	IO		AD3	19	IO		CBE2#	**69**	**P**		**GNDSUS**	77	IO		USBP3–
42	IO		AD4	3	IO		CBE3#	**87**	**P**		**GNDUSB1**	78	IO		USBP3+
40	IO		AD5	23	IO		DEVSEL#	**83**	**P**		**GNDUSB2**	73	IO		USBP4–
39	IO		AD6	55	O	PD	EECK	**79**	**P**		**GNDUSB3**	74	IO		USBP4+
38	IO		AD7	56	O		EECS	**75**	**P**		**GNDUSB4**	**4**	**P**		**VCC25**
37	IO		AD8	50	O		EEDI	112	I		GNT#	**35**	**P**		**VCC25**
32	IO		AD9	49	I	PU	EEDO	6	I		IDSEL	**53**	**P**		**VCC25**
31	IO		AD10	104	-		NC	105	O		INTA#	**115**	**P**		**VCC25**
30	IO		AD11	103	-		NC	106	O		INTB#	**10**	**P**		**VCC33**
29	IO		AD12	58	-		NC	107	O		INTC#	**18**	**P**		**VCC33**
16	IO		AD13	97	-		NC	21	IO		IRDY#	**26**	**P**		**VCC33**
15	IO		AD14	57	-		NC	27	IO		PAR	**34**	**P**		**VCC33**
14	IO		AD15	59	-		NC	109	P		PCICLK	**44**	**P**		**VCC33**
13	IO		AD16	20	IO		FRAME#	111	I		PCIRST#	**52**	**P**		**VCC33**
12	IO		AD17	**5**	**P**		**GND**	67	O		PME#	**62**	**P**		**VCC33**
11	IO		AD18	**9**	**P**		**GND**	113	O		REQ#	**101**	**P**		**VCC33**
8	IO		AD19	**17**	**P**		**GND**	88	A		REXT	**110**	**P**		**VCC33**
7	IO		AD20	**25**	**P**		**GND**	60	O		SMI#	**120**	**P**		**VCC33**
2	IO		AD21	**33**	**P**		**GND**	24	IO		STOP#	**128**	**P**		**VCC33**
1	IO		AD22	**36**	**P**		**GND**	102	IO		TEST2	**96**	**P**		**VCCOSC**
126	IO		AD23	**43**	**P**		**GND**	99	IO		TEST3	**91**	**P**		**VCCPLL**
125	IO		AD24	**51**	**P**		**GND**	98	IO		WAKEUP_EN	**89**	**P**		**VCCPLLA**
124	IO		AD25	**54**	**P**		**GND**	64	I	PD	TESTMODE	**70**	**P**		**VCCSUS**
123	IO		AD26	**61**	**P**		**GND**	22	IO		TRDY#	**84**	**P**		**VCCUSB1**
122	IO		AD27	**100**	**P**		**GND**	71	I	PU	USBOC1#	**80**	**P**		**VCCUSB2**
121	IO		AD28	**108**	**P**		**GND**	68	I	PU	USBOC2#	**76**	**P**		**VCCUSB3**
118	IO		AD29	**114**	**P**		**GND**	66	I	PU	USBOC3#	**72**	**P**		**VCCUSB4**
117	IO		AD30	**119**	**P**		**GND**	65	I	PU	USBOC4#	94	I		XIN
116	IO		AD31	**127**	**P**		**GND**	85	IO		USBP1–	95	O		XOUT

Pin Descriptions

Table 2. VT6212 / VT6212L Pin Descriptions

PCI Interface				
Signal Name	**Pin #**	**I/O**	**Power**	**Signal Description**
AD[31:0]	(see pin list)	IO	**VCC33**	**Address and Data.** Addresses are passed during the first clock cycle. Data is passed in subsequent cycles.
CBE[3 :0]#	3, 19, 28, 41	IO	**VCC33**	**Command / Byte Enables.** The command for the current cycle is driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are then driven on following clocks.
PAR	27	IO	**VCC33**	**Parity.** A single parity bit is provided over AD[31:0] and CBE[3:0]# to check that the data has been transferred accurately..
IDSEL	6	I	**VCC33**	**Initialization Device Select.** Used as a chip select during configuration read and write cycles.
DEVSEL#	23	IO	**VCC33**	**Device Select.** As an output, this signal is asserted to claim PCI transactions through positive or subtractive decoding. As an input, DEVSEL# indicates the response to a VT6212-initiated transaction and is also sampled when decoding whether to subtractively decode the cycle.
FRAME#	20	IO	**VCC33**	**Cycle Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
STOP#	24	IO	**VCC33**	**PCI Stop.** Asserted by the target (the VT6212 / VT6212L chip) to request the master (PCI device) to stop the current transaction.
IRDY#	21	IO	**VCC33**	**Initiator Ready.** Asserted when the initiator is ready for data transfer.
TRDY#	22	IO	**VCC33**	**Target Ready.** Asserted when the target is ready for data transfer.
PCIRST#	111	I	**VCC33**	**PCI Reset.** When detected low, an internal hardware reset is performed. PCIRST# assertion or deassertion may be asynchronous to PCICLK, however, it is recommended that deassertion be synchronous to guarantee a clean and bounce free edge.
PCICLK	109	I	**VCC33**	**PCI Clock.** 33 MHz. Used to clock all PCI bus transactions.
INTA#	105	O	**VCC33**	**PCI Interrupt A.** Asynchronous signal used to request an interrupt.
INTB#	106	O	**VCC33**	**PCI Interrupt B.** Asynchronous signal used to request an interrupt.
INTC#	107	O	**VCC33**	**PCI Interrupt C.** Asynchronous signal used to request an interrupt.
REQ#	113	O	**VCC33**	**PCI Bus Request.** Asserted by the VT6212 / VT6212L to request bus use.
GNT#	112	I	**VCC33**	**PCI Bus Grant.** Asserted by the bus arbiter to grant permission to the VT6212 / VT6212L for access to the PCI bus for bus master operations.

Serial EEPROM Interface				
Signal Name	**Pin #**	**I/O**	**Power**	**Signal Description**
EECS	56	O	**VCC33**	**EEPROM Chip Select.** Connect to EEPROM EECS pin.
EECK	55	O	**VCC33**	**EEPROM Clock.** Connect to EEPROM EECK pin.
EEDI	50	O	**VCC33**	**EEPROM Data In.** Connect to EEPROM EEDI pin.
EEDO	49	I	**VCC33**	**EEPROM Data Output.** Connect to EEPROM EEDO pin.

Chipset South Bridge Interface				
Signal Name	**Pin #**	**I/O**	**Power**	**Signal Description**
SMI#	60	O	**VCC33**	**System Management Interrupt.**
PME#	67	O	**VCCSUS**	**Power Management Event Interrupt.**

No Connection				
Signal Name	**Pin #**	**I/O**	**Power**	**Signal Description**
NC	57-59, 97, 103-104	-		**No connection.**

USB Ports				
Signal Name	**Pin #**	**I/O**	**Power**	**Signal Description**
USBP1+	86	IO	**VCCUSB1**	**USB Port 1 Differential Data Plus.** Asserted high (> 2.8V) †
USBP1–	85	IO	**VCCUSB1**	**USB Port 1 Differential Data Minus.** Asserted low (< 0.3V) †
USBP2+	82	IO	**VCCUSB2**	**USB Port 2 Differential Data Plus.** Asserted high (> 2.8V) †
USBP2–	81	IO	**VCCUSB2**	**USB Port 2 Differential Data Minus.** Asserted low (< 0.3V) †
USBP3+	78	IO	**VCCUSB3**	**USB Port 3 Differential Data Plus.** Asserted high (> 2.8V) †
USBP3–	77	IO	**VCCUSB3**	**USB Port 3 Differential Data Minus.** Asserted low (< 0.3V) †
USBP4+	74	IO	**VCCUSB4**	**USB Port 4 Differential Data Plus.** Asserted high (> 2.8V) †
USBP4–	73	IO	**VCCUSB4**	**USB Port 4 Differential Data Minus.** Asserted low (< 0.3V) †
USBOC1#	71	I	**VCCSUS**	**USB Over-Current Input Port 1.** When the supplied current exceeds 500 mA on a USB port, USBOC# should be asserted. If this input is asserted low, the host controller will disable USB port 1. The port will remain disabled as long as the condition persists. See Design Guide and evaluation board schematics for overcurrent detection scheme.
USBOC2#	68	I	**VCCSUS**	**USB Over-Current Input Port 2.** Same as above but for port 2.
USBOC3#	66	I	**VCCSUS**	**USB Over-Current Input Port 3.** Same as above but for port 2.
USBOC4#	65	I	**VCCSUS**	**USB Over-Current Input Port 4.** Same as above but for port 2.
XIN	94	I	**VCCOSC**	**Crystal Input.** May be connected to a 24 MHz parallel resonant fundamental mode crystal (see Design Guide for specific connection details).
XOUT	95	O	**VCCOSC**	**Crystal Output.** Must be connected to a 24 MHz parallel resonant fundamental mode crystal (see Design Guide for specific connection details).
REXT	88	A	**VCCPLL**	**External Resistor.** Typical 6.12kΩ 1% pull down to analog ground (see Design Guide for specific connection details).

† Data encoding is NRZI (Non Return to Zero Inverted) so at times the reverse may be true (i.e., the plus pin may be asserted low and the minus pin asserted high.)

Test Pins and Reserved Pins				
Signal Name	**Pin #**	**I/O**	**Power**	**Signal Description**
ATPG_EN	63	I	**VCC25**	**Automatic Test Program Generator Enable.** Do not connect for normal operation. Internal pulldown.
TESTMODE	64	I	**VCC25**	**Test Mode Enable.** Do not connect for normal operation. Internal pulldown.
TEST2	102	IO	**VCC25**	**Test Signal 2.** Leave unconnected for normal operation.
TEST3	99	IO	**VCC25**	**Test Signal 3.** Pull down 4.7K-ohm for normal operation.
WAKEUP_EN	98	IO	**VCC25**	**WAKEUP_EN.** Enable wakeup function

Power and Ground			
Signal Name	**Pin #**	**Power**	**Signal Description**
VCC33	10, 18, 26, 34, 44, 52, 62, 101, 110, 120, 128	**Digital I/O**	**Digital I/O Power.** 3.3V ±100mV
VCC25	4, 35, 53, 115	**Internal**	**Internal Logic Power.** 2.5V ±5%
GND	5, 9, 17, 25, 33, 36, 43, 51, 54, 61, 100, 108, 114, 119, 127	**Ground**	**Ground.** Connect to primary PCB ground plane.
VCCSUS	70	**Suspend**	**Suspend I/O Power.** Connect to system 3.3V ±5% suspend power for support of wakeup on USB incoming port activity.
GNDSUS	69	**Suspend**	**Suspend I/O Ground.** Connect to analog ground plane (connected to primary PCB ground plane through ferrite beads for isolation from digital switching noise). See Design Guide for details.
VCCUSB[4-1]	72, 76, 80, 84	**USB Ports**	**USB Port Power.** Connect to system 3.3V ±5% suspend power for support of wakeup on USB incoming port activity.
GNDUSB[4-1]	75, 79, 83, 87	**USB Ports**	**USB Port 1-4 Analog Ground**. Connect to analog ground plane (connected to primary PCB ground plane through ferrite beads for isolation from digital switching noise). See Design Guide for details.
VCCPLL	91	**PLL**	**PLL Digital Power.** Connect to quiet 2.5V ±5% power source.
GNDPLL	92	**PLL**	**PLL Digital Ground.** Connect to analog ground plane (connected to primary PCB ground plane through ferrite beads for isolation from digital switching noise). See Design Guide for details.
VCCPLLA	89	**PLL**	**PLL Analog Power.** Connect to quiet 2.5V ±5% power source.
GNDPLLA	90	**PLL**	**PLL Analog Ground.** Connect to analog ground plane (connected to primary PCB ground plane through ferrite beads for isolation from digital switching noise). See Design Guide for details.
VCCOSC	96	**OSC**	**Oscillator Power.** Connect to quiet 2.5V ±5% power source.
GNDOSC	93	**OSC**	**Oscillator Analog Ground.** Connect to analog ground plane (connected to primary PCB ground plane through ferrite beads for isolation from digital switching noise). See Design Guide for details.

ELECTRICAL SPECIFICATIONS

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Comment
T_{STG}	Storage temperature	-55	125	°C	
T_C	Case operating temperature	0	85	°C	
V_{CC}	Power supply voltages	-0.5	4.0	V	
V_I	Input voltage	-0.5	5.5	V	
V_O	Output voltage at any output	-0.5	V_{CC} + 0.5	V	
V_{ESD}	Electrostatic discharge		2	kV	Human Body Model

Note: Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

Table 4. DC Characteristics

T_C = 0-55°C, V_{CCPCI} = V_{CCSUS} = V_{CCUSBN} = 3.3V+/-5%, V_{CC25} = V_{CCOSC} = V_{CCPLL} = V_{CCPLLA} =2.5V+/-5%, GND = 0V

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input Low Voltage	-0.50	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage	-	0.45	V	I_{OL}=4.0mA
V_{OH}	Output High Voltage	2.4	-	V	I_{OH}=-1.0mA
I_{IL}	Input Leakage Current	-	+/-10	µA	$0<V_{IN}<V_{CC}$
I_{OZ}	Tristate Leakage Current	-	+/-20	µA	$0.45<V_{OUT}<V_{CC}$

Table 5. Power Specifications

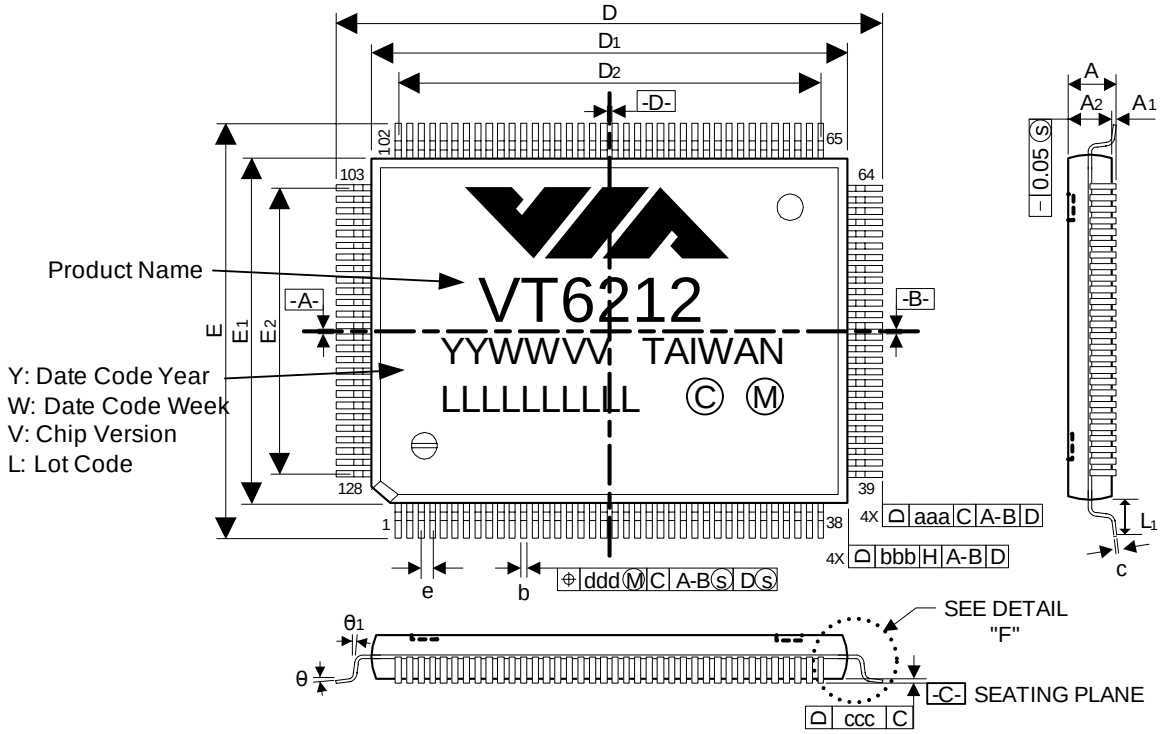
T_C = 0-55°C, V_{CC33} = V_{CCSUS} = V_{CCUSB} = 3.3V+/-5%, V_{CC25} = V_{CCOSC} = V_{CCPLL} = V_{CCPLLA} =2.5V+/-5%, GND = 0V

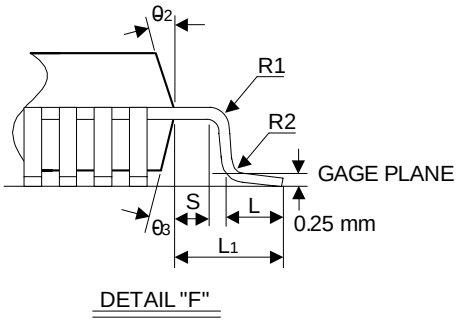
Symbol	Parameter	Typ	Max	Unit	Condition
$I_{CC25-PD}$	Power Supply Current – 2.5V	0	-	mA	Power down or suspend
$I_{CC33-PD}$	Power Supply Current – 3.3V	0	-	mA	Power down or suspend
I_{CC25}	Power Supply Current – VCC25 (2.5V)	14.5	-	mA	Idle with no port activity
I_{CC33}	Power Supply Current – VCC33 (3.3V)	0.05	-	mA	Idle with no port activity
I_{CC25A}	Power Supply Current – Analog (2.5V)†	61.5	-	mA	Idle with no port activity
I_{CC0USB}	Power Supply Current – USB (3.3V)‡	32.9	-	mA	Idle with no port activity
I_{CC1USB}	Power Supply Current – USB (3.3V)‡	71	-	mA	One port transmitting
I_{CC2USB}	Power Supply Current – USB (3.3V)‡	108.9	-	mA	Two ports transmitting
I_{CC3USB}	Power Supply Current – USB (3.3V)‡	159	-	mA	Three ports transmitting
I_{CC4USB}	Power Supply Current – USB (3.3V)‡	200	-	mA	Four ports transmitting
P_{D-PD}	Overall Chip Power Dissipation	3.35	-	mW	Power down or suspend
P_{D-IDLE}	Overall Chip Power Dissipation	298	-	mW	Idle with no port activity
P_{D-4USB}	Overall Chip Power Dissipation	943	-	mW	Four ports transmitting

†"Analog 2.5V" power includes VCCPLL, VCCPLLA, and VCCOSC

‡ "USB 3.3V" power includes VCCUSB and VCCSUS

PACKAGE MECHANICAL SPECIFICATIONS





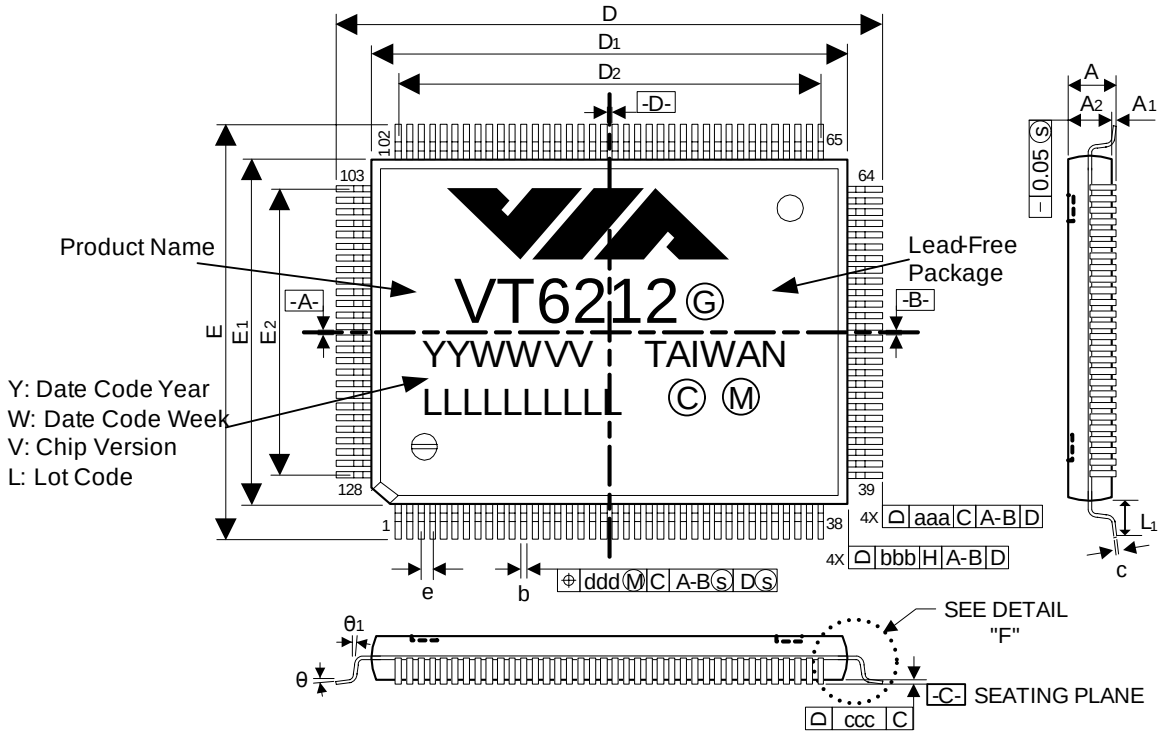
CONTROL DIMENSIONS ARE IN MILLIMETERS

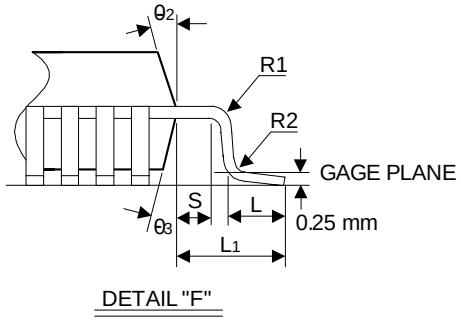
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	3.40	—	—	0.134
A1	0.25	—	—	0.010	—	—
A2	2.50	2.72	2.90	0.098	0.107	0.114
D	23.20 BASIC			0.913 BASIC		
E	17.20 BASIC			0.677 BASIC		
D1	20.00 BASIC			0.787 BASIC		
E1	14.00 BASIC			0.551 BASIC		
D2	18.50 BASIC			0.728 BASIC		
E2	12.50 BASIC			0.492 BASIC		
R1	0.13	—	0.30	0.005	—	0.012
R2	0.13	—	—	0.005	—	—
θ	0	—	7	0	—	7
θ1	0	—	—	0	—	—
θ2	15 REF			15 REF		
θ3	15 REF			15 REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

Figure 3. VT6212 Mechanical Specifications – 128 Pin PQFP Package





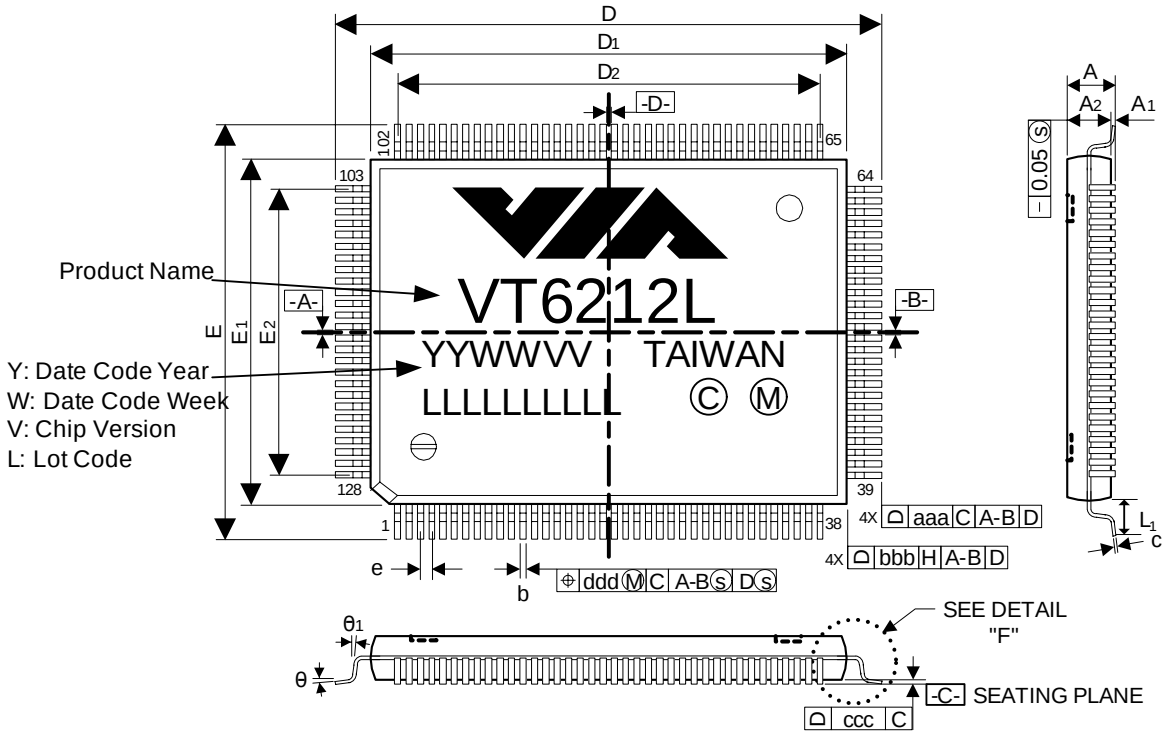
CONTROL DIMENSIONS ARE IN MILLIMETERS

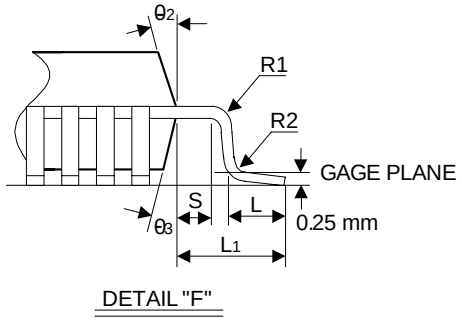
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	3.40	—	—	0.134
A1	0.25	—	—	0.010	—	—
A2	2.50	2.72	2.90	0.098	0.107	0.114
D	23.20 BASIC			0.913 BASIC		
E	17.20 BASIC			0.677 BASIC		
D1	20.00 BASIC			0.787 BASIC		
E1	14.00 BASIC			0.551 BASIC		
D2	18.50 BASIC			0.728 BASIC		
E2	12.50 BASIC			0.492 BASIC		
R1	0.13	—	0.30	0.005	—	0.012
R2	0.13	—	—	0.005	—	—
θ	0	—	7	0	—	7
θ1	0	—	—	0	—	—
θ2	15 REF			15 REF		
θ3	15 REF			15 REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

Figure 4. VT6212 Lead-free Mechanical Specifications – 128 Pin PQFP Package





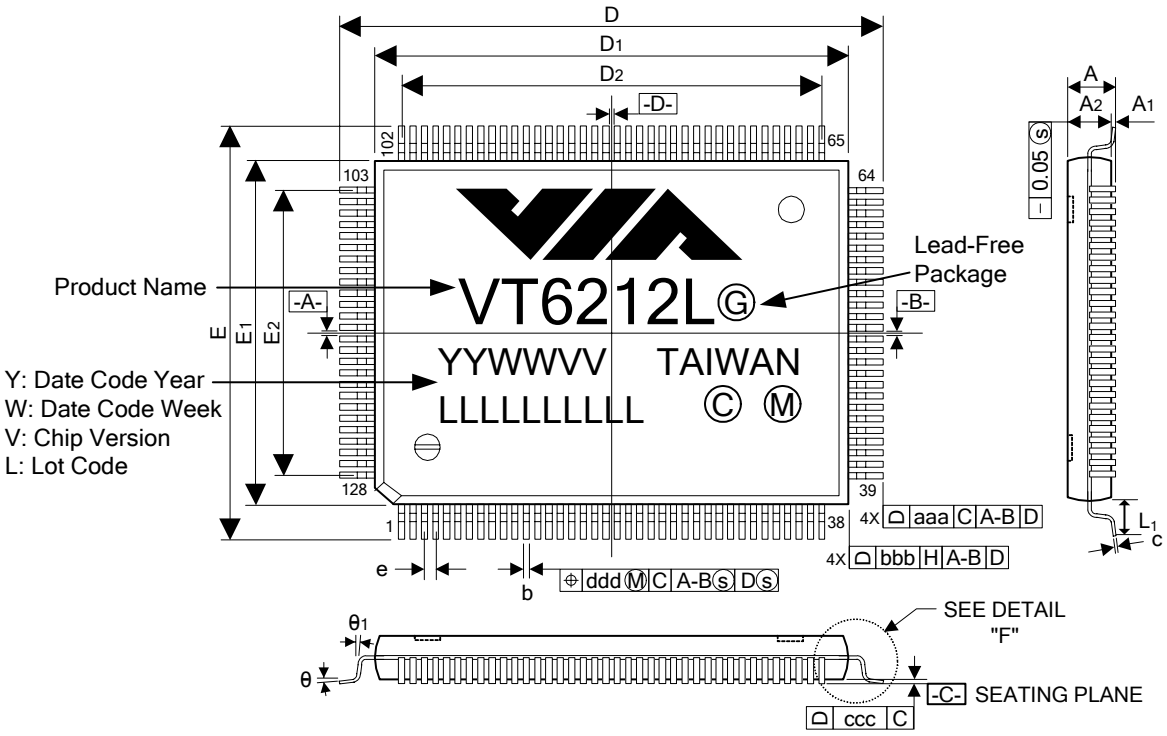
CONTROL DIMENSIONS ARE IN MILLIMETERS

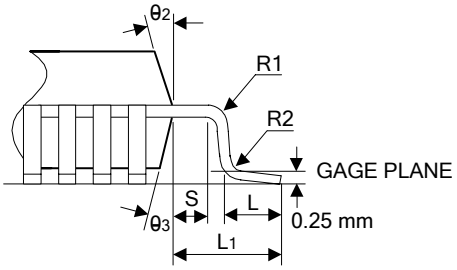
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	22.00 BASIC			0.866 BASIC		
E	16.00 BASIC			0.630 BASIC		
D1	20.00 BASIC			0.787 BASIC		
E1	14.00 BASIC			0.551 BASIC		
D2	18.50 BASIC			0.728 BASIC		
E2	12.50 BASIC			0.492 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0	3.5	7	0	3.5	7
θ1	0	—	—	0	—	—
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

Figure 5. VT6212L Mechanical Specifications – 128 Pin LQFP Package





DETAIL "F"

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	22.00 BASIC			0.866 BASIC		
E	16.00 BASIC			0.630 BASIC		
D1	20.00 BASIC			0.787 BASIC		
E1	14.00 BASIC			0.551 BASIC		
D2	18.50 BASIC			0.728 BASIC		
E2	12.50 BASIC			0.492 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0	3.5	7	0	3.5	7
θ1	0	—	—	0	—	—
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Figure 6. VT6212L Lead-free Mechanical Specifications – 128 Pin LQFP Package