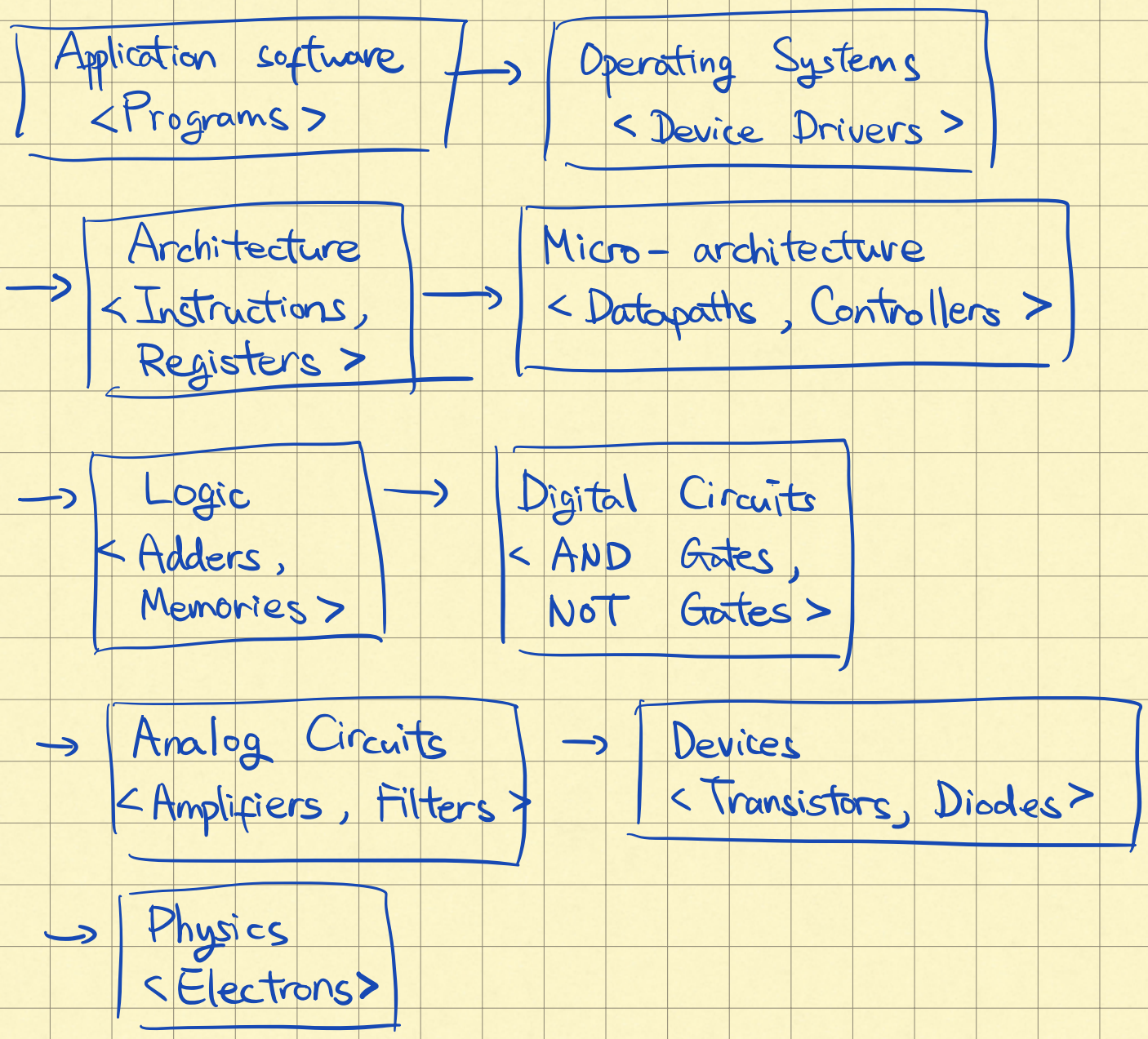
1.2.1 Abstraction.



1.2.2 Discipline

e.g. Interchangeable parts

restrict our designs intentionally.

1.2.3 The Three - Y's

- Hierarchy → dividing a system into modules.
- Modularity → well-defined modules.
- Regularity → uniformity among modules.

§1.3 THE DIGITAL ABSTRACTION

The amount of information D:

$$D = \log_2 N \text{ bits} \qquad (N \text{ distinct states}).$$

e.g. binary ($D = \log_2 2 = 1$ bits) conveys 1 bit of information.

1.4.4 Bytes, Nibbles, and All that Jazz.

8 bits = 1 byte. = 256 possibilities.
4 bits = 1 nibble = 16 possibilities.

One hexadecimal → 1 nibble
Two hexadecimal → 1 byte.

64-bit architecture processor

1 word = 64 bits.

$2^{10} \simeq$ 1 Kilo $= 10^3$

$2^{20} \simeq$ 1 million $= 10^6$

$2^{30} \simeq$ 1 billion $= 10^9$

§1.5 LOGIC GATES

§1.6. BENEATH THE DIGITAL ABSTRACTION

e.g.) 0V => 0 5V => 1.

What about 2.6V? 4.99 V?

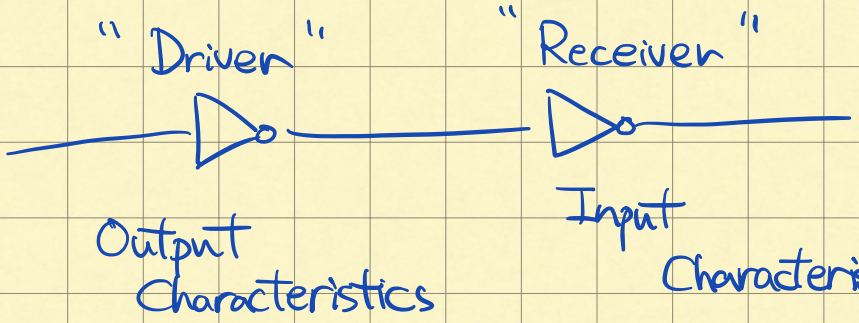
1.6.1 Supply Voltage.

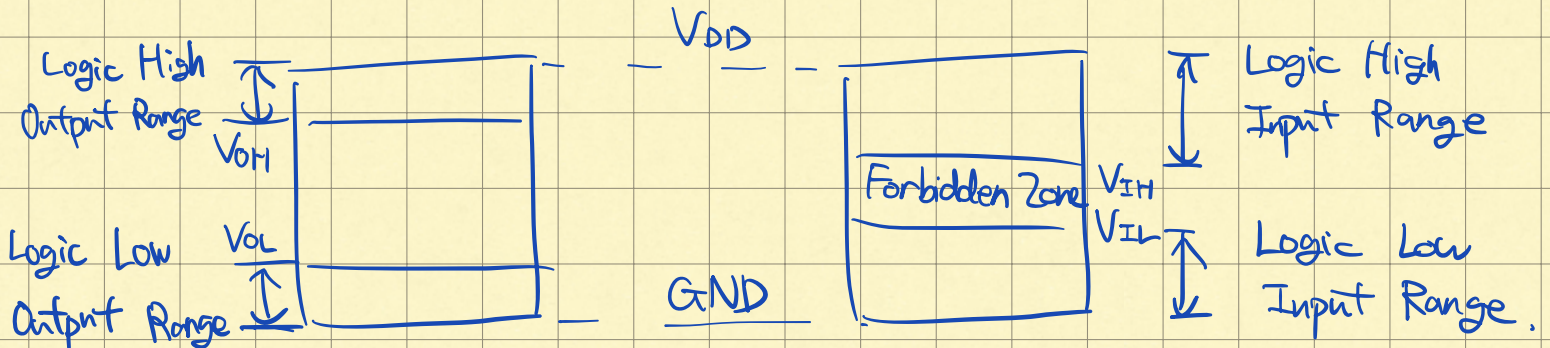
V_{DD} = 5V, 3.3V, 2.5V, ...

got lower.

1.6.2 Logic Levels.

The mapping of continuous to discrete value is defined by logic levels.





V_{OH}, V_{OL}, V_{IH}, and V_{IL} are called logic levels.

1.6.3 Noise Margins

In order to correctly intepret the output from driver,

$$V_{OL} < V_{IL}, \quad V_{IH} < V_{OH}$$

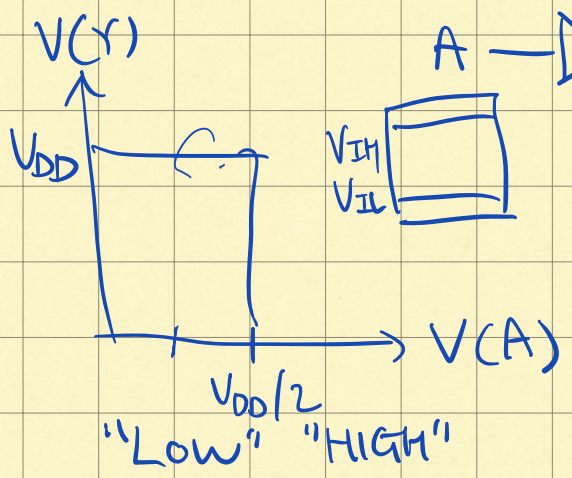
Thus, the difference of above values are called Noise Margins, :

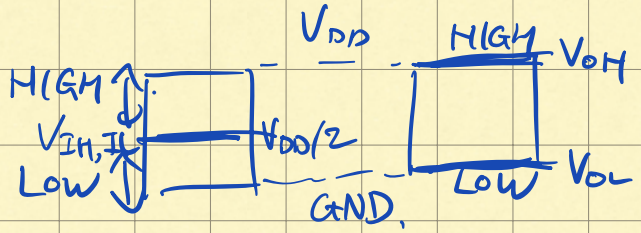
$$NM_L = V_{IL} - V_{OL}, \quad NM_H = V_{OH} - V_{IH}$$

1.6.4 DC Transfer Characteristics

Describes the relationship between input and output voltages.

IDEAL INVERTER





$V_{IH} = V_{IL} = V_{DD}/2$

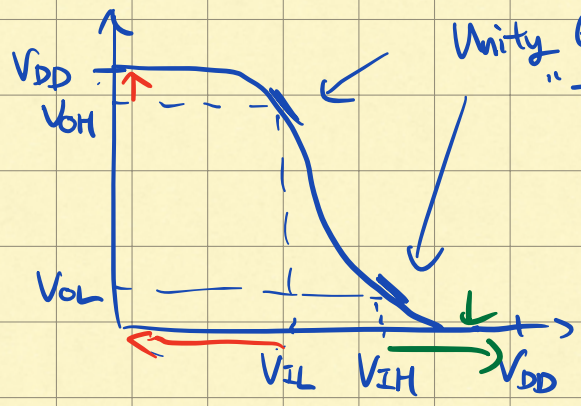
$V_{OH} = V_{DD}$ and $V_{OL} = 0$.

① When $V(A) < V_{DD}/2$, meaning LOW,
$V(Y) = V_{DD}$ (HIGH)

② When $V(A) > V_{DD}/2$, meaning HIGH,
$V(Y) = 0$ (LOW)

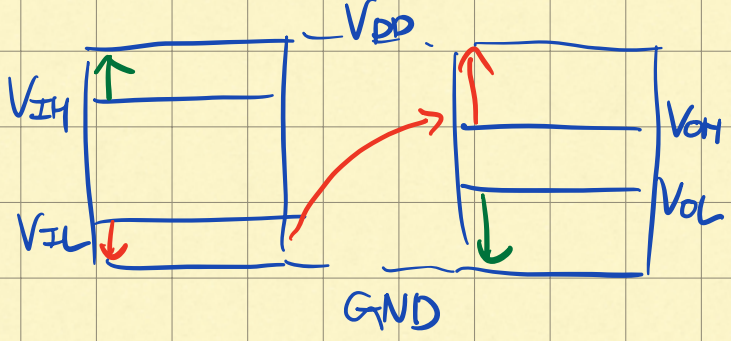
⇒ IDEAL INVERTER.

REAL INVERTER



Unity Gain Points. → This points usually maximizes the NM.
"-1"

If V_{IL} were reduced, V_{OH} would only increase by a small amount.



If V_{IL} were increased, V_{OH} would drop precipitously. (steeply)

1.6.5 The Static Discipline

To avoid inputs falling into the forbidden zone, digital logic gates are designed to conform to the static discipline.

Logic gates in same logic families obey the same static discipline.
(Meaning same supply voltages and logic levels.)

Logic family	V_{DD}	V_{IL}	V_{IH}	V_{OL}	V_{OH}
TTL	5 (5.25-4.75)	0.8	2.0	0.4	2.4
CMOS	5 (4.5 – 6)	1.35	3.15	0.33	3.84
LVTTL	3.3 (3 – 3.6)	0.8	2.0	0.4	2.4
LVCMOS	3.3 (3-3.6)	0.9	1.8	0.36	2.7

Compatibility of Logic Families

	Receiver			
Driver	TTL	CMOS	LVTTL	LVCMOS
TTL	OK	NO	MAYBE	MAYBE
CMOS	OK	OK	MAYBE	MAYBE
LVTTL	OK	NO	OK	OK
LVCMOS	OK	NO	OK	OK.