4. (20) Find the current listing (57 th) for the Top500 list for 2021. Review the system architecture for each of the top 10 systems on this list. Provide a summary of trends that you find and discuss what kind of system you would design in the future so that it could be included in this impressive list. Make sure to provide a diagram of the architecture you would develop, and include details of the CPUs, memory and interconnect used.

Top500 Top 10 Supercomputers Summary:

S.No	Name	Number of cores	Memory	Number of GPUs, Type	Processor	Interconnect
1	Fugaku	7,630,848	5,087,232 GB	0	A64FX 48C 2.2GHz	Tofu interconnect D
2	Summit	2,414,592	2,801,664 GB	27,648 Tesla V100	IBM POWER9 22C 3.07GHz	Dual-rail Mellanox EDR Infiniband
3	Sierra	1,572,480	1,382,400 GB	17,280 Tesla V100	IBM POWER9 22C 3.1GHz	Dual-rail Mellanox EDR Infiniband
4	Sunway	10,649,600	1,310,720 GB	0	Sunway SW26010 260C 1.45GHz	Sunway
5	Perlmutter	706,304	390,176 GB	6000 Nvidia A100	AMD EPYC 7763 64C 2.45GHz	Slingshot-10
6	Selene	555,520	1,120,000 GB	4,480 Nvidia A100	AMD EPYC 7742 64C 2.25GHz	Mellanox HDR Infiniband
7	Tianhe - 2A	4,981,760	2,277,376 GB	35,584 Matrix-2000	Intel Xeon E5-2692v2 12C	TH Express-2

					2.2GHz	
8	Juwels booster	449,280	628,992 GB	3,744 Nvidia A100	AMD EPYC 7402 24C 2.8GHz	Mellanox HDR InfiniBand
9	HPC5	669,760	349,440 GB	7,280 Tesla V100	Xeon Gold 6252 24C 2.1GHz	Mellanox HDR Infiniband
10	frontera	448,448	1,537,536 GB	0	Xeon Platinum 8280 28C 2.7GHz	Mellanox InfiniBand HDR

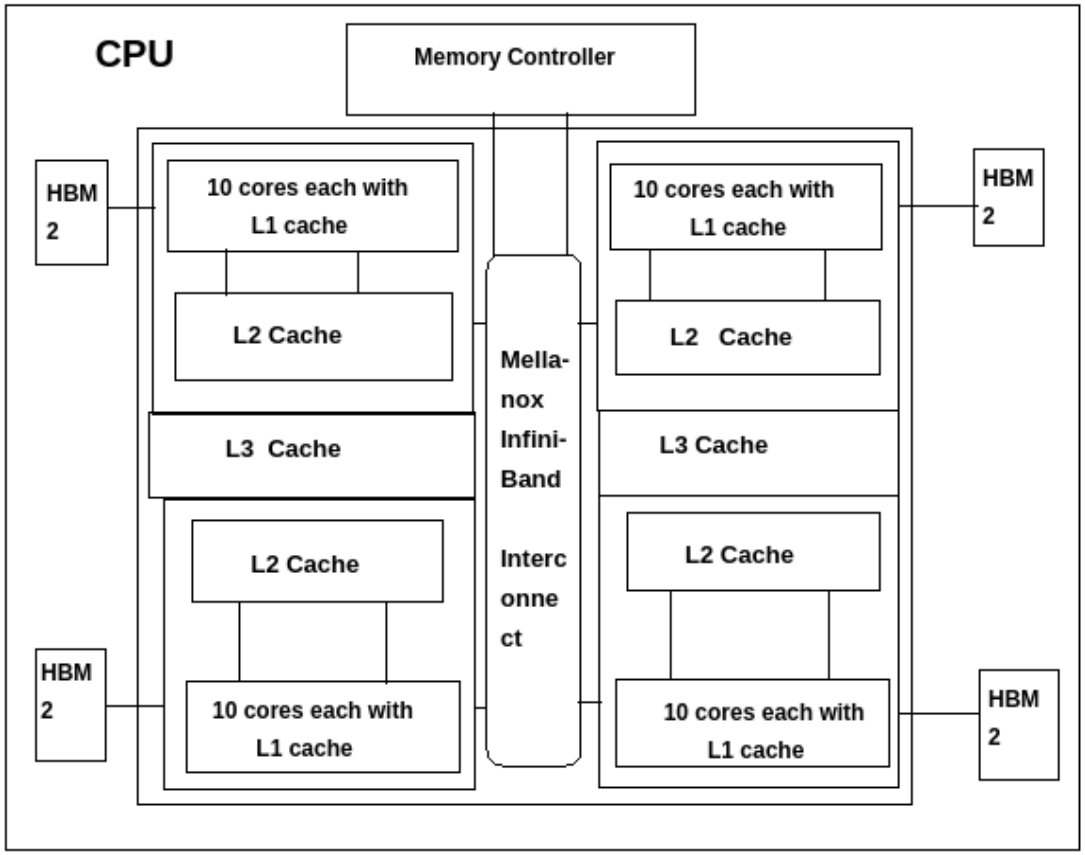
Here are the following trends I observed in the above list,

1. Fugaku supercomputer which tops the list, has A64FX CPU as the processor. Each cpu block has four core memory groups(CMGs). Each CMG has 13 cores. L1 caches are present inside each core. Two L2 caches are present in each CMG and are shared among these 13 cores. It does not have a L3 cache. Whereas in Summit, which is in second position, each power9 chip has 22 or 24 cores with L1 in each core, L2 shared between only two cores and L3 shared between 11 cores.
2. In the Fugaku supercomputer, ring buses are connected to each CMG and each CMG is always connected with each other also. Due to the CMG interconnect paths we can avoid the effect of the use of ring buses. Similarly in Summit, each chip is interconnected with Dual-rail Mellanox EDR Infiniband interconnect.
3. Summit supercomputer and Sierra are similar to each other with Sierra having fewer cores and memory less than Summit.
4. Sunway taihulight supercomputer's system architecture is quite different from others where each Computer Processing Element (CPE) Cluster is composed of a Management Processing Element (MPE) which is a 64-bit RISC core which supports both user and system modes, 264-bit vector instructions, 32 KB L1 instruction cache and 32 KB L1 data cache, and a 256KB L2 cache. The CPE is composed of an 8×8 mesh of 62-bit RISC cores, supporting only user mode, with 264-bit vector instructions, 16 KB L1 instruction cache and 64 KB Scratch Pad Memory (SPM).
5. As we go down the list from Fugaku supercomputer to Frontera supercomputer, the number of cores reduces and the memory also reduces with some variations at the end.
6. Many of the supercomputers in this list contain *Mellanox InfiniBand HDR* as the interconnect and variants of *AMD EPYC* as the processor.
7. Many of the supercomputers in this list have Nvidia GPUs connected to the processor via NVlinks.

My design:

Below is the diagram of system architecture I designed.

- There are 4 groups with each having 10 cores.
- L1 cache is inside each core.
    - L1 data cache size = 32 KB
    - L1 instruction cache size = 32 KB
- L2 cache is shared among all the 10 cores in a group. L2 cache size = 512KB (8-way associative)
- L3 cache is shared between two adjacent groups. L3 cache size = 10 MB (20-way associative)



- Interconnect used: Mellanox InfiniBand
- Number of cores per CPU = 22.
- Total number of CPUs = 16384
- Total number of cores = 360, 448
- High Bandwidth Memory allows upto 8GB per package. So 32(4*8) GB per CPU.
- Total Memory = 16384 (number of CPUs) * 32(Memory per CPU) = 524, 288 GB.