**ELEC 204 Digital Design Lab Report**

Lab 1

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1. **Introduction and objectives**

There were many objectives for the first lab. One of the objectives of the lab was to help with getting familiar with the Xilinx ISE software package by creating a project using the Xilinx ISE Project Navigator, implementing VHDL codes, and simulating the codes’ behavior. Although we haven’t received an FPGA board yet, another objective of the lab was to becoming familiar with the Prometheus FPGA board by loading and testing the design on the board. The last objective of the lab was to implement an exclusive XOR gate in VHDL and test our design in a computer simulation.

My code was implemented for the last objective of the lab which was designing an exclusive XOR gate in VHDL. I used a lab instruction sheet for the implementation of my design and how to set up a test by using computer simulation.

1. **Methods**

I had two inputs and these inputs were X and Y. They were both 1-bit inputs.

I had one output and it was called Z. It was a 1-bit output.

The VHDL code was the implementation of the given XOR gate schematic in the lab manual. The VHDL code had to take two inputs as X and Y and give Z as output by following the XOR gate structure.

My code takes X and Y as inputs and goes through AND gates as **not X and Y** and **not Y and X**. Following AND gates I defined two intermediate signals as **NXY** and **NYX**. Finally, these intermediate signals go through an OR gate as **NXY or NYX** for the desired output Z.

Later on, I tested my code by performing a computer simulation using the Xilinx ISE simulator. I implemented a simulation code. Since I had two inputs, the test bench had four possible combinations and these were {00, 01, 10, 11}. After these inputs, I returned to the initial value to see my test cases.

Finally, I went through my simulation and checked if my design was correct. For my inputs I got the following shown as a truth table:

|  |  |  |
| --- | --- | --- |
| **X** | **Y** | **Z** |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Since the exclusive XOR gate gives 0 when the inputs are alike and 1 otherwise, my output gave the correct results and showed that my VHDL code was working.

1. **Problems encountered, errors and warnings resolved**

Following the instructions in the lab manual, I encountered no synthesis errors or warnings when implementing my code.

1. **Conclusion**

Overall, I implemented a VHDL code for the exclusive XOR gate. Then I tested my design using the Xilinx ISE Simulation tool and observed that my design was giving the correct output.

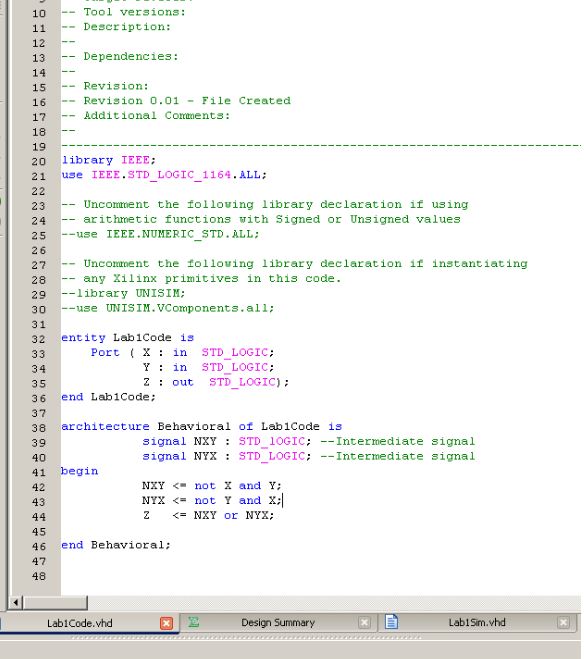
In this lab, I’ve learned how to use the Xilinx ISE software by writing VHDL codes and test my code by running a simulation. Moreover, I have learned what is an XOR gate and how it is implemented.

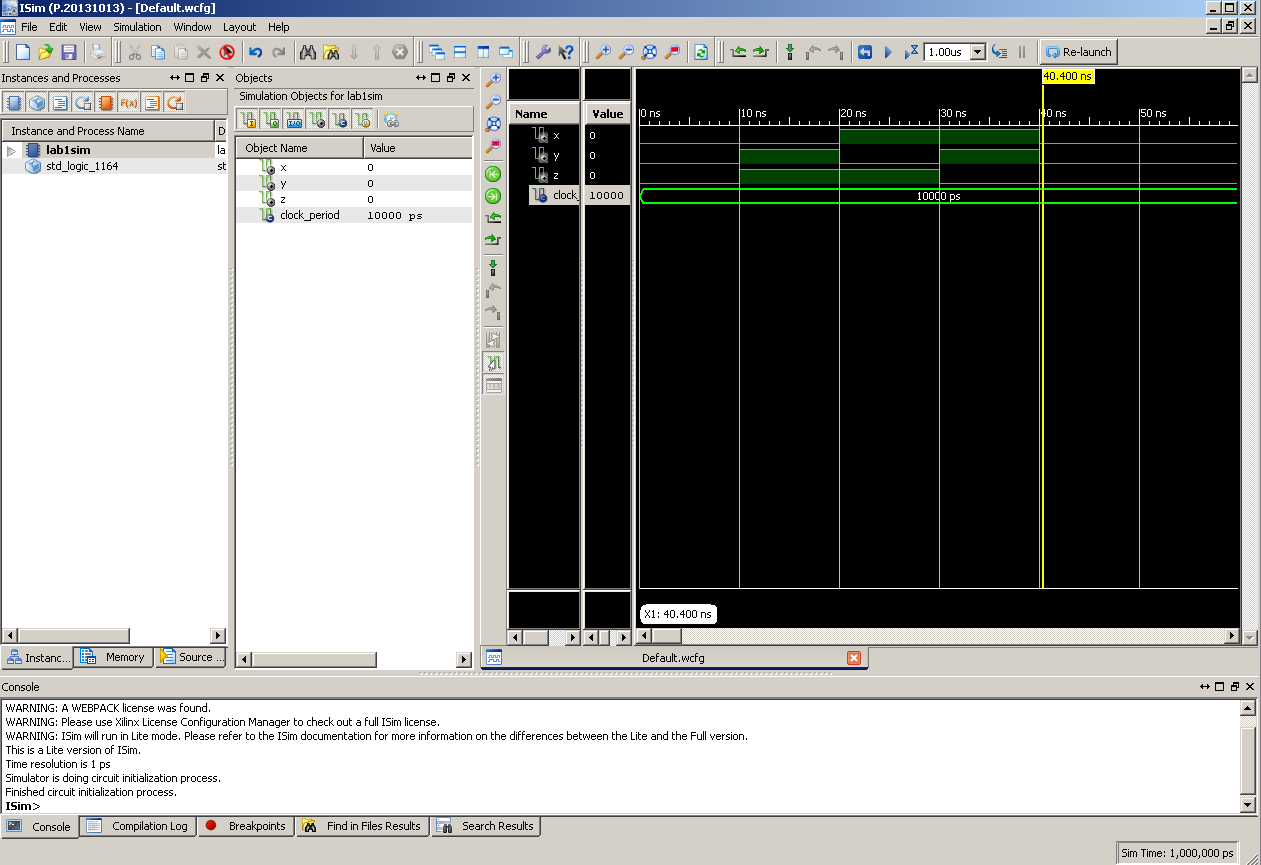
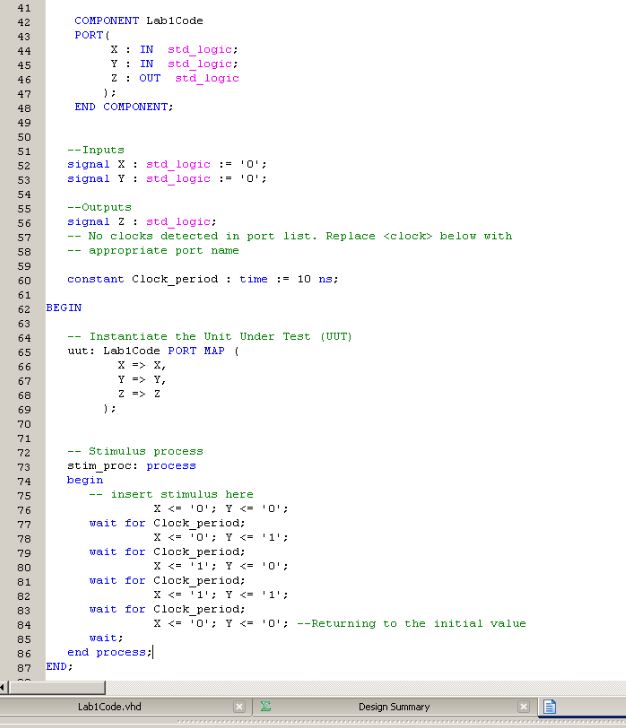
Lastly, although I couldn’t perform my design on a Prometheus Spartan 3A board, I’ve also learned how to do that by going through the lab manual.

References

1. ELEC 204 Digital System Design Laboratory Manual, Experiment #1 Introductory Tutorial For Xilinx ISE v14.7 & Implementing XOR Gate PDF.

**Appendix 1. Lab source code**

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**Appendix 2. RTL schematics**

**Appendix 3. FPGA Board photos showing working code**

**Appendix 4. Screenshots from Xilinx for the errors and other board issues**