Embedded Systems

CycloneV & DE1-SoC

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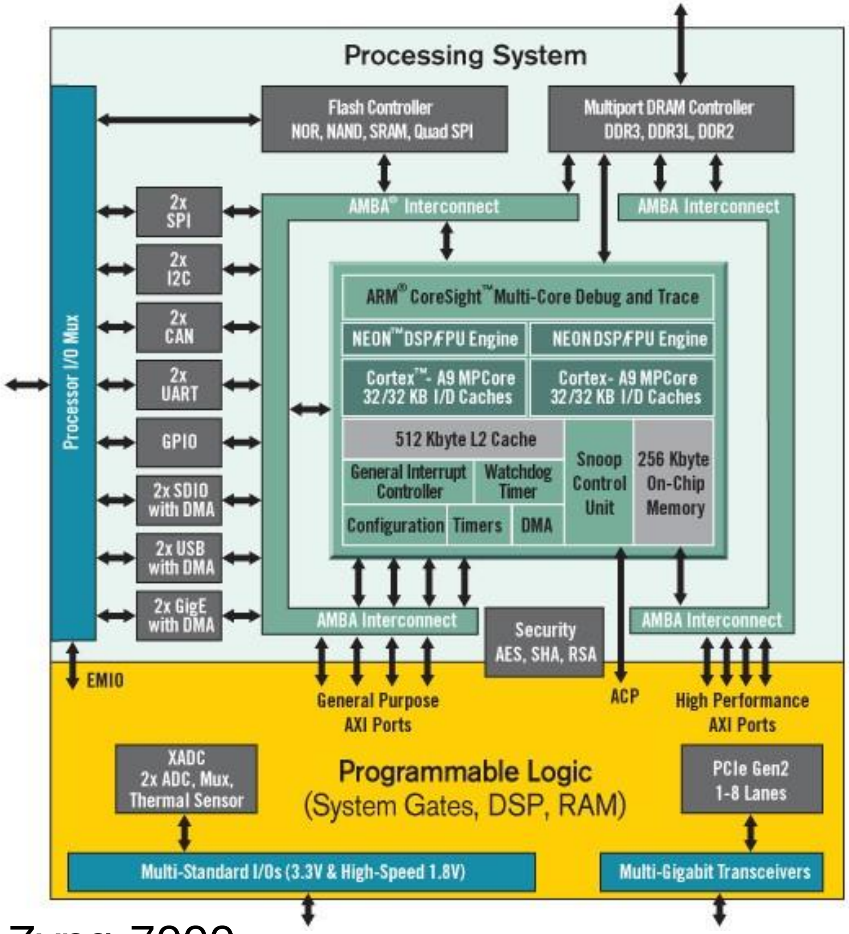
FPGA WITH SOC ARCHITECTURE

2 main actors

- IntelFPGA (Altera (www.altera.com))
  - ➢Cyclone V SOC, Cyclone 10
  - ➢Arria V SOC, Arria 10
  - ➢Stratix 10
- Xilinx (www.xilinx.com)::
  - ➢ Zynq® 7000 family
  - ➢Zynq UltraScale+ MPSoC

2 main actors, Common Features

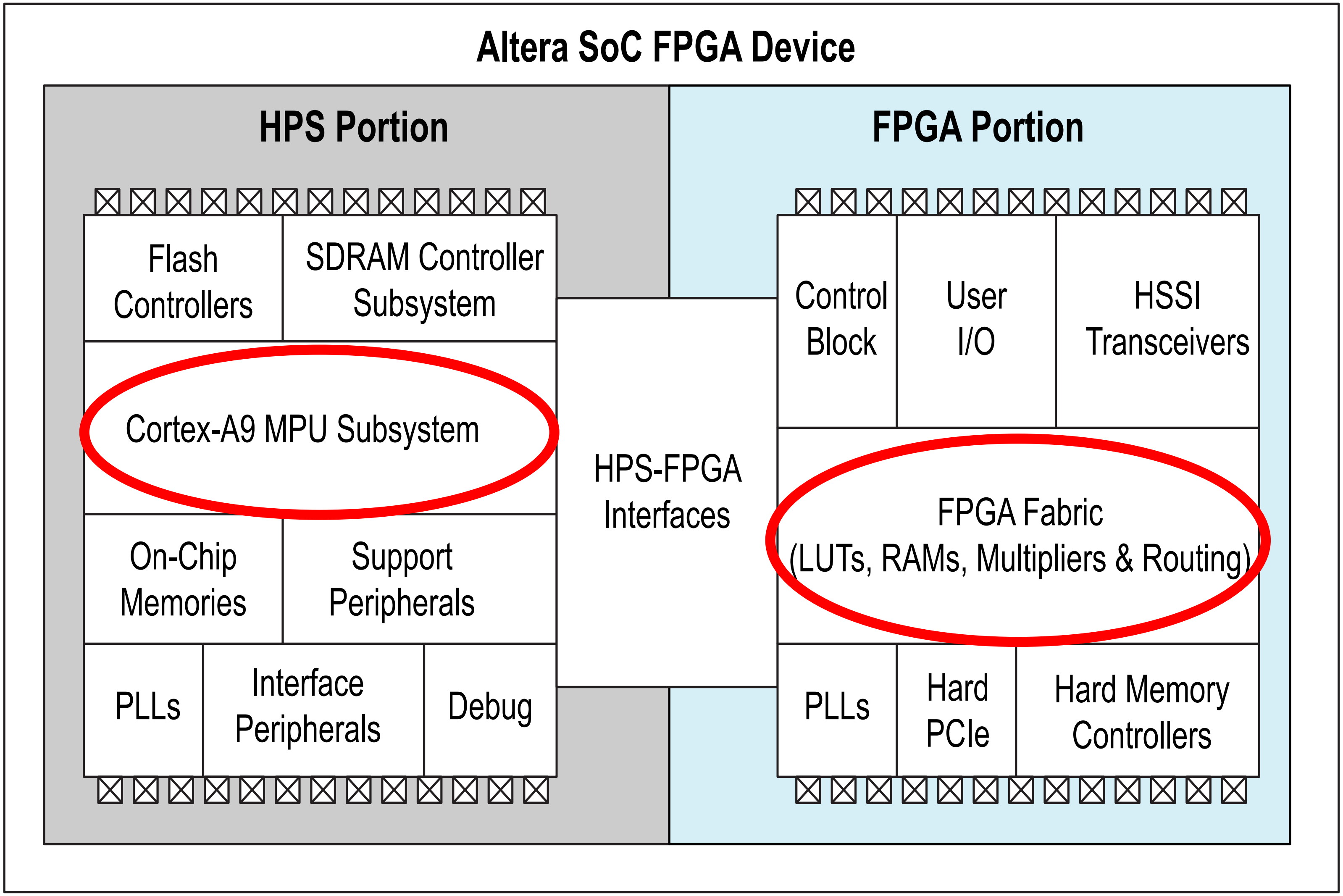
- 2x ARM-Cortex A9 hardcore
  - ➢ 2x NEON DSP/FPU
  - ➢ Many programmable interface in hardcore
  - ➢ Amba interconnect
  - ➢ Large FPGA part
  - ➢ DDR Controller



Ex: Zynq-7000

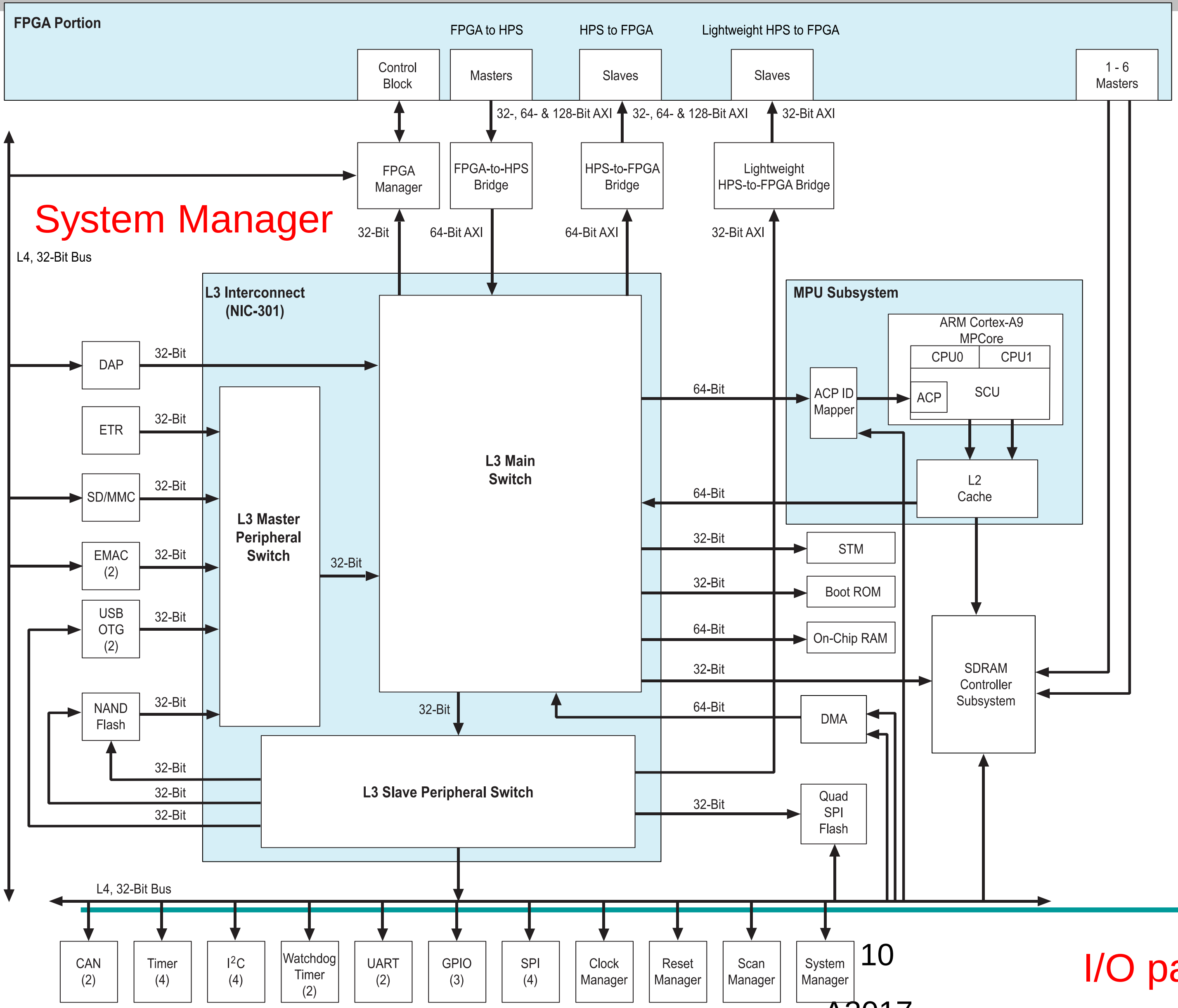
CYCLONE V-SOC ARCHITECTURE (INTELFPGA)

Cyclone V SoC Overview



http://www.altera.com/literature/hb/cyclone-v/cv_5v4.pdf

Cyclone V HPS (Hard Processor System)

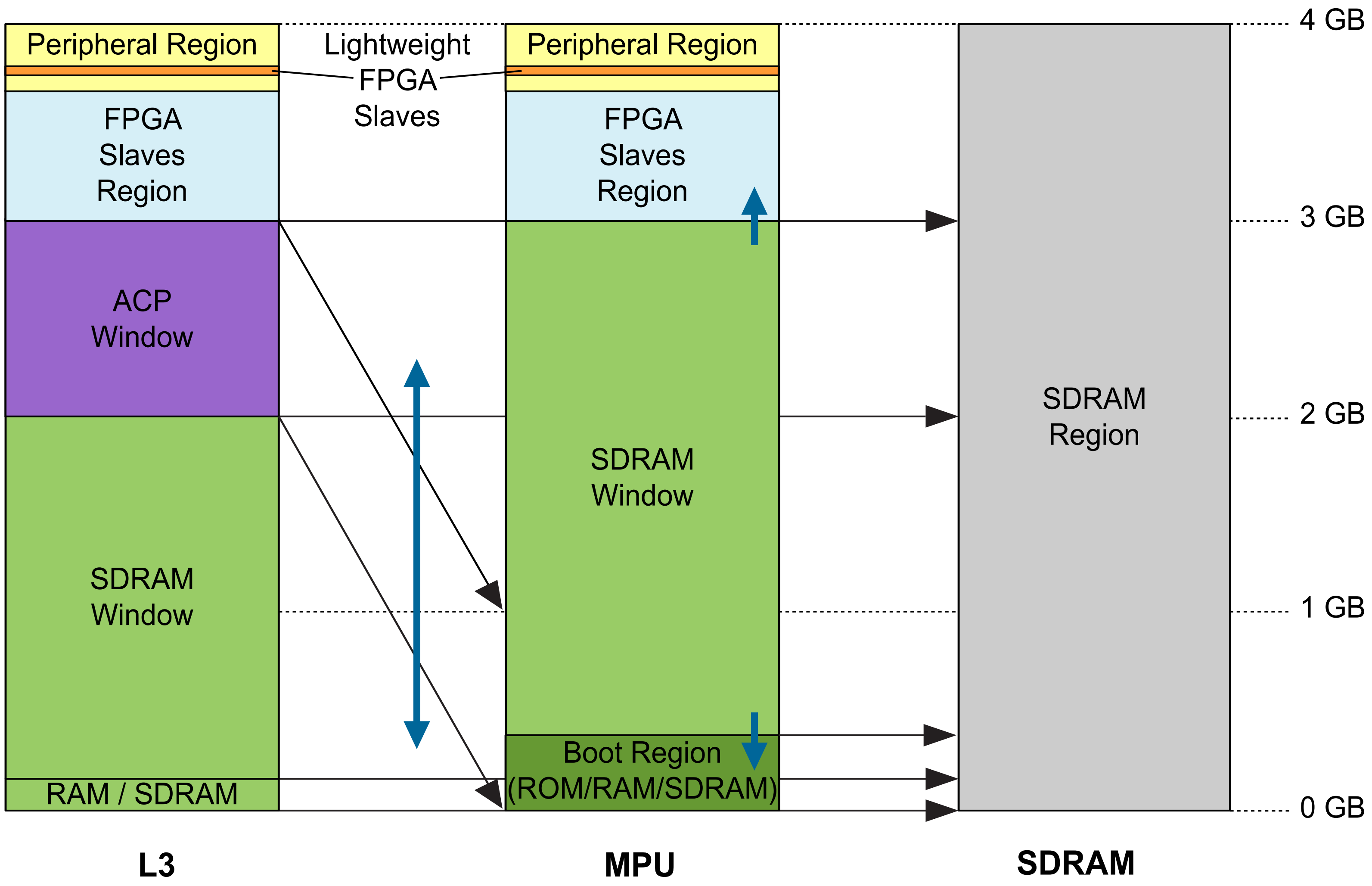


System Manager

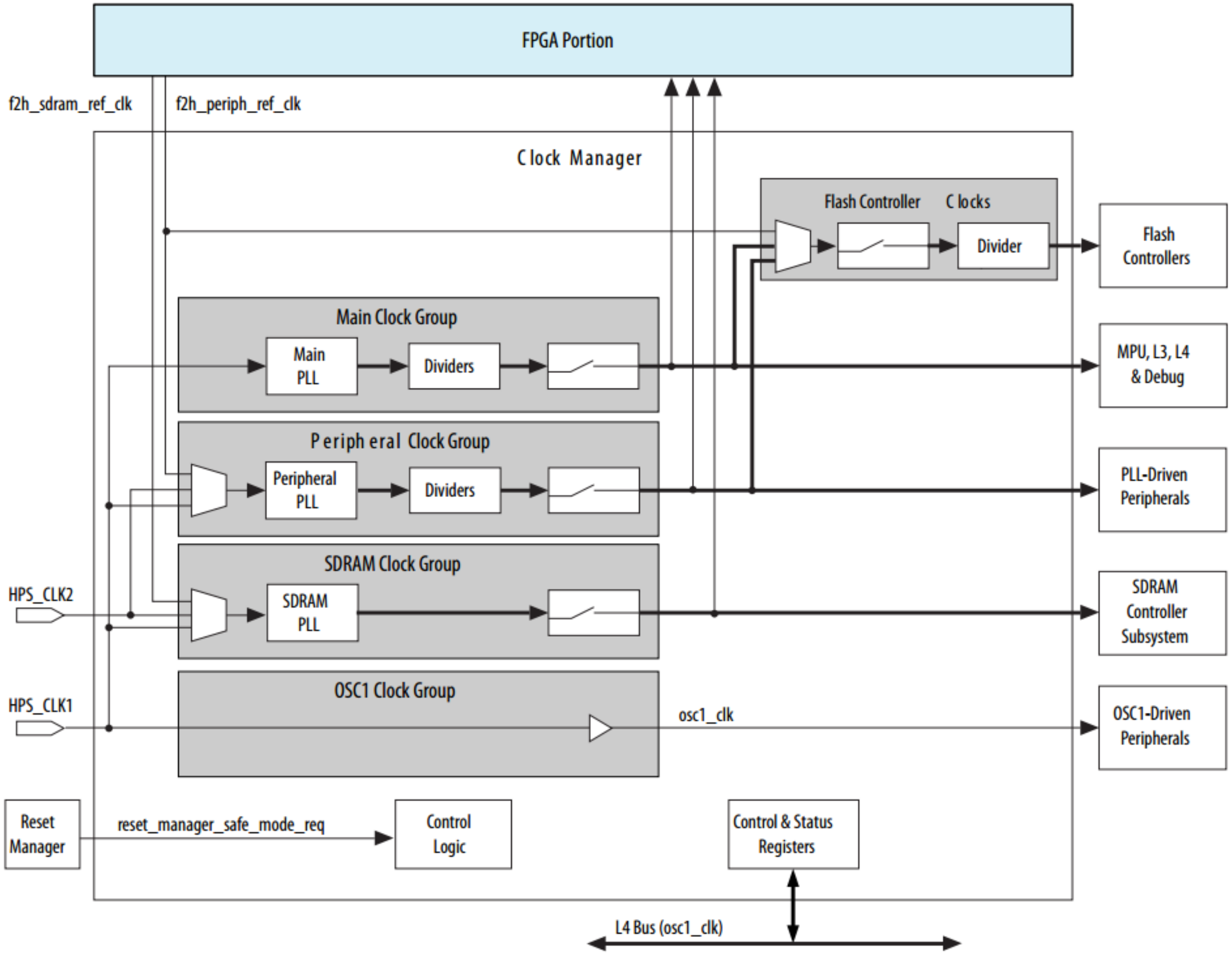
FPGA part

I/O part

HPS-FPGA Address Space



Clock manager



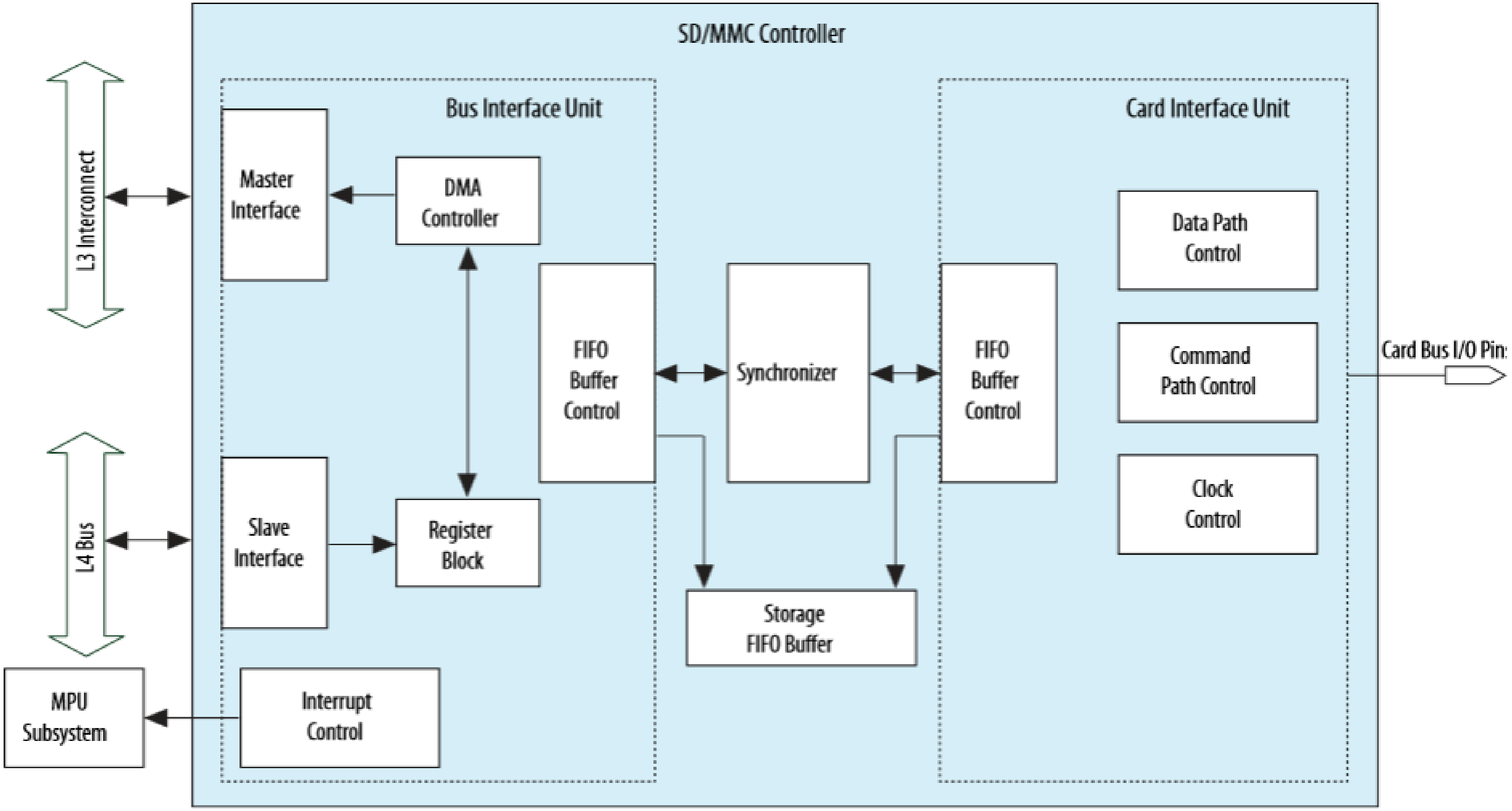
Abbreviation

STM	System Trace Module
DMA	Direct Memory Access
DAP	Debug Access Port
ETR	Embedded Trace Router
SD/	Supporte: SDSC(SD), SDHC, SDXC, eSD, SDIO, eSDIO
MMC	MMC, RSMMC, MMCPlus, MMCMobile, eMMC
EMAC	Ethernet Media Access Controller

Abbreviation

ACP	Accelerator Coherency Port
USB	Universal Serial Bus
UART	Universal Asynchronous Receiver-Transmitter
SPI	Synchronous Peripheral Interface
CAN	Controller Area Network
I2C	Inter-Integrated Circuit

Ex. Programmable Interface SD/MMC Unit

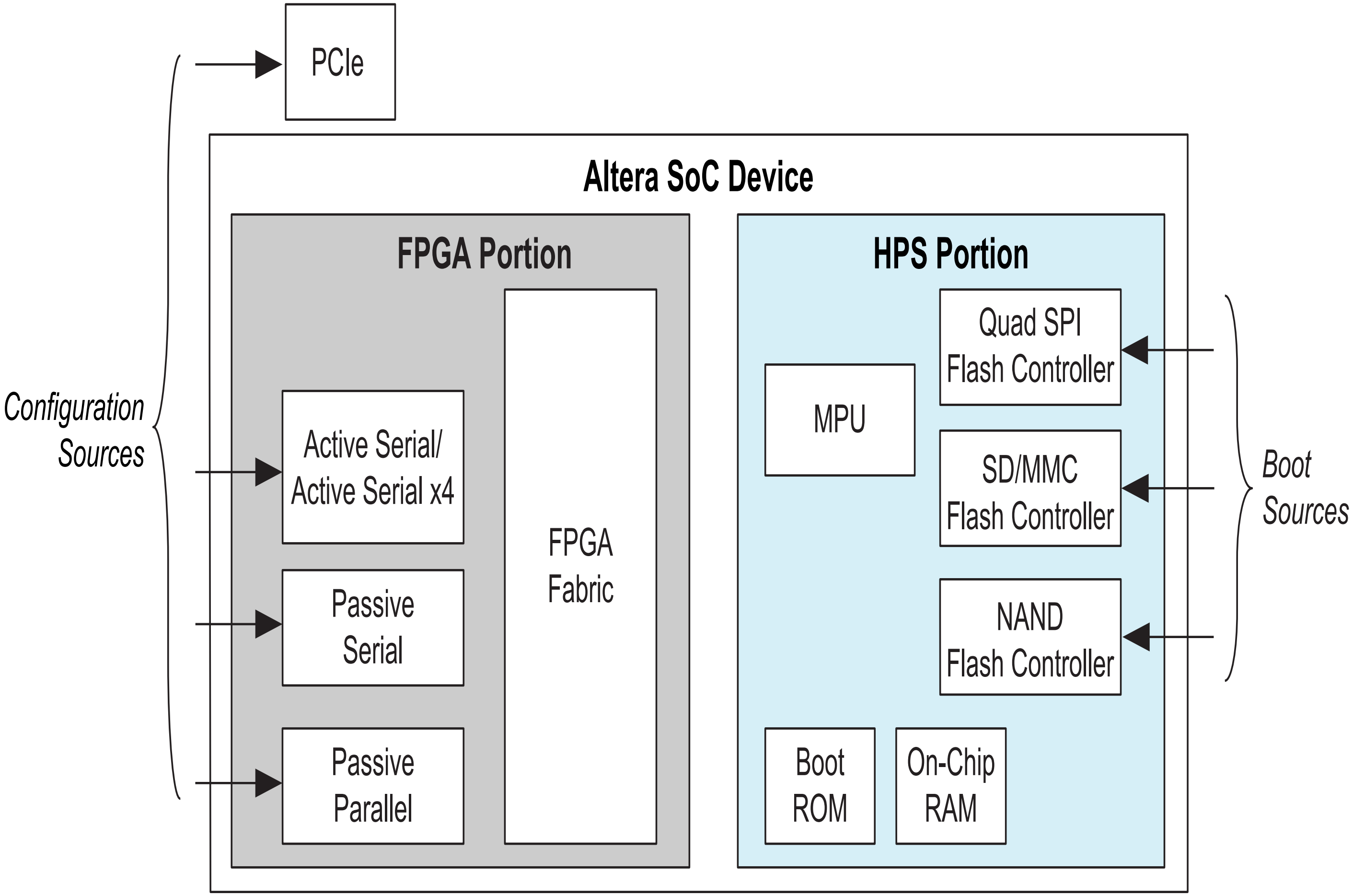


Boot process

- It is possible to use the Cyclone V SoC in 3 different configurations:
  - FPGA-only
  - HPS-only
  - HPS & FPGA
- The configurations using the HPS are more difficult to set up than the *FPGA-only* one.

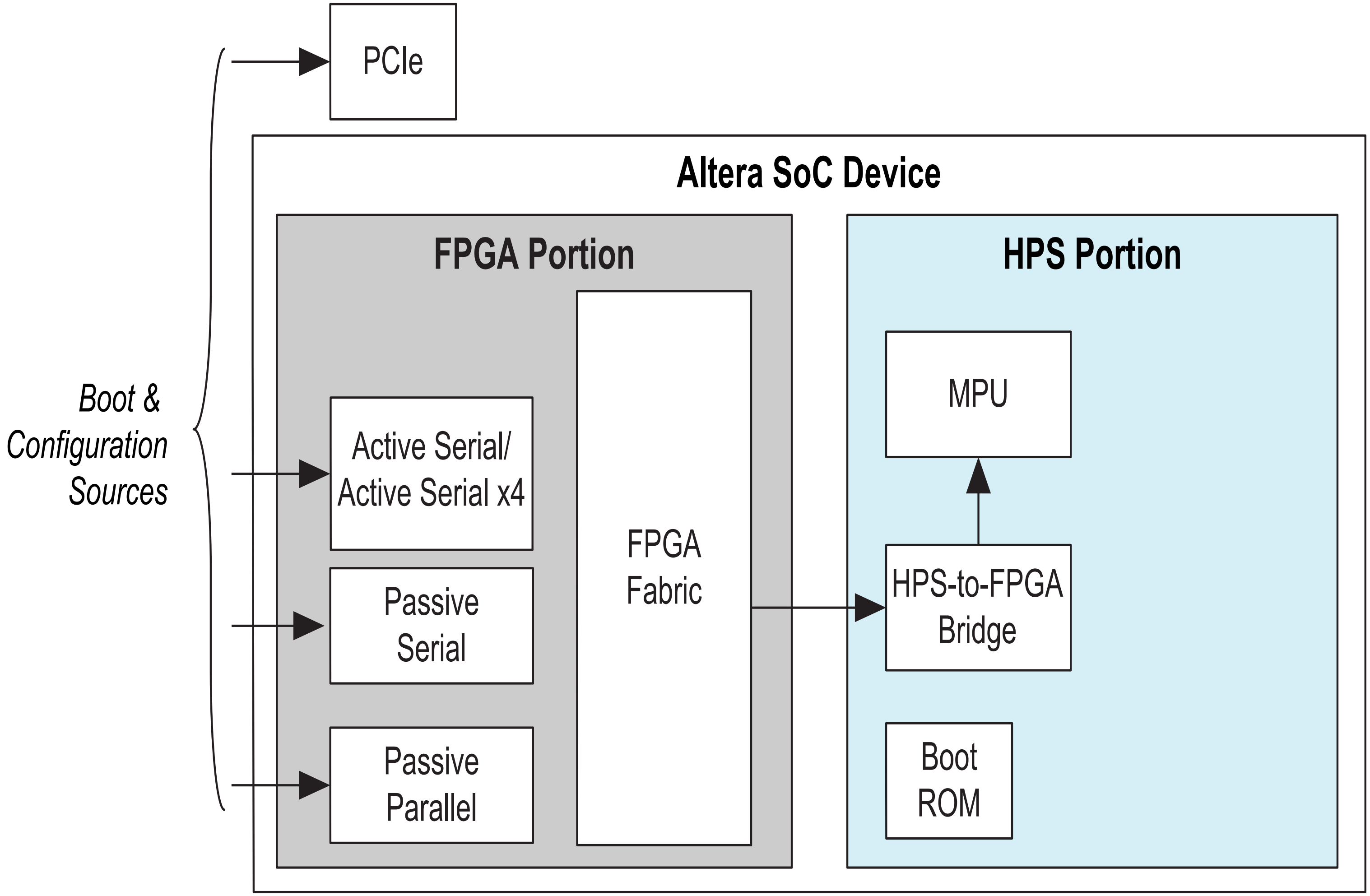
HPS/FPGA Boot (1)

Independent FPGA Configuration and HPS Booting



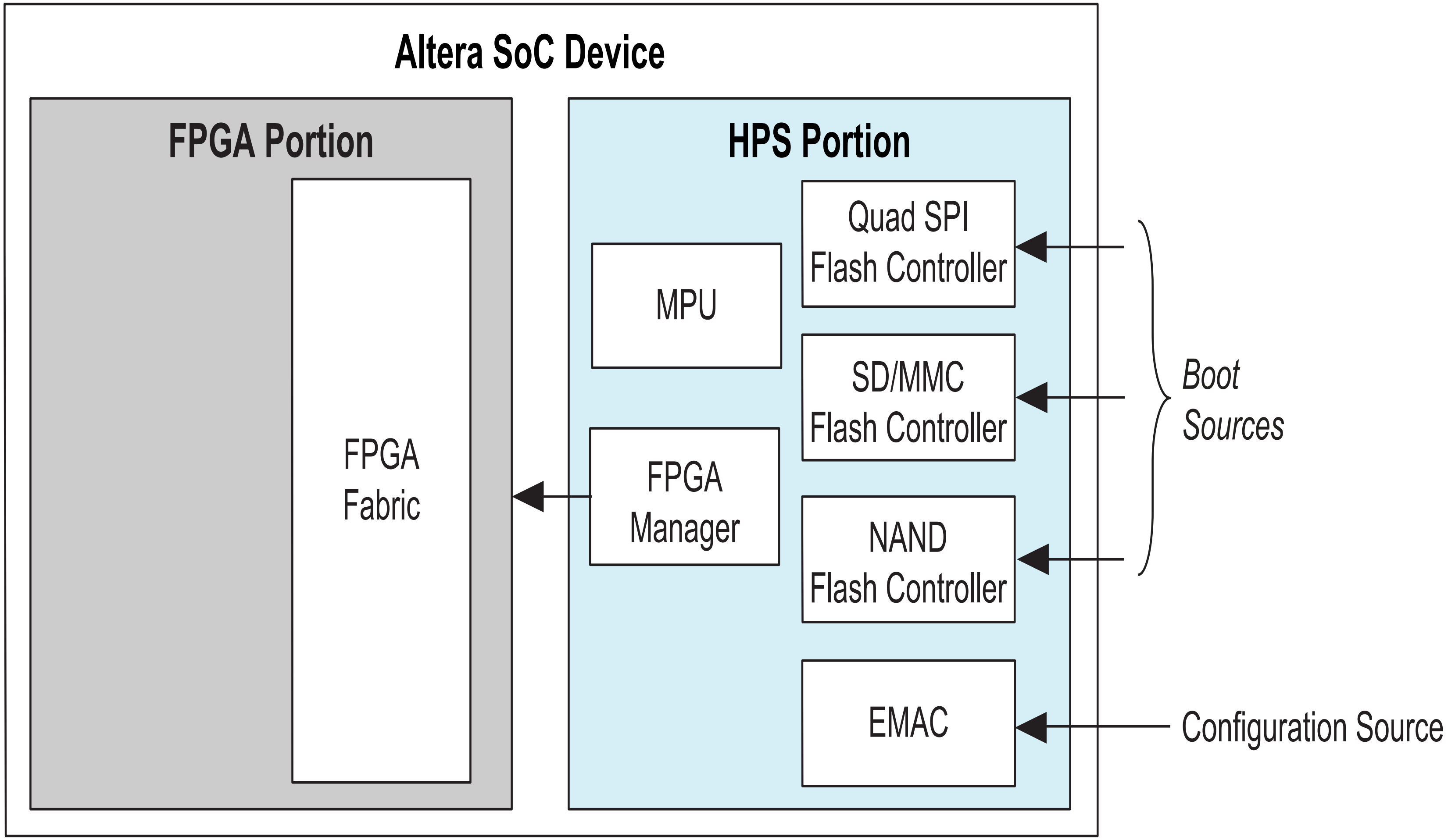
HPS/FPGA Boot (2)

FPGA Configuration before HPS Booting
(HPS boots from FPGA)



HPS/FPGA Boot (3)

HPS Boots and Performs FPGA Configuration



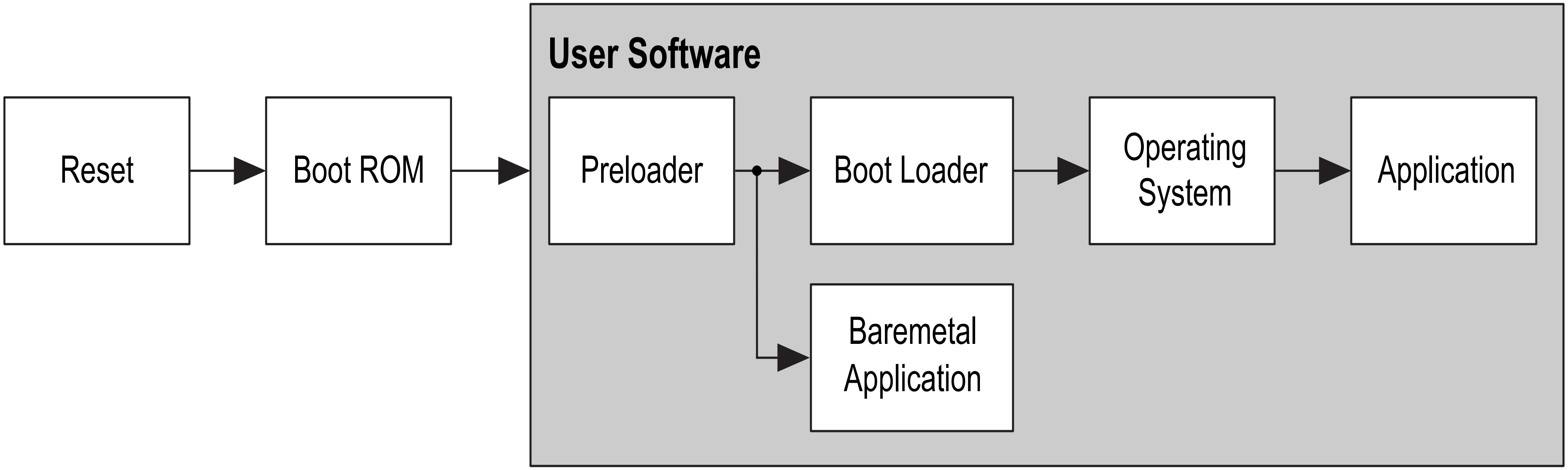
FPGA only case

- Exclusively using the FPGA part of the Cyclone V is easy, as the design process is identical to any other Altera FPGA.
- We can build a complete design in *Quartus II & Qsys*, simulate it in *ModelSim-Altera*, then program the FPGA through the *Quartus II Programmer*.
- We can instantiate a Nios II processor in *Qsys,* we can use the *Nios II SBT* IDE to develop software for the processor.

Type of Application

- OS based (ie: Linux)
- Bare-metal (No OS)

HPS Boot Flows



*Although the HPS has a **DUAL**-processor,*
CPU1 is under reset, and the boot flow only executes on CPU0.

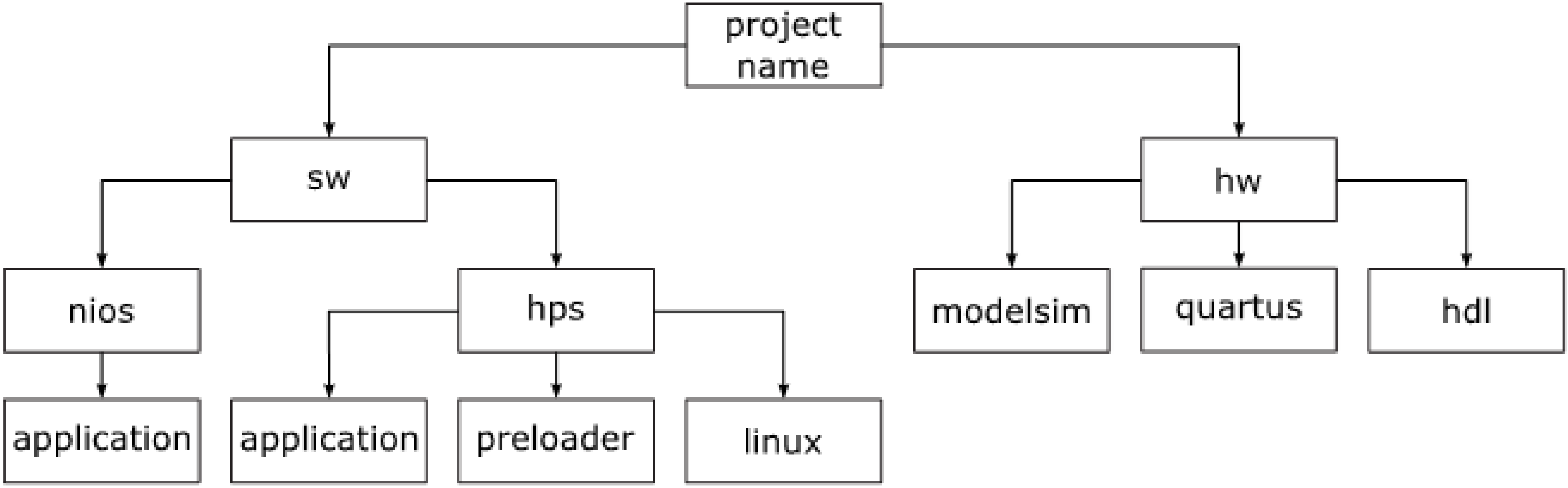
If we want to use both processors,
*then **USER SOFTWARE** executing on CPU0 is responsible*
for releasing CPU1 from reset

Preloader

- The preloader is one of the most important boot stages. It is actually what one would call the boot "*source*", as **all stages before it are unmodifiable**. The preloader can be stored on external flash-based memory, or in the FPGA fabric.
- The preloader typically performs the following actions:
  - Initialize the SDRAM interface
  - Configure the HPS I/O through the scan manager
  - Configure pin multiplexing through the system manager
  - Configure HPS clocks through the clock manager
  - Initialize the flash controller (NAND, SD/MMC, QSPI) that contains the next stage boot software
  - Load the next boot software into the SDRAM and pass control to it

- The preloader does ***NOT*** release CPU1 from reset. The subsequent stages of the boot process are responsible for it if they want to use the extra processor.

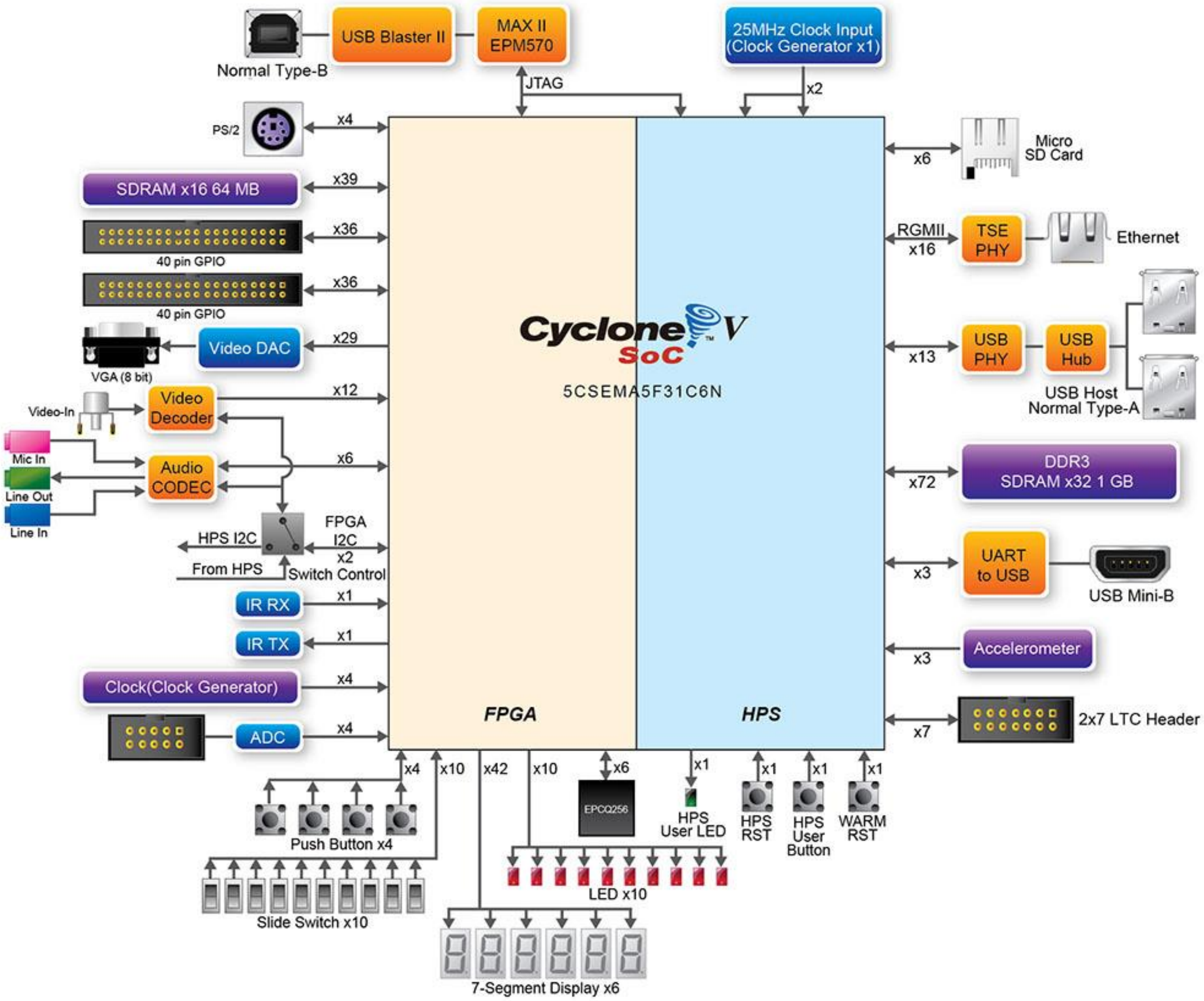
Project structure



DE1-SOC BOARD (TERASIC)

www.terasic.com.tw

DE1-SOC Bloc Diagramm

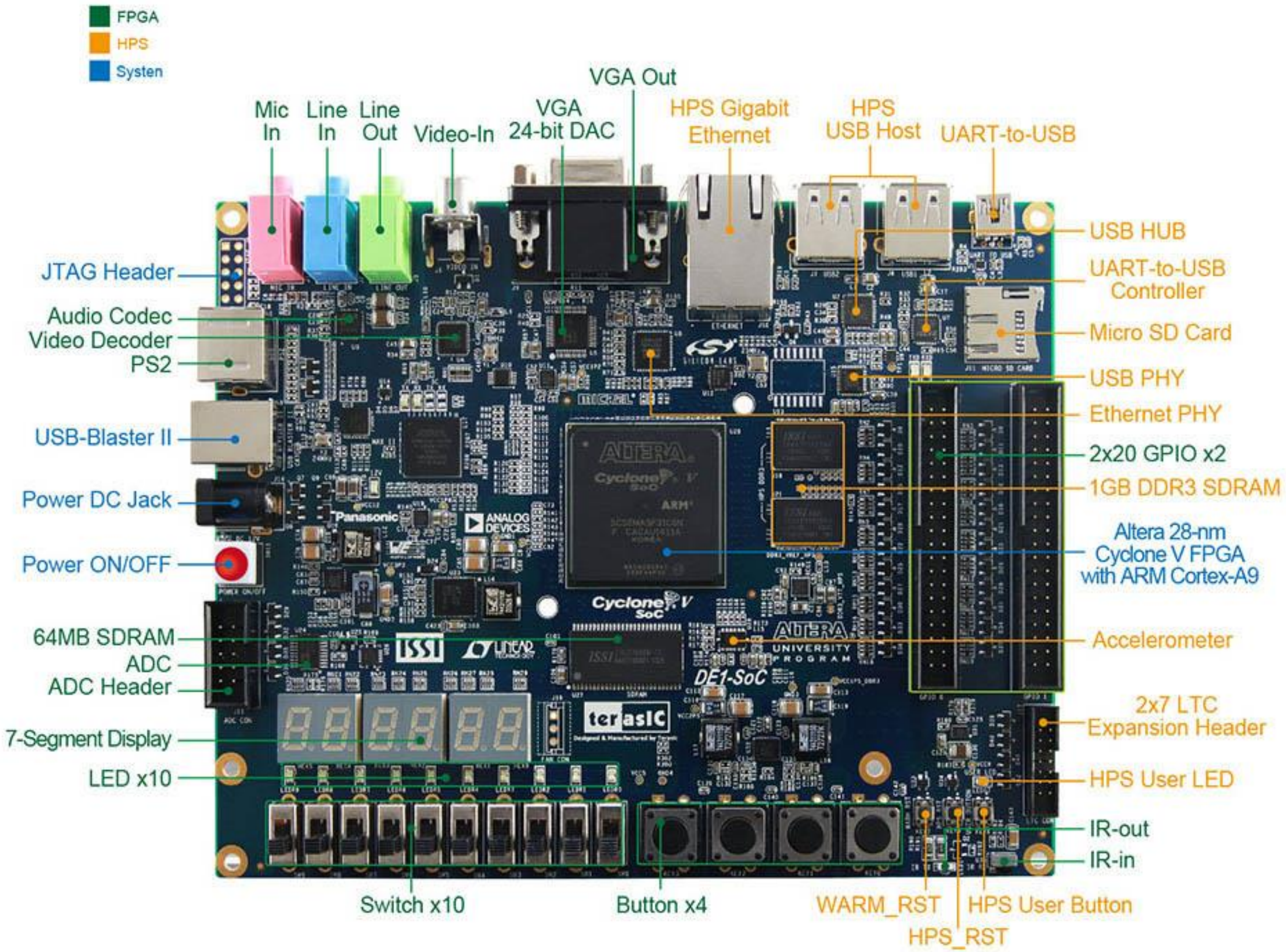


DE1-SoC

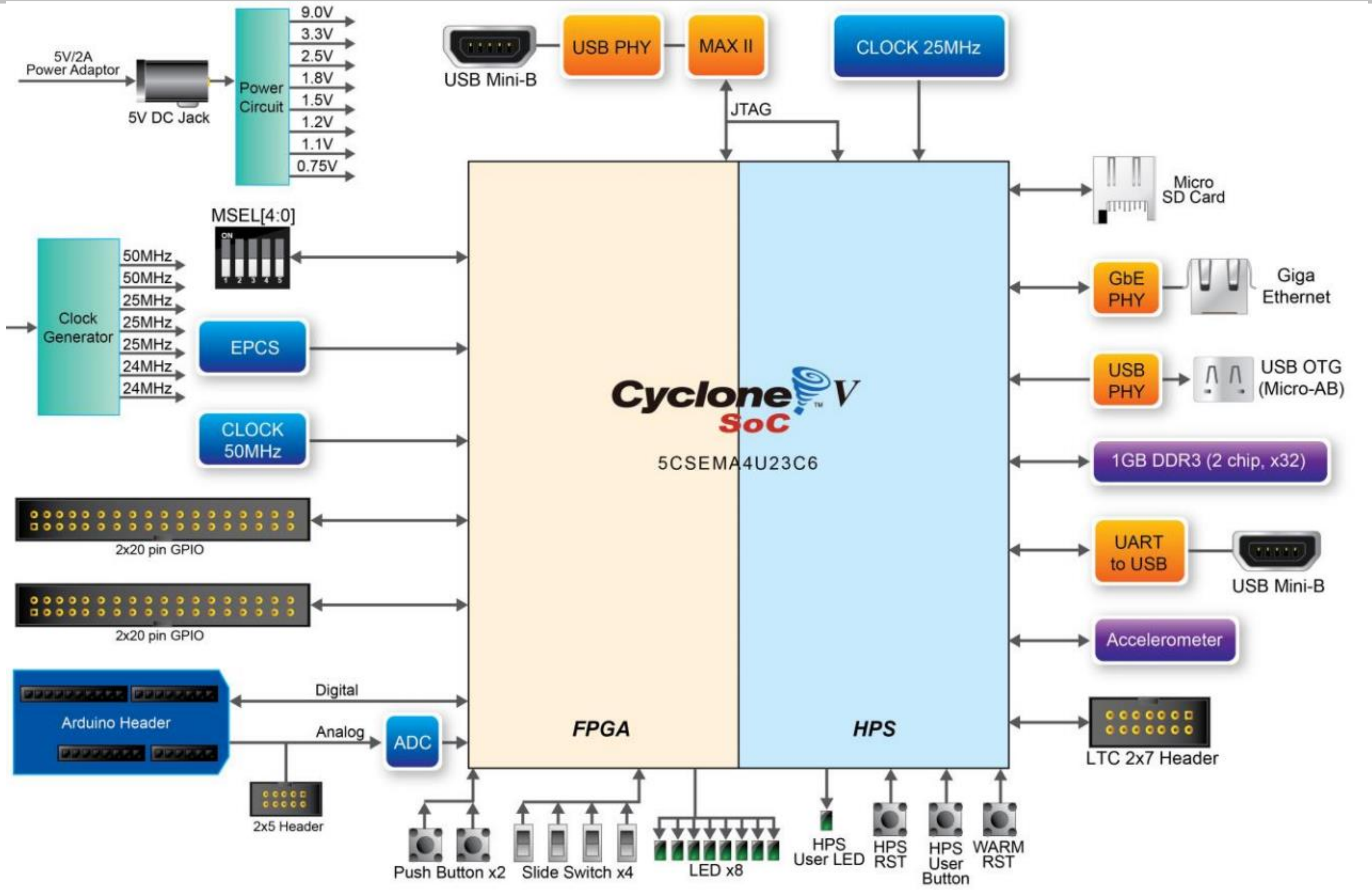
Green for peripherals directly connected to the FPGA

Orange for peripherals directly connected to the HPS

Blue for board control

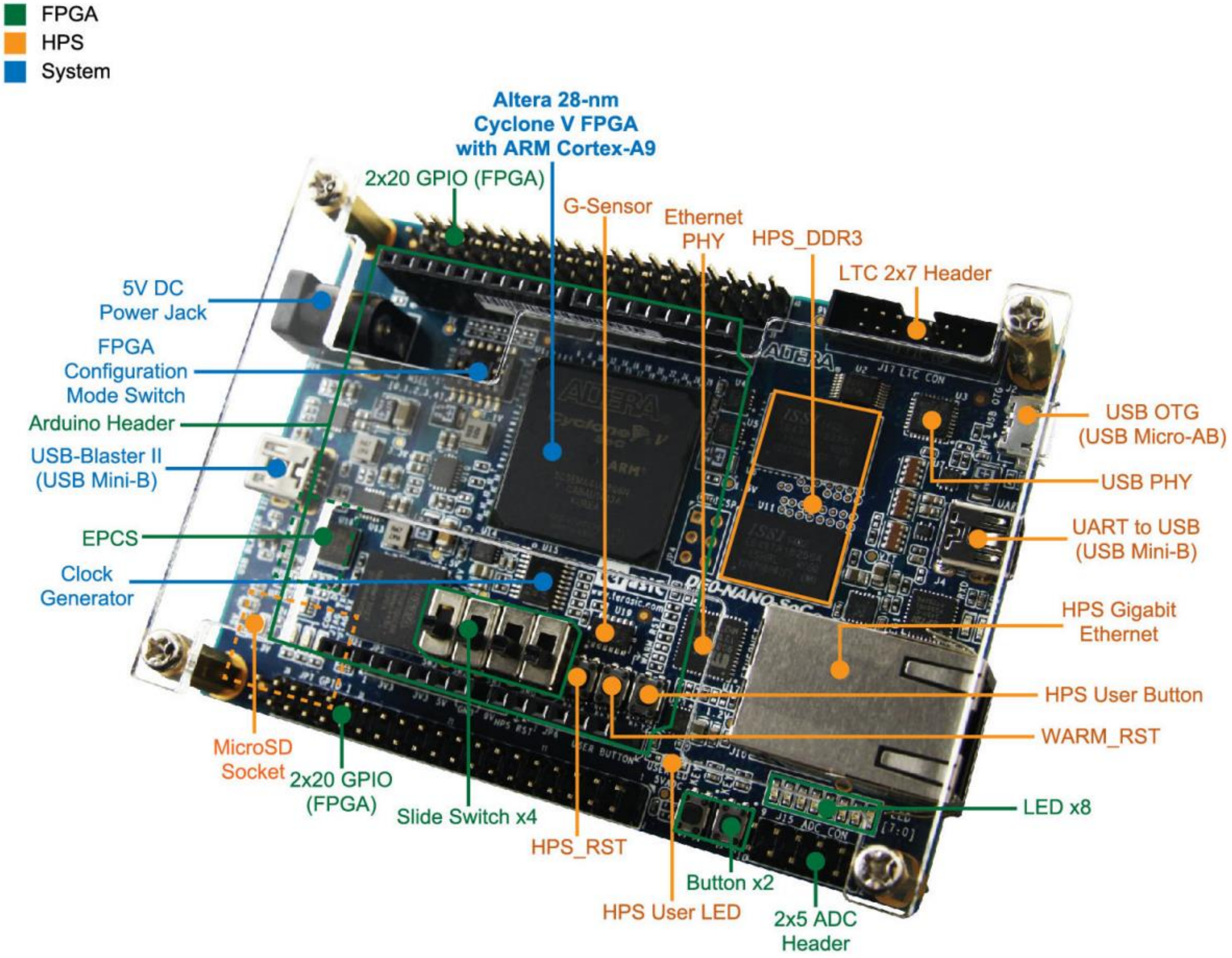


DE0-nano-SoC

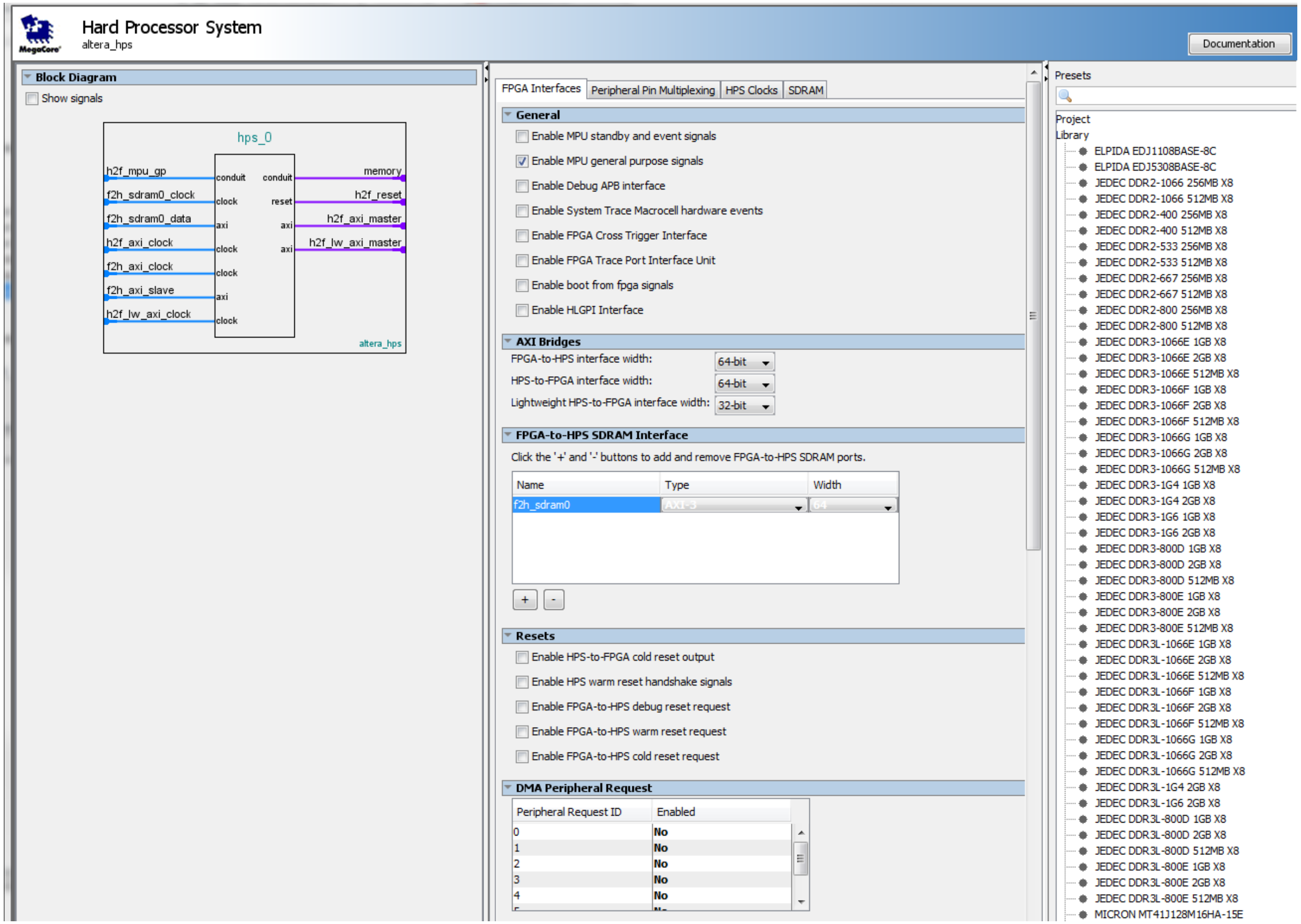


http://www.terasic.com.tw/attachment/archive/941/DE0-Nano-SoC_User_manual_rev.C1.pdf

DE0-nano-SoC


🟩 FPGA
🟧 HPS
🟦 System
Altera 28-nm Cyclone V FPGA with ARM Cortex-A9
2x20 GPIO (FPGA)
G-Sensor
Ethernet PHY
HPS_DDR3
LTC 2x7 Header
5V DC Power Jack
FPGA Configuration Mode Switch
Arduino Header
USB-Blaster II (USB Mini-B)
EPCS
Clock Generator
USB OTG (USB Micro-AB)
USB PHY
UART to USB (USB Mini-B)
HPS Gigabit Ethernet
HPS User Button
WARM_RST
LED x8
MicroSD Socket
2x20 GPIO (FPGA)
Slide Switch x4
HPS_RST
Button x2
HPS User LED
2x5 ADC Header

Qsys, hps definition (1)



Hard Processor System
altera_hps

□ Show signals

General

□ Enable MPU standby and event signals

☑ Enable MPU general purpose signals

□ Enable Debug APB interface

□ Enable System Trace Macrocell hardware events

□ Enable FPGA Cross Trigger Interface

□ Enable FPGA Trace Port Interface Unit

□ Enable boot from fpga signals

□ Enable HLGPI Interface

AXI Bridges

FPGA-to-HPS interface width: 64-bit

HPS-to-FPGA interface width: 64-bit

Lightweight HPS-to-FPGA interface width: 32-bit

FPGA-to-HPS SDRAM Interface

Click the '+' and '-' buttons to add and remove FPGA-to-HPS SDRAM ports.

Name	Type	Width
f2h_sdram0	AXI-3	64

Resets

□ Enable HPS-to-FPGA cold reset output

□ Enable HPS warm reset handshake signals

□ Enable FPGA-to-HPS debug reset request

□ Enable FPGA-to-HPS warm reset request

□ Enable FPGA-to-HPS cold reset request

DMA Peripheral Request

Peripheral Request ID	Enabled
0	**No**
1	**No**
2	**No**
3	**No**
4	**No**

Presets

Project
Library
- ELPIDA EDJ1108BASE-8C
- ELPIDA EDJ5308BASE-8C
- JEDEC DDR2-1066 256MB X8
- JEDEC DDR2-1066 512MB X8
- JEDEC DDR2-400 256MB X8
- JEDEC DDR2-400 512MB X8
- JEDEC DDR2-533 256MB X8
- JEDEC DDR2-533 512MB X8
- JEDEC DDR2-667 256MB X8
- JEDEC DDR2-667 512MB X8
- JEDEC DDR2-800 256MB X8
- JEDEC DDR2-800 512MB X8
- JEDEC DDR3-1066E 1GB X8
- JEDEC DDR3-1066E 2GB X8
- JEDEC DDR3-1066E 512MB X8
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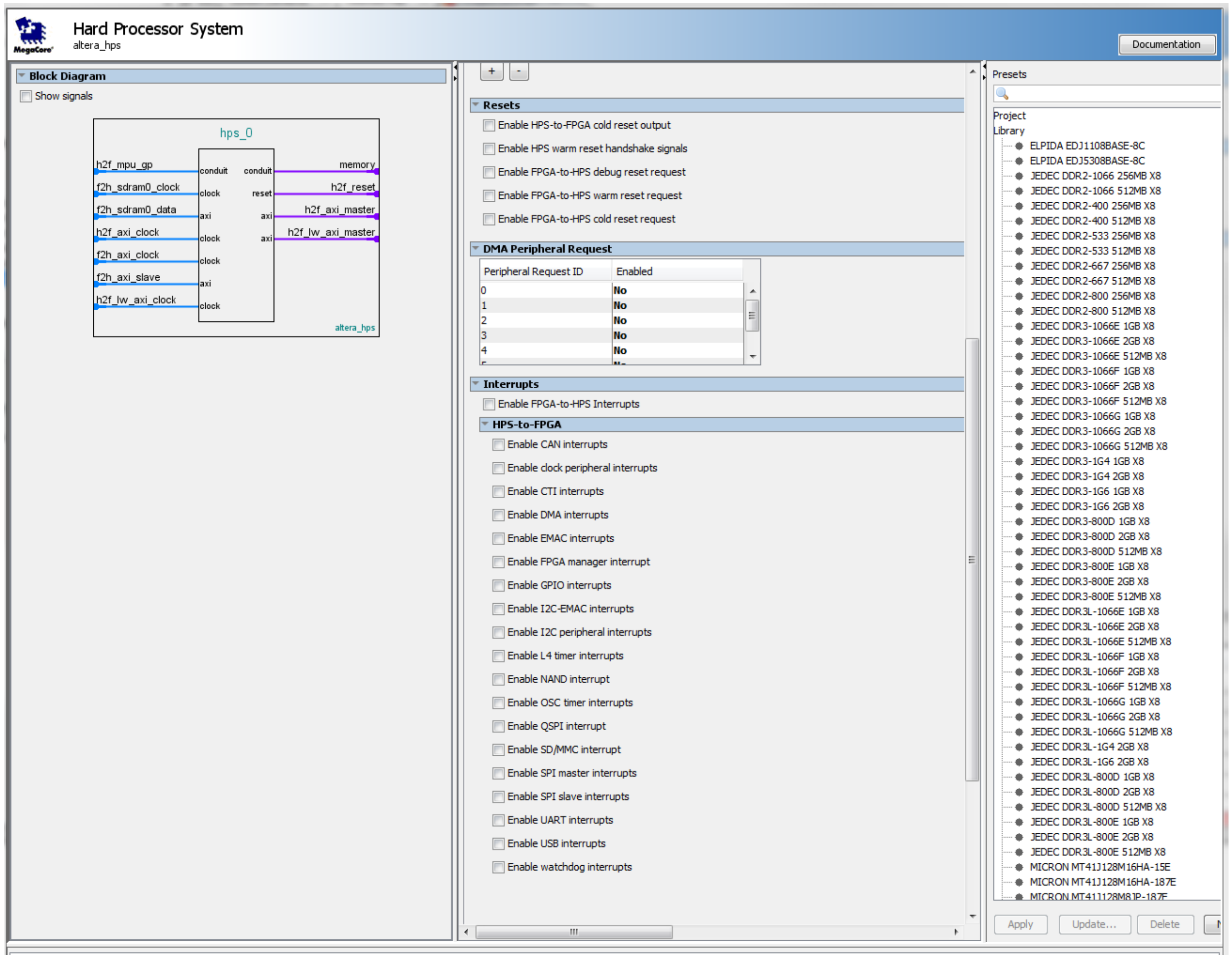
- MICRON MT41J128M16HA-15E

Qsys, hps definition (2)



Resets

- ☐ Enable HPS-to-FPGA cold reset output
- ☐ Enable HPS warm reset handshake signals
- ☐ Enable FPGA-to-HPS debug reset request
- ☐ Enable FPGA-to-HPS warm reset request
- ☐ Enable FPGA-to-HPS cold reset request

DMA Peripheral Request

Peripheral Request ID	Enabled
0	No
1	No
2	No
3	No
4	No

Interrupts

- ☐ Enable FPGA-to-HPS Interrupts

HPS-to-FPGA

- ☐ Enable CAN interrupts
- ☐ Enable clock peripheral interrupts
- ☐ Enable CTI interrupts
- ☐ Enable DMA interrupts
- ☐ Enable EMAC interrupts
- ☐ Enable FPGA manager interrupt
- ☐ Enable GPIO interrupts
- ☐ Enable I2C-EMAC interrupts
- ☐ Enable I2C peripheral interrupts
- ☐ Enable L4 timer interrupts
- ☐ Enable NAND interrupt
- ☐ Enable OSC timer interrupts
- ☐ Enable QSPI interrupt
- ☐ Enable SD/MMC interrupt
- ☐ Enable SPI master interrupts
- ☐ Enable SPI slave interrupts
- ☐ Enable UART interrupts
- ☐ Enable USB interrupts
- ☐ Enable watchdog interrupts

Presets

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- MICRON MT41J128M16HA-15E
- MICRON MT41J128M16HA-187E
- MICRON MT41J128M8JP-187E

IO PIN in HPS

- With the ***PeripheralPin Multiplexing***, some I/O interface can be used by the **HPS part** or the **FPGA part**.
- The selection is done here.

Exercises / Mini Project

1. Use the DE1-SOC/DE0-nano-SoC without the ARM-A9
   - NIOS design to access the Switches and LEDs
   - Adapt the LCD/camera controller for the NIOSII

2. Use the ARM-A9 with ARM DS-5 software
   - Access through the AXI bridge the Avalon part of the FPGA
   - Control the LCD/camera from the ARM

- Try the Linux access of the FPGA…to control LCD and Camera

- In option !