Embedded Systems

Micro Controller Unit (MCU)
MSP432 P401R
MSP430 G2x53

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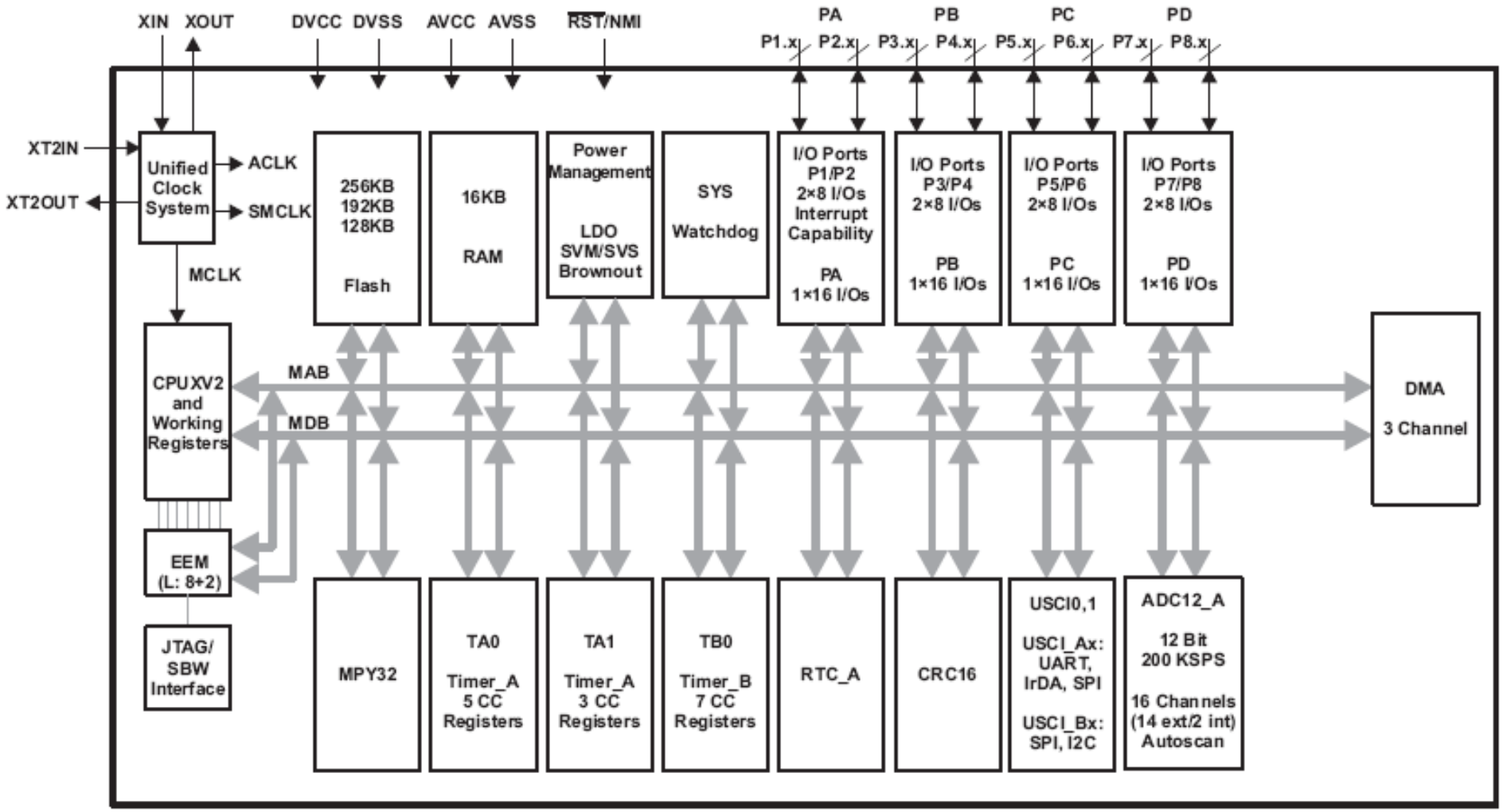
From ti documentation

Microcontroller

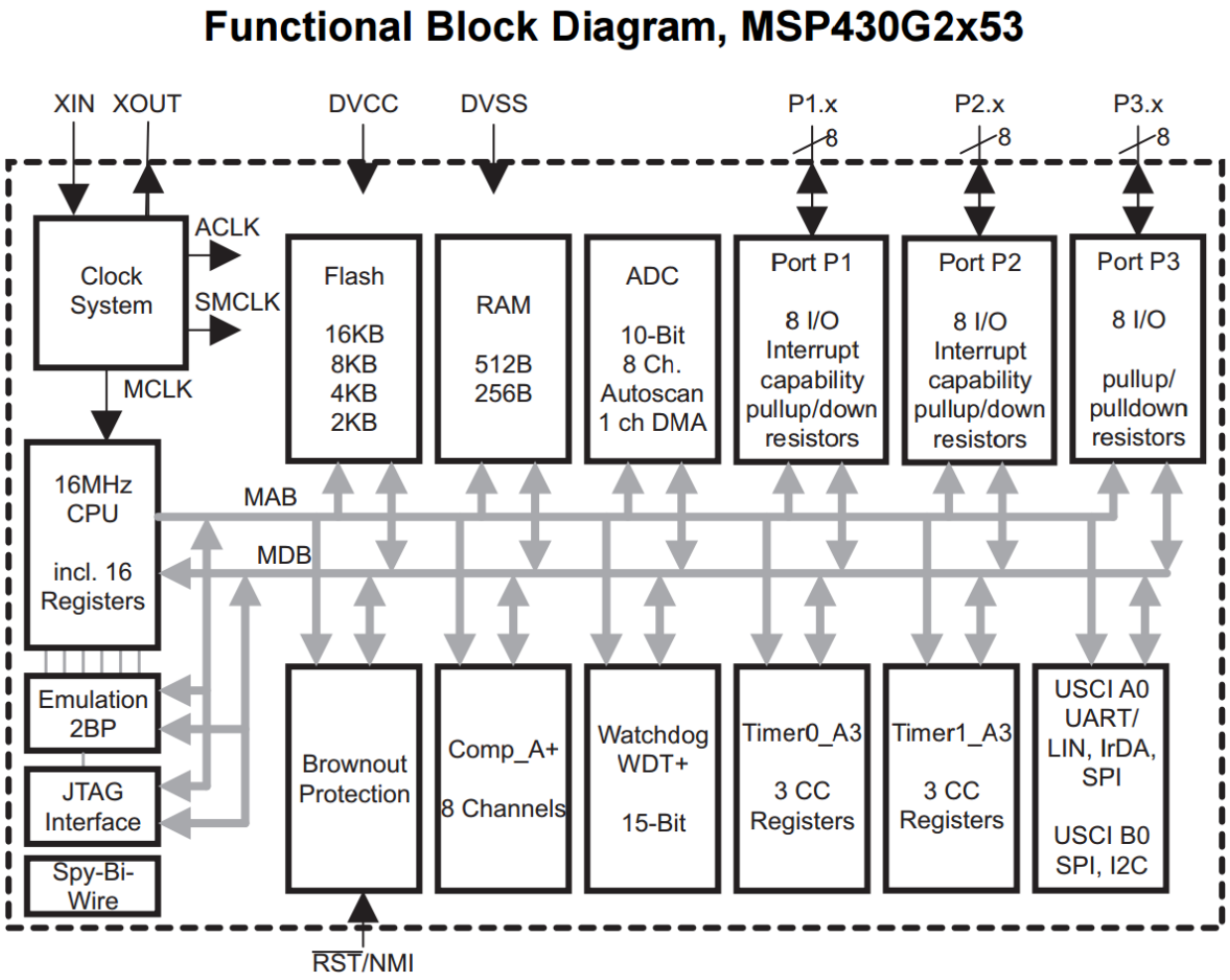
- A microcontroller is an integrated circuit with:
  - A **processor** (one or many)
  - Some **memories** as:
    - Flash EPROM
    - SRAM
  - Some **programmable interfaces** as:
    - GPIO (parallel port)
    - Timer
    - Serial port (UART, SPI, i2c, USB, …)
    - ADC, DAC
    - Lot more…

General View, MSP430

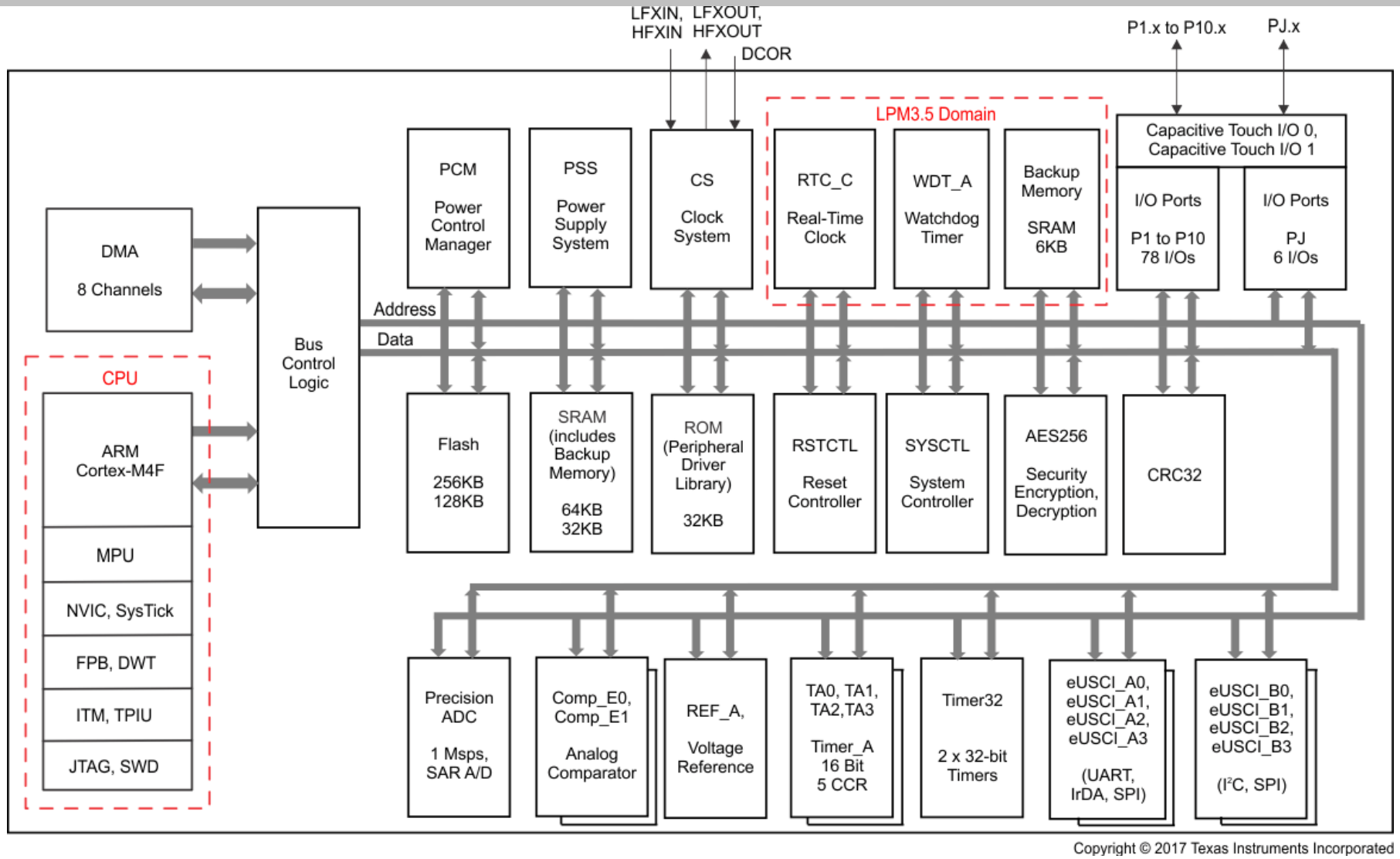
Functional Block Diagram, MSP430F5437IPN, MSP430F5435IPN, MSP430F5418IPN



General View, MSP430



General View, MSP432P401



MSP432, family members

- Few examples of this family

DEVICE	FLASH (KB)	SRAM (KB)	Precision ADC (Channels)	COMP_E0 (Channels)	COMP_E1 (Channels)	Timer_A[2]	eUSCI		20-mA DRIVE I/O	TOTAL I/Os	PACKAGE
							CHANNEL A: UART, IrDA, SPI	CHANNEL B: SPI, I^2C			
MSP432P401RIPZ	256	64	24 ext, 2 int	8	8	5, 5, 5, 5	4	4	4	84	100 PZ
MSP432P401MIPZ	128	32	24 ext, 2 int	8	8	5, 5, 5, 5	4	4	4	84	100 PZ
MSP432P401RIZXH	256	64	16 ext, 2 int	6	8	5, 5, 5	3	4	4	64	80 ZXH
MSP432P401MIZXH	128	32	16 ext, 2 int	6	8	5, 5, 5	3	4	4	64	80 ZXH
MSP432P401RIRGC	256	64	12 ext, 2 int	2	4	5, 5, 5	3	3	4	48	64 RGC
MSP432P401MIRGC	128	32	12 ext, 2 int	2	4	5, 5, 5	3	3	4	48	64 RGC

Features MSP432

- **Core**
  - ARM® 32-Bit Cortex®-M4F CPU With Floating-Point Unit and Memory Protection Unit
  - Frequency up to 48 MHz
  - ULPBench™ Benchmark:
    - 192.3 ULPMark™-CP
  - Performance Benchmark:
    - 3.41 CoreMark/MHz
    - 1.22 DMIPS/MHz (Dhrystone 2.1)

Features

- **Advanced Low-Power Analog Features**
  - SAR Analog-To-Digital Converter (ADC) With 16-Bit Precision and up to 1 Msps
    - Differential and Single-Ended Inputs
    - Two Window Comparators
    - Up to 24 Input Channels
  - Internal Voltage Reference With 10-ppm/°C Typical Stability
  - Two Analog Comparators

Features

- **Memories**
  - Up to 256KB of Flash Main Memory (Organized Into Two Banks Enabling Simultaneous Read/Execute During Erase)
  - 16KB of Flash Information Memory (Used for BSL, TLV, and Flash Mailbox)
  - Up to 64KB of SRAM (Including 6KB of Backup Memory)
  - 32KB of ROM With MSP432™ Peripheral Driver Libraries

Features

- **Ultra-Low-Power Operating Modes**
  - Active: 80 µA/MHz
  - Low-Frequency Active: 83 µA at 128 kHz
  - LPM3 (With RTC): 660 nA
  - LPM3.5 (With RTC): 630 nA
  - LPM4: 500 nA
  - LPM4.5: 25 nA

Features

- **Operating Characteristics**
  - Wide Supply Voltage Range: 1.62 V to 3.7 V
  - Temperature Range (Ambient): –40°C to 85°C
- **JTAG and Debug Support**
  - 4-Pin JTAG and 2-Pin SWD Debug Interfaces
  - Serial Wire Trace
  - Power Debug and Profiling of Applications

Features

- **Code Security Features**
  - JTAG and SWD Lock
  - IP Protection (up to Four Secure Flash Zones, Each With Configurable Start Address and Size)

Features

- **Flexible Clocking Features**
  - Tunable Internal DCO (up to 48 MHz)
  - 32.768-kHz Low-Frequency Crystal Support (LFXT)
  - High-Frequency Crystal Support (HFXT) up to 48 MHz
  - Low-Frequency Internal Reference Oscillator (REFO)
  - Very Low-Power Low-Frequency Internal Oscillator (VLO)
  - Module Oscillator (MODOSC)
  - System Oscillator (SYSOSC)

Features

- **Enhanced System Features**
  - Programmable Supervision and Monitoring of Supply Voltage
  - Multiple-Class Resets for Better Control of Application and Debug
  - 8-Channel DMA
  - RTC With Calendar and Alarm Functions

Features

- **Flexible I/O Features**
  - Ultra-Low-Leakage I/Os (±20 nA Maximum)
  - All I/Os With Capacitive-Touch Capability
  - Up to 48 I/Os With Interrupt and Wake-up Capability
  - Up to 24 I/Os With Port Mapping Capability
  - Eight I/Os With Glitch Filtering Capability

Features

- **Timing and Control**
  - Up to Four 16-Bit Timers, Each With up to Five Capture, Compare, PWM Capability
  - Two 32-Bit Timers, Each With Interrupt Generation Capability

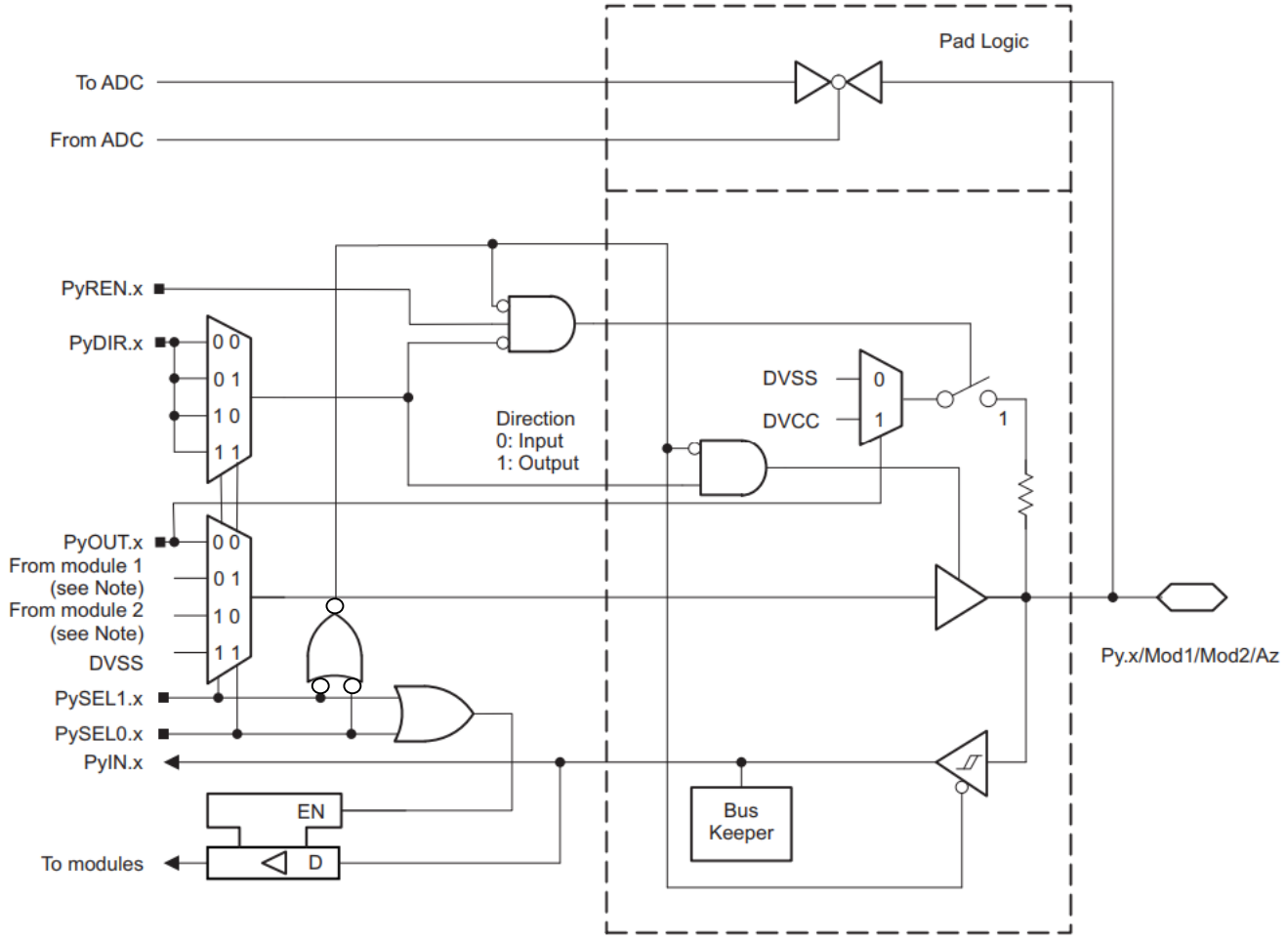
Features

- **Serial Communication**
  - Up to Four eUSCI_A Modules
    - UART With Automatic Baud-Rate Detection
    - IrDA Encode and Decode
    - SPI (up to 16 Mbps)
  - Up to Four eUSCI_B Modules
    - I^2C (With Multiple-Slave Addressing)
    - SPI (up to 16 Mbps)

Features

- **Encryption and Data Integrity Accelerators**
  - 128-, 192-, or 256-Bit AES Encryption and Decryption Accelerator
  - 32-Bit Hardware CRC Engine

Parallel Port
One bit of port P4 of MSP432P401R



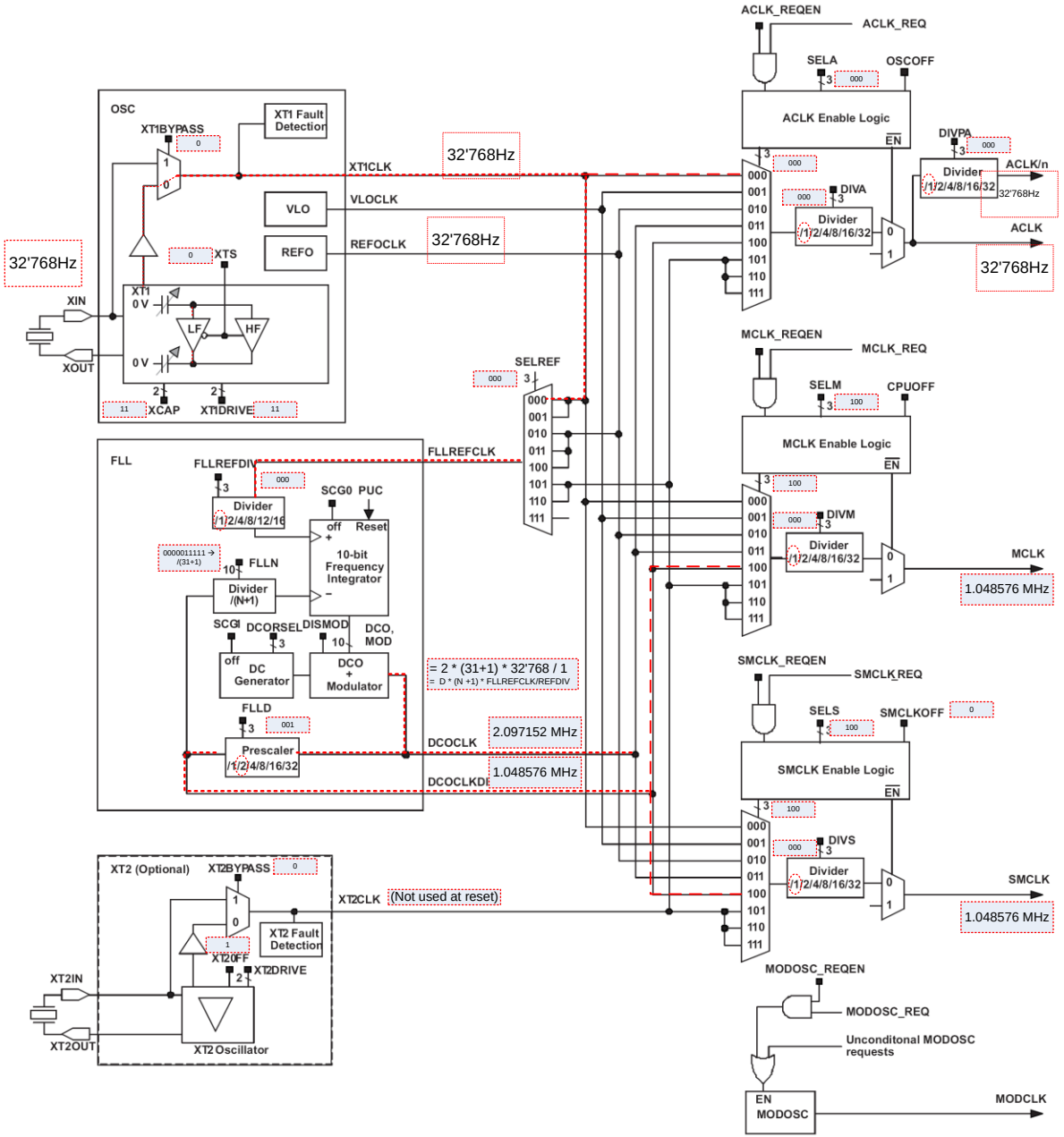
Note: Output is DVSS if module 1 or module 2 function is not available. See the pin function tables.
Functional representation only.

http://www.ti.com/lit/ds/symlink/msp432p401r.pdf p.150

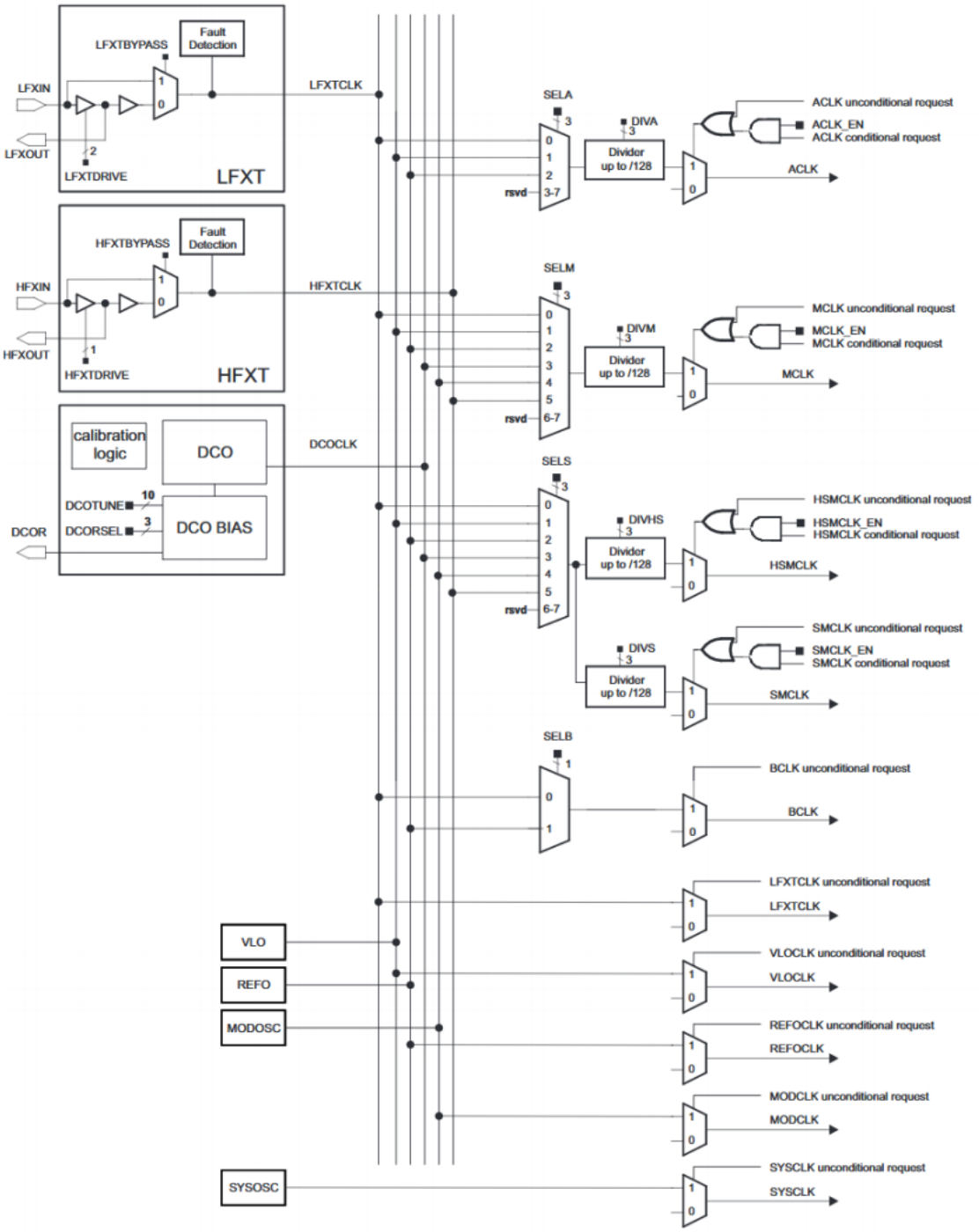
Parallel Port control registers

- ***PyIN*** is the state at the pin level and can be read
- ***PySEL1, PySEL0*** select the pin function.
  “00” → As Port
  “01” → module 1
  “10” → module 2
  “11” → Analog module for Ports 4, 5, 6, 8, 9
- As Port, ***PyOUT*** specifies the data to output
- ***PyDIR*** specifies the direction (‘0’ as input (reset state), ‘1’ as output)
- ***PyREN*** (Resistor Enable) allows a Pull_up or Pull_Down to be activated if the direction is Input

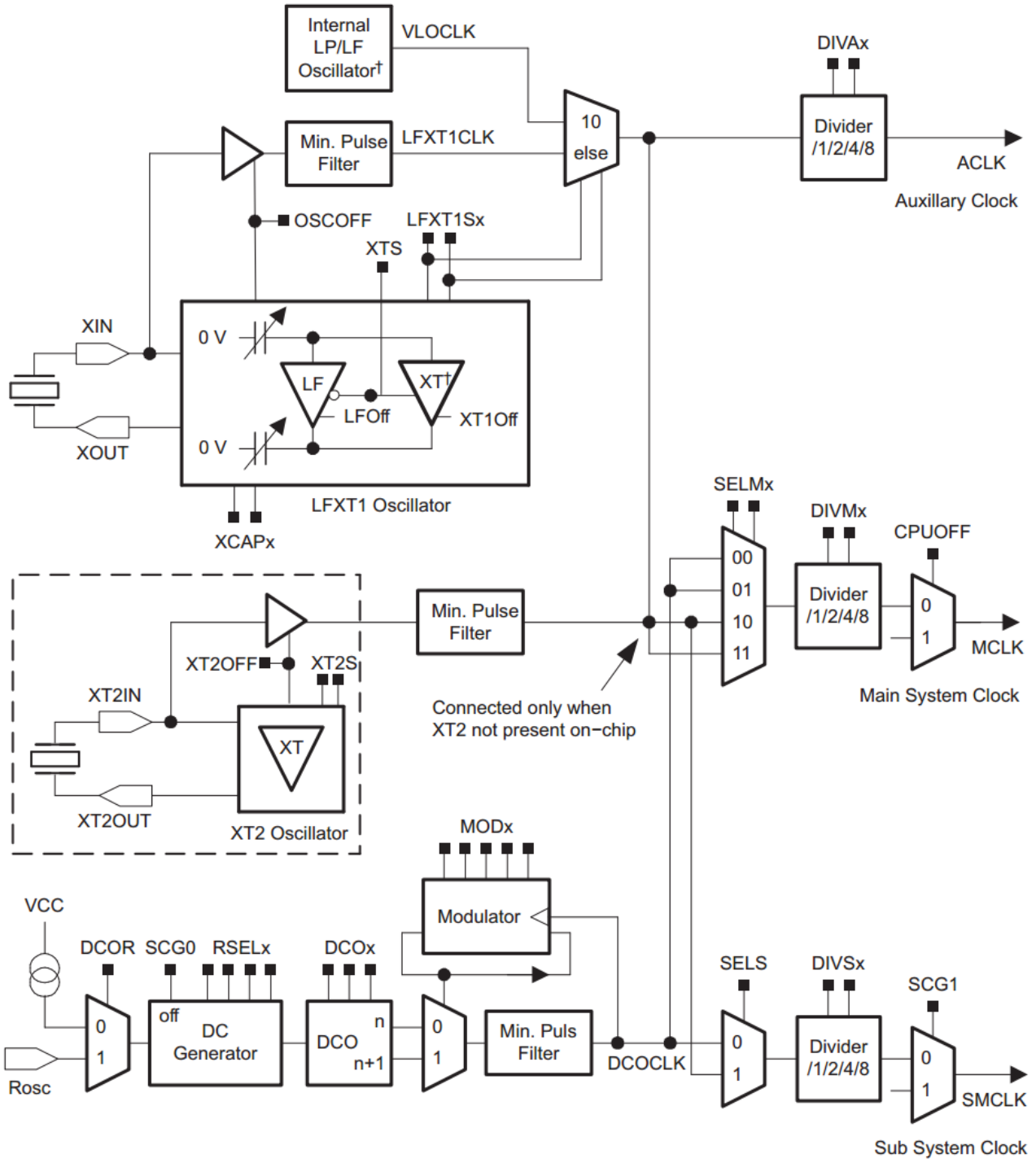
Clock generation
MSP430F54xx



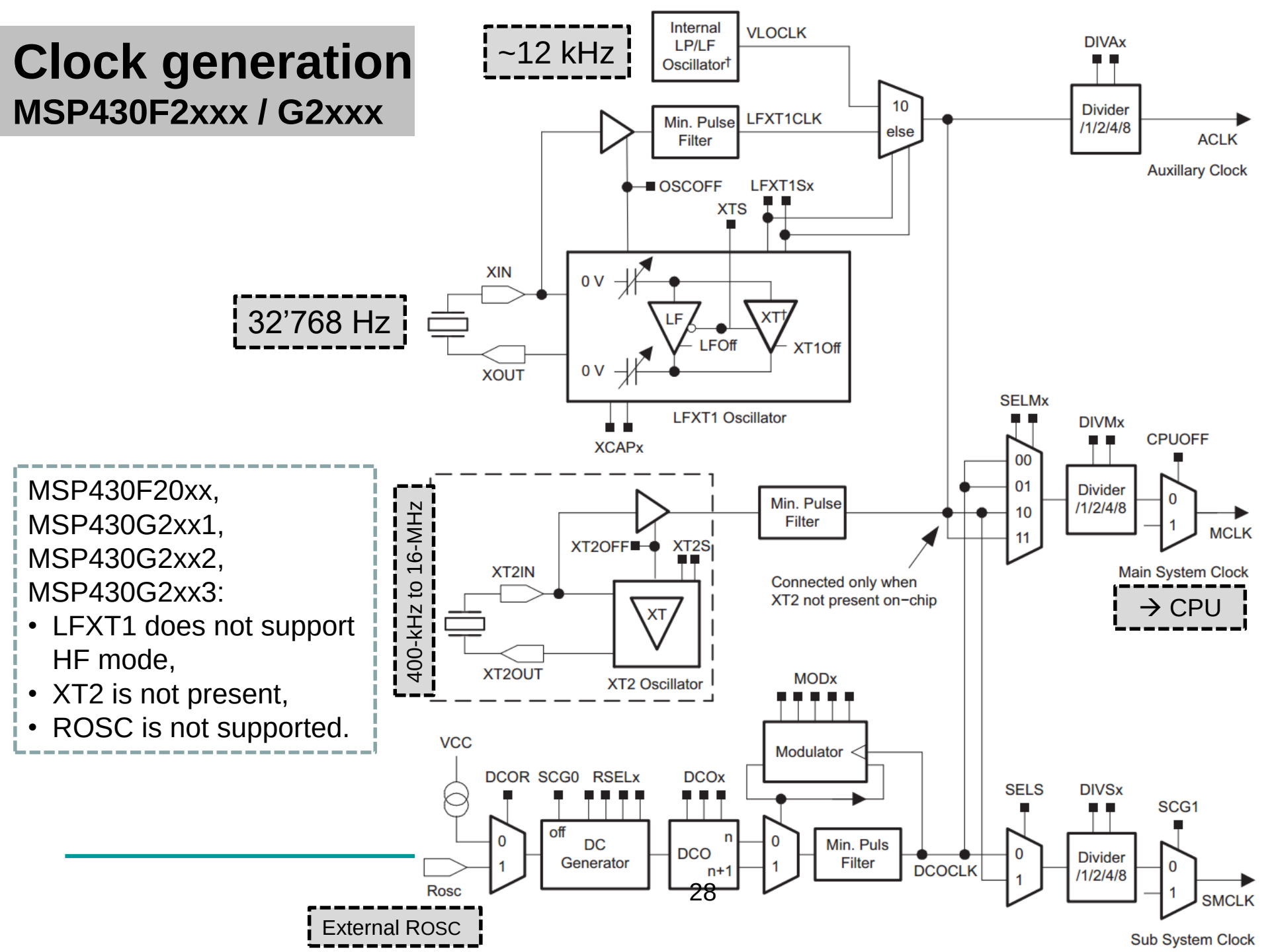
MSP432R401, Clock



Clock generation
MSP430F2xxx / G2xxx



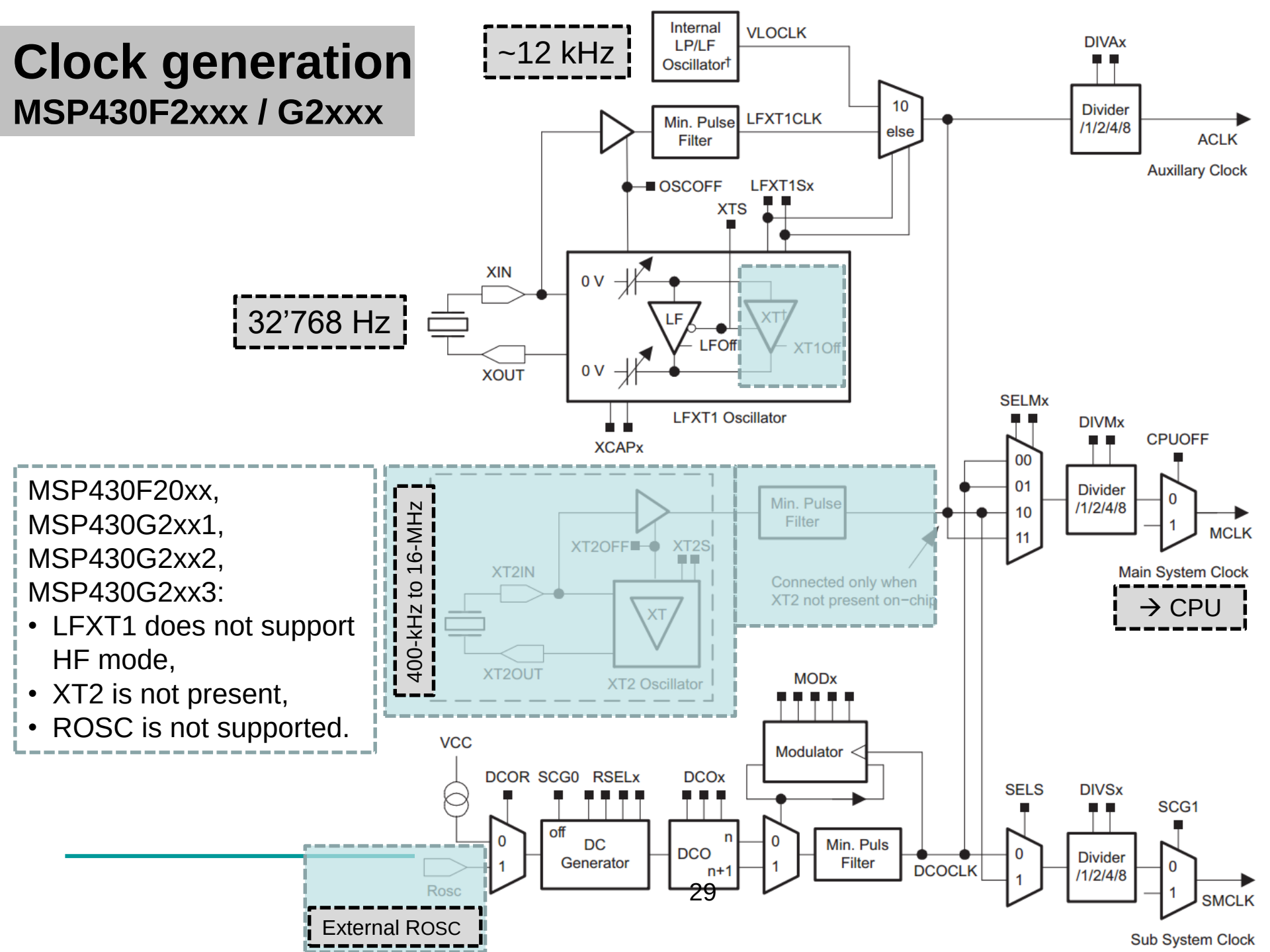
Clock generation
MSP430F2xxx / G2xxx



MSP430F20xx,
MSP430G2xx1,
MSP430G2xx2,
MSP430G2xx3:

- LFXT1 does not support HF mode,
- XT2 is not present,
- ROSC is not supported.

Clock generation
MSP430F2xxx / G2xxx



MSP430F20xx,
MSP430G2xx1,
MSP430G2xx2,
MSP430G2xx3:

- LFXT1 does not support HF mode,
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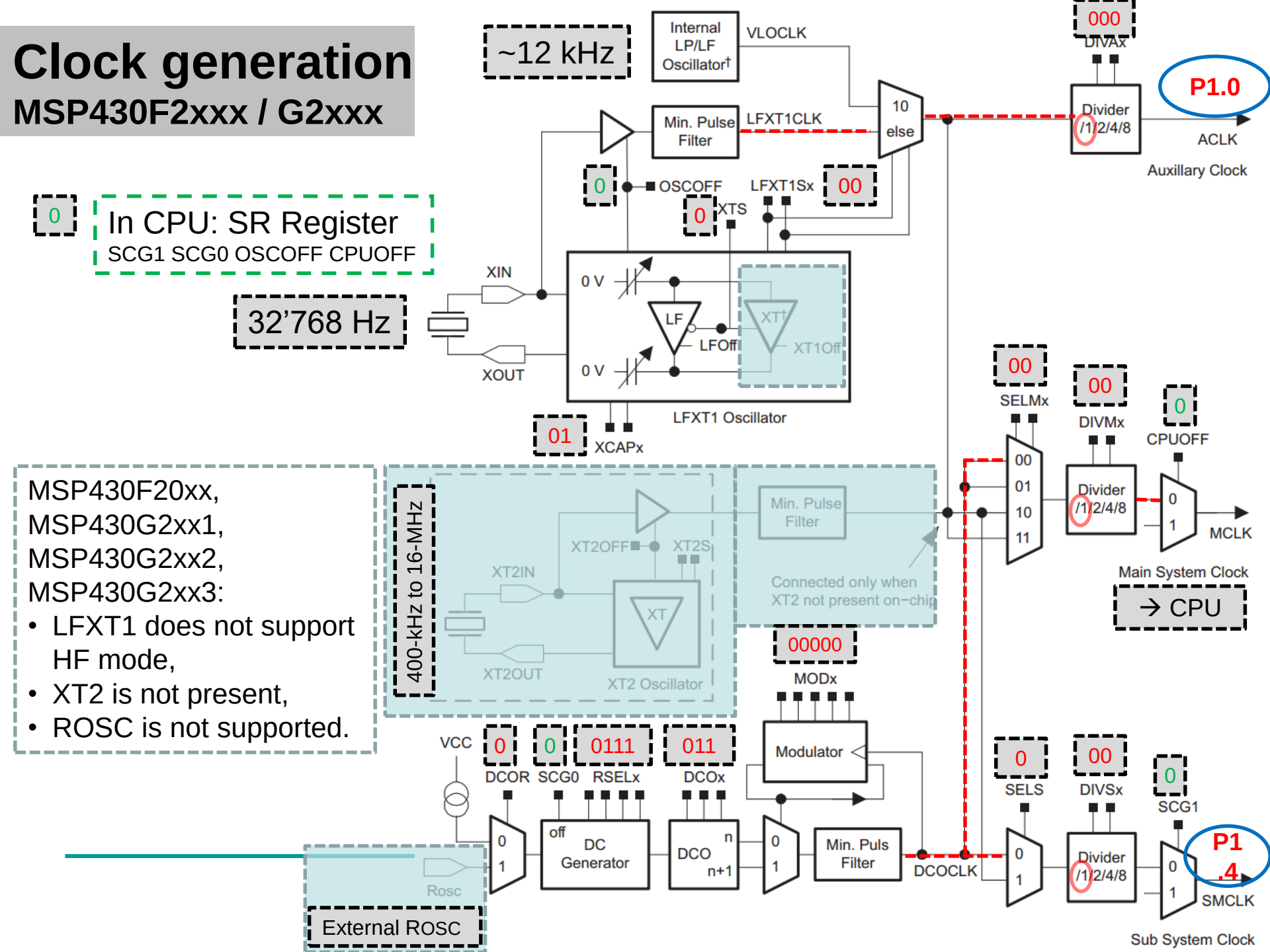
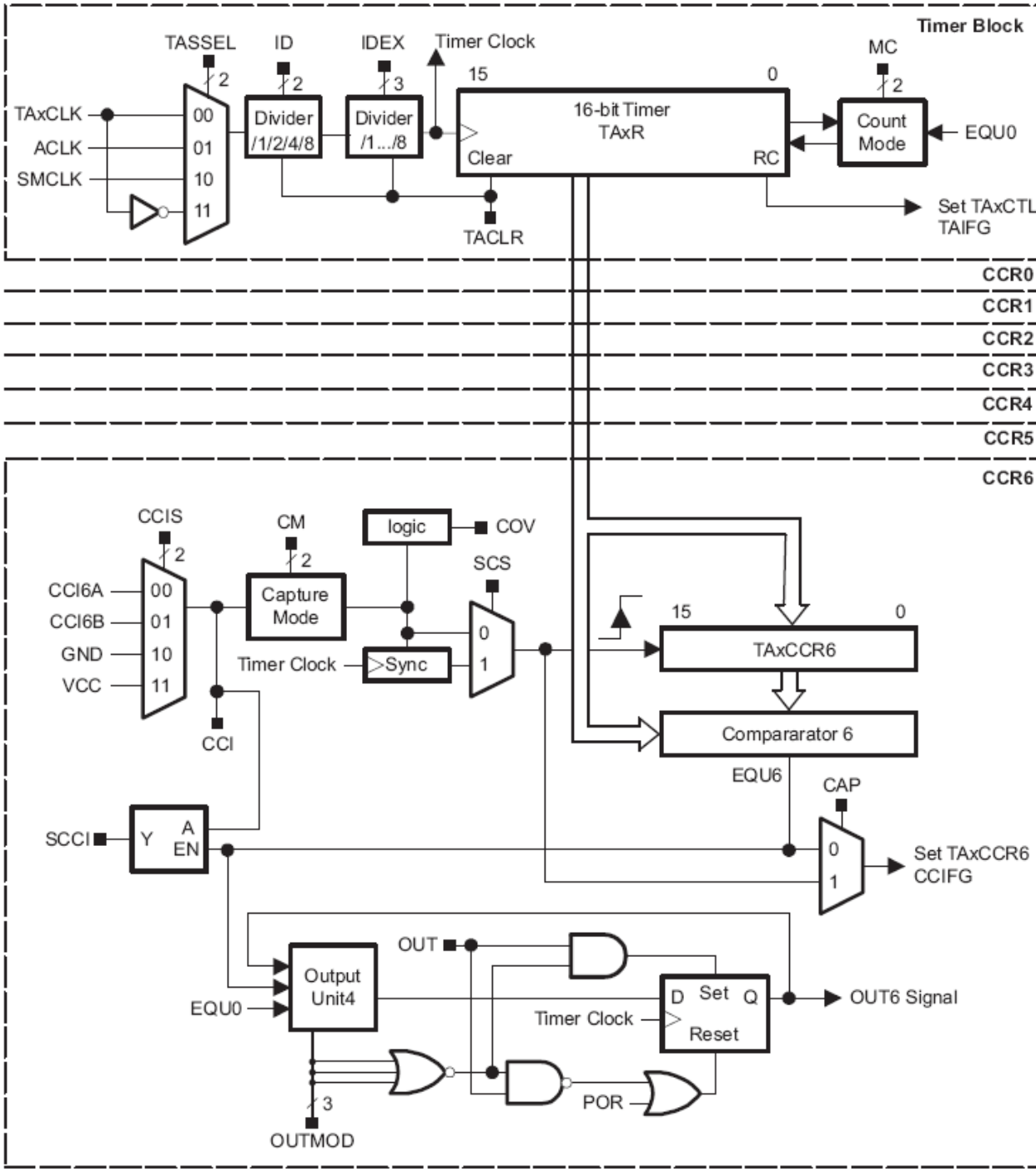
Clock generation
MSP430F2xxx / G2xxx



TimerA

- 1x Counter: TBxR
- Up to 6 Capture/ Compare units



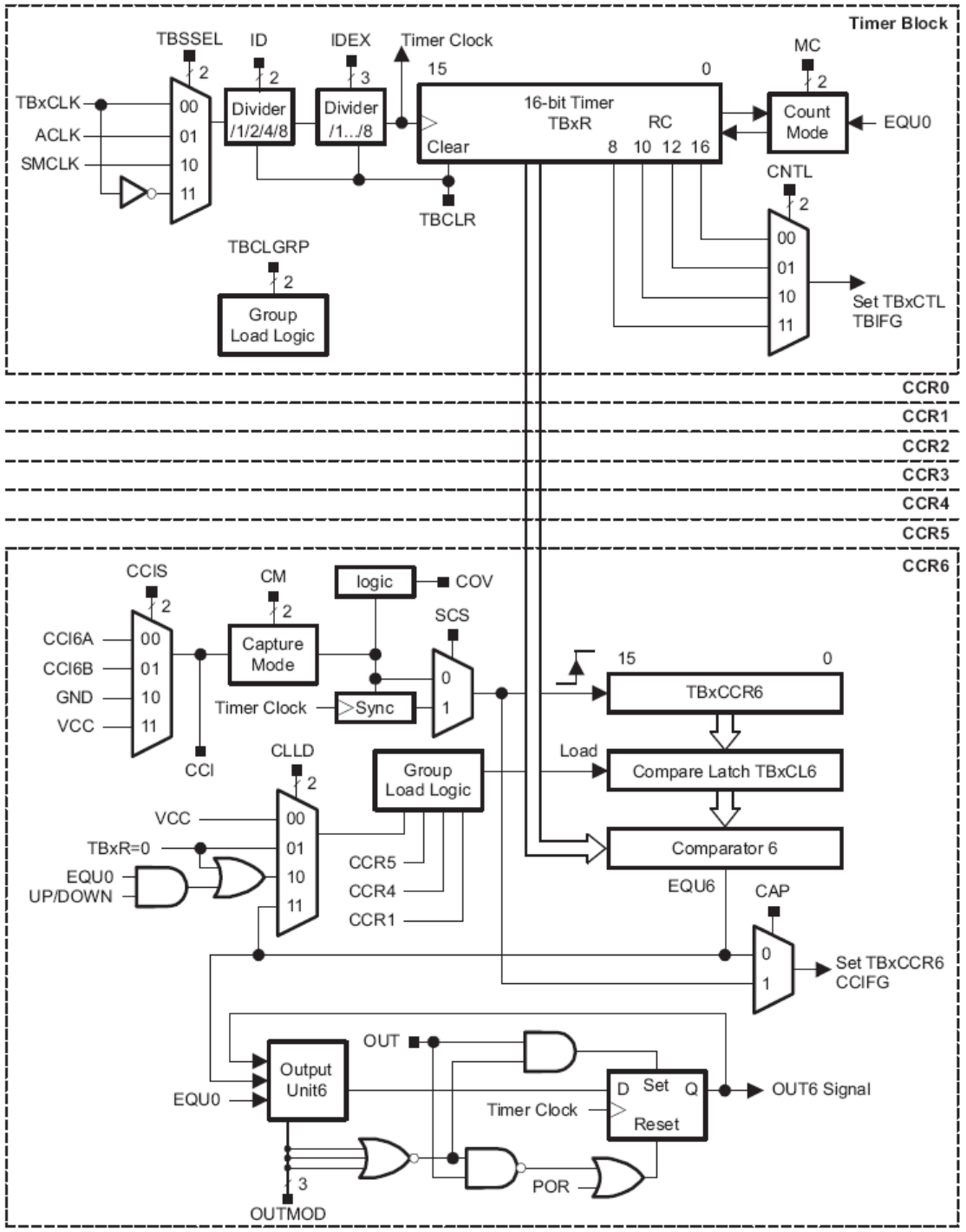
Timer A features

Timer_A features include:

- Asynchronous 16-bit timer/counter with four operating modes
- Selectable and configurable clock source
- Up to seven configurable capture/compare registers
- Configurable outputs with PWM (pulse width modulation) capability
- Asynchronous input and output latching
- Interrupt vector register for fast decoding of all Timer_A interrupts

TimerB architecture

- 1x Counter: TBxR
- Up to 6 Capture/Compare units



Timer B features

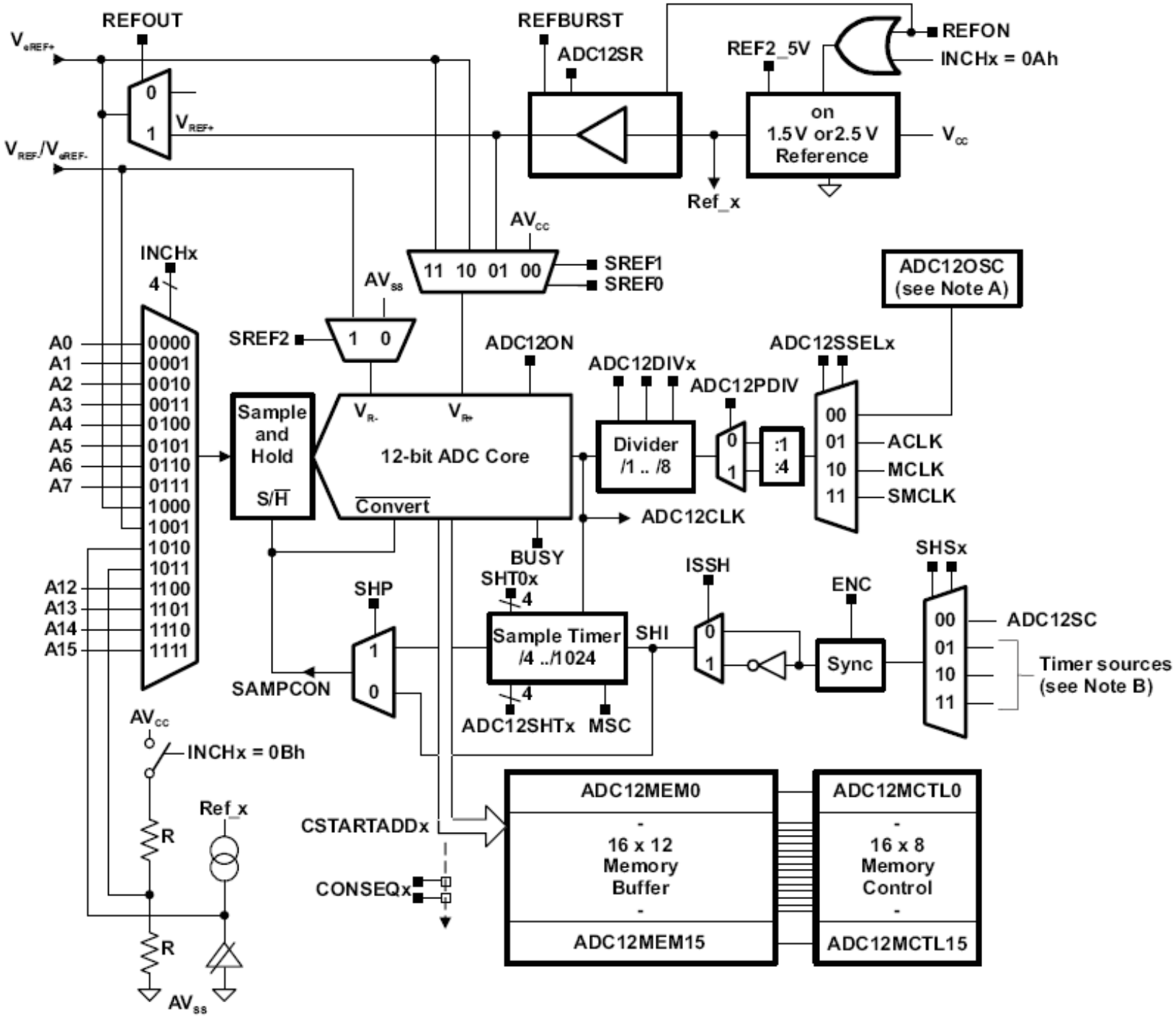
Timer_B features include :

- Asynchronous 16-bit timer/counter with four operating modes and **four selectable lengths**
- Selectable and configurable clock source
- Up to seven configurable capture/compare registers
- Configurable outputs with PWM capability
- **Double-buffered compare latches with synchronized loading**
- Interrupt vector register for fast decoding of all Timer_B interrupts

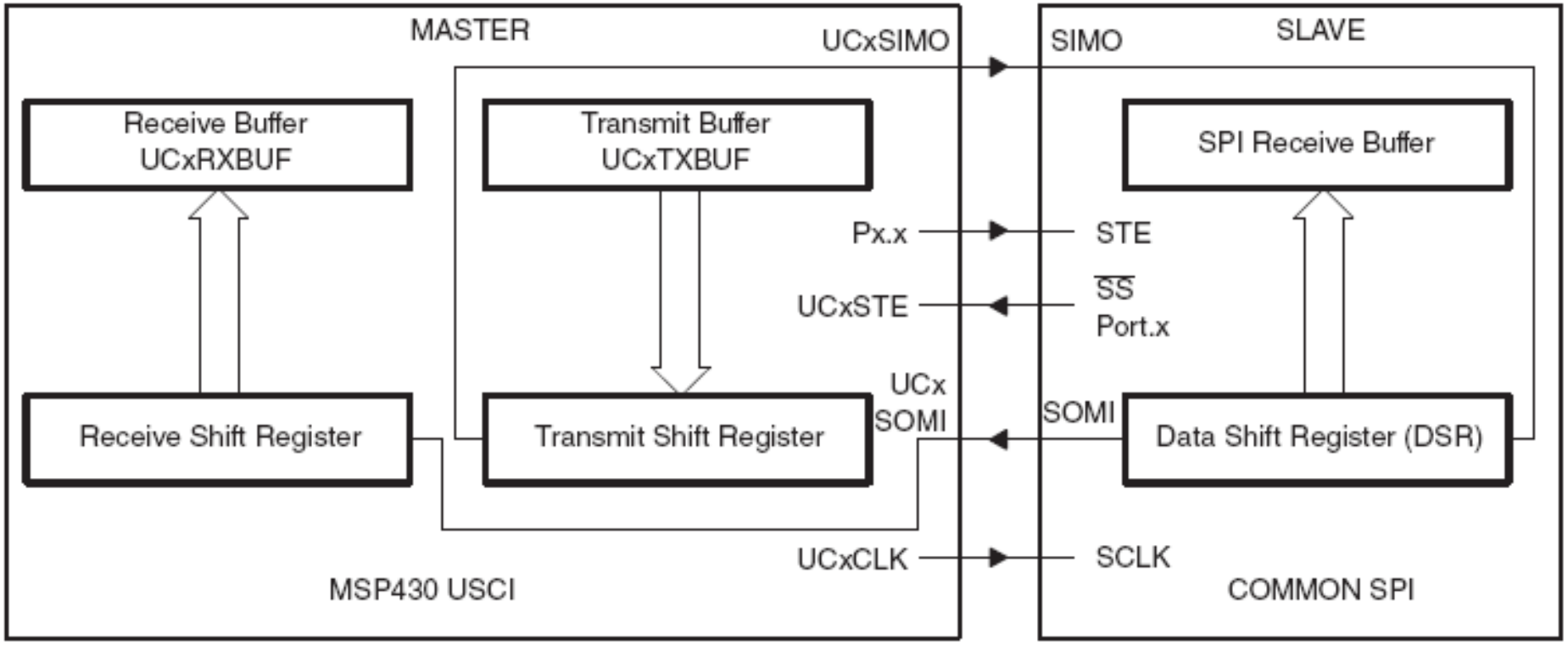
TimerB architecture

Timer_B is identical to Timer_A with the following exceptions:

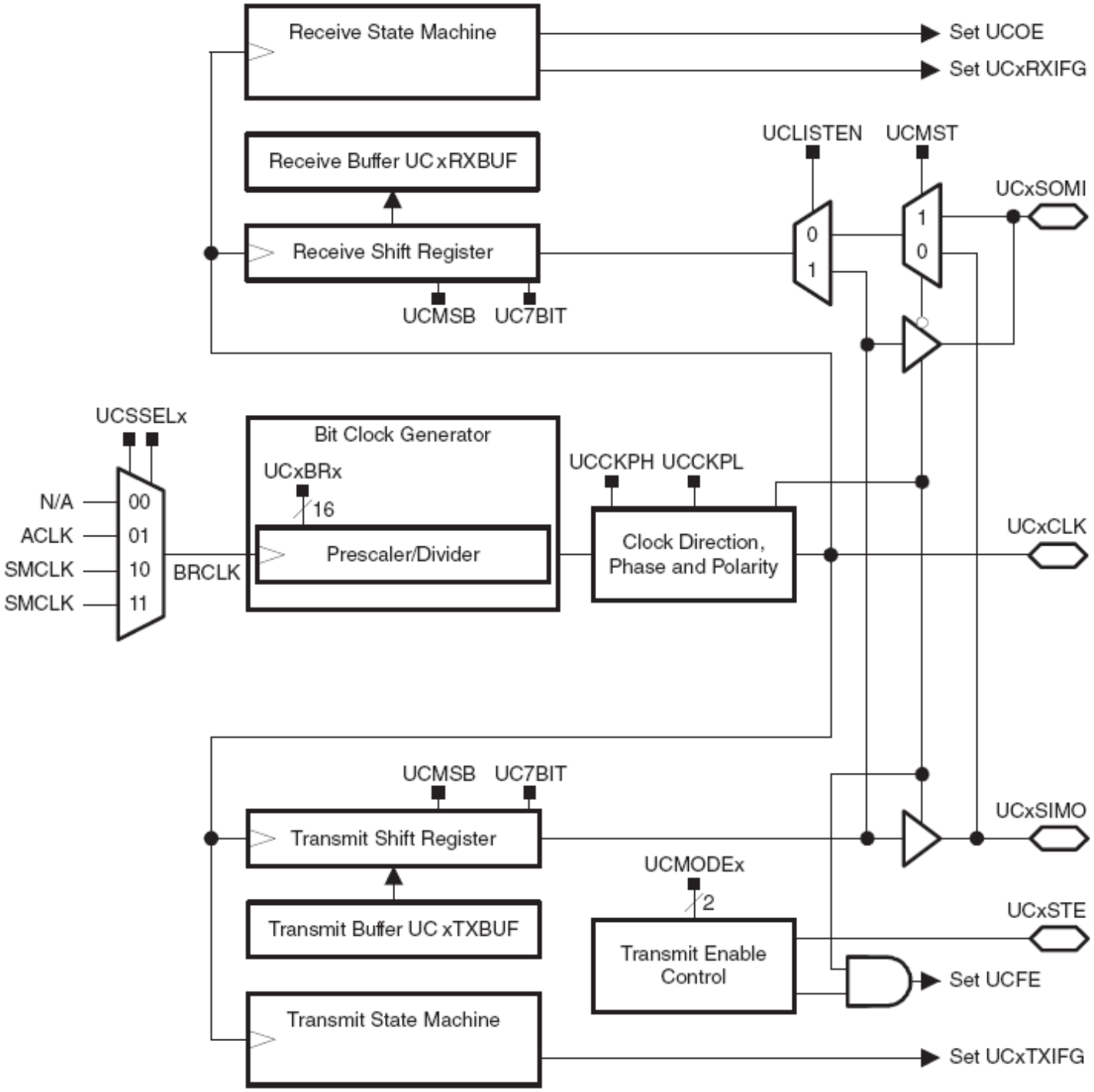
- The length of Timer_B is programmable to be 8, 10, 12, or 16 bits.
- Timer_B TBxCCRn registers are double-buffered and can be grouped.
- All Timer_B outputs can be put into a high-impedance state.
- The SCCI bit function is not implemented in Timer_B.


REFOUT
REFBURST
ADC12SR
REF2_5V
REFON
INCHx = 0Ah
on
1.5 V or2.5 V
Reference
Ref_x
INCHx
SREF1
SREF0
SREF2
ADC12OSC
(see Note A)
ADC12ON
ADC12DIVx
ADC12PDIV
ADC12SSELx
Sample
and
Hold
S/H
12-bit ADC Core
Convert
Divider
/1 .. /8
:1
:4
ACLK
MCLK
SMCLK
ADC12CLK
BUSY
SHT0x
SHP
ISSH
ENC
SHSx
Sample Timer
/4 ../1024
SHI
Sync
ADC12SC
Timer sources
(see Note B)
SAMPCON
ADC12SHTx
MSC
INCHx = 0Bh
R
CSTARTADDx
CONSEQx
ADC12MEM0
16 x 12
Memory
Buffer
ADC12MEM15
ADC12MCTL0
16 x 8
Memory
Control
ADC12MCTL15

SPI master-slave

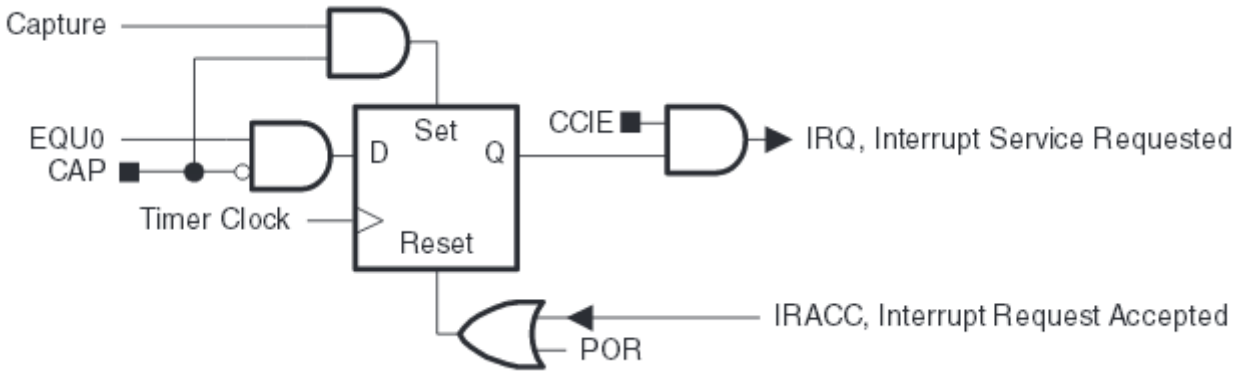


SPI


Receive State Machine
Set UCOE
Set UCxRXIFG
Receive Buffer UCxRXBUF
Receive Shift Register
UCMSB
UC7BIT
UCLISTEN
UCMST
UCxSOMI
0
1
1
0
UCSSELx
N/A
ACLK
SMCLK
SMCLK
00
01
10
11
BRCLK
Bit Clock Generator
UCxBRx
16
Prescaler/Divider
UCCKPH UCCKPL
Clock Direction, Phase and Polarity
UCxCLK
UCMSB
UC7BIT
Transmit Shift Register
UCxSIMO
UCMODEx
2
Transmit Buffer UCxTXBUF
Transmit Enable Control
UCxSTE
Set UCFE
Transmit State Machine
Set UCxTXIFG

Interrupts: Hardware model (MSP430)

- Interrupt source for CCR0



Interruption (MSP430)

```
#pragma vector=TIMER0_A1_VECTOR
__interrupt void TimerA0(void)
// source of interrupt:
    TA0CCR1:    CCIFG1
    TA0CCR2:    CCIFG2
    TA0CCR3:    CCIFG3
    TA0CCR4:    CCIFG4
    TA0CTL :    TAIFG
{
// something to do… search source with TA0IV register
    TA0CTL &= (~TAIFG);   // Clear TAIFG flag in TA0CTL register
}
```

Interruption (MSP430)

```
#pragma vector=TIMER0_A0_VECTOR
__interrupt void TimerA0_CCIFG0(void)
// source of interrupt:
    TA0CCR0:    CCIFG0
{
// something to do… only one source
     TA0CCTL0 &= (~CCIFG); // Clear CCIFG flag in
    TA0CCTL0 register, in fact done automatically
}
```

Reference (MSP430)

Texas Instrument:

- MSP430F543x_Datasheet: slas612c.pdf
- MSP430x5xx_x6xx: slau208g.pdf