Memory access
Transfers modelling
Little-Endian / Big-Endian

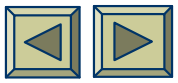
- Data Bus width byte ordering
- Transfers direction

- Little-Endian ←→ Big-Endian

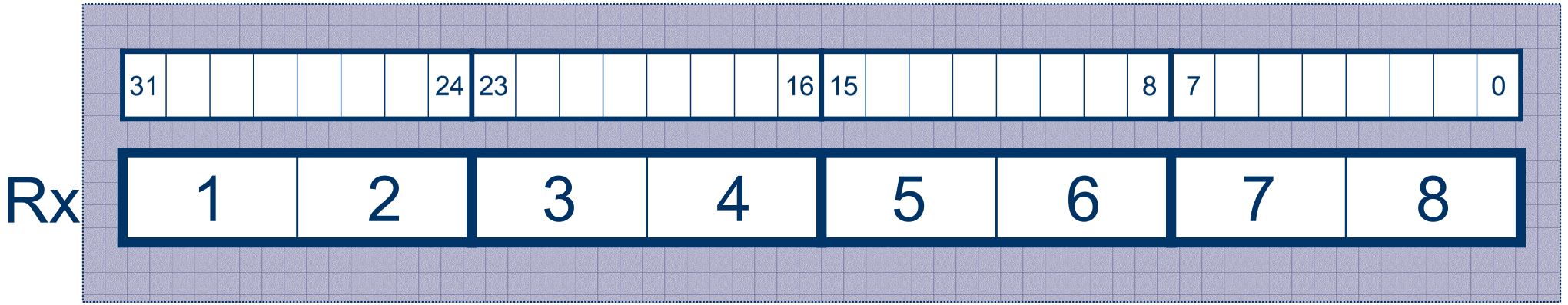
Definition

- **MSB** **M**ost **S**ignificant **B**yte
- **MSb** **M**ost **S**ignificant **b**it

- **LSB** **L**east **S**ignificant **B**yte
- **LSb** **L**east **S**ignificant **b**it



32 bits processor register



Move.Byte Rx, $1000 8 bits

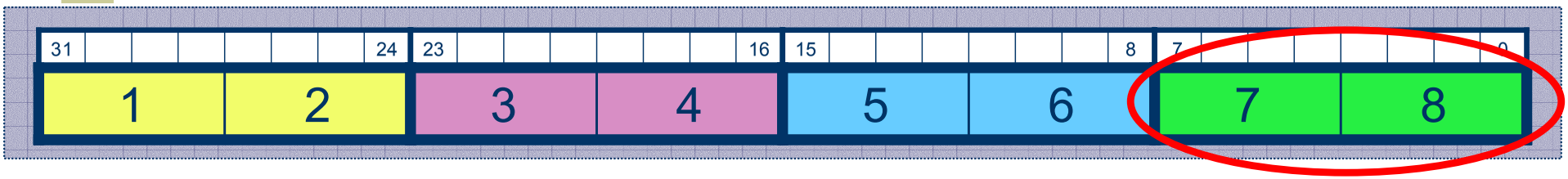
Move.Word Rx, $1000 16 bits

Move.LongWord Rx, $1000 32 bits

Transfert 8 bits

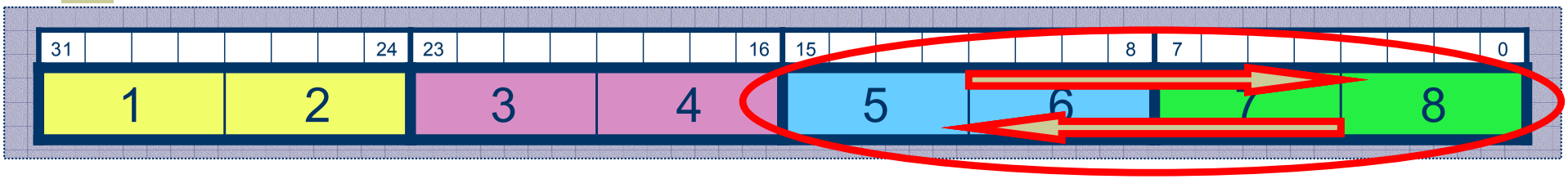
Move.B **Rx, $1000**

Rx



	8 bits memory	16 bits Memory		32 bits Memory			
		+1	+0	+3	+2	+1	+0
Little-Endian	1000 78	1000	78	1000			78
	1001	1002		1004			
	1002	1004		1008			
	1003	1006		100C			
		+0	+1	+0	+1	+2	+3
Big-Endian	1000 78	1000	78	1000	78		
	1001	1002		1004			
	1002	1004		1008			
	1003	1006		100C			

Transfert 16 bits Move.W Rx, $1000



8 bits memory | 16 bits Memory | 32 bits Memory

Little-Endian

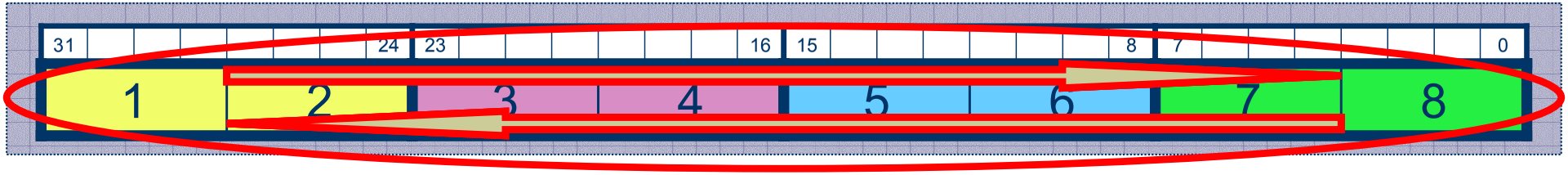
	8 bits memory	16 bits Memory (+1 +0)	32 bits Memory (+3 +2 +1 +0)
1000	78	56 78	56 78
1001	56		
1002		1002	1004
1003		1004	1008
		1006	100C

Big-Endian

	8 bits memory	16 bits Memory (+0 +1)	32 bits Memory (+0 +1 +2 +3)
1000	56	56 78	56 78
1001	78		
1002		1002	1004
1003		1004	1008
		1006	100C

Transfert 32 bits

Move.L Rx, $1000

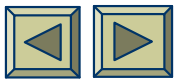


	8 bits memory		16 bits Memory			32 bits Memory			
			+1	+0		+3	+2	+1	+0
Little-Endian	1000	78	1000	56	78	1000	12	34	56	78
	1001	56	1002	12	34	1004				
	1002	34	1004			1008				
	1003	12	1006			100C				
			+0	+1		+0	+1	+2	+3
Big-Endian	1000	12	1000	12	34	1000	12	34	56	78
	1001	34	1002	56	78	1004				
	1002	56	1004			1008				
	1003	78	1006			100C				

Memory addressing

68'000 Familly

- **Big**-Endian Mode :
  - **Highest Weight at lower addresses**
  - **Memory / listing Observation : number reading from left (MSB) to right (LSB)**
  - **Ex: AB 12 34 56 → AB123456 32 bits value**



Memory addressing

x86 Familly

- **Little**-Endian Mode :
  - **Lowest Weight at lower addresses**
  - **Memory / listing Observation : number reading from right (MSB) to left (LSB)**
  - **Ex: AB 12 34 56 → 563412AB 32 bits value**