Cereon

Cereon FDC1 reference manual

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Revision history

Date	Comment
20 March 2019	Initial draft.

1 Contents

2 Introduction

This manual is a definitive specification of the Cereon FDC1 architecture and operation.

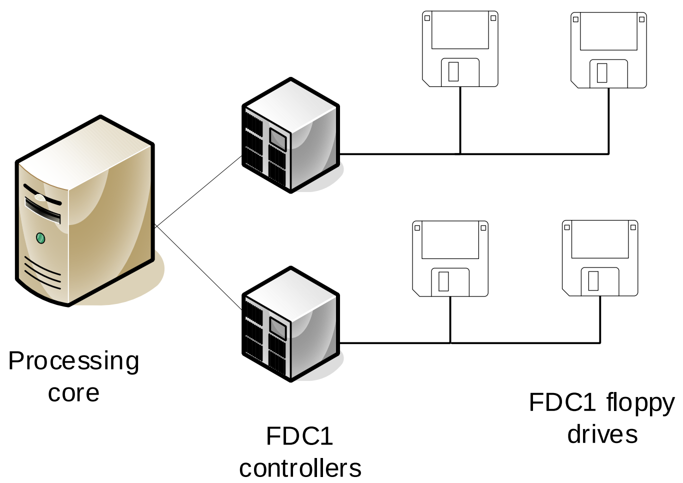
2.1 Features overview

The Cereon FDC1 (Floppy Drive Controller, version 1, henceforth referred to as simply FDC1) architecture defines a set of hardware components used for providing data storage access that uses 3” 1.44 MB floppy disks as the storage medium

All of these features are natural consequences of the main KIS1 design goal of supporting massively multi-user system configurations geared towards development and office activities.

2.2 Architecture overview

The following diagram presents a general overview of the KIS1 architecture:



Individual components of the FDC1 are explained in the following sections:

2.2.1 Processing core

This is a main processing core of a computer system, which contains main processor(s), memory, and other system components.

2.2.2 FDC1 controllers

Depending on the specific model and configuration of the computer where the FDC1 subsystem is used, FDC1 controllers can be bundled with the main processing core, connected as external devices or even bundled with FDC1 keyboards. In either case, there is no logical difference in the functions performed by FDC1 controllers – the said functions being performing storage and retrieval of data from/to 1.44MB floppy disks inserted into connected FDC1 floppy drives.

A single FDC1 controller can manage from up to 4 independent FDC1 floppy drived. Similarly, particular computer systems can be equipped with any number of FDC1 controllers. In practice, a typical system will be equipped with a single FDC1 controller that manages at most 2 FDC1 floppy drives (most high-end systems may not be equipped with an FDC1 controller at all).

2.2.3 FDC1 floppy drive

A FDC1-compatible floppy drive accepts the standard 3-inch floppy disks formatted to 1.44MB capacity (with 80 cylinders, 2 heads, 18 sectors-per-track and 512 bytes-per-sector). Other floppy disk formats are not supported.

2.3 Programming overview

As far as the main processing core is concerned, each FDC1 controller connected to the main processing core is represented by a set of registers. Writing to these registers sends commands to the FDC1 controller; similarly, reading from these registers allows the main processing core to examine the status of the FDC1 controller.

The exact means by which FDC1 controller registers are made available to the main processing core can vary from system to system. For example:

- On a system with memory-mapped I/O, registers of a particular FDC1 controller can be mapped at predefined memory addresses within the I/O memory address space.
- On a system with non-memory-mapped I/O, registers of a particular FDC1 controller can be mapped onto a predefined set of I/O ports.

The above list is not exhaustive (for example, some system may allocate a separate coprocessor for FDC1 subsystem and map FDC1 controller registers to that coprocessor’s registers, etc.) However, regardless of how FDC1 registers are presented to the main processing core, the same set of FDC1 registers is always defined for a FDC1 controller.

In the remainder of this manual, all information about programming FDC1 controllers will be given in terms of these logical FDC1 controller registers. In order to apply this documentation to a particular computer system, the programmer shall consult that computer system’s documentation in order to understand how FDC1 registers are accessed by the main processing core.

3 Programming the FDC1

This chapter describes the programmer's interface to a FDC1 subsystem.

3.1 The FDC1 controller basics

A single FDC1 controller is capable of managing up to 4 FDC1 floppy drives. Depending on the system, the actual number of available FDC1 drives can vary (including the case when there are no floppy drives).

Floppy drives managed by a given FDC1 controller are identified by their numbers in range [0..3]. At any given time, one of the floppy drives within a FDC1 controller is selected as "current" (note, that the drive does not necessarily have to exist – i.e. if an FDC1 controller manages only two floppy drives, then it is possible to select drive 0, 1, 2 or 3 as "current"; however, any attempt to perform I/O on drives 2 or 3 will fail).

3.1.1 Controller registers

Registers of a KIS1 controller are subdivided into:

- Public registers, which are used for communication between the main processing core and the KIS1 controller, and
- Private registers, which are not directly accessible to the main processing core, but must be manipulated using commands sent to the public registers.

For example, to change the LED state of a specific keyboard the program must write a new value to the private `DEVICE_STATE` register of that keyboard. Since that private register is not directly accessible by the main processing core, the goal is achieved by selecting the keyboard in question as the "current" within the controller, then writing to the `DEVICE_STATE` controller public register.

3.2 Public controller registers

This section describes public registers of a FDC1 controller. These registers are used for communications between the FDC1 controller and the main processing core.

3.2.1 STATE

The `STATE` register of a FDC1 controller is a 8-bit read-only register that reflects the current state of the controller. Any attempts of the main processing core to change the value of this register are ignored.

Individual bits within the `STATE` register have the following meaning:

Bit	Mask	Meaning
`ON`	`0x80`	1 if the FDC1 controller is operational, 0 otherwise.
`BUSY`	`0x40`	1 if the controller is busy executing a command, 0 if it is idle. An attempt to read any of the controller's public

		registers (except for STATE) while the controller is busy may result in an unpredictable value; similarly, an attempt to write to any of the controller's public registers while the controller is busy is ignored. Typically, writing to any of the controller's public registers will cause the controller to become busy for some time in order to handle the state change.
INPUT_READY	0x20	1 when the controller is ready to accept another DATA byte from the processor (in this case BUSY will always be 0).
OUTPUT_READY	0x10	1 when the controller is ready to provide another DATA byte to the processor (in this case BUSY will always be 0).
MOTD	0x08	1 if the floppy drive 3 is attached and its motor is spinning at full speed.
MOTC	0x04	1 if the floppy drive 2 is attached and its motor is spinning at full speed.
MOTB	0x02	1 if the floppy drive 1 is attached and its motor is spinning at full speed.
MOTA	0x01	1 if the floppy drive 0 is attached and its motor is spinning at full speed.

3.2.2 CONTROL

The CONTROL register is a write-only register that controls drive motors and controller configuration/reset. Any attempt to read from the CONTROL register yield an unpredictable value.

Individual bits within the CONTROL register have the following meaning:

Bit	Mask	Meaning
RESET	0x80	1 to perform the hard reset of the FDC controller; 0 for normal operation.
-	0x40	Unused
DR1,DR0	0x30	The drive (0..3) to select as "current".
MOTD	0x08	1 to turn the motor of the floppy drive 0 on, 0 to turn if off.
MOTC	0x04	1 to turn the motor of the floppy drive 0 on, 0 to turn if off.
MOTB	0x02	1 to turn the motor of the floppy drive 0 on, 0 to turn if off.
MOTA	0x01	1 to turn the motor of the floppy drive 0 on, 0 to

		turn if off.

Note that:

- When a byte with RESET bit set to 1 is written to the CONTROL register, the FDC controller (and all attached floppy drives) perform full reset. The while subsystem will not be available until a byte with RESET bit set to 0 is written to the CONTROL register.
- While selection of “current drive” is nearly instantaneous, turning drive motors on and off is not. Therefore, after using the CONTROL register to turn on one or more of the drive motors, examine the corresponding bits of the STATE register to determine when the motor reaches its full speed.

3.2.3 DATA

The DATA register is used to send commands to the controller and to read back the results of these commands.

3.2.4 INTERRUPT_MASK

The INTERRUPT_MASK register of a FDC1 controller is a 8-bit read/write register used by the FDC1 controller to determine which state change events cause I/O interrupts to be sent to the main processing core. Individual bits within this register have the following meaning:

Bit	Mask	Meaning
BUSY_OFF	0x01	When this bit is 1, a BUSY_OFF I/O interrupt occurs each time the BUSY bit of the STATE register changes from 1 to 0.
INPUT_READY_ON	0x02	When this bit is 1, an INPUT_READY_ON I/O interrupt occurs each time the INPUT_READY bit of the STATE register changes from 0 to 1.
OUTPUT_READY_ON	0x04	When this bit is 1, an OUTPUT_READY_ON I/O interrupt occurs each time the OUTPUT_READY bit of the STATE register changes from 0 to 1.
-	0xFC	Reserved for future use.

When a new value is written into the INTERRUPT_MASK register, it takes effect from the moment the controller finishes handling the write (i.e. when the BUSY flag of the STATE register becomes 0 after the write).

3.3 Issuing commands

The general sequence of issuing a command is:

1. The processor waits for the INPUT_READY bit of STATE to become 1, then write the command byte to the DATA register of the FDC.
2. If the command requires one or more parameter bytes, these are sent, in sequence, using the same technique (i.e. wait for the INPUT_READY bit of STATE to become 1, then write the next parameter byte to the DATA register). The number of parameter bytes can always be deduced from the command byte.
3. As soon as FDC notices that enough bytes have been supplied to it, it starts executing the command. For the duration of execution, the BUSY bit if STATE will be 1 and INPUT_READY and OUTPUT_READY bits will both be 0.
4. When the command has finished execution, FDC issues an interrupt and enters the result phase. At least 1 byte of the result (command status) will always be provided; for some (e.g. read) commands more than 1 byte of result will be available.
5. To read each byte of the result, wait until the INPUT_READY bit of STATE becomes 1, then read one byte from the DATA register of the FDC.

As a special case, when the FDC is in a result phase from an execution of the previous command the INPUT_READY bit if STATE is 1. This allows the processor to write the next command byte to the DATA register. If this happened, the result phase of the previous command is aborted (with unclaimed result bytes discarded) and a new command is started (this effectively executes the step (1) of the above sequence).

3.4 Interrupts

The following table summarizes I/O interrupts that can be raised by a VDS1 controller:

Name	Code	Occurs when…
BUSY_OFF	0x01	The BUSY_OFF I/O bit of the INTERRUPT_MASK register is 1 and the BUSY bit of the STATE register changes from 1 to 0.
INPUT_READY_ON	0x02	The INPUT_READY_ON I/O bit of the INTERRUPT_MASK register is 1 and the INPUT_READY bit of the STATE register changes from 0 to 1.
OUTPUT_READY_ON	0x04	The OUTPUT_READY_ON I/O bit of the INTERRUPT_MASK register is 1 and the OUTPUT_READY bit of the STATE register changes from 0 to 1.

3.4.1 Pending interrupts

A situation may occur when a FDC1 controller is ready to issue an I/O interrupt before the previous I/O interrupt issued by the same FDC1 controller has been processed by the main processing core.

In this situation, the interrupt remains pending within the I/O controller. As soon as the previous interrupt has been processed, the pending interrupt is issued.

Interrupts in an I/O controller are pending in the order in which they occurred; however, only one pending interrupt of each type can exist at any given moment.

3.5 Command status byte

The command status byte is always the first byte available for reading from the `DATA` register after a command execution has finished, successfully or otherwise.

Individual bits within the command status byte have the following meaning:

Bit	Mask	Meaning
`INVALID_COMMAND`	`0x80`	Unrecognized or invalid command byte
`INVALID_PARAMETER`	`0x40`	Unrecognized or invalid command parameter byte
`NOT_READY`	`0x20`	Drive not ready (drive absent, drive door open, no disk in drive, etc.)
`NOT_WRITABLE`	`0x10`	Floppy disk is write-protected
`SEEK_ERROR`	`0x08`	Cylinder seek error
`INVALID_CYLINDER`	`0x04`	The head is over an invalid cylinder
`DATA_ERROR`	`0x02`	Controller detected error(s) in ID or data fields of the physical floppy disk sector (e.g. CRC error, media not formatted, etc.)
`TIMEOUT`	`0x01`	The controller has received no response from the floppy drive within the required time interval

Note that several bits may be set at the same time if more than one error has been detected during the execution of the command. Only the all-zeroes command status byte signals a successful execution of the command.

3.6 Commands

This section gives detailed description of commands recognized by the FDC1 controller.

On general, the command type is determined by its 2 upper bits as follows:

- 00 – read data
- 01 – write data
- 111 – control command
- 100, 101, 110 - seek

3.6.1 Get controller status

Queries the status of the controller.

Command:

1	1	1	0	0	0	0	0

Command parameters:

None

Result phase:

- Byte 0 (always present): command status byte.
- Byte 1 (present only when byte 0 is 0, i.e. upon success):

0	0	0	0	0	0	DS1	DS0

Where:

- DS1, DS0 – the "current" drive 0..3.

3.6.2 Calibrate

"Calibrates" the "current" drive by positioning its read/write head over cylinder 0.

Command:

1	1	1	0	0	0	0	1

Command parameters:

None

Result phase:

- Byte 0 (always present): command status byte.

3.6.3 Format track

Formats the track in the "current" cylinder of the "current" drive.

Command:

1	1	1	0	0	0	1	HD

Where:

- HD == head 0 or 1.

Command parameters:

None

Result phase:

- Byte 0 (always present): command status byte.

3.6.4 Get drive status

Queries the status of the "current" drive.

Command:

1	1	1	0	0	1	0	0

Command parameters:

None

Result phase:

- Byte 0 (always present): command status byte.
- Byte 1 (present only when byte 0 is 0, i.e. upon success):

P	C	C	C	C	C	C	C

Where:
  - P – the presence indicator (1 when "current" drive is present, 0 when it is absent).
  - CCCCCCC – the "current" cylinder, 1111111 if the read/write head is "parked".

3.6.5 Park

"Parks" the "current" drive by positioning its read/write head in the special "park" area.

Command:

1	1	1	1	1	1	1	1

Command parameters:
None

Result phase:
- Byte 0 (always present): command status byte.

3.6.6 Seek

Moves the read/write head to the specified cylinder.

Command:

1	C	C	C	C	C	C	C

Where:
  - CCCCCCC == cylinder number (valid values are from 0 to 79).

Parameters
None.

Result phase:
- Byte 0 (always present): command status byte.

3.6.7 Read sector

Reads a single sector from the "current" cylinder or the "current" drive.

Command:

0	0	S	S	S	S	S	HD

Where:
  - SSSSS == sector number (valid values are 0 through 17).
  - HD == head 0 or 1.

Command parameters:
None

Result phase:

- Byte 0 (always present): command status byte.
- Bytes 1..512 (present only when byte 0 is 0x00, i.e. upon success): the actual data bytes read from the specified sector.

3.6.8 Read track

Reads a whole track (18 sectors) from the “current” cylinder or the “current” drive.

Command:

0	0	1	1	1	1	1	HD

Where:

- HD == head 0 or 1.

Command parameters:

None

Result phase:

- Byte 0 (always present): command status byte.
- Bytes 1..9216 (present only when byte 0 is 0x00, i.e. upon success): the actual data bytes read from the specified track (a sequence of 18 512-byte sectors starting with sector 0).

3.6.9 Write sector

Writes a single sector to the “current” cylinder or the “current” drive.

Command:

0	1	S	S	S	S	S	HD

Where:

- SSSSS == sector number (valid values are 0 through 17).
- HD == head 0 or 1.

Parameters

512 bytes of data to be written to the floppy disk sector.

Result phase:

- Byte 0 (always present): command status byte.

3.6.10 Write track

Writes a whole track (18 sectors) to the “current” cylinder or the “current” drive.

Command:

0	1	1	1	1	1	1	HD

Where:

- HD == head 0 or 1.

Parameters

9216 bytes of data to be written to the floppy disk sector (a sequence of 18 512-byte sectors starting with sector 0).

Result phase:

- Byte 0 (always present): command status byte.

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Version 1.2, November 2002

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