

Cereon

Cereon CMOS1 reference manual

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1 Contents

1	CONTENTS.....	3
2	INTRODUCTION.....	4
2.1	FEATURES OVERVIEW.....	4
2.2	PROGRAMMING OVERVIEW.....	4
3	PROGRAMMING THE CMOS1.....	5
3.1	THE CMOS1 CONTROLLER BASICS.....	5
3.2	CONTROLLER REGISTERS.....	5
3.2.1	<i>STATE</i>	5
3.2.2	<i>ADDRESS</i>	5
3.2.3	<i>DATA</i>	5
3.2.4	<i>INTERRUPT_MASK</i>	6
3.3	I/O INTERRUPTS.....	6
3.3.1	<i>Pending interrupts</i>	7
4	Appendix A: GNU Free Documentation License.....	8

2 Introduction

This manual is a definitive specification of the Cereon CMOS1 architecture.

2.1 Features overview

The Cereon CMOS1 architecture defines a set of hardware components that implement a small non-volatile memory used for storing persistent settings in Cereon-based workstations. The architecture has the following characteristics:

- 256 bytes of non-volatile byte-addressed memory.
- Random access to the non-volatile memory contents.
- Integrated I/O controller/device bundle.

2.2 Programming overview

As far as the main processing core is concerned, each CMOS1 controller/device bundle connected to the main processing core is represented by a set of registers. Writing to these registers sends commands to the CMOS1 controller; similarly, reading from these registers allows the main processing core to examine the status of the CMOS1 controller.

The exact means by which CMOS1 controller registers are made available to the main processing core can vary from system to system. For example:

- On a system with memory-mapped I/O, registers of a particular CMOS1 controller can be mapped at predefined memory addresses within the I/O memory address space.
- On a system with non-memory-mapped I/O, registers of a particular CMOS1 controller can be mapped onto a predefined set of I/O ports.

The above list is not exhaustive (for example, some system may allocate a separate coprocessor for CMOS1 subsystem and map CMOS1 controller registers to that coprocessor's registers, etc.) However, regardless of how CMOS1 registers are presented to the main processing core, the same set of CMOS1 registers is always defined for a CMOS1 controller.

In the remainder of this manual, all information about programming CMOS1 controllers will be given in terms of these logical CMOS1 controller registers. In order to apply this documentation to a particular computer system, the programmer shall consult that computer system's documentation in order to understand how CMOS1 registers are accessed by the main processing core.

3 Programming the CMOS1

This chapter describes the programmer's interface to a CMOS1 subsystem.

3.1 The CMOS1 controller basics

Each CMOS1 controller manages 1 block of non-volatile memory 256 bytes long. Individual bytes within that block are assigned addresses in range [0..255].

3.2 Controller registers

A CMOS1 controller has 4 1-byte registers: STATE, ADDRESS, DATA and INTERRUPT_MASK.

3.2.1 STATE

The STATE register of a CMOS1 controller is an 8-bit read-only register that reflects the current state of the controller. Any attempts of the main processing core to change the value of this register are ignored.

Individual bits within the STATE register have the following meaning:

Bit	Mask	Meaning
ON	0x01	1 if the CMOS1 controller is operational, 0 otherwise.
ADDRESS_READY	0x02	1 if the controller is ready to accept a read/write request from/to the ADDRESS register. Any attempt to read from/write to the ADDRESS register when this bit is 0 is ignored.
DATA_READY	0x04	1 if the controller is ready to accept a read/write request from/to the DATA register. Any attempt to read from/write to the DATA register when this bit is 0 is ignored.
-	0xF8	Unused bits; read as unpredictable.

3.2.2 ADDRESS

The ADDRESS register is an 8-bit read/write register that contains the address of the non-volatile memory byte that will be read or written via the DATA register. Reading from the ADDRESS register yields its current value; writing to the ADDRESS register changes that value.

3.2.3 DATA

The DATA register is a read/write register that is used to transfer actual data bytes between the main processing core and the non-volatile CMOS1 memory. Reading from the DATA register yields the byte stored in non-volatile memory at the address currently stored in ADDRESS register; writing to the DATA register causes the written

byte to be stored into the non-volatile memory at the address currently stored in ADDRESS register. Both reading and writing from/to the DATA register do not affect the value of an ADDRESS register.

3.2.4 INTERRUPT_MASK

The INTERRUPT_MASK register of a CMOS1 controller's compartment is an 8-bit read/write register used by the CMOS1 controller to determine which state change events cause I/O interrupts to be sent to the main processing core. Individual bits within this register have the following meaning:

Bit	Mask	Meaning
ADDRESS_READY_ON	0x01	When this bit is 1, an ADDRESS_READY_ON I/O interrupt occurs each time the ADDRESS_READY bit of the STATE register changes from 0 to 1.
DATA_READY_ON	0x02	When this bit is 1, a DATA_READY_ON I/O interrupt occurs each time the DATA_READY bit of the STATE register changes from 0 to 1.
-	0xFC	These bits are unused. They read as unpredictable; an attempt to write to these bits is ignored.

When a new value is written into the INTERRUPT_MASK register, it takes effect immediately. Any pending I/O interrupts are discarded.

3.3 I/O interrupts

The following table summarizes I/O interrupts that can be raised by a CMOS1 controller:

Name	Code	Occurs when...
ADDRESS_READY_ON	0x01	The ADDRESS_READY_ON I/O bit of the INTERRUPT_MASK register is 1 and the ADDRESS_READY bit of the STATE register changes from 0 to 1.
DATA_READY_ON	0x02	The DATA_READY_ON bit of the INTERRUPT_MASK register is 1 and the DATA_READY bit of the STATE register changes from 0 to 1.

3.3.1 Pending interrupts

A situation may occur when a CMOS1 controller is ready to issue an I/O interrupt before the previous I/O interrupt issued by the same CMOS1 controller has been processed by the main processing core.

In this situation, the interrupt remains pending within the I/O controller. As soon as the previous interrupt has been processed, the pending interrupt is issued.

Interrupts in an I/O controller are pending in the order in which they occurred; however, only one pending interrupt of each type can exist at any given moment.

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