**Introduction to Computing: Homework 4**

**Fall 2018**

**The University of Texas at Austin**

Due: Wednesday, October 24, 11:59pm

Instructions:

You may discuss the problem set solutions with your fellow classmates but the write-up must be your own. Please use the TAs and the Instructor for help before you seek out a friend or classmate. Show your work. You may handwrite or type-write your answers.

1. An LDR instruction, located at x3200, uses R4 as its base register. The value currently in R4 is x4011.
   1. What is the largest address that this instruction can load from?
   2. Suppose we redefine the LDR offset to be zero-extended, rather than sign-extended. Then what would be the largest address that this instruction could load from?
   3. With the new definition, what would be the smallest address that this instruction could load from?
2. (Adapted from 4.8) Suppose a 32-bit instruction has the following format:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| OPCODE | DR | SR1 | SR2 | UNUSED |

If there are 500 opcodes and 100 registers, and every register is available as a source or destination for every opcode,

1. What is the minimum number of bits required to represent the OPCODE?
2. What is the minimum number of bits required to represent the Destination Register (DR)?
3. What is the maximum number of UNUSED bits in the instruction encoding?
4. Suppose that an instruction cycle of the LC-3 has just finished and another one is about to begin. The following table describes the values in select LC-3 registers and memory locations:

|  |  |
| --- | --- |
| **Register** | **Value** |
| IR | x3000 |
| PC | x3003 |
| R1 | x3002 |
| R2 | x3003 |
| **Memory Location** | **Value** |
| x3000 | x62BF |
| x3001 | x3000 |
| x3002 | x3001 |
| x3003 | x62BE |

For each phase of the new instruction cycle, specify the values that PC, IR, MAR, MDR, R1, and R2 will have at the end of the phase in the following table:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | **PC** | **IR** | **MAR** | **MDR** | **R1** | **R2** |
| **Fetch** |  |  |  |  |  |  |
| **Decode** |  |  |  |  |  |  |
| **Evaluate Address** |  |  |  |  |  |  |
| **Fetch Operands** |  |  |  |  |  |  |
| **Execute** |  |  |  |  |  |  |
| **Store Result** |  |  |  |  |  |  |

Hint: Example 4.2 from the book illustrates the LDR instruction of the LC-3. Notice that values of memory locations x3000 and x3003 can be interpreted as LDR instructions.

4. Consider the following piece of code:

.ORIG x3000

LD R0, Addr1

LEA R1, Addr1

LDI R2, Addr1

LDR R3, R0, #-6

LDR R4, R1, #0

ADD R1, R1, #3

ST R2, #5

STR R1, R0, #3

STI R4, Addr4

HALT

Addr1 .FILL x300B

Addr2 .FILL x000A

Addr3 .BLKW 1

Addr4 .FILL x300D

Addr5 .FILL x300C

.END

Without using the simulator, answer the following questions:

* 1. Which lines of code are changed after the program terminates?
  2. What will the values of registers R0 through R4 be after the LC-3 finishes executing the ADD instruction?
  3. What will the values of memory locations Addr1 through Addr5 be after the LC-3 finishes executing the HALT instruction?

5. Consider the following piece of code:

.ORIG x3000

LEA R0, hello

ADD R0, R0, #6

LEA R1, drc

AND R2,R2, #0 ;<- A

loop ADD R3, R1, R2

LDR R4, R3, #0

ADD R5, R0, R2

STR R4, R5, #0

ADD R2, R2, #1

ADD R3, R2, #-5

BRn loop

TRAP x25

hello .STRINGZ "HELLO WORLD!\n"

drc .STRINGZ "DR. C"

* + - * 1. What are the contents of R0 and R1 after the instruction at location A is executed?
        2. Draw a memory map from x3000 to x3010, showing what hex values are stored in each memory location, after the program terminates.
        3. What does this program do?