

CSE 112: Computer Organization

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Lecture 8

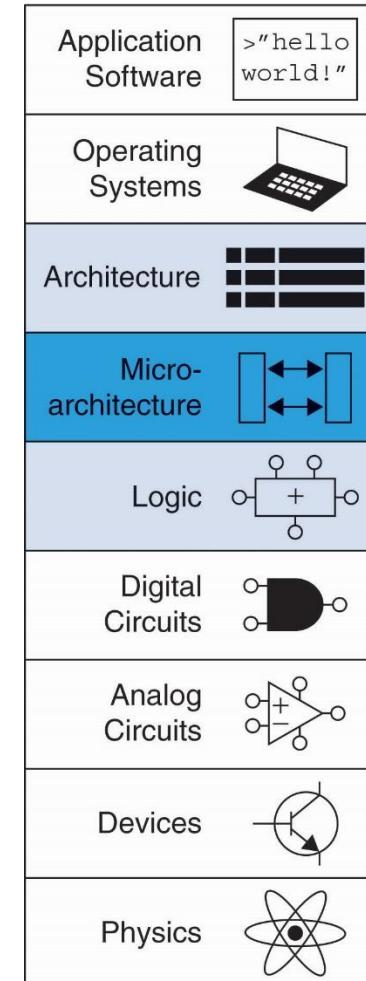


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Introduction to RISC V Microarchitecture

- **Microarchitecture:** how to implement an architecture in hardware
- Processor:
 - **Datapath:** functional blocks
 - **Control:** control signals



Microarchitecture

- **Multiple implementations** for a single architecture:
 - **Single-cycle**: Each instruction executes in a single cycle
 - **Multicycle**: Each instruction is broken up into series of shorter steps
 - **Pipelined**: Each instruction broken up into series of steps & multiple instructions execute at once

Processor Performance

- **Program execution time**

Execution Time = (#instructions)(cycles/instruction)(seconds/cycle)

- **Definitions:**

- CPI: Cycles/instruction
- clock period: seconds/cycle
- IPC: instructions/cycle = IPC

- **Challenge is to satisfy constraints of:**

- Cost
- Power
- Performance

RISC-V Processor

- Consider **subset** of RISC-V instructions:
 - R-type ALU instructions:
 - **add, sub, and, or, slt**
 - Memory instructions:
 - **lw, sw**
 - Branch instructions:
 - **beq**

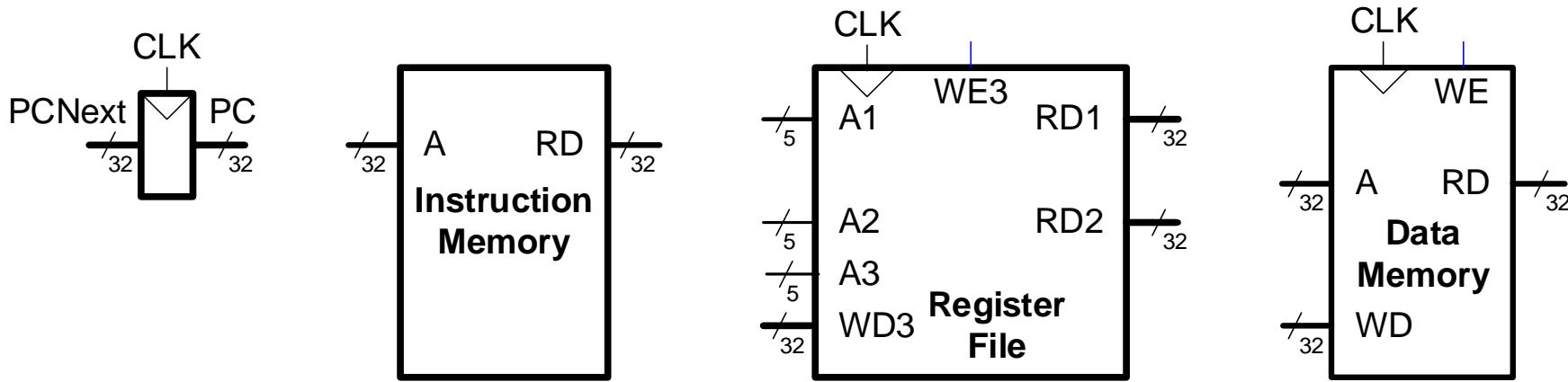
Architectural State

Determines everything about a processor:

- **Architectural state:**

- 32 registers
- PC
- Memory

RISC-V Architectural State Elements



Class Interaction # 10



Single-Cycle RISC-V Processor

Single-Cycle RISC-V Processor

- Datapath
- Control

Example Program

- Design datapath
- View example program executing

Example Program:

Address	Instruction	Type	Fields						Machine Language	
0x1000	l7: lw x6, -4(x9)	I	imm _{11:0} 111111111100	rs1 01001	f3 010	rd 00110	op 0000011	FFC4A303		
0x1004	sw x6, 8(x9)	S	imm _{11:5} 0000000	rs2 00110	rs1 01001	f3 010	imm _{4:0} 01000	op 0100011	0064A423	
0x1008	or x4, x5, x6	R	funct7 0000000	rs2 00110	rs1 00101	f3 110	rd 00100	op 0110011	0062E233	
0x100C	beq x4, x4, l7	B	imm _{12,10:5} 1111111	rs2 00100	rs1 00100	f3 000	imm _{4:1,11} 10101	op 1100011	FE420AE3	

Single-Cycle RISC-V Processor

- **Datapath:** start with `lw` instruction
- **Example:** `lw x6, -4(x9)`
`lw rd, imm(rs1)`

