CSE 112:
Computer Organization
Sujay Deb

# Quiz II | Set-A

IIIT-Delhi, Winter 2025

Duration : 60 Minutes
Date: Mar 18, 2025
Points: 30

## Guidelines

*If you found any ambiguity in any of the questions or there appears to be a lack of information, then write an assumption on the answer sheet to explain your side interpretation of the problem and solve accordingly.*

| First Block Instructions | Description | Operation |
|---|---|---|
| addi rd,rs, imm[11:0] | Add immediate | rd = rs + sext(imm[11:0]) |
| sub rd, rs1, rs2 | Subtract registers | rd = rs1 - rs2 |
| add rd, rs1, rs2 | Add registers | rd = rs1 + rs2 |
| and rd, rs1, rs2 | Add registers | rd = rs1 & rs2 |
| xor rd, rs1, rs2 | Perform XOR boolean operation | rd = rs1 xor rs2 |
| slt rd, rs1, rs2 | Set Less than | rd = 1. If signed(rs1) < signed(rs2) else rd=0 |
| sltu rd,rs1,rs2 | Set Less than unsigned | rd = 1. If unsigned(rs1) < unsigned(rs2) else rd=0 |
| beq rs1, rs2, imm[12:1] | Branch if equal | PC = PC + sext({imm[12:1],1'b0}) if rs1 == rs2 |
| **beq x0,x0,#0** | Branch if equal | **HALT** |

| Second Block Instructions | Description | Operation |
|---|---|---|
| bne rs1, rs2, imm[12:1] | Branch if not equal | PC = PC + sext({imm[12:1],1'b0}) if rs1 =! rs2 |
| bge rs1,rs2, imm[12:1] | Branch if Greater than or Equal | PC= PC + sext({imm[12:1],1'b0}) If signed(rs1) > signed(rs2) |

**[CO3] <u>Problem I: Frequency of Operation</u>** **[01+02 Points]**

We need to calculate the maximum frequency of operation for the two below-mentioned processors.

a. A single stage processor with stage delay of 5ns.
b. A Five stage processor having Fetch, Decode, Execute, Memory and Writeback and the stage delays are 7ns, 3ns, 4ns, 8ns and 4ns respectively.

**[CO2} <u>Problem II: Assembly Encoding</u>** **[10 Points]**

We need to write an assembly code to produce the below-mentioned pattern.

<u>Pattern</u>

* * * * *
**# # # #**
* * *
**# #**
*

**[CO3] <u>Problem III: MicroProcessor MicroArchitecture Design</u>** **[3x4 Points]**

A task of designing a Microarchitecture for the Microprocessor having five stages (Fetch, Decode, Execute, memory, Writeback) is assigned to us. A set of stage components of different specifications are allocated to us. We need to design 4 microprocessors of the required specifications while minimizing the microprocessor cost by using the below-mentioned stage components.

**Cost** of any **Stage** component = **40 – delay_of_this_component**.

| **Stage Components** | **(Name, Specification)** | | | |
|---|---|---|---|---|
| Fetch Component | (F_A, 4ns) | (F_A, 6ns) | (F_A, 8ns) | (F_A, 9ns) |
| Decode Component | (D_A, 2ns) | (D_A, 10ns) | (D_A, 7ns) | (D_A, 5ns) |
| Execute Component | (E_A, 3ns) | (E_A, 18ns) | (E_A, 40ns) | (E_A, 22ns) |
| Memory Component | (M_A, 20ns) | (M_A, 2ns) | (M_A, 21ns) | (M_A, 32ns) |
| Writeback Component | (W_A, 3ns) | (W_A, 25ns) | (W_A, 6ns) | (W_A, 30ns) |

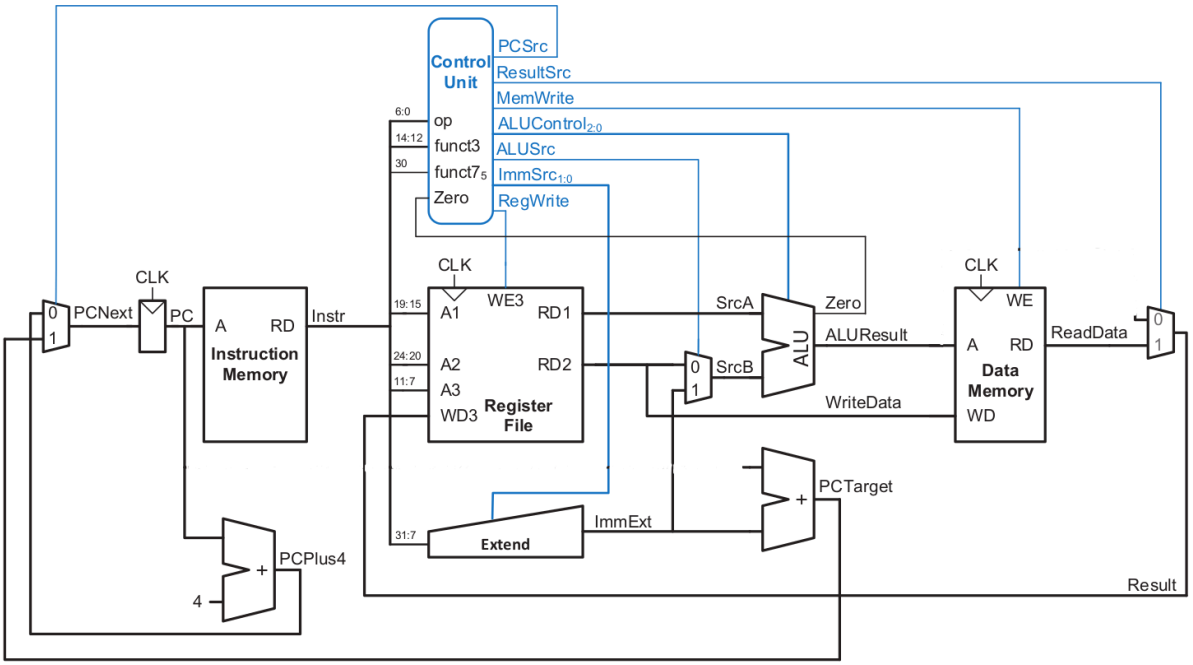
| Microprocessor | **Kamet** | **Kabru** | **Kangto** | **Langpo** |
|---|---|---|---|---|
| Specification (Maximum Operating Frequency) | 200 MHz | 50 MHz | 40 MHz | 25 MHz |

**[CO3] Problem IV: Processor MicroArchitecture** **[5 Points]**

A Instructor intentionally removed some data paths from the below-mentioned Single Cycle Processor Microarchitecture to evaluate the student's understanding.

We as students need to answer which of the below-mentioned instructions will produce functionally correct results even after removal of datapaths.

Use **YES** or **NO** for correct and incorrect functionality respectively.




Single Cycle Processor [1]

| **Instruction** | **Status** |
|---|---|
| add rd,rs1,rs2 | |
| addi rd,rs,imm[11:0] | |
| lw rs2,imm[11:0](rs1) | |
| sw rs2,imm[11:0](rs1) | |
| beq rs1,rs2,imm[12:1] | |

[1] Harris, S., & Harris, D. (2021). *Digital Design and Computer Architecture, RISC-V Edition*. Morgan Kaufmann.

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# Quiz II | Set-B

Sujay Deb

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| First Block Instructions | Description | Operation |
|---|---|---|
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| sub rd, rs1, rs2 | Subtract registers | rd = rs1 - rs2 |
| add rd, rs1, rs2 | Add registers | rd = rs1 + rs2 |
| and rd, rs1, rs2 | Add registers | rd = rs1 & rs2 |
| xor rd, rs1, rs2 | Perform XOR boolean operation | rd = rs1 xor rs2 |
| slt rd, rs1, rs2 | Set Less than | rd = 1. If signed(rs1) < signed(rs2) else rd=0 |
| sltu rd,rs1,rs2 | Set Less than unsigned | rd = 1. If unsigned(rs1) < unsigned(rs2) else rd=0 |
| beq rs1, rs2, imm[12:1] | Branch if equal | PC = PC + sext({imm[12:1],1'b0}) if rs1 == rs2 |
| jal rd,imm[20:1] | Jump and Link | rd=PC+4, PC=sext(PC+{imm[20:1],1'b0}) |
| out */ # / \|**n** | Print */ # / **newline** | No update on any CPU register. |
| **beq x0,x0,#0** | Branch if equal | **HALT** |

| Second Block Instructions | Description | Operation |
|---|---|---|
| bne rs1, rs2, imm[12:1] | Branch if not equal | PC = PC + sext({imm[12:1],1'b0}) if rs1 =! rs2 |
| bge rs1,rs2, imm[12:1] | Branch if Greater than or Equal | PC= PC + sext({imm[12:1],1'b0}) If signed(rs1) > signed(rs2) |

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We need to calculate the maximum frequency of operation for the two below-mentioned processors.

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**[CO2} Problem II: Assembly Encoding** **[10 Points]**

We need to write an assembly code to produce the below-mentioned pattern.

Pattern

```
*
# #
* * *
# # # #
* * * * *
```

**[CO3] Problem III: MicroProcessor MicroArchitecture Design** **[3x4 Points]**

A task of designing a Microarchitecture for the Microprocessor having five stages (Fetch, Decode, Execute, memory, Writeback) is assigned to us. A set of stage components of different specifications are allocated to us. We need to design 4 microprocessors of the required specifications while minimizing the microprocessor cost by using the below-mentioned stage components.

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| Writeback Component | (W_A, 3ns) | (W_A, 25ns) | (W_A, 6ns) | (W_A, 30ns) |

| Microprocessor | **Kamet** | **Kabru** | **Kangto** | **Langpo** |
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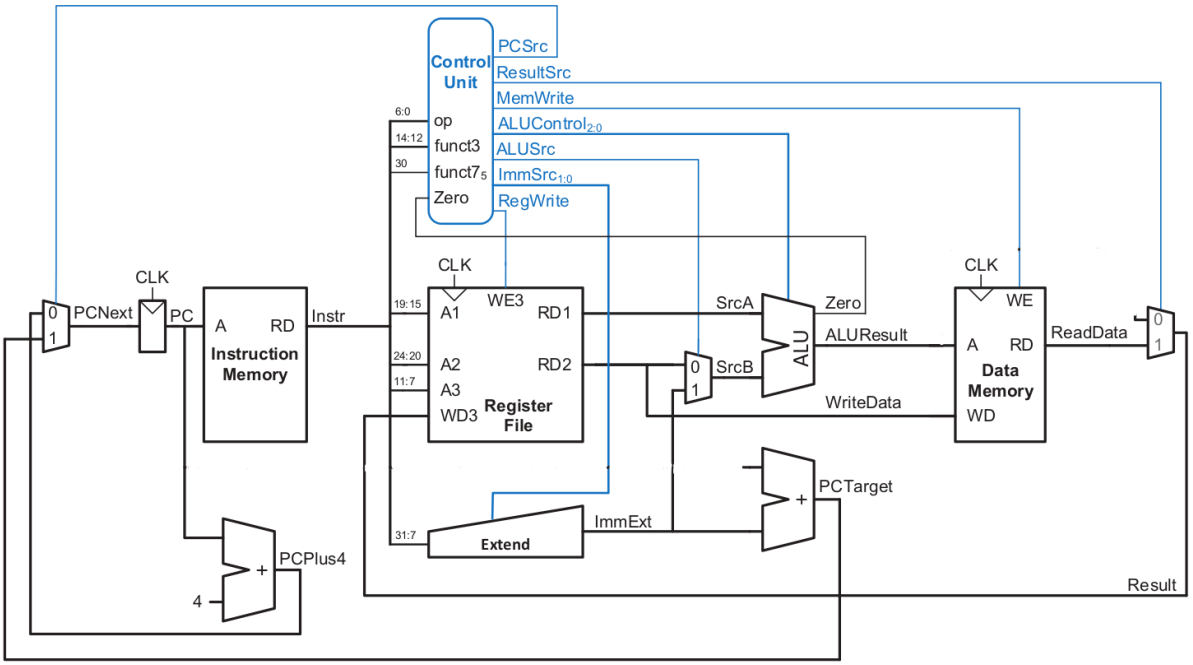


Single Cycle Processor [1]

| **Instruction** | **Status** |
|---|---|
| lw rs2,imm[11:0](rs1) | |
| sub rd,rs1,rs2 | |
| sw rs2,imm[11:0](rs1) | |
| jalr rd,x6,offset[11:0] | |
| beq rs1,rs2,imm[12:1] | |

[1] Harris, S., & Harris, D. (2021). *Digital Design and Computer Architecture, RISC-V Edition*. Morgan Kaufmann.