CSE 112: Computer Organization (Section A & B)

Instructor: Sujay Deb

Class Room: C102 & Zoom

Meeting: Tue & Thr 9:30 AM
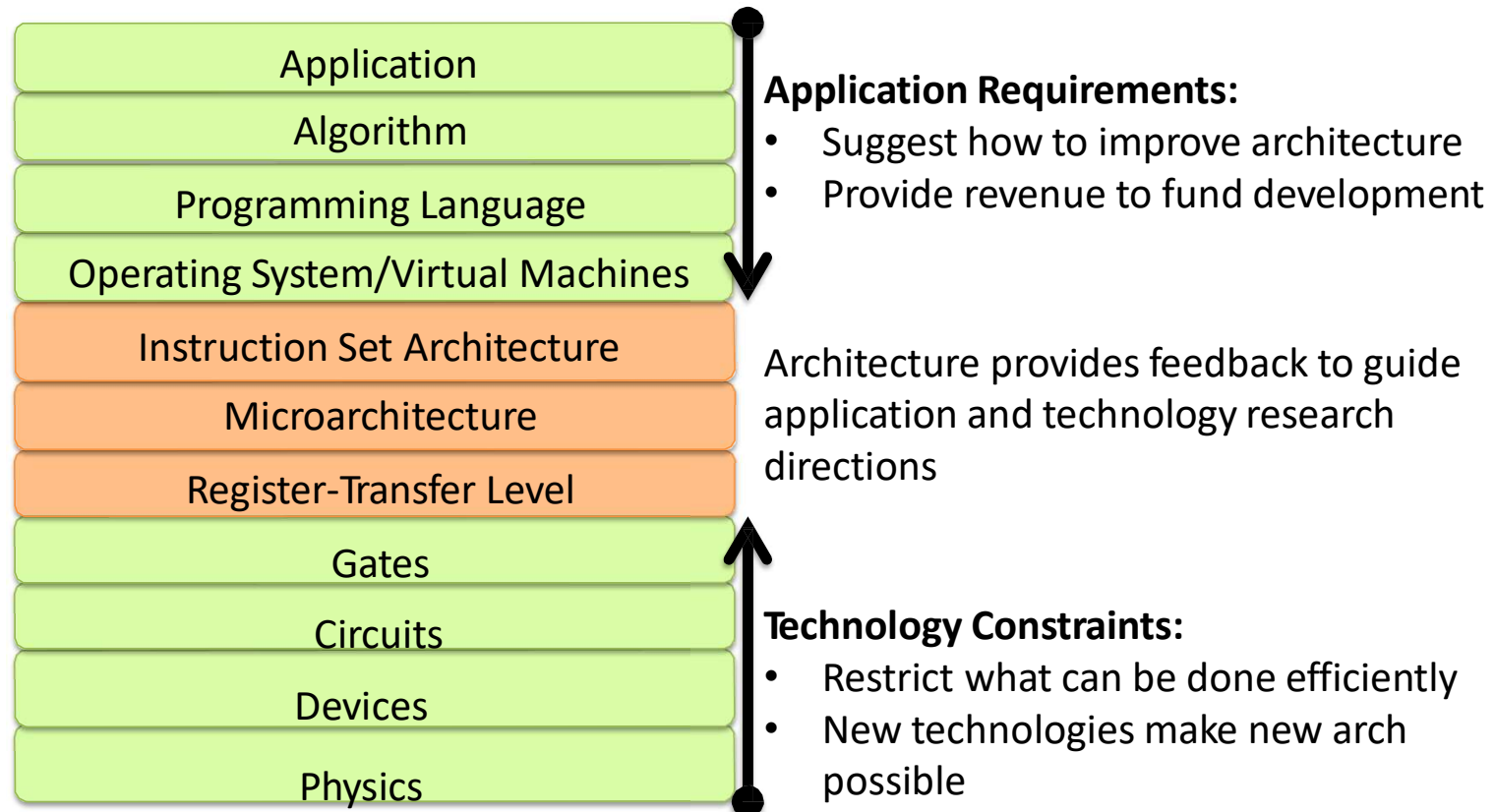
Lecture 2

INDRAPRASTHA INSTITUTE *of* INFORMATION TECHNOLOGY DELHI

AMS Lab @IIITD

Abstractions in Modern Computing Systems

Application
Algorithm
Programming Language
Operating System/Virtual Machines
Instruction Set Architecture
Microarchitecture
Register-Transfer Level
Gates
Circuits
Devices
Physics

Application Requirements:
- Suggest how to improve architecture
- Provide revenue to fund development

Architecture provides feedback to guide application and technology research directions

Technology Constraints:
- Restrict what can be done efficiently
- New technologies make new arch possible

NVIDIA and MediaTek's new Arm-based AI chip rumored for 1H 2025 to fight Intel, AMD, Qualcomm
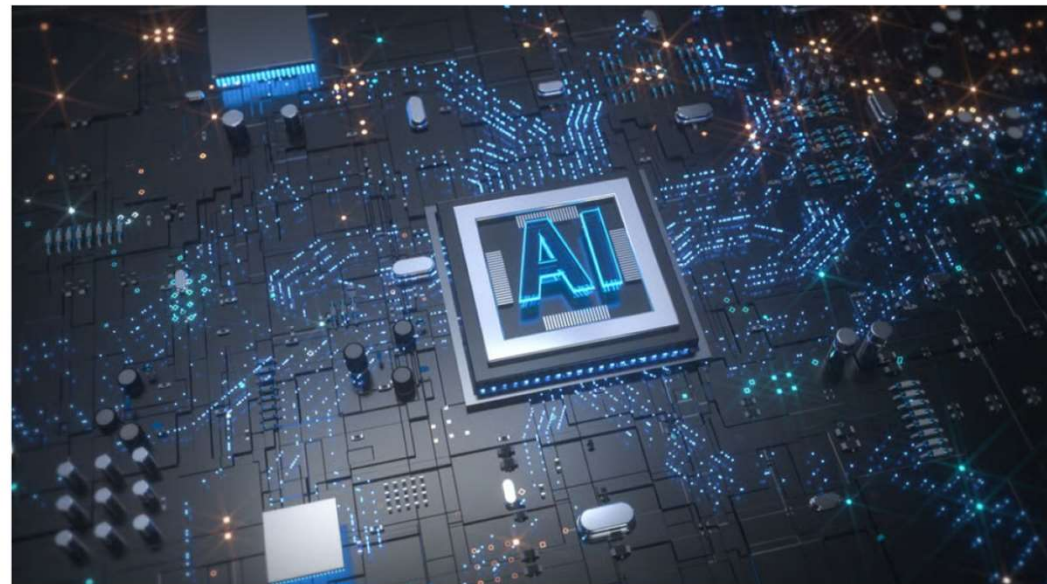
6-Core CPU, 40-

MediaTek and NVIDIA expected to unveil their Arm-based AI processor in the first half of 2025, will

By Mayank Sharma

April 23, 2024

Google and Meta unveil their Nvidia challengers

Custom AI chips can give Nvidia headaches

Meta and Google have just shown the way to take on Nvidia in the AI chips race

Meta and Google just announced their intention to push further into the AI chip race, currently dominated by Nvidia. Both companies are touting their new custom AI chips as a key element of their AI strategies.

Apple's M3 Max chip is expected to power the 14- and 16-inch MacBook Pro models in 2024.

IEEE Spectrum | Expect a Wave of Wafer

NEWS | SEMICONDUCTORS

Expect a Wave of Wafer
allows for one version no
in 2027

'Feels like magic!': Groq's ultrafast LPU could
well be the first LLM-native processor — and
its latest demo may well convince Nvidia
and AMD to get out their checkbooks

News   By Wayne Williams published 28 February 2024

onal bottlenecks

● NEWS FEED

Google's Tensor G5 processor to enter
tape-out stage, manufactured with TSMC's
3nm process

ate commission. Here's how it

News

NVIDIA plans ARM chip for laptops: A potential Apple M4 killer?

Philipp Briel   · 13. August 2024

by **TechNode Feed**   Jul 2, 2024

TSMC's wafer-scale integration tech is the key to
TESLA

Popular Posts

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  in the 400 euro segment

> Backforce One Plus review: B
  the competition look old again

> Backforce One (Plus) Discoun
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> Backforce One review: Can In
  convince with a gaming chair?

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  gaming chairs (almost) at eye

> Backforce versus SecretLab:
  versus e-sports experience

> Coupons & Discount Codes

News around u

Innovation At The 'Edge': Hardware Startup From Surat Pioneers The Reconfigurable Edge Computer — And Reshapes Computing As We Know It

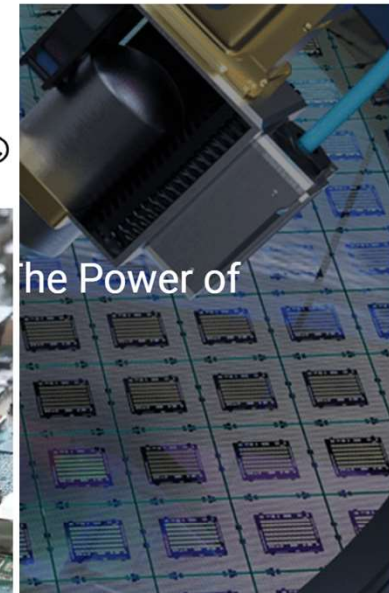KARAN KAMBLE
May 25, 2024, 02:02 PM | Updated 02:02 PM IST
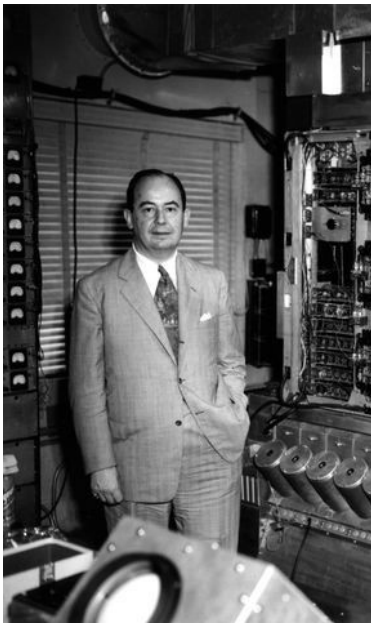
Vicharak's Vaaman edge computing board

Last month, Surat-based hardware startup Vicharak launched their very first product — an edge computing board called Vaaman.

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India is promoting the use o...
ARM technology that is ...

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The Power of

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or (DIR-V) Programme.
conductor design, instead of

Computers Then..

John von Neumann with the IAS
Levy Archives Center, Institute for Advanced Stud...

RISC V AI Chips

- RISC V adoption will be accelerated by AI

- RISC V AI Chips will be everywhere

- The flexibility, efficiency and scalability of the ISA to address specific workloads

- Vector extension to address AI

- No legacy issue

Class Interaction #2

- Link: https://forms.gle/ZsFJmmbARv9w7v5s5

Course Objectives

1. Able to explain the building blocks of processors and their working principle

2. Able to analyze concepts in assembly language and how they might be used

3. Ability to analyze pipeline and hazards related to pipeline

4. Able to explain different memory types and concepts like caches etc.

Course Description

- Introduction to computer systems
    - general overview of computer abstraction and technology

- Instruction set architecture
    - instruction type
    - format
    - operand
    - addressing mode

Course Description

- Computer arithmetic
  - addition
  - subtraction
  - multiplication and division
  - floating-point representation

- Basics of microprocessor
  - pipeline
  - datapath and control
  - data and control hazards

Course Description

- Parallelism
  - instruction level parallelism

- Memory hierarchy
  - exploiting locality using cache memory
  - virtual memory

- I/O and storage
  - performance of disk and file systems
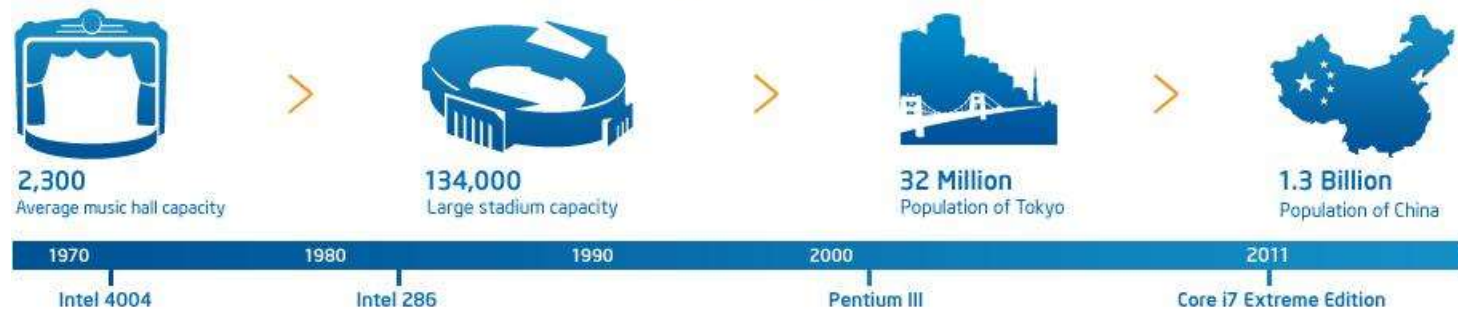
Evolution of Computing Devices

Moore's Law

VISUALIZING PROGRESS

If transistors were people

If the transistors in a microprocessor were represented by people, the following timeline gives an idea of the pace of Moore's Law.
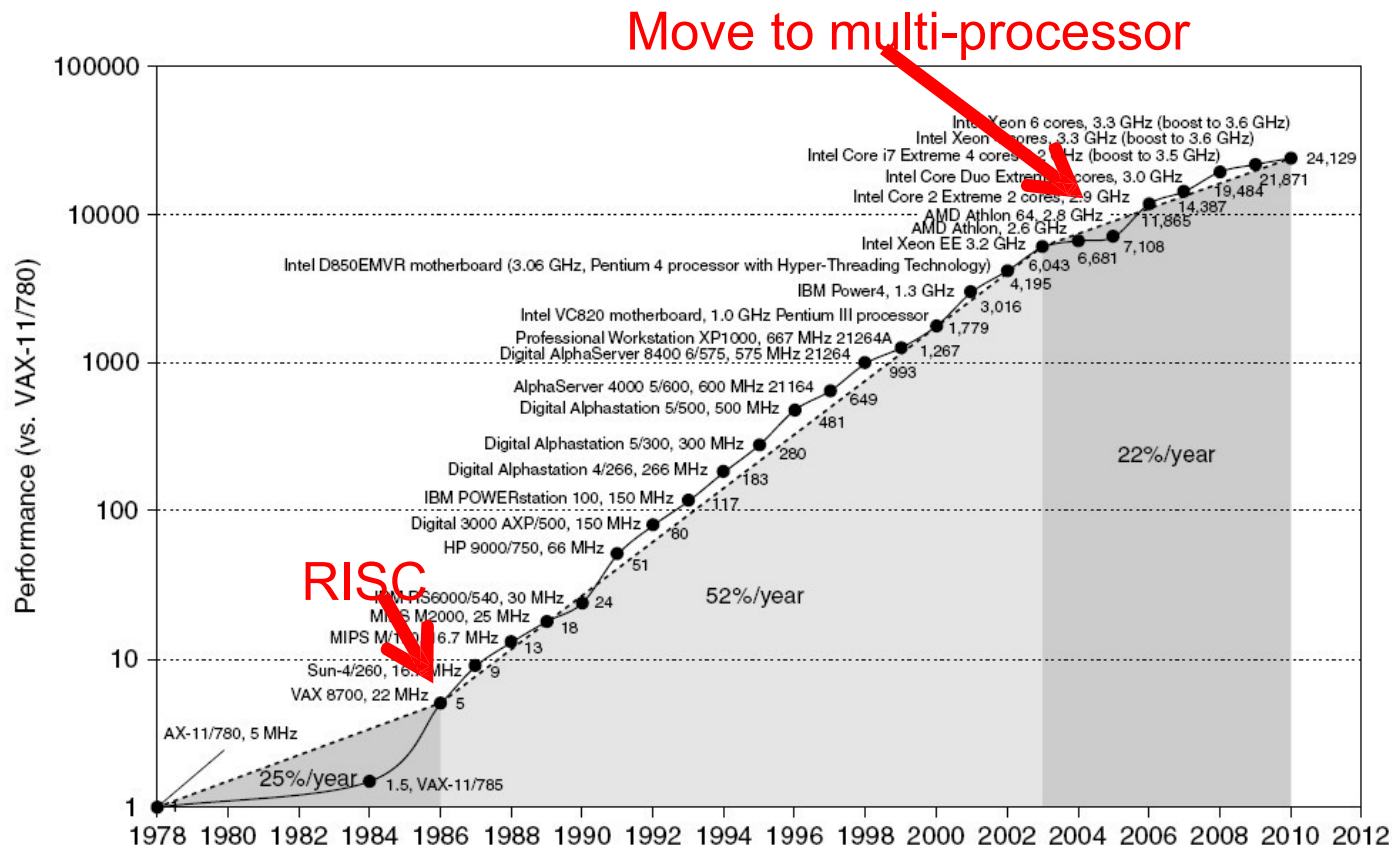
2,300
Average music hall capacity

134,000
Large stadium capacity

32 Million
Population of Tokyo

1.3 Billion
Population of China

1970	1980	1990	2000	2011
Intel 4004	Intel 286		Pentium III	Core i7 Extreme Edition

Now imagine that those 1.3 billion people could fit onstage in the original music hall. That's the scale of Moore's Law.

Courtesy:

http://www.intel.com/content/www/us/en/silicon-innovations/moores-law-technology.html

Sequential Processor Performance

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