

CSE 112: Computer Organization (Section A)

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Lecture 3



INDRAPRASTHA INSTITUTE of
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DELHI



Abstractions in Modern Computing Systems



Application Requirements:

- Suggest how to improve architecture
- Provide revenue to fund development

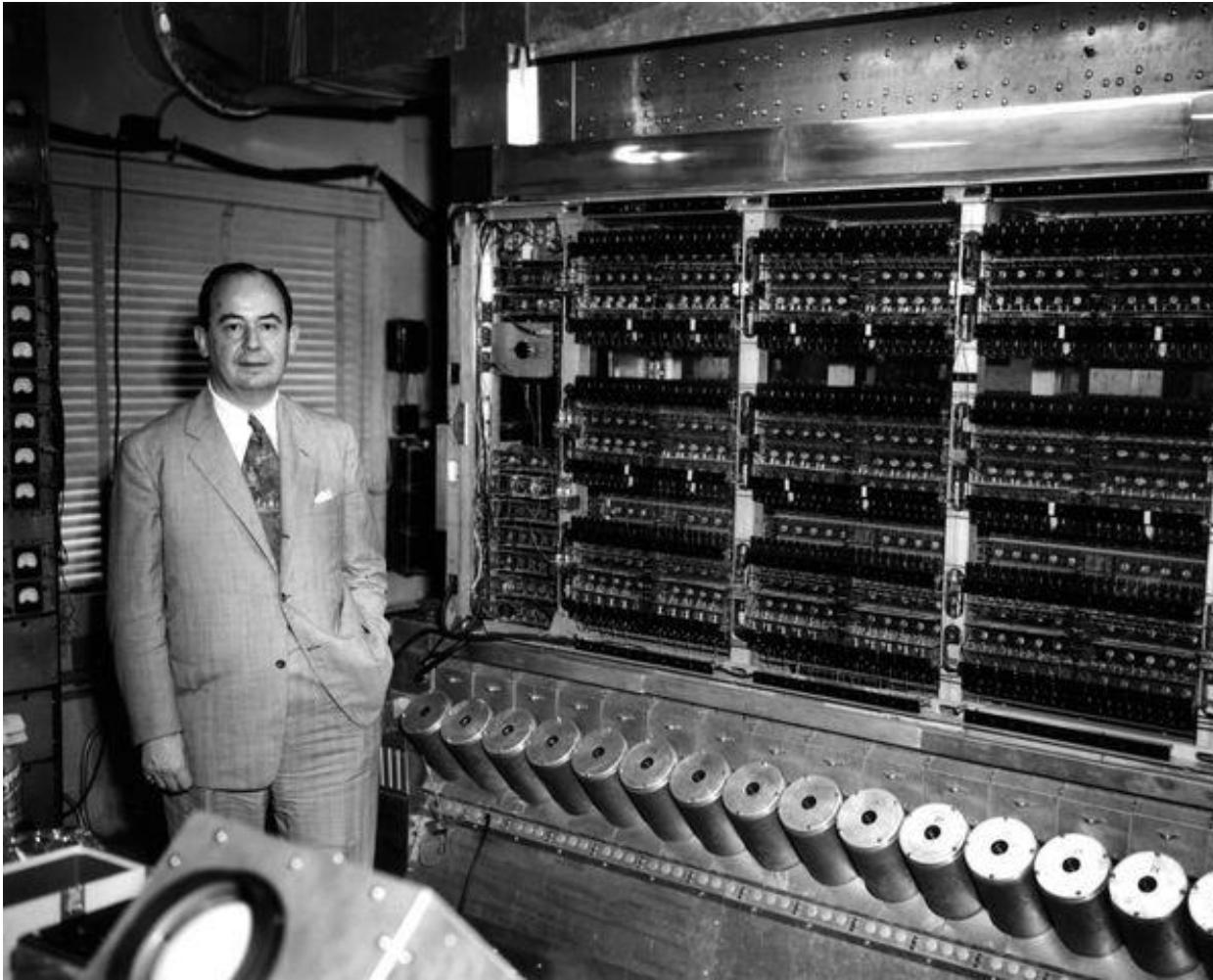


Technology Constraints:

- Restrict what can be done efficiently
- New technologies make new arch possible



Computers Then..



John von Neumann with the IAS Computer (Courtesy of the Shelby White and Leon Levy Archives Center, Institute for Advanced Study (IAS))

Computers Now



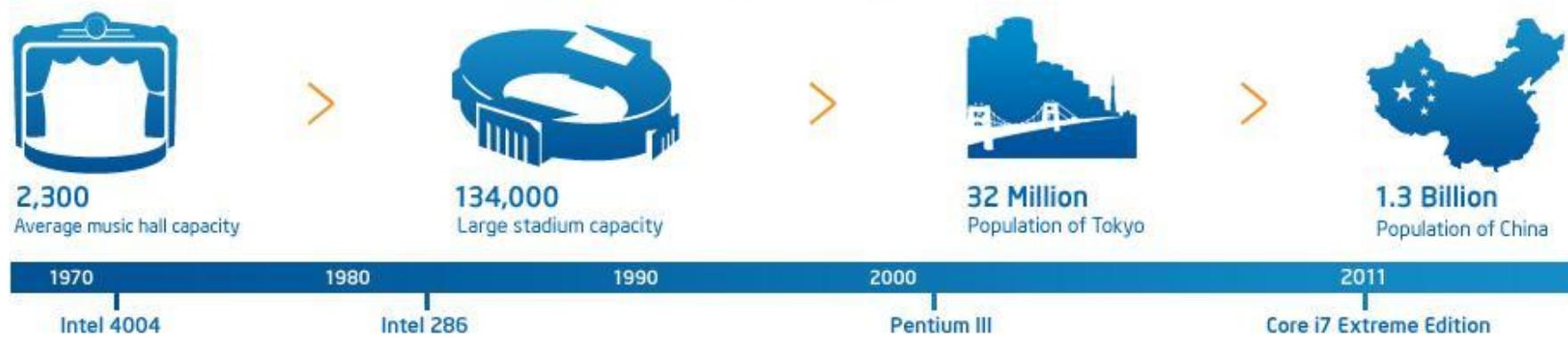
Evolution of Computing Devices



VISUALIZING PROGRESS

If transistors were people

If the transistors in a microprocessor were represented by people, the following timeline gives an idea of the pace of Moore's Law.

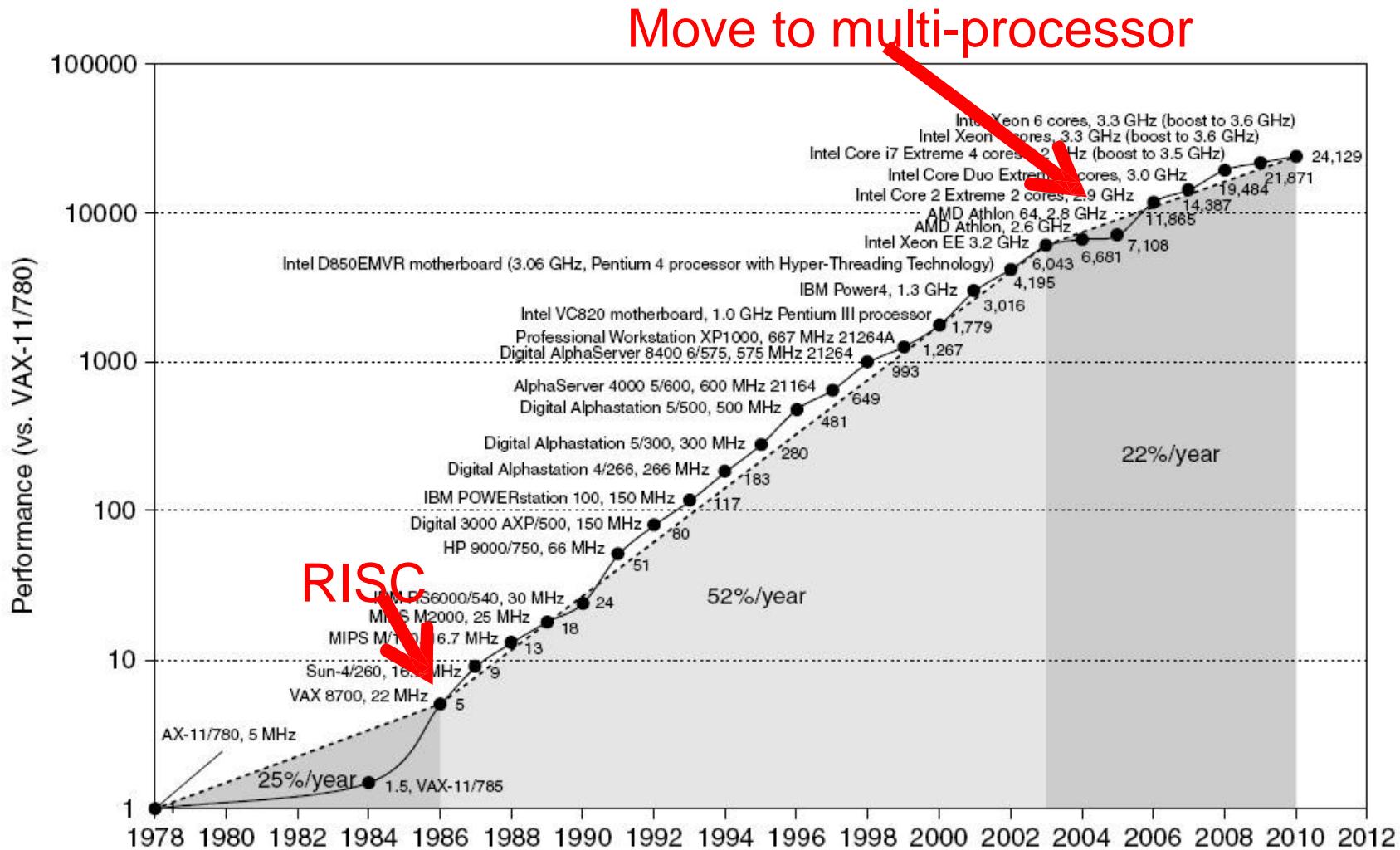


Now imagine that those 1.3 billion people could fit onstage in the original music hall. That's the scale of Moore's Law.

Courtesy:

<http://www.intel.com/content/www/us/en/silicon-innovations/moores-law-technology.html>

Sequential Processor Performance



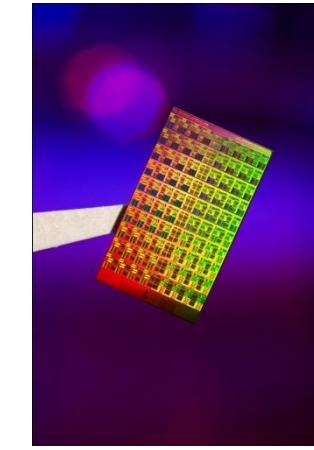
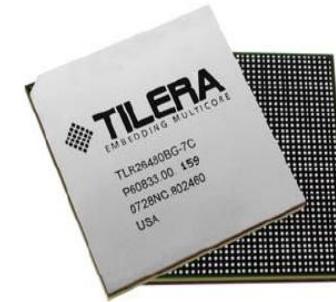
The era of Many-Core systems



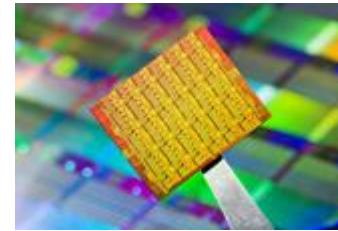
- How to keep up with demands on computational power?
 - Can not scale clock frequency
 - Solution: Increase number of cores - parallelism
 - Mass Market production of Intel, AMD dual-core and quad-core CPUs
 - Custom Systems-on-Chip (SoCs)
 - Many Core chips from Tilera for networking, cloud computing and multimedia applications.



Adapteva's
Epiphany



Intel 80 core
processor



Single-chip
Cloud
Computer

'Number of cores will double every 18 months'
- Prof. A. Agarwal, MIT, founder of Tilera Corporation

The era of Many-Core systems



- We are at the early stage of Many-core Processor evolution
 - Many-core is going to be ubiquitous
- Immense possibilities:
 - Server-type performance on handheld devices

	
ASCI Red: 1TF	Knights Corner: 1TF
1997 First System 1 TF Sustained	2011 First Chip 1 TF Sustained
9298 Pentium II Xeon	1 22nm Chip
OS: Cougar	OS: Linux
72 Cabinets	1 PCI express slot

Class Interaction # 3





Architecture vs. Organization

“Architecture”/ Instruction Set Architecture:

- Programmer visible state (Memory & Register)
- Operations (Instructions and how they work)
- Execution Semantics (interrupts)
- Input/Output
- Data Types/Sizes

Microarchitecture/ Organization:

- Tradeoffs on how to implement ISA for some metric (Speed, Energy, Cost)
- Examples: Pipeline depth, number of pipelines, cache size, silicon area, peak power, execution ordering, bus widths, ALU widths

How to Instruct a Computer ?



- Write a program in a high-level language – C, C++, Java
- **Compile** it into a format that the computer understands
- Execute the program

Instruction Set Architecture:



- The semantics of all the instructions supported by a processor is known as its instruction set architecture (ISA). This includes the semantics of the instructions themselves, along with their operands, and interfaces with peripheral devices.



Features of an ISA

- Example of instructions in an ISA
 - Arithmetic instructions : add, sub, mul, div
 - Logical instructions : and, or, not
 - Data transfer/movement instructions
- Complete
 - It should be able to implement all the programs that users may write.



Features of an ISA – II

- Concise
 - The instruction set should have a limited size.
Typically, an ISA contains 32-1000 instructions.
- Generic
 - Instructions should not be too specialized, e.g.
add14 (adds a number with 14) instruction is too
specialized
- Simple
 - Should not be very complicated.





Designing an ISA

- Important questions that need to be answered :
 - How many instructions should we have ?
 - What should they do ?
 - How complicated should they be ?

Two different paradigms : RISC and CISC

RISC
(Reduced Instruction Set Computer)

CISC
(Complex Instruction Set Computer)



RISC vs CISC

A reduced instruction set computer (**RISC**) implements simple instructions that have a simple and regular structure. The number of instructions is typically a small number (64 to 128). Examples: ARM, IBM PowerPC, RISC V

A complex instruction set computer (**CISC**) implements complex instructions that are highly irregular, take multiple operands, and implement complex functionalities. Secondly, the number of instructions is large (typically 500+). Examples: Intel x86, VAX



Summary so far ...

- Computers are dumb yet ultra-fast machines.
- Instructions are basic rudimentary commands used to communicate with the processor. A computer can execute billions of instructions per second.
- The compiler transforms a user program written in a high-level language such as C to a program consisting of basic machine instructions.
- The instruction set architecture(ISA) refers to the semantics of all the instructions supported by a processor.
- The instruction set needs to be complete. It is desirable if it is also concise, generic, and simple.