Tutorial 7
CSE 112 Computer Organisation

Q1. What are Data Path and Control Path?

Q2. What are the two basic functions of the fetch stage in a processor?

Q3. Consider a processor which consists of five stages: fetch(F), decode (D), execute (EX), memory access (MA), and register writeback (RW). Explain the role of these 5 stages.

Q4. A processor consists of five stages: Fetch, Decode, eXecute, Memory, Writeback
All instructions follow the following conventions:

```
mnemonic destination source1 source2
mnemonic destination source1
```

Draw the pipeline diagram for the following assembly programs. Assume that you have different instructions and data memories. Also, point out the number of cycles required to execute the code.

A.
```
add r1 r2 r3
add r4 r5 r6
add r7 r2 r3
add r8 r2 r5
```

B.
```
add r1 r2 r3
jmp label
add r4 r5 r6
add r7 r2 r3
add r8 r2 r5
add r10 r12 r13
label: add r14 r15 r15
```

N.B. A pipeline refers to a technique used to enhance the performance and efficiency of instruction execution. It allows multiple instructions to be processed simultaneously in a sequential manner, similar to an assembly line, where different stages of instruction execution are overlapped. TA should explain what is pipelines using examples like car factory assembly and help solve Q4.