Tutorial 9

CSE 112 Computer Organisation

Q1. Consider a four-stage pipeline with the stages, Fetch (F), Decode (D), Execute (E), and Writeback (W) following Rv32I ISA. The description of the stages is given as follows:

1. Fetch - Fetches the instructions from instruction memory
2. Decode - Decodes the instructions and type of operations. It also reads the input operands. If the input operands are not present, the decode stage is stalled to read the operands after they are made available.
    - The address of the unconditional branch is assigned to PC at the end of the decode stage.
3. Execute - Executes the instruction in the ALU
4. Writeback - Updates the register value at the end of the stage.

Considering the above stages, determine the following program's CPI (Cycles Per Instruction).

1. ADD x1, x2, x3
2. SUB x4, x1, x2
3. Jal x0, 5 // branch to instruction 5
4. SUB x5, x6, x7
5. ADD x4, x5, x6

Q2. Consider two different machines. The first has a single-stage, non-pipelined machine with a cycle time of 15 ns. The second is a pipelined machine with 5 pipeline stages and a cycle time of 3ns.

a. What is the speedup of the pipelined machine versus the single-cycle machine, assuming there are no stalls?
b. What is the speedup of the pipelined machine versus the single cycle machine if the pipeline stalls 1 cycle for 25% of the instructions?
c. Now consider a 4-stage pipeline machine with a cycle time of 3.1 ns. Again, assuming no stalls, is this implementation faster or slower than the original 5-stage pipeline? Explain your answer.

Q3. Consider a processor A with a clock frequency of 1 MHz. The processor executes one instruction per cycle.

a. Determine the clock period of processor A and the time needed to implement 197 instructions.
b. Processor A is now upgraded to a four-stage pipelined processor, say fetch [F], Decode [D], Execute [E], and Writeback [W], which have delays of 180 ns, 190 ns, 140 ns and 170 ns, respectively. The registers between the pipeline stages have a delay of 10 ns (**Note:** This time includes sequential overheads). Determine the new clock period of the upgraded processor.
c. Determine the time needed to implement 197 instructions after the upgradation of the processor. Assume no hazards are present.
d. Determine the speedup obtained by upgrading the processor [Hint: Take the ratio of time of 197 instructions obtained in parts a and c].

Q4. The 5 stages of the processor have the following latencies:

	Fetch	Decode	Execute	Memory	Writeback
1	300ps	400ps	350ps	550ps	100ps
2	200ps	150ps	100ps	190ps	140ps

Assume that when pipelining, each pipeline stage costs 20ps extra for the registers between pipeline stages. If you could split one of the pipeline stages into 2 equal halves, which one would you choose? What is the new cycle time? What is the new latency? What is the new throughput?