

Tutorial 7
CSE 112 Computer Organisation

Q1. What are Data Path and Control Path?

Ans: The data path consists of all the elements in a processor that are dedicated to storing, retrieving, and processing data such as register files, memories, and ALUs. The control path primarily contains the control unit, whose role is to generate appropriate signals to control the movement of instructions and data in the data path.

Q2. What are the two basic functions of the fetch stage in a processor?

Ans: The two basic functions of the fetch stage are:

- a. Fetching the instruction
- b. Computation of the next program counter

Q3. Consider a processor which consists of five stages: fetch(F), decode (D), execute (EX), memory access (MA), and register writeback (RW). Explain the role of these 5 stages.

Ans:

- (a) The F stage fetches the contents of the instruction, whose address is stored in the PC, and computes the next program counter (PC).
- (b) In the D stage, we decode the instruction and read its operands from the register file.
- (c) In the EX stage, we compute the address of the branch operation and perform the ALU operations.
- (d) In the MA stage, we perform loads and stores, if the instruction is not load and store, then this stage has no effect.
- (e) Lastly, in the RW stage, we write back the values computed by ALU or load instructions or the return address in the linked register for a call instruction to the register file.

Q4. A processor consists of five stages: Fetch, Decode, eXecute, Memory, Writeback

All instructions follow the following conventions:

mnemonic destination source1 source2
mnemonic destination source1

Draw the pipeline diagram for the following assembly programs. Assume that you have different instructions and data memories. Also, point out the number of cycles required to execute the code.

A. add r1 r2 r3

add r4 r5 r6
add r7 r2 r3
add r8 r2 r5

B. add r1 r2 r3

jmp label
add r4 r5 r6
add r7 r2 r3

add r8 r2 r5
 add r10 r12 r13
 label: add r14 r15 r15

Ans:

- A. 1.add r1 r2 r3
- 2.add r4 r5 r6
- 3.add r7 r2 r3
- 4.add r8 r2 r5

Instruction	1	2	3	4	5	6	7	8
add r1 r2 r3	F	D	X	M	W			
add r4 r5 r6		F	D	X	M	W		
add r7 r2 r3			F	D	X	M	W	
add r8 r2 r5				F	D	X	M	W

Number of cycles = 8

- B. 1 add r1 r2 r3
- 2 jmp label
- 3 add r4 r5 r6
- 4 add r7 r2 r3
- 5 add r8 r2 r5
- 6 add r10 r12 r13
- 7 label: add r14 r15 r15

Instruction	1	2	3	4	5	6	7	8	9
add r1 r2 r3	F	D	X	M	W	W			
jmp label		F	D	X	M				
add r4 r5 r6			F	D	nop	nop	nop		
add r7 r2 r3				F	nop	nop	nop	nop	
label: add r14 r15 r15					F	D	X	M	W

Number of Cycles = 9

N.B. a pipeline refers to a technique used to enhance the performance and efficiency of instruction execution. It allows multiple instructions to be processed simultaneously in a sequential manner, similar to an assembly line, where different stages of instruction execution are overlapped.