Tutorial 12

CSE 112 Computer Organisation

Q1. For a memory chip with 256 addresses, where each address represents a space of 8 bits, what is the address bus and data bus size required to access the whole memory? Also, how many 4-bit values can we store in the given memory chip?

Ans:

Let the size of the address bus = S

=> $2^S = 256$ address

=> $2^S = 2^8$

=> S = 8

Let the size of the data bus = D

D requires to send 1 byte of data which will be 8 bits

D = 8 bits

We can break each memory location into two 4-bit chunks. Therefore, we can store 512 4-bit values.

Q2. What will happen to the spatial locality when X increases (X>=1)?

```
for(i = 0; i < 10; i++)
        a = b[i*X];
```

Ans:

As X increases from 0 to infinity, the successive memory access for both arrays will become more spread out. The spatial distance of access will increase. This will decrease spatial locality.

For example:

X=1: The code accesses b[0], b[1], b[2] and so on as “i” goes from 0 to 9.

X=2: The code accesses b[0], b[2], b[4] and so on as “i” goes from 0 to 9.

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X=100: The code accesses b[0], b[100], b[200] and so on as “i” goes from 0 to 9.

Therefore the consecutive memory access will be farther away from each other as X increases. Hence the spatial locality will decrease as X increases.

Q3. What will happen to the temporal locality when X increases (X>=1)?

```
for(i = 0; i < 10; i++)
        for(j = 0; j < X; j++)
                a = b[j];
```

Ans:

As X increases, we access the element a[0] once every X iteration. As X increases, the temporal locality decreases.

Example

If X=1, the access pattern looks like:

b[0], b[0], b[0], ... 10 times

We access b[0] in every iteration.

If X=2, the access pattern looks like:

b[0], b[1]; b[0], b[1]; b[0], b[1]; ... 10 times

We access b[0] once every 2 iterations.

... and so on.

As X increases, the time between consecutive accesses to the same location also increases, decreasing the temporal locality.

Q4. Suppose we have L1 cache and main memory in the system. The latencies of different kinds of access are as follows:

- Cache hit - 1 cycle
- Cache miss - 105 cycles (Including the latency required to know that the access was a miss and the latency of bringing the data from memory)

When you run a program with an overall 5% miss rate. Give average memory access time in Cycles.

Ans:

Here, Hit rate = 1- miss_rate =0.95

Average Memory Access Time= hit_rate*hit_latency + miss_rate*miss_latency

=0.95 X 1 + 0.05 X 105 = 6.2 cycles

Q5. Consider a processor having byte-addressable memory with a direct mapped cache of size 16 KB with block size 256 bytes. The size of the main memory is 128 KB. Find the number of bits in tag, set index, and block offset**.**

Ans:

Given-

Cache memory size = 16 KB

Block size = Line size = 256 bytes

Main memory size = 128 KB

We have,

Size of main memory = 128 KB

$= 2^{17}$ bytes

Thus, the number of bits in the address = 17 bits

Number of Bits in Block Offset-

We have,

Block size = 256 bytes

$= 2^{8}$ bytes

Thus, the number of bits in block offset = 8 bits

Number of Bits in set Index-

Total number of lines in cache

= Cache size / line size

= 16 KB / 256 bytes

= 2^{14} bytes / 2^{8} bytes

= 2^{6} lines

Thus, the number of bits in set index = 6 bits

Number of Bits in Tag-

Number of bits in tag

= Number of bits in physical address – (Number of bits in index + Number of bits in block offset)

= 17 bits – (6 bits + 8 bits)

= 17 bits – 14 bits

= 3 bits

Thus, the number of bits in tag = 3 bits

Tag (3 bit)	Set index (6 bits)	Block Offset (8 bits)

Q6. Consider a processor with byte-addressable Main memory of size 16GB. If the block size is 16KB and the number of tag bits is 10. What is the size of cache?

Ans:

Given

Main memory size = 16GB = 2^{4} x 2^{30} B =2^{34} B

Number of bit in physical address = 34

Block Size = 16KB= 2^{4} x 2^{10} B = 2^{14} B

Block offset = 14

Then,

Number of index bit = physical address - (tag + offset)

= 34 - (10 +14) = 10

No. of cache lines (index)= 2^{10}

Cache Size = 2^{10} x 2^{14}

= 2^{24}B

= 16 MB