Tutorial 12

CSE 112 Computer Organisation

Q1. For a memory chip with 256 addresses, where each address represents a space of 8 bits, what is the address bus and data bus size required to access the whole memory? Also, how many 4-bit values can we store in the given memory chip?

Q2. What will happen to the spatial locality when X increases (X>=1)?

```
for(i = 0; i < 10; i++)
        a = b[i*X];
```

Q3. What will happen to the temporal locality when X increases (X>=1)?

```
for(i = 0; i < 10; i++)
        for(j = 0; j < X; j++)
                a = b[j];
```

Q4. Suppose we have L1 cache and main memory in the system. The latencies of different kinds of access are as follows:

- Cache hit - 1 cycle
- Cache miss - 105 cycles (Including the latency required to know that the access was a miss and the latency of bringing the data from memory)

When you run a program with an overall 5% miss rate. Give average memory access time in Cycles.

Q5. Consider a processor having byte-addressable memory with a direct mapped cache of size 16 KB with block size 256 bytes. The size of the main memory is 128 KB. Find the number of bits in tag, set index, and block offset**.**

Q6. Consider a processor with byte-addressable Main memory of size 16GB. If the block size is 16KB and the number of tag bits is 10. What is the size of the cache?