CSE 112 Computer Organization 2025: Quiz 1
(SET A)

Total Time: 60 Minutes **Maximum: 30 Points**

Instructions:
1. **Write the SET name on the top of the first page of answer script for it to get evaluated.**
2. **Mobile phones, bags, and wristwatches of any kind are NOT Permitted in the examination hall.**
3. **Write all the assumptions clearly, if any. *Only reasonable assumptions will be considered if any ambiguity is found in the question*.**
4. **Institute's plagiarism policy will apply if any unfair means are observed.**
5. **Use of calculators is permitted.**

[CO1] Q1. INSTRUCTION DECODING: [10 points]

Consider the subset of R-type instruction of RISC V ISA given below:

R-type instruction:

Format:

funct7	**rs2**	**rs1**	**funct3**	**rd**	**opcode**
[31:25]	[24:20]	[19:15]	[14:12]	[11:7]	[6:0]

funct7	**rs2**	**rs1**	**funct3**	**rd**	**opcode**	**Semantics**	**Explanation**
[31:25]	[24:20]	[19:15]	[14:12]	[11:7]	[6:0]		
0000000			000		0110011	add rd, rs1, rs2	rd = rs1 + rs2
0100000			000		0110011	sub rd, rs1 rs2	rd = rs1 - rs2.
0000000			010		0110011	slt rd, rs1, rs2	Set less than rd=1 only if signed(rs1) < signed(rs2)
0000000			011		0110011	sltu rd, rs1, rs2	Set less than unsigned rd=1 only if unsigned(rs1) < unsigned(rs2)
0000000			100		0110011	xor rd, rs1, rs2	***Bitwise Xor*** rd=rs1 ⊕ rs2
0000000			110		0110011	or rd, rs1, rs2	***Bitwise Or*** rd=rs1 | rs2
0000000			111		0110011	and rd, rs1, rs2	***Bitwise And*** rd=rs1 & rs2

We have 32 registers each of size 32-bit, these are uniquely addressed using 5-bit, we shall name as x0, x1, x2,..., x31 and the addressing is done in such a way that the address 0x0 → x0; 0x1 →x1; 0x2 →x2 and so on

Answer the following question:

A. Convert the following instruction to binary format

add x2, x3, x4
sub x7, x6, x5
xor x1, x0, x1
and x24, x12, x10
sltu x6, x1, x2

B. How many maximum number of instructions can this given ISA support?

Hint: The number of bits for the opcode, funct3, funct7 is fixed.

C. What are the minimum and maximum signed and unsigned values that can be stored in any register?

D. If this ISA supports an address space of 256 Kilobytes with byte-addressable memory. What are the minimum bits required to represent a memory address uniquely?

[CO2] Q2. Instruction Execution and Program Counter Flow [10 points]

A Processor is designed based on the ISA mentioned in question1, with each instruction encoded in 32 bits. The processor follows a byte addressable memory scheme and has 32 bits read data width. The instructions of the assembly program are stored in the contiguous memory locations.

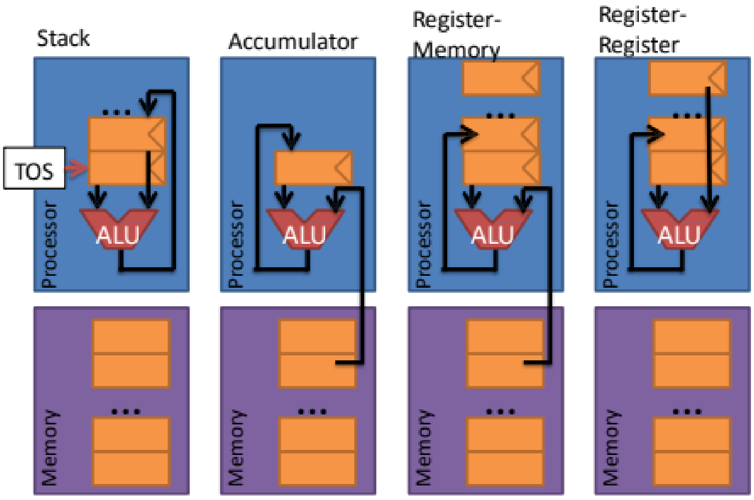
Assume all registers are initialized with their index numbers (x0 with 0, x1 with 1, x2 with 2, etc.). We need to execute the assembly program mentioned below under the three program counter-update mechanisms. Provide the values of the registers (x6, x7, x8, x9) during the execution of the program under these three mechanisms.

	Program Counter Update Mechanism		
Assembly Program	a) PC=PC+4	b) PC=PC+8	c) PC=PC+16
add x5,x6,zero			
sub x7,x6,x6			
xor x9,x9,x1			
sub x9,x9,x1			
or x7, x9, x1			
HALT			
HALT			
HALT			
HALT			

[CO1, CO2] Q3. Machine Model [7 points]

For the machine model shown below, write the assembly to perform A=C*(B+D).

Note that the ALU can do **mul, add** operations, and you have registers R1, R2, and R3 in the register model.



[CO1] Q4. Numerical: [3 points]

Propose logical conditions to detect Overflow in 2's Complement Addition and make a suitable table.

CSE 112 Computer Organization 2025: Quiz 1
(SET B)

Total Time: 60 Minutes **Maximum: 30 Points**

Instructions:

6. **Write the SET name on the top of the first page of answer script for it to get evaluated.**
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8. **Write all the assumptions clearly, if any. *Only reasonable assumptions will be considered if any ambiguity is found in the question*.**
9. **Institute's plagiarism policy will apply if any unfair means are observed.**
10. **Use of calculators is permitted.**

[CO1] Q1. INSTRUCTION DECODING: [10 points]

Consider the subset of R-type instruction of RISC V ISA given below:

R-type instruction:

Format:

funct7	**rs2**	**rs1**	**funct3**	**rd**	**opcode**
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funct7	**rs2**	**rs1**	**funct3**	**rd**	**opcode**	**Semantics**	**Explanation**
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We have 32 registers each of size 32-bit, these are uniquely addressed using 5-bit, we shall name as x0, x1, x2,..., x31 and the addressing is done in such a way that the address 0x0 → x0; 0x1 →x1; 0x2 →x2 and so on

Answer the following question:

E. Convert the following instruction to binary format

 add x2, x3, x4
 and x24, x12, x10
 xor x1, x0, x1
 sub x7, x6, x5
 sltu x6, x1, x2

F. How many maximum number of instructions can this given ISA support?

 Hint: The number of bits for the opcode, funct3, funct7 is fixed.

G. What are the minimum and maximum signed and unsigned values that can be stored in any register?

H. If this ISA supports an address space of 256 Kilobytes with byte-addressable memory. What are the minimum bits required to represent a memory address uniquely?

[CO2] Q2. Instruction Execution and Program Counter Flow [10 points]

A Processor is designed based on the ISA mentioned in question1, with each instruction encoded in 32 bits. The processor follows a byte addressable memory scheme and has 32 bits read data width. The instructions of the assembly program are stored in the contiguous memory locations.

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xor x9,x9,x1			
sub x9,x9,x1			
or x7, x9, x1			
HALT			
HALT			
HALT			
HALT			

[CO1, CO2] Q3. Machine Model [7 points]

For the machine model shown below, write the assembly to perform A=C+(B*D).

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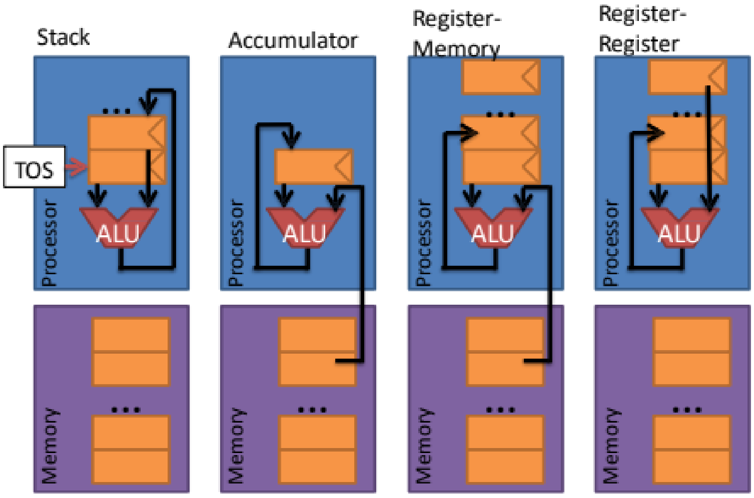

[CO1] Q4. Numerical: [3 points]

Propose logical conditions to detect Overflow in 2’s Complement Addition and make a suitable table.