CSE 112:
Computer Organization
Sujay Deb

Quiz II Rubric | Set-A

IIIT-Delhi, Winter 2025
Duration : 60 Minutes
Date: Mar 18, 2025
Points: 30

[CO3] <u>Problem I: Frequency of Operation</u> **[01+02 Points]**

We need to calculate the maximum frequency of operation for the two below-mentioned processors.

a. A single stage processor with stage delay of 5ns.
b. A Five stage processor having Fetch, Decode, Execute, Memory and Writeback and the stage delays are 7ns, 3ns, 4ns, 8ns and 4ns respectively.

<u>Solution:</u>

The maximum clock frequency is bounded by the critical path or the slowest stage delay in any digital circuit.

The maximum delay of any combinational between the two flip-flops bounds the maximum clock frequency on which the flip-flops can be operated. In processors (sequential circuits) every stage is encapsulated within flip flops. So, the processor's maximum operating frequency is determined by the slowest combinational circuit or the maximum stage delay.

a. For a single stage processor only one stage so that stage delay is the maximum delay. The correspondingly maximum clock frequency is 1/5ns=200MHz.
b. For the five stage pipelined processor the maximum stage delay is 8ns. The correspondingly maximum clock frequency is 1/8ns=125MHz.

Marking Scheme:

If the calculation is correct, award one point in part(a) and two points in part (b). If the calculation is incorrect, award zero points. We are following a binary marking scheme.

[CO2} <u>Problem II: Assembly Encoding</u> **[10 Points]**

We need to write an assembly code to produce the below-mentioned pattern.

<u>Pattern</u>

* * * * *
# # # #
* * *
# #
*

<u>Solution:</u> The key idea is. If the number is odd print * if even print #.

Assembly Program	
	addi x1,x0,#1
	addi x2,x0,#5

AGAIN:	beq x2,x0,**HALT**
	out **\n**
	and x4,x2,x1
	beq x4,x0,**EVEN**
ODD:	add x3,x2,x0
INSIDE1:	out *
	sub x3,x3,x1
	bne x3,x0,**INSIDE1**
	Jal x0,**AGAIN**
EVEN:	add x3,x2,x0
INSIDE2:	out #
	sub x3,x3,x1
	bne x3,x0,**INSIDE2**
	Jal x0,**AGAIN**
HALT:	beq x0,x0,#0

Pattern

*

# #

* * *

# # # #

* * * * *

Assembly Program	
	addi x1,x0,#1
	addi x2,x0,#5
	addi x5,x0,#1
AGAIN:	beq x2,x0,**HALT**
	out **\n**
	and x4,x2,x1

	beq x4,x0,**EVEN**
ODD:	add x3,x5,x0
INSIDE1:	out *
	sub x3,x3,x1
	bne x3,x0,**INSIDE1**
	addi x5,x5,#1
	sub x2,x2,x1
	Jal x0,**AGAIN**
EVEN:	add x3,x5,x0
INSIDE2:	out #
	sub x3,x3,x1
	bne x3,x0,**INSIDE2**
	addi x5,x5,#1
	sub x2,x2,x1
	Jal x0,**AGAIN**
HALT:	beq x0,x0,#0

Marking Scheme:

1. If the logic and pattern is correct and the algorithm is designed using the mentioned instructions only award 10 points.
2. If the logic and pattern is correct but any instruction out of the above-mentioned is used. Then deduct 2 points or award 8/10.
3. If the logic and pattern is correct but with incorrect dimension size. Or, say instead of five lines four/six lines are being printed. But still in the above-mentioned format deduct 3 points or award 7/10.
4. The other cases will be awarded with zero marks.

[CO3, CO4] <u>Problem III: MicroProcessor MicroArchitecture Design</u> [3x4 Points]

A task of designing a Microarchitecture for the Microprocessor having five stages (Fetch, Decode, Execute, memory, Writeback) is assigned to us. A set of stage components of different specifications are allocated to us. We need to design 4 microprocessors of the required specifications while minimizing the microprocessor cost by using the below-mentioned stage components.

Cost of any **Stage** component = **40 – delay_of_this_component**.

Stage Components Specification Table

Stage Components	**(Name, Specification)**			
Fetch Component	(F_A, 4ns)	(F_A, 6ns)	(F_A, 8ns)	(F_A, 9ns)
Decode Component	(D_A, 2ns)	(D_A, 10ns)	(D_A, 7ns)	(D_A, 5ns)
Execute Component	(E_A, 3ns)	(E_A, 18ns)	(E_A, 40ns)	(E_A, 22ns)
Memory Component	(M_A, 20ns)	(M_A, 2ns)	(M_A, 21ns)	(M_A, 32ns)
Writeback Component	(W_A, 3ns)	(W_A, 25ns)	(W_A, 6ns)	(W_A, 30ns)

Microprocessor Specification Table

Microprocessor	**Kamet**	**Kabru**	**Kangto**	**Langpo**
Specification (Maximum Operating Frequency)	200 MHz	50 MHz	40 MHz	25 MHz

Solution:

We just need to choose the slowest stage component which is responsible for critical path or restricting the maximum frequency.

The Logic is this:

Maximum_Delay_of_the_critical_stage_component <=
1 / Maximum_desired_frequency_of_processor

We want to choose the cheapest stage component or the stage component having maximum delay. But, we can not go beyond the Maximum_Delay_Calculated above for any stage component**.**

	Kamet	**Kabru**	**Kangto**	**Langpo**
Max Stage Delay	5ns	20ns	25ns	40ns
Fetch Component	(F_A, 4ns)	(F_A, 9ns)	(F_A, 9ns)	(F_A, 9ns)
Decode Component	**(D_A, 5ns)**	(D_A, 10ns)	(D_A, 10ns)	(D_A, 10ns)
Execute Component	(E_A, 3ns)	(E_A, 18ns)	(E_A, 22ns)	**(E_A, 40ns)**
Memory Component	(M_A, 2ns)	**(M_A, 20ns)**	(M_A, 21ns)	(M_A, 32ns)
Writeback Component	(W_A, 3ns)	(W_A, 6ns)	**(W_A, 25ns)**	(W_A, 30ns)
Total Delay	17ns	63ns	87ns	121ns
Cost	40*5 - 17	40*5 - 63	40*5 - 87	40*5 - 121
	183 Units	137 Units	113 Units	79 Units

Note:

The red marked component was a typographical error. The **correct** component is **(F_A, 9ns).**

Marking Scheme:

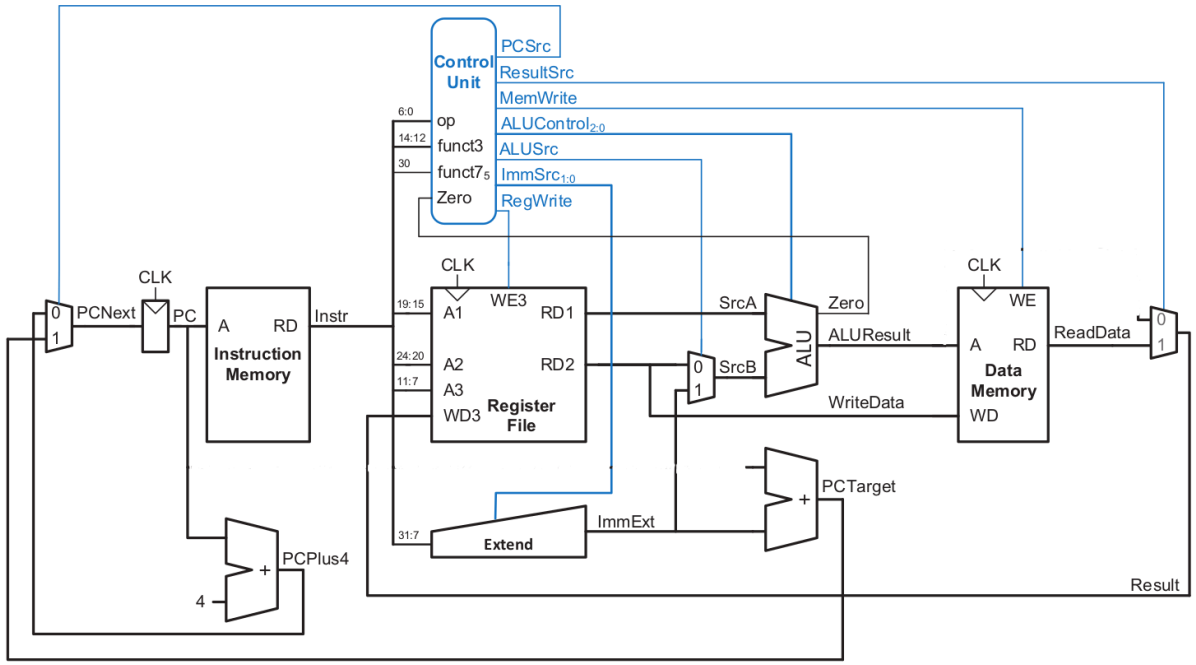
1. The magenta component is the critical one. If the magenta component is chosen correctly, award one mark. If the magenta component is chosen incorrectly, award zero points for that processor.
2. After the choice of magenta component, if other components are chosen correctly, award two further points, else zero point for the rest portion or 1/3 for one processor.
3. It's not explicitly asked. So, no deduction of points here. If cost calculation is Exact, award one point else zero point. No partial marking for design of the processor using correct components but incorrect cost calculation.

[CO3] Problem IV: Processor MicroArchitecture **[5 Points]**

A Instructor intentionally removed some data paths from the below-mentioned Single Cycle Processor Microarchitecture to evaluate the student's understanding.

We as students need to answer which of the below mentioned instructions will produce functionally correct results even after removal of datapaths.

Use **YES** or **NO** for correct and incorrect functionality respectively.



Single Cycle Processor [1]

Instruction	Status
add rd,rs1,rs2	NO
addi rd,rs,imm[11:0]	NO
lw rs2,imm[11:0](rs1)	YES
sw rs2,imm[11:0](rs1)	YES
beq rs1,rs2,imm[12:1]	NO
sub rd,rs1,rs2	NO
jalr rd,x6,offset[11:0]	NO

Marking Scheme:

If the choice is correct, award one point else 0 point. The marking is completely binary.

[1] Harris, S., & Harris, D. (2021). *Digital Design and Computer Architecture, RISC-V Edition*. Morgan Kaufmann.

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c. A single stage processor with stage delay of 5ns.
d. A Five stage processor having Fetch, Decode, Execute, Memory and Writeback and the stage delays are 7ns, 4ns, 5ns, 6ns and 8ns respectively.

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The maximum clock frequency is bounded by the critical path or the slowest stage delay in any digital circuit.

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[CO2} Problem II: Assembly Encoding **[10 Points]**

We need to write an assembly code to produce the below-mentioned pattern.

Pattern

```
*
# #
* * *
# # # #
* * * * *
```

One Possible Assembly Program	
	addi x1,x0,#1
	addi x2,x0,#5

	addi x5,x0,#1
AGAIN:	beq x2,x0,**HALT**
	out **\n**
	and x4,x2,x1
	beq x4,x0,**EVEN**
ODD:	add x3,x5,x0
INSIDE1:	out *
	sub x3,x3,x1
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EVEN:	add x3,x5,x0
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	sub x3,x3,x1
	bne x3,x0,**INSIDE2**
	addi x5,x5,#1
	sub x2,x2,x1
	Jal x0,**AGAIN**
HALT:	beq x0,x0,#0

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Execute Component	(E_A, 3ns)	(E_A, 18ns)	(E_A, 22ns)	**(E_A, 40ns)**
Memory Component	(M_A, 2ns)	**(M_A, 20ns)**	(M_A, 21ns)	(M_A, 32ns)
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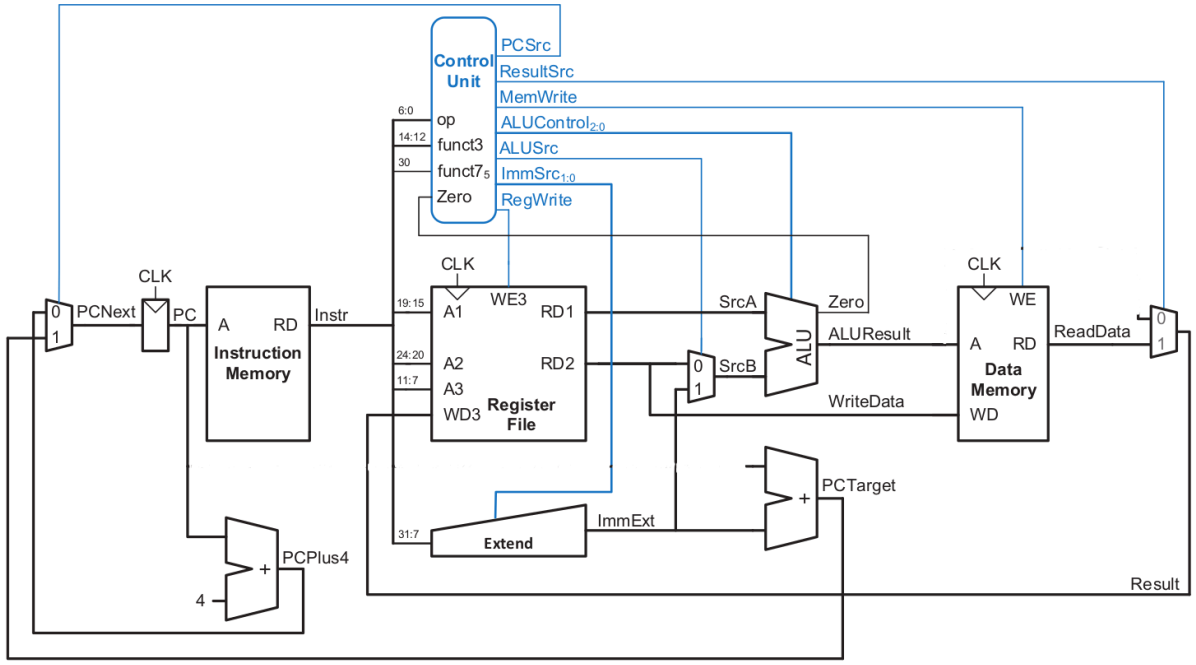

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