IMPLEMENTATION OF HIGH SPEED 3-BIT FLASH TYPE ANALOG TO DIGITAL CONVERTER (ADC)

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Abstract —
ADC is an integral component of any electronic circuit which converts continuous time continuous amplitude analog signal into continuous time discrete amplitude digital signal. Among all the types of ADCs, flash type or direct conversion ADC is considered as the high speed ADC. This paper describes the circuit implementation & simulation of flash type ADC

Keywords — **Flash, Comparator, Encoder**

I. INTRODUCTION

A flash ADC uses linear voltage ladder with comparators at every stage which compares the input voltage with successive reference voltages which gives output in terms of 0 or 1 i.e. in digital form. Comparing with other types of ADC, flash ADC requires only single clock cycle for conversion, hence it is called as high speed ADC among all.
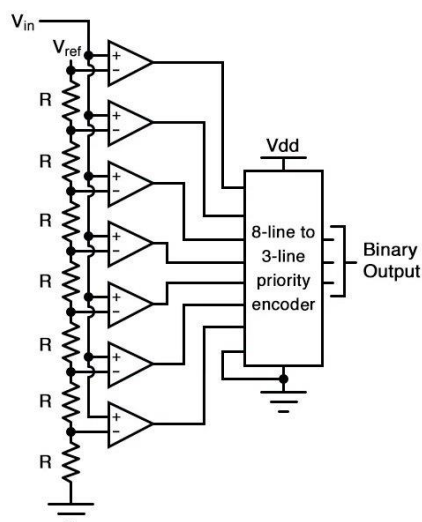
II. PROPOSED CIRCUIT DIAGRAM

Fig.1 : 3-Bit Flash type ADC

At every resistor ladder tap, the voltages are created as $7Vref/8$, $6Vref/8$ upto $1Vref/8$ respectively from top to bottom, connected to inverting terminal of opamp at every stage. These voltages are compared with input analog voltage and output of the opamp will be either Vsat or 0 which is represented as digital 1 & 0 respectively. These signals are provided to a 8:3 priority encoder which converts the digital data in binary format.

Resolution is one of the important design constraint of any ADC. It basically indicates the smallest incremental change in input to which output can respond. In the proposed design, we are keeping Vref as 5V, hence resolution of proposed ADC design is calculated by the formula :

$$Resolution = \frac{Reference\ Voltage}{2^n} = \frac{5}{2^3} = 0.625V$$

Where, n is the number of output binary bits.

For methodology, I have plan to write a verilog code for 8:3 encoder which will acts as digital block in the design. Rest of the components (resistor & opamp) will be designed in analog domain to combinely form a mixed signal design.
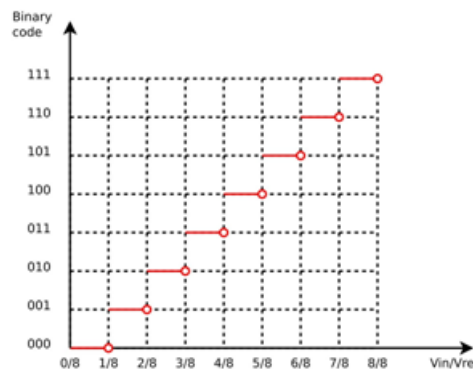
III. EXPECTED WAVEFORMS

Fig.2 : Expected Waveforms

Here, we can see from the DC characteristics, each step size for binary output code is equivalent to 0.7142V ($Vref/2^n-1$). Also, on X-axis, the ratio of Vin/Vref will result in multiples of resolution i.e. 0.625V.

IV. REFERENCES

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