A Term Paper on

PVT ANALYSIS OF CURRENT MIRROR CIRCUITS AT 90nm PROCESS TECHNOLOGY NODE

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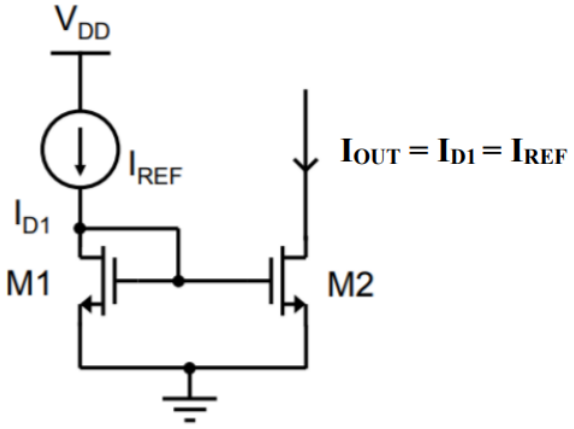
ABSTRACT

Current mirror is a fundamental unit, widely used for current amplification biasing and active load in various analog/mixed mode integrated circuits. Its efficient design plays a major role in deciding the overall performance of these circuits. This paper has proposed the extraction of performance parameters of various current mirror circuits and their comparative analysis like accuracy, input resistance, output resistance and bandwidth etc. The discussed circuits have been simulated using Cadence Virtuoso Tool at 90nm process technology node with supply voltage of 1V.

WORKING PRINCIPLE OF CURRENT MIRROR

A current mirror is a circuit designed to copy a current through one active device by controlling the current in another active device of a circuit, keeping the output current constant regardless of loading. The current being "copied" can be, and sometimes is, a varying signal current. Conceptually, an ideal current mirror is simply an ideal inverting current amplifier that reverses the current direction as well. Or it can consist of a current-controlled current source (CCCS). The current mirror is used to provide bias currents and active loads to circuits. It can also be used to model a more realistic current source (since ideal current sources don't exist).



In analog IC design, current mirror structure is one of the most used concepts. It is commonly used to replicate current from one branch of the circuit to another, but it can also be used as a biasing network or as a “pseudo” current source. In fig. 1, M1 and M2 are MOSFETs with samearea process, and V_{GS}, I_{REF} is the current we are trying to mirror and I_{out} is the mirrored current. Since the gate of M1 and M2 are shorted, both MOSFETs experience the same Vov, V_{GS}-V_{TH}. Operation of current mirrors is based on the governing equation of MOSFET current in saturation. Based on the $I_{d,sat}$, one can see that the current is modeled by the square of overdrive voltage, $V_{OV} = V_{GS} – V_{TH}$. The first-order operation of a current mirror can be realized as two MOSFET with same process and overdrive voltage, then the current flowing through the MOSFETs should be equivalent if they have the same width and length as shown in Eq. 3, assuming

negligible channel length modulation. However, this may not always be the case in application. Some non-idealities such as process variation, V_{DS} difference, and V_{TH} mismatch may cause current mismatches.

Governing Equation :

$$I_{d,sat} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

$$\frac{I_{OUT}}{I_{REF}} = \frac{\frac{1}{2}\mu C_{ox}\frac{W_2}{L}(V_{GS}-V_{TH})^2}{\frac{1}{2}\mu C_{ox}\frac{W_1}{L}(V_{GS}-V_{TH})^2} = \frac{W_2}{W_1}$$

Mismatches

Assume $\beta = \mu C_{ox}\frac{W}{L}$ $\qquad gm = \frac{2I_D}{Vov}$

$$\Delta I_{D,\beta} = \frac{\Delta\beta}{2}(V_{OV})^2$$

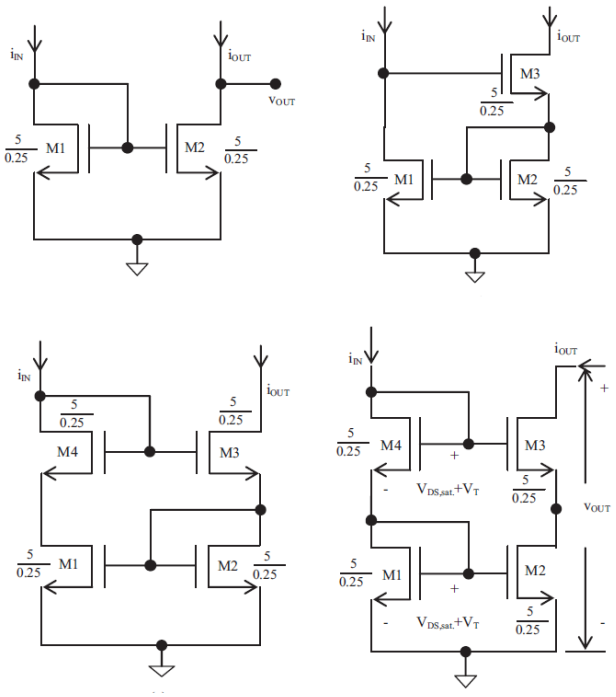
$$\Delta I_{D,vth} \cong -\Delta V_{TH}\beta Vov^2$$

$$\frac{\Delta I_D}{I_D} \cong \frac{\Delta I_{D,\beta} + \Delta I_{D,vth}}{I_D} = \frac{\Delta\beta}{\beta} - \frac{gm}{I_D}\Delta V_{TH}$$

Mismatches in current mirror topology is referred to as the current difference between the reference current, I_{REF} and the output current, I_{OUT}. The causes of current mismatches can be summarized into the following three categories: Process Variation, threshold voltage mismatches(V_{th}), and drain to source voltage difference (V_{DS}).

BASIC CURRENT MIRROR CIRCUITS

In this paper, we have considered four basic current mirror circuits i.e. Simple CMC, Wilson CMC, Modified Wilson CMC, Cascode CMC. The circuit diagram of these is shown in below figure.



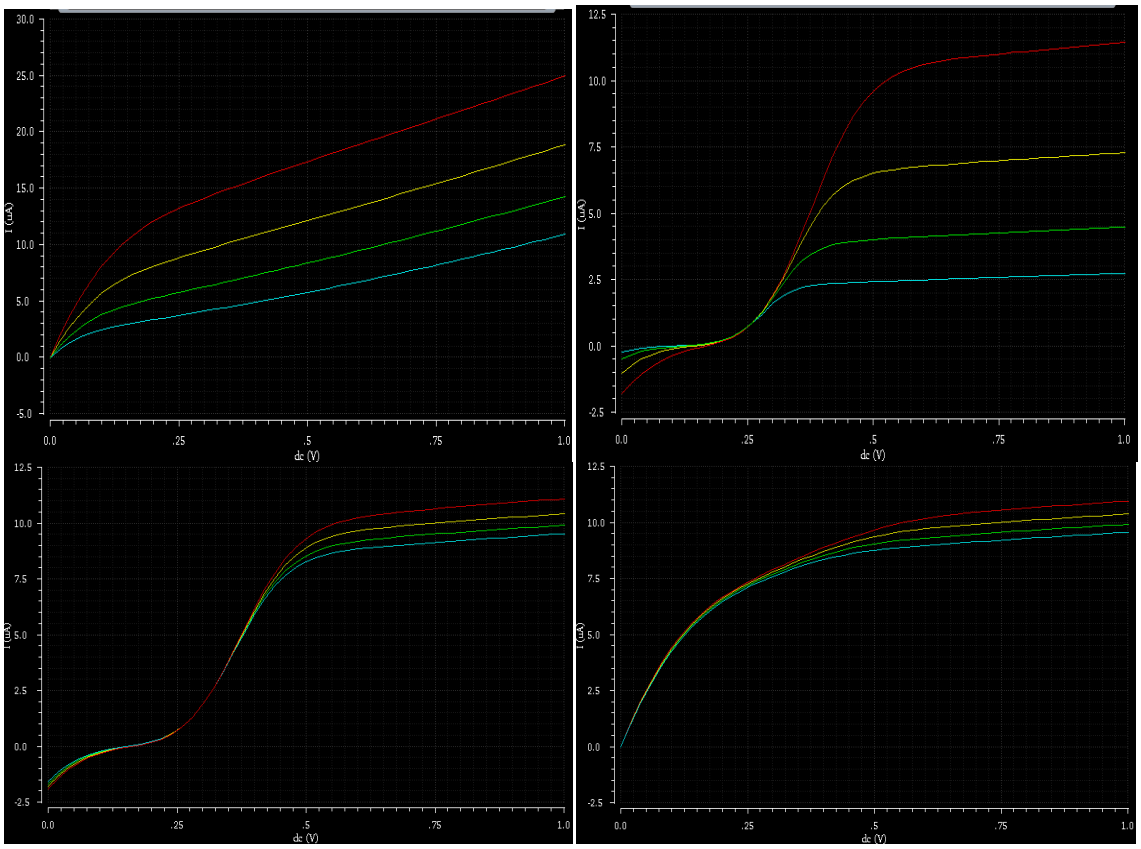
(Figure 1 : Current Mirror Circuits)

Wilson current mirror is the current mirror circuit named after its inventor George Wilson. The circuit consist of negative feedback network to improve the performance. Here if the current through M3, Iout, increases, it causes an increase in current through transistor M2. This increase in drain current through M2 is linearly reflected in M1 causing its drain current to increase. Now since Iref is constant, this increase in drain current through M1 will cause a voltage drop across the gate of M3 which causes Iout to be stable thus, enhancing the performance by providing an increased output impedance. Biggest drawback of this circuit is the mismatching between the output and input side. The cascade of a common source stage and common gate stage is called a “cascode” topology. The cascode connection achieves a very high output impedence. Since this is a

desirable characteristic for a current mirror, exploring the use of cascodes for high performance current mirrors is natural. In ideal condition, the effect of channel length modulation is simply ignored. Cascode structures have been employed in a number of analog designs. However, the use of cascode structure increases the gain but it decreases the output signal swing at the same time. The self-cascode does not require high compliance voltages at output nodes and provides high output impedance to give high output gains. This approach has potential applications in low-voltage design.

PROCESS VARIATION ANALYSIS

For the process variation analysis, we have taken variation into W/L ratio of input transistor, which will result into high output voltage swing. The W/L taken accounts are 0.5, 1, 2 and 4. The respective I-V characteristics of each CMC are shown as follows:



(Figure 2 : Process Variation Analysis)

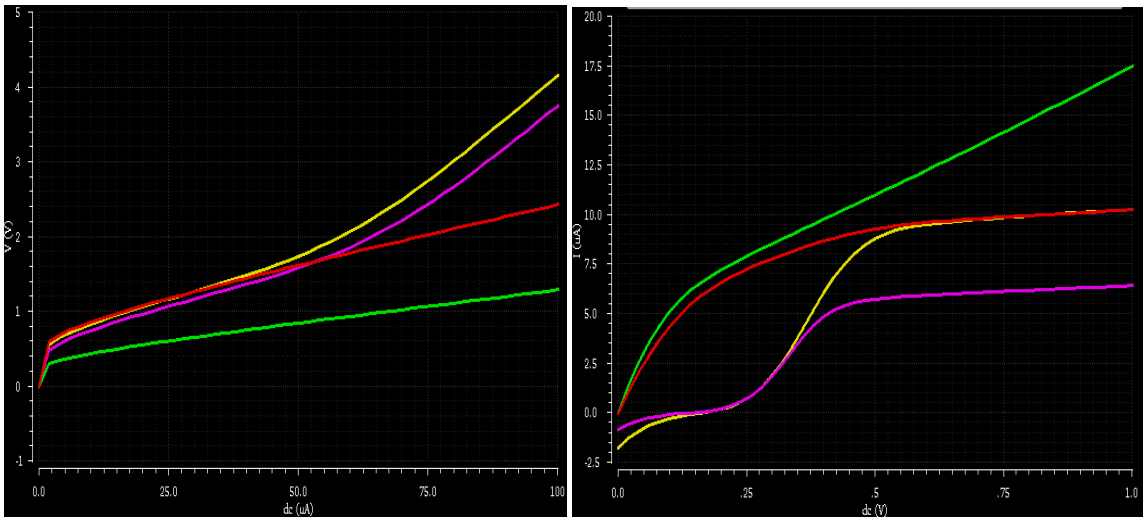
(Graph Sequence : Simple CMC, Wilson CMC, Modified Wilson CMC, Cascode CMC)

The interesting fact that we have observed in Wilson & Modified Wilson CMC is that, at low output load voltage ranges (0-0.2mV), output current is negative, indicating current mirror is acting as current source. But we know that NMOS current mirror is a current sink, so this creates contradictory behavior. One more thing is, this behavior has been observed only in 90nm technology node; this error is not there in design implemented in 180nm technology node.

As drain current has direct relation with W/L ratio, it is increasing by increasing the ratio. Also, due to channel width modulation, we see the increment in drain current in saturation region. From characteristics, it is clearly inferred that, the cascade CMC have the least variations towards incremental change in drain current in saturation along with change in W/L ratio.

VOLTAGE VARIATION ANALYSIS

The voltage variations of CMC can be analyzed by plotting input & output characteristics as:



(Figure 3 : Input & Output Characteristics of CMC)

(Notations : Green : Simple CMC, Pink : Wilson CMC, Yellow : Modified Wilson CMC, Red : Cascode CMC)

The slope of input characteristics gives the input resistance of CMC, whereas the inverse of slope of output characteristics gives the output resistance of CMC. The major

desirable specification of any CMC is that it should provide the maximum output voltage swing as much as possible. The comparative analysis of extracted parameters of these CMC is given in below table.

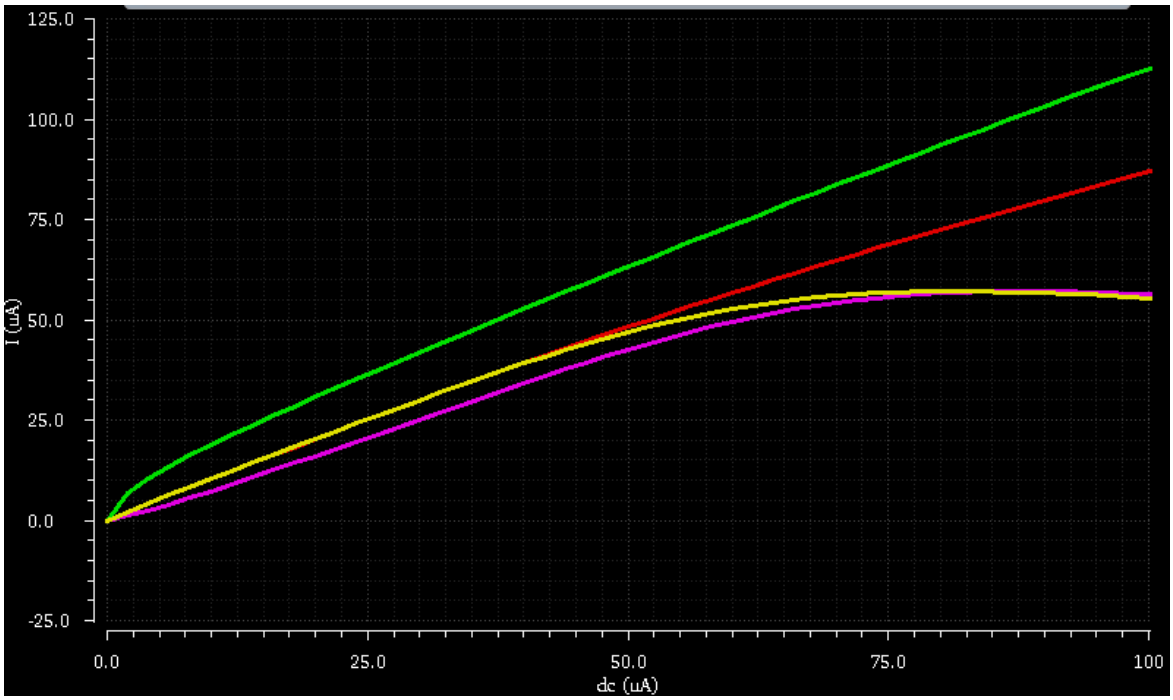
Parameter	Simple CMC	Wilson CMC	Modified Wilson CMC	Cascode CMC
Mirroring Capability	Very Poor	Poor	Good	Very Good
Output Voltage Swing 10% Tol (V)	0.45-0.5V	0.4-0.5V	0.4-0.6V	0.45-1V
Rin (Ω)	4.36KΩ	7.59KΩ	8.02KΩ	8.17KΩ
Rout (Ω)	533.4KΩ	704.2KΩ	937.5KΩ	1.8MΩ
Bandwidth (Hz)	1.01G	2.59G	2.52G	930.9M

In Wilson & Modified Wilson CMC, MOSFET M3 provides negative current feedback that not only improves the current mirroring accuracy but also increases output resistance of CMC by a factor of gmRo. It has been observed that in order to achieve improvement in performance parameters of a CM, designer has to use more number of MOSFETs, which leads to an increase in effective parasitic capacitance of the circuit. Bandwidth of a CM majorly depends upon its input time constant and thereby input capacitance. Generally, increase in parasitic capacitances leads to an increase in the effective input capacitance and hence lowers the bandwidth for the circuit.

In cascade CMC, if(W/L)2 /(W/L)1 = (W/L)3/(W/L)4, V_{DS2} follows V_{DS1} as long as M2 and M3 remain in saturation. Moreover, M3 tries to maintain M2 in saturation region irrespective of variations in output voltage(shielding effect),thereby I_{OUT} closely tracks I_{IN}. Its output compliance voltage is similar to that of Wilson and improved Wilson CMC

and is higher than the minimum voltage required for M2 and M3 to operate in saturation region. The output resistance and hence the performance of a cascode CMC is proved

CURRENT TRANSFER CHARACTERISTICS



(Figure 4 : Current Transfer Characteristics of CMC)

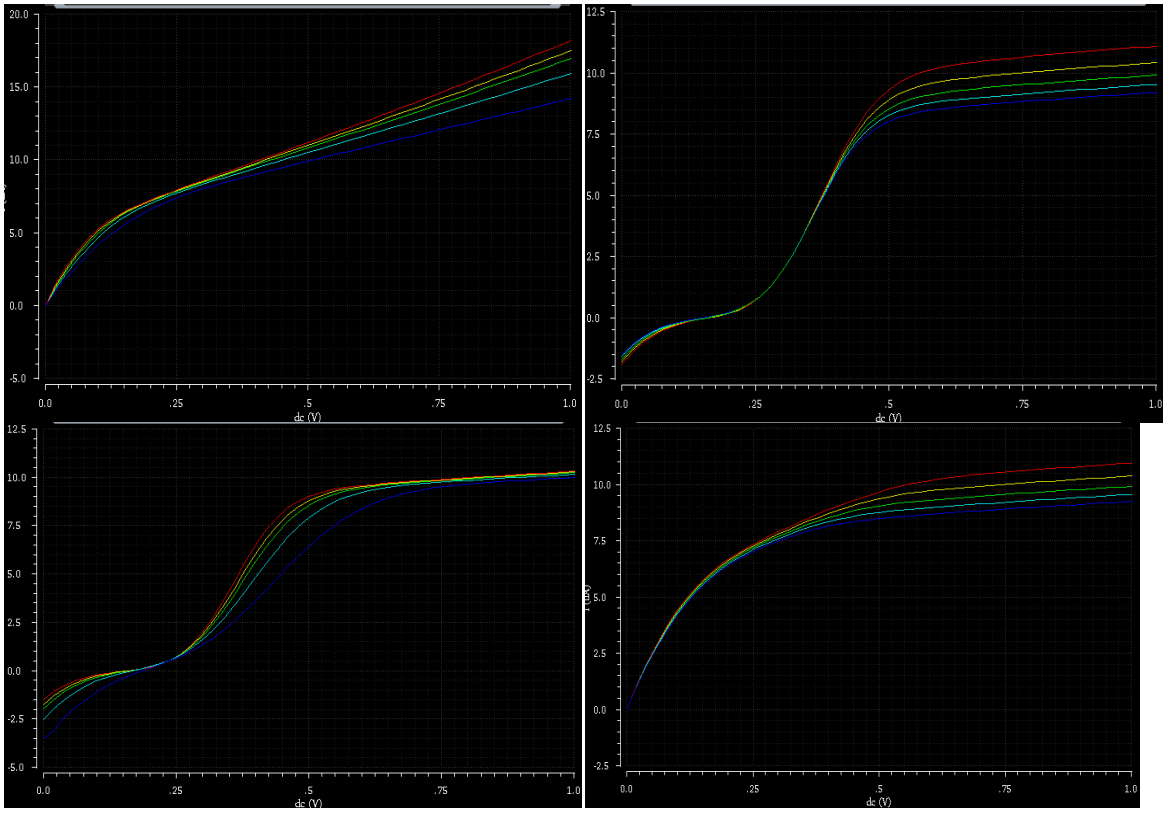
(Notations : Green : Simple CMC, Pink : Wilson CMC, Yellow : Modified Wilson CMC, Red : Cascode CMC)

Current mirroring indicates that the input and output current of circuit must have to be same i.e. the ideal current transfer characteristic should a straight line with slope 1. But, due to non-ideal behavior of transistor and various effects, the slope of characteristics changes which can be seen in simple CMC characteristics. At high current input (>50uA), the transistor behavior gets non-linear and unpredictable hence the characteristics bends which can seen in Wilson & Modified CMC. The most ideal characteristics among all is shown by cascode CMC which is exact linear with slope approximately equal to 1.

TEMPERATURE VARIATION ANALYSIS

The transistor density is not uniform throughout the chip. Some regions of the chip have higher density and higher switching, resulting in higher power dissipation and Some regions of the chip have lower density and lower switching, resulting in lower power dissipation Hence the junction temperature at these regions may be higher or lower depending upon the density of transistors. Because of the variation in temperature across the chip, it introduces different delays across all the transistors. The temperature variation is with respect to the junction and not ambient temperature. The temperature at the junction inside the chip can vary within a big range and that's why temperature variation needs to be considered.

For temperature variation, we have considered temperature as -50℃, 0℃, 27℃ (room temp.), 50℃, 100℃. respective I-V characteristics of each CMC are shown as follows:



(Figure 4 : Process Variation Analysis)

(Graph Sequence : Simple CMC, Wilson CMC, Modified Wilson CMC, Cascode CMC)

CONCLUSION

The basic current mirror circuits like Simple CMC, Wilson CMC, Modified Wilson CMC, Cascode CMC have been studied in depth and simulated by using Cadence Virtuoso Tool at 90nm process technology node. It has been concluded that the cascade CMC gives the best performance with respect to mirroring accuracy, output voltage swing, input & output resistance.

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