FCH: Computer Organization

Course Title: Computer Organization
Course No: CS220
Instructor's Name: Debapriya Basu Roy
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Credits: 3-0-4-13
Prerequisite: ESC111, ESC112, ESC201

Course Objective: Modern computer technology requires professionals of every computing specialty to understand both hardware and software. The interaction between hardware and software at a variety of levels also offers a framework for understanding the fundamentals of computing. Whether your primary interest is hardware or software, computer science or electrical engineering, the central ideas in computer organization and design are the same. Thus, the main emphasis of this course is to show the relationship between hardware and software and to focus on the concepts that are the basis for current computers.

Course Structure: The module wise description of the course is given in the table below:

Topic	Subtopics	Lecture Hours
Hardware Description Language	Verilog Syntax and Framework	2
	Combinational Circuit Design: Multiplexer, Encoder, Decoders etc.	1
	Sequential Circuits: Flip flops, Counters, Finite State Machine	1
Computer Arithmetic	Quine–McCluskey Method	1
	Adders: Ripple Carry, Carry-Look-Ahead, Carry Skip, Carry Select, Carry Save, FPGA	3
	Multipliers: Booth, Karatsuba, Montgomery, Number Theoretic Transformation	3
	Division: Restoring and Non-restoring	2
	Algorithmic State Machine	1
	Case Study: GCD Processor using Extended Euclidean Algorithm	1
Number Representation	IEEE Floating Point	2
Instruction Set Arhitecture	Different kind of ISA	1
	Case Study: MIPS	2
	Single Instruction Computer	1
CPU Construction	ALU	1
	Register File	1
	Instruction Execution Phase	1
	Control Unit	1
	Hardware Performance Counters	1
	Single Cycle and Multi-Cycle CPU	3
Pipelining	Main Concept	1
	Hazard and Predictors	2
	Performance Computation	2
Cache Memory	Overview	2
	Replacement Policies	1
	Placement Policies	3

Policies:

- Please be on time for the lectures.
- You are allowed up to two late days to submit your assignment, with a 25% penalty for each day.
- Students caught cheating or plagiarizing will automatically fail the course and will be reported to the institute.
- If you are unwell, follow standard IITK procedure.

- We will have laboratory assigmnets on every Monday and Wednesday. The students will be divided into two sections randomly, one section will come join the lab session on Monday and another section will join the lab session on Wednesday.
- The lab assignments can be done in a group of two students. The groups will be made randomly.
- The lab assignments may get checked for plagiarism and strict penalty will be imposed on the students who will have high degree of similarity in their codes.
- No request of make-up labs will be entertained.
- You can make request to change your lab sections. However, any such request without a proper reason will be rejected.
- There will be two additional lab sessions on 29th March and on 19th April.
- There will be two additional theory classes on 8th February and 19th April.
- No mobile phones will be allowed in the labs.
- Lab exams will happen in 4 sessions. The students will be allocated to session randomly. No request of any normalization will be entertained. The lab exam questions will be of equivalent difficulty. The decision of instructor in this regard will be final.
- For doubt clearing, write me an email or meet me directly in my room at KD319.
- We might add new, drop existing, or reorder topics depending on progress and class feedback.
- Things may be changed by mutual consent after discussion in class.
- Grading will be relative.

Non-mandatory Case Studies: We will have two case studies which are completely optional. They are:

- Designing hardware architecture of AES-256 block cipher supporting both encryption and decryption. (not graded and optional)
- Designing hardware architecture of elliptic curve scalar multiplier in Curve-25519. (On successful completion of this case-study, you can replace the marks of quiz or three labs with full credit)

Evaluation:

Category	**Split**
Quiz	10%
Lab Assignments	5%
Mid Sem	30%
End Sem	35%
Lab Exam	20%

Books:

1. Computer Organization and Design: The Hardware/Software Interface, David A Patterson, John L. Hennessy.
2. Computer Architecture and Organization by William Stallings, PHI Pvt. Ltd., Eastern Economy Edition.
3. Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Prentice Hall, 1996.
4. Computer System Architecture by M Morris Mano, Prentice Hall of India.
5. Computer Architecture and Organization by John P Hayes.
6. Assembly Language, Online notes, http://linuxassembly.org/.