CIRCUISTICS 2025

This event focuses on Electrical and Electronic circuits, where participants are tested on their knowledge of basics of electrical and electronic engineering and their skill of building functional circuits from scratch.

TIMELINE:

DAY 1 (21.02.25): PRELIMS for both Tier 1 & Tier 2 (1hr written test)

DAY 2 (22.02.25): FINALS for both Tier 1 & Tier 2 (3hrs for hardware design)

RULES & REGULATIONS:

- There will be two *Tiers* for this event : Tier 1 for UG1 and UG2 and Tier 2 for UG3 and UG 4.

a. PRELIMS

- For Tier 1, there will be *two different sets of question papers*: one for UG1 & another for UG2. Tier 2 will have the *same question paper provided* to both years.
- Questions will be mostly *MCQ* and *NAT* in the PRELIMS with *MSQ* only for Tier 2.
- Participants just need to bring their *pen, exam board* and *calculator*. *Rough sheet* will be given.
- Each participant in a team will be given an individual question paper but only *one of them needs to be properly marked*, and that will be considered as the *final answer script* of that team.
- Discussion among team members is allowed but between other teams & use of any electronic device other than calculator is not allowed. *Such use of unfair means if found shall lead to immediate disqualification of the respective team.*

b. FINALS

- The top 8 teams will move to the FINALS from each tier.
- All hardware components required to build the circuit will be provided to the respective teams.
- Finalists of both Tiers will have to build a fully functional electronic circuit according to the given problem statement.
- Winner will be selected by the judges. Prize distribution after the FINALS.

SYLLABUS FOR PRELIMS:

- ***Tier 1, UG1***: Network Theory: RL, RC, RLC circuits, D.C. Network theorems (Superposition Theorem, Thevenin's Theorem, Norton's Theorem, Maximum Power Transfer Theorem), A.C. Resonance, Steady state analysis w.r.t. A.C. circuits, Analog Electronics: Diode basics, Zener diode, Diode circuits (Rectifier, Clipper, Clamper). Digital Electronics: Logic gates, Boolean algebra.

- ***Tier 1, UG2*****:** Network Theory: RL, RC, RLC circuits, A.C. & D.C. Network Theorems, D.C. transient analysis, A.C. resonance, Steady state analysis w.r.t. A.C. circuits. Analog Electronics: Diode circuits: clipper, clamper, peak detector, Voltage multiplier, Rectifier, BJT (biasing), Operational amplifier circuits. Digital Electronics: Logic gates, Boolean algebra, Multiplexer, Demultiplexer, Half-adder, Full-adder.

- ***Tier 2***: Network Theory: RL, RC, RLC circuits, a.c. & d.c. network theorems, d.c. transient analysis, a.c. resonance, Steady state analysis w.r.t.a.c. circuits. Analog Electronics: Analog passive & active filters, Switched capacitors, Advanced diode circuits, MOSFET and BJT amplifiers: biasing, Equivalent circuit, Oscillators & feedback amplifiers,Operational amplifier, Timer circuits. Digital Electronics: Combinational & sequential logic circuits, A/D and D/A converters, Logic gate implementation using CMOS circuits. Control Systems: Transfer function, Transient & steady-state analysis of linear time invariant systems, Stability analysis using Routh-Hurwitz & Nyquist criteria, Bode plots, Root loci. Signals and Systems: Representation of continuous linear time invariant and causal systems and its response, Applications of Fourier series & Fourier transform for continuous time signals, Laplace transform.