Spice Project

EE619A

Group Members

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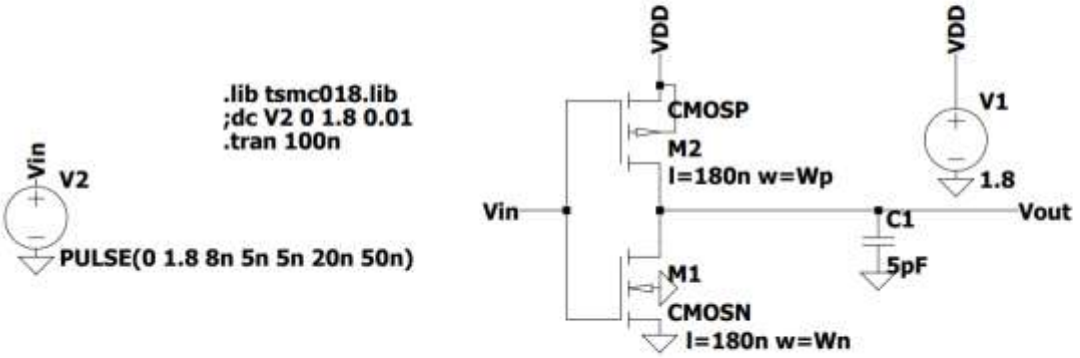
```
.meas TRAN  t_hl TRIG V(Vout)=1.62 TD=0 FALL=1 TARG V(Vout)=0.18 TD=0 FALL=1
.meas TRAN  t_lh TRIG V(Vout)=.18 TD=0 RISE=1 TARG V(Vout)=1.62 TD=0 RISE=1
```



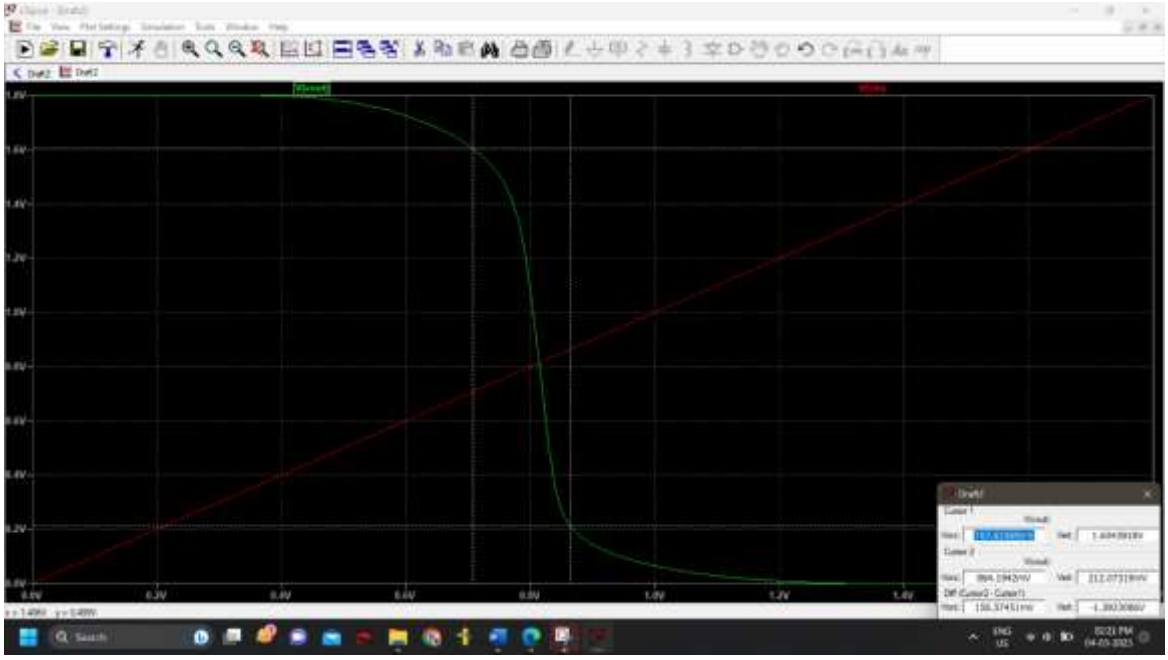
Circuit Parameters

NMOS $l = 180\ nm,\ \ W = W_n$

PMOS $l = 180\ nm,\ \ W = W_p$

$V_{DD} = 1.8\ v$

a) After analysis, we got PMOS to NMOS size ratio of the minimum-sized CMOS inverter to have equal rise and fall time as 2.77



Using the Slope = -1 criteria,

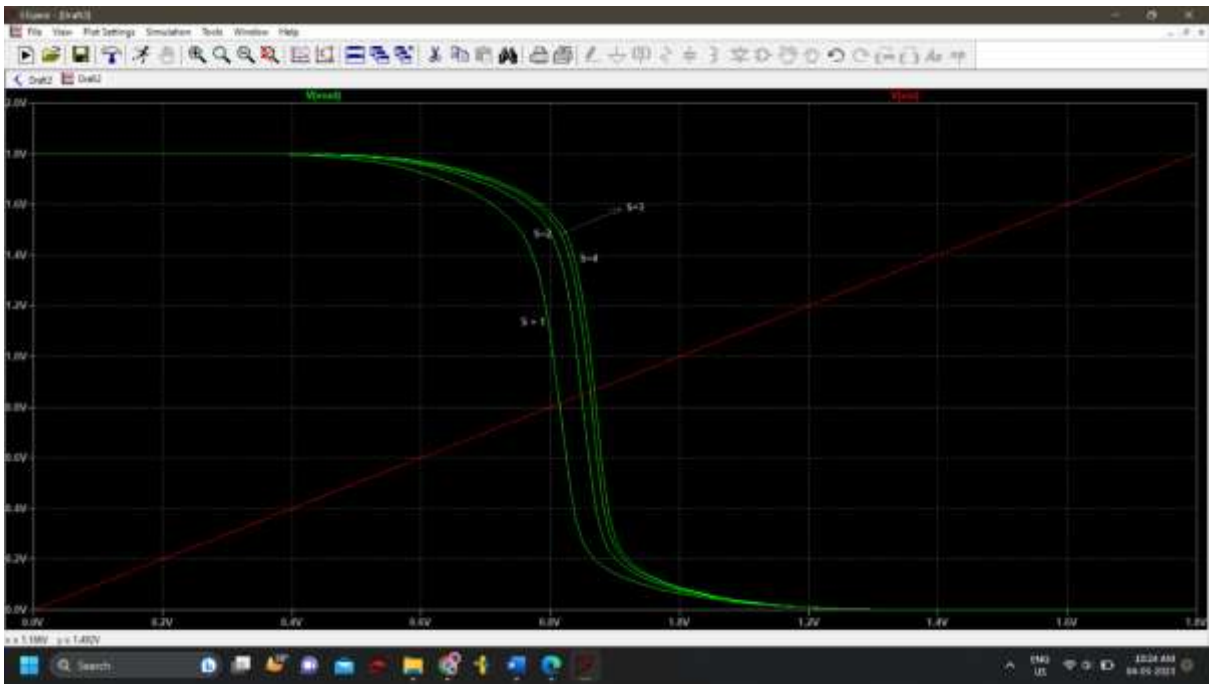
$V_{IL} = 0.7$, $V_{OH} = 1.6$

$V_{IH} = 0.86$, $V_{OL} = 0.2$

$NM_H = V_{OH} - V_{IH}$ = 0.74

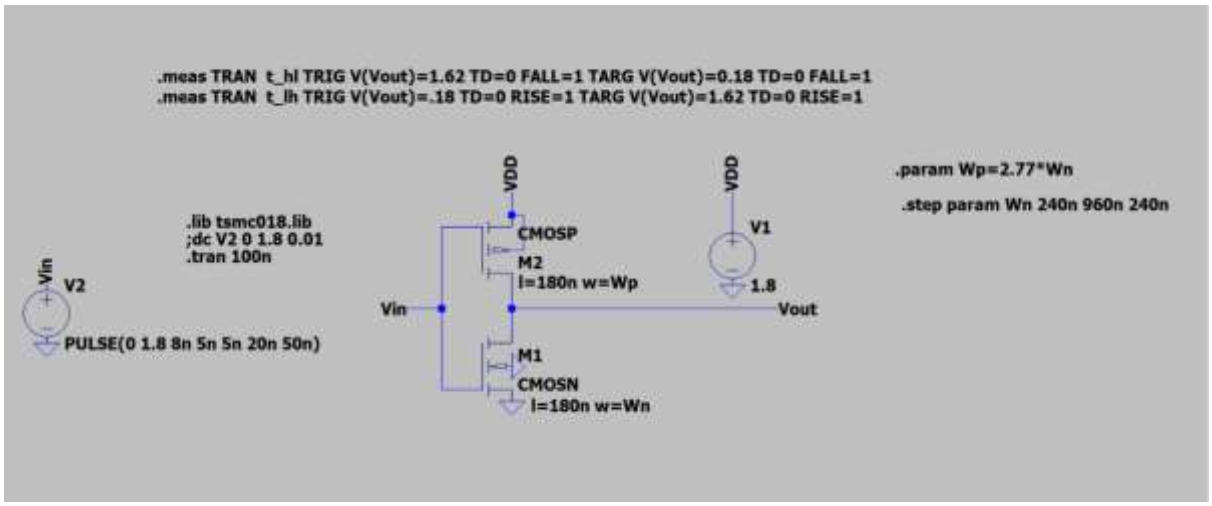
$NM_L = V_{IL} - V_{OL}$ = 0.5

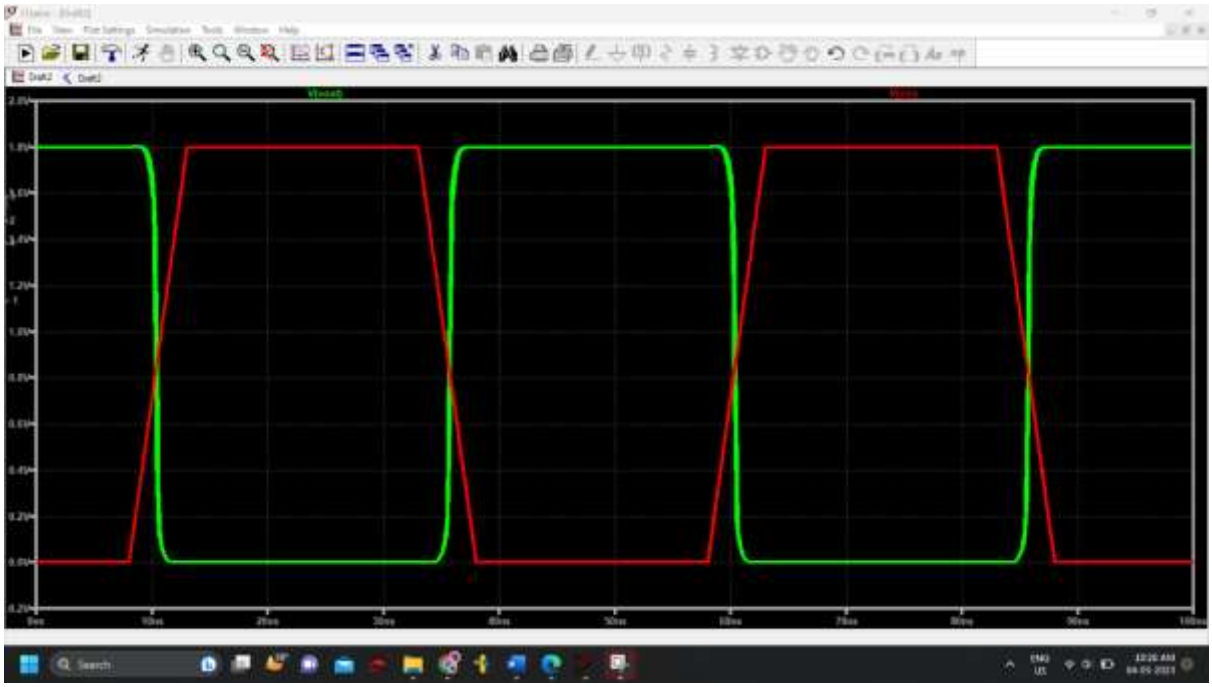
$NM = \min(NM_L, NM_H) = 0.5$



b. Transient analysis result (Vout vs Vin)

Case1. No external capacitor is attached

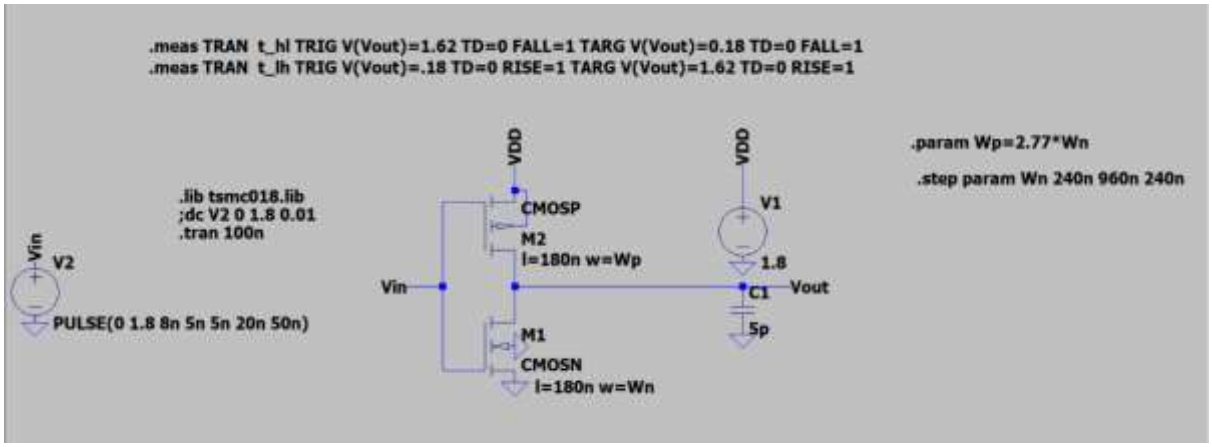


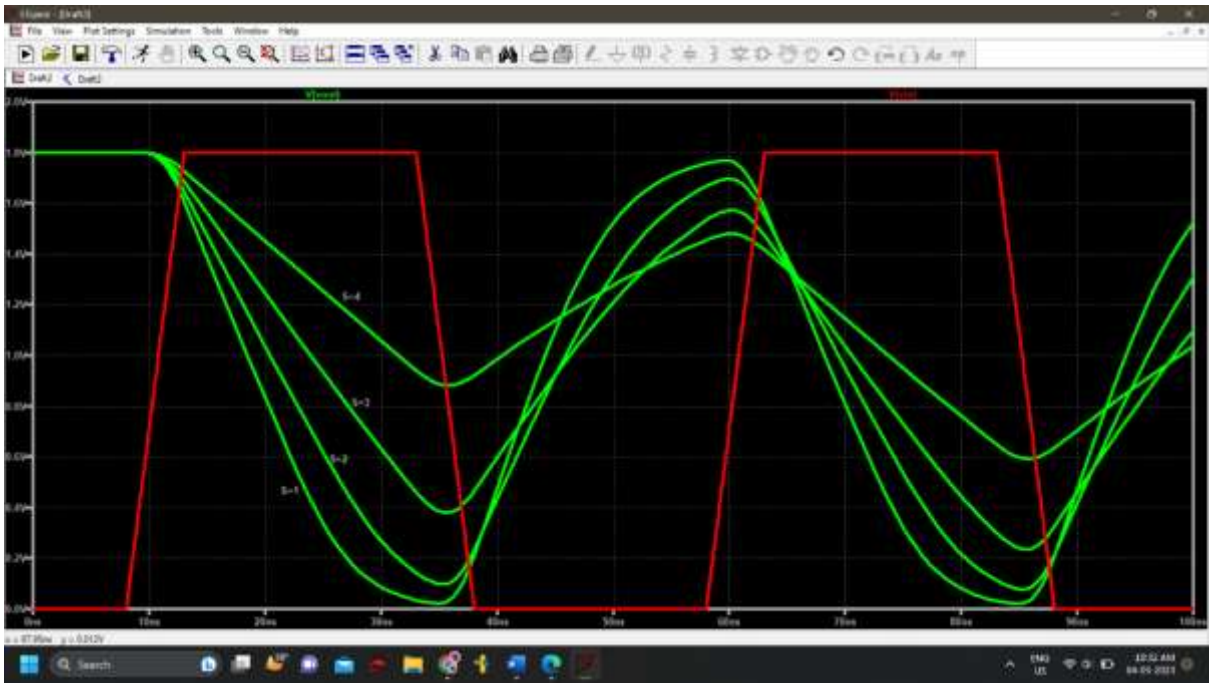


```
Measurement: t_hl
  step      t_hl   FROM   TO
     1      5.49759e-10 9.93779e-09 1.04875e-08
     2      5.09718e-10 1.00763e-08 1.05861e-08
     3      5.18332e-10 1.01232e-08 1.06416e-08
     4      5.1002e-10  1.01477e-08 1.06578e-08

Measurement: t_lh
  step      t_lh   FROM   TO
     1      5.42293e-10 3.55436e-08 3.60859e-08
     2      5.00775e-10 3.54539e-08 3.59547e-08
     3      4.76966e-10 3.5431e-08  3.5908e-08
     4      4.6912e-10  3.54116e-08 3.58807e-08
```

Case2. When an external capacitor of 5 pF is attached to the output node





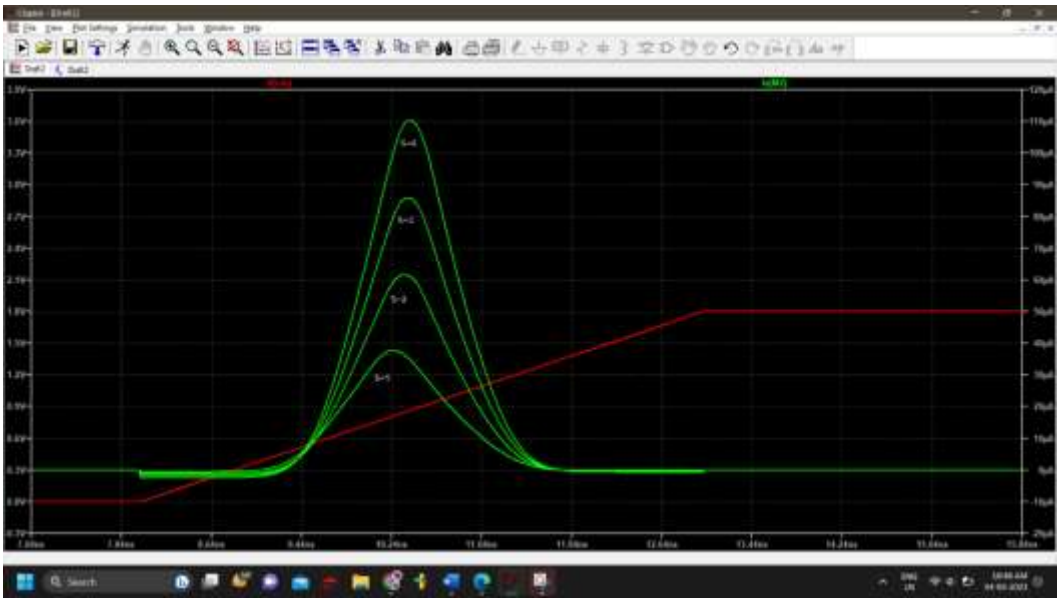
```
Measurement: t_hl
  step      t_hl   FROM   TO
     1      0      1.57354e-08 0
     2      0      1.4081e-08  0
     3      1.86152e-08 1.33187e-08 3.1934e-08
     4      1.45721e-08 1.28848e-08 2.74569e-08

Measurement: t_lh
  step      t_lh   FROM   TO
     1      0      0      0
     2      0      0      0
     3      1.8836e-08  3.73715e-08 5.62075e-08
     4      1.42217e-08 3.77328e-08 5.19545e-08
```

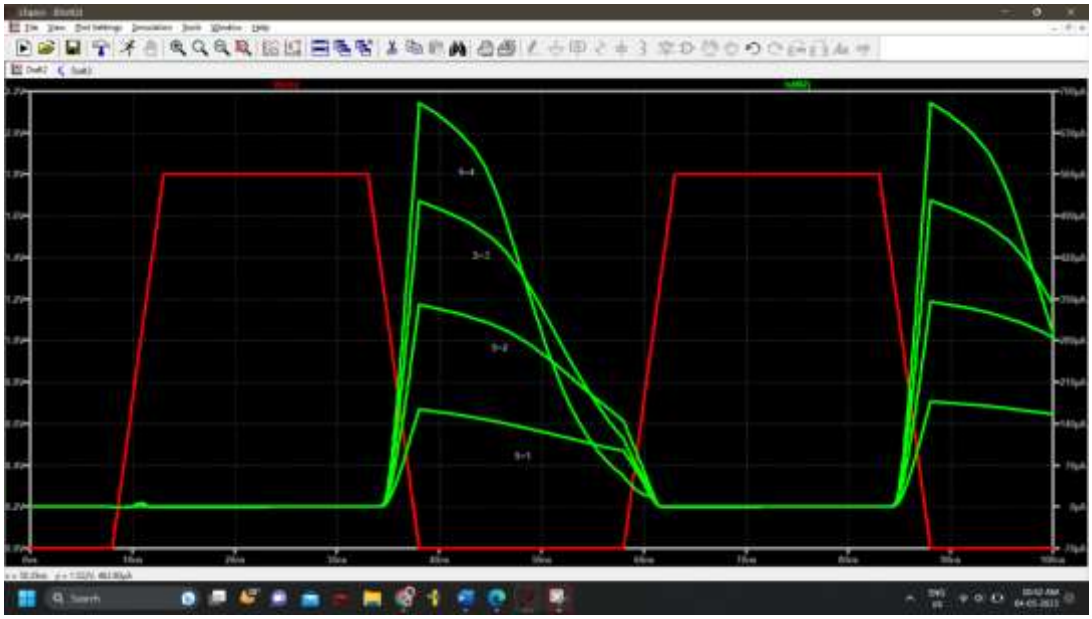
As we are increasing the value of W_n and W_p the resistance is getting decreased so, the time constant also reduces. So, the capacitor is getting charged at a faster rate.

Current drawn from the power supply in all cases as the input voltage is swept slowly w.r.t the output

Without capacitor

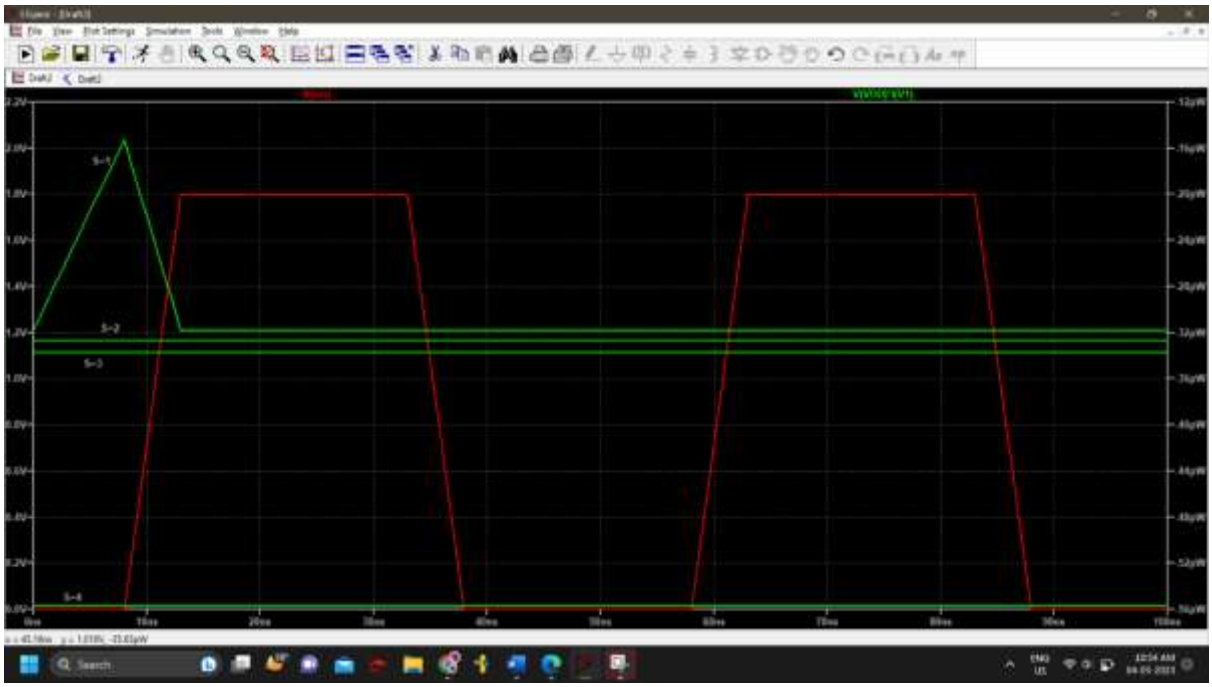


With capacitor

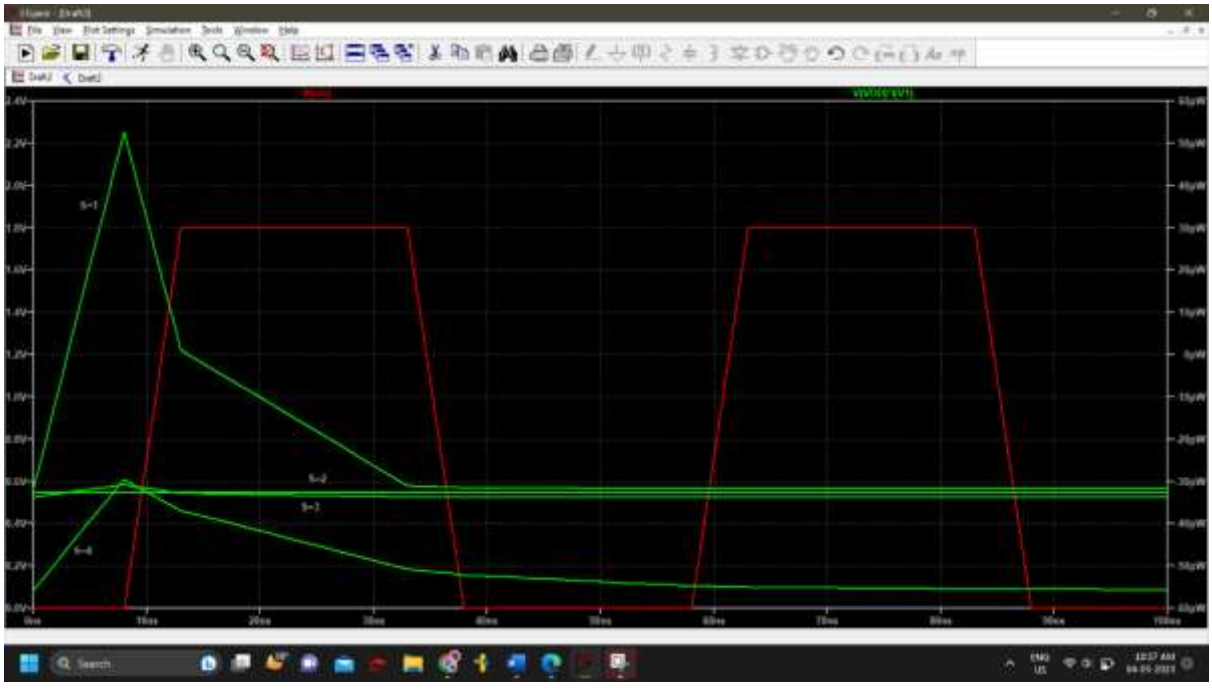


Static Power dissipation

Without capacitor

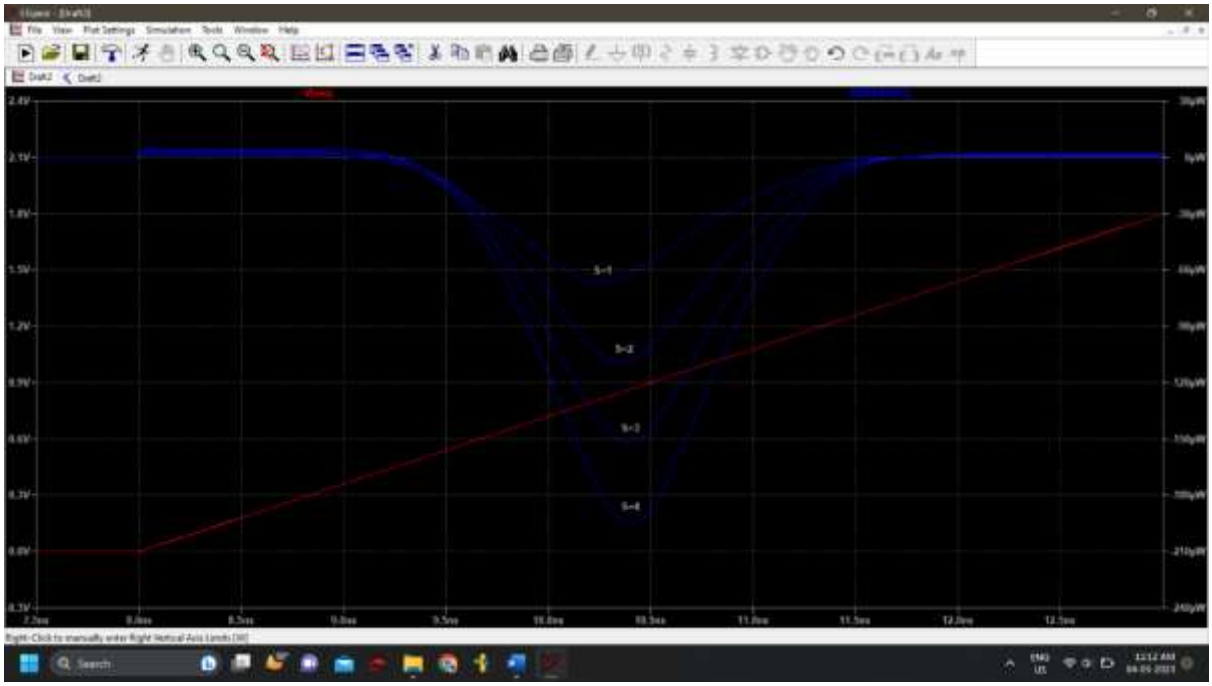


With capacitor

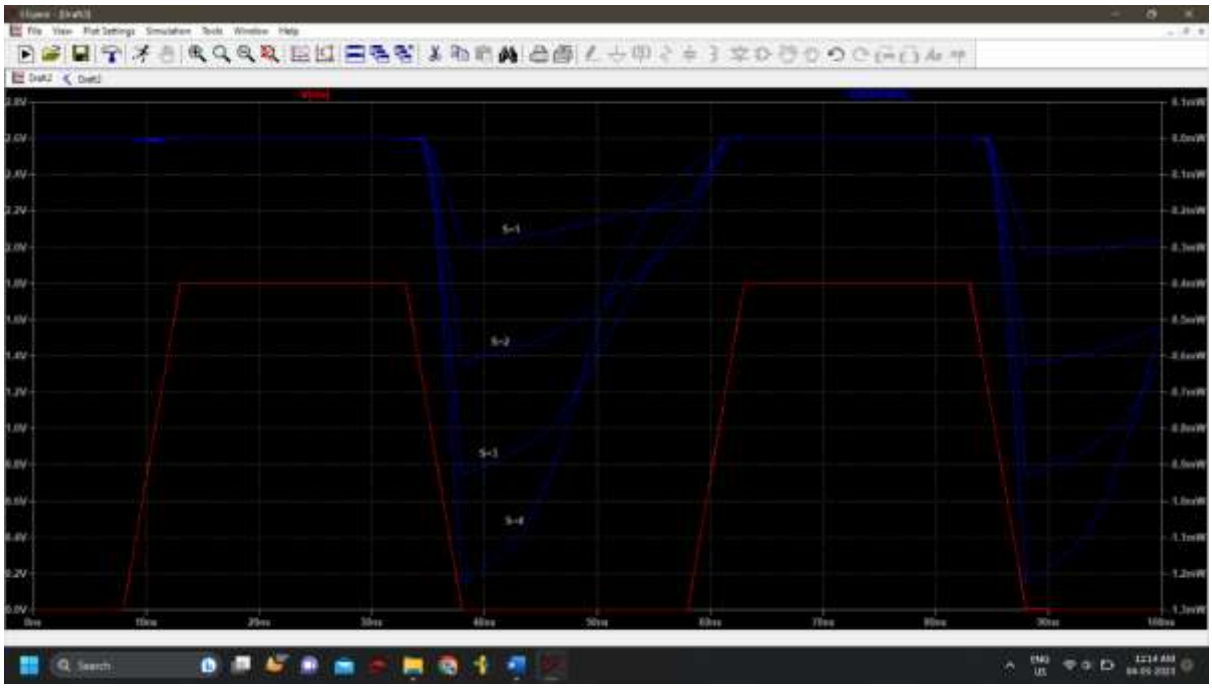


Dynamic power dissipation

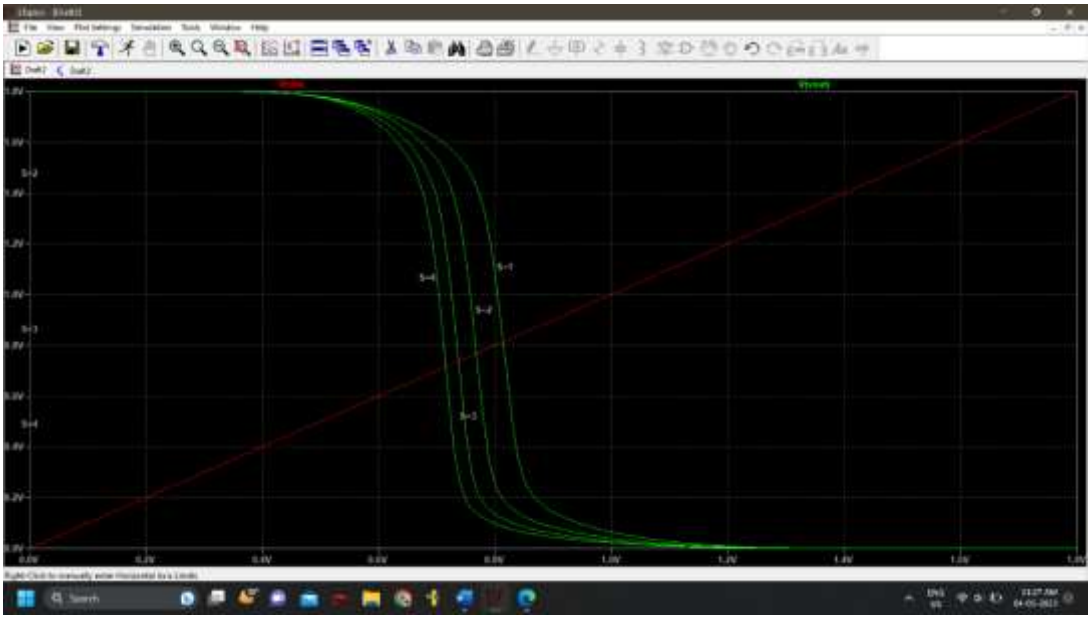
Without capacitor



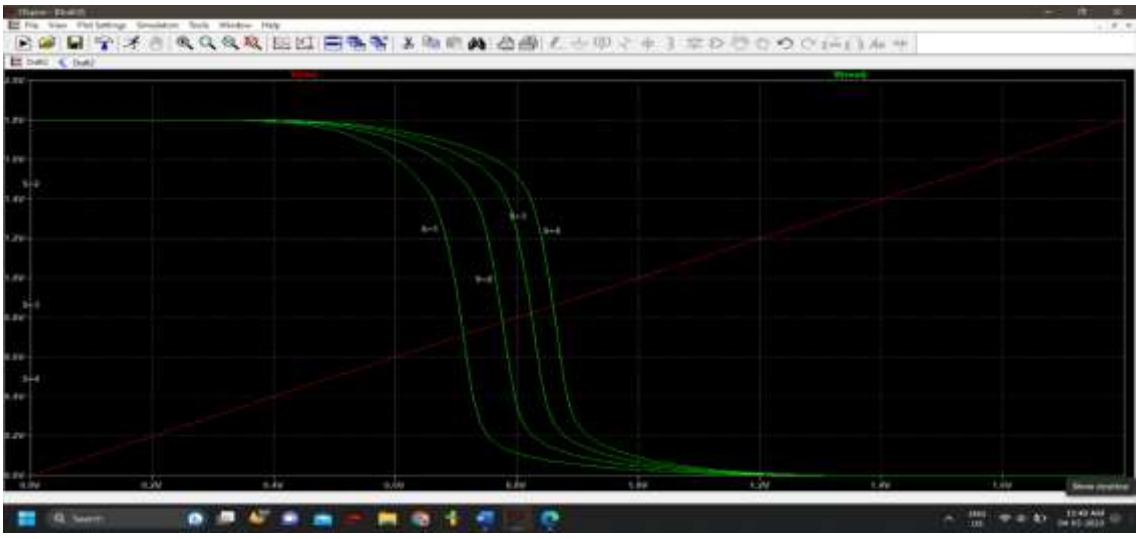
With capacitor



c) Simulate the static VTC of an inverter in which the NMOS is sized Kn times the size of the corresponding NMOS of the minimum-sized inverter for Kn = 1,2,4, keeping the size of the PMOS the same as that of the corresponding PMOS of the minimum-sized inverter.



ii. simulate the static VTC of an inverter in which the PMOS is sized Kp times the size of the corresponding PMOS of the minimum-sized inverter for Kp = 1,2,4, keeping the size of the NMOS the same as that of the corresponding NMOS of the minimum-sized inverter.



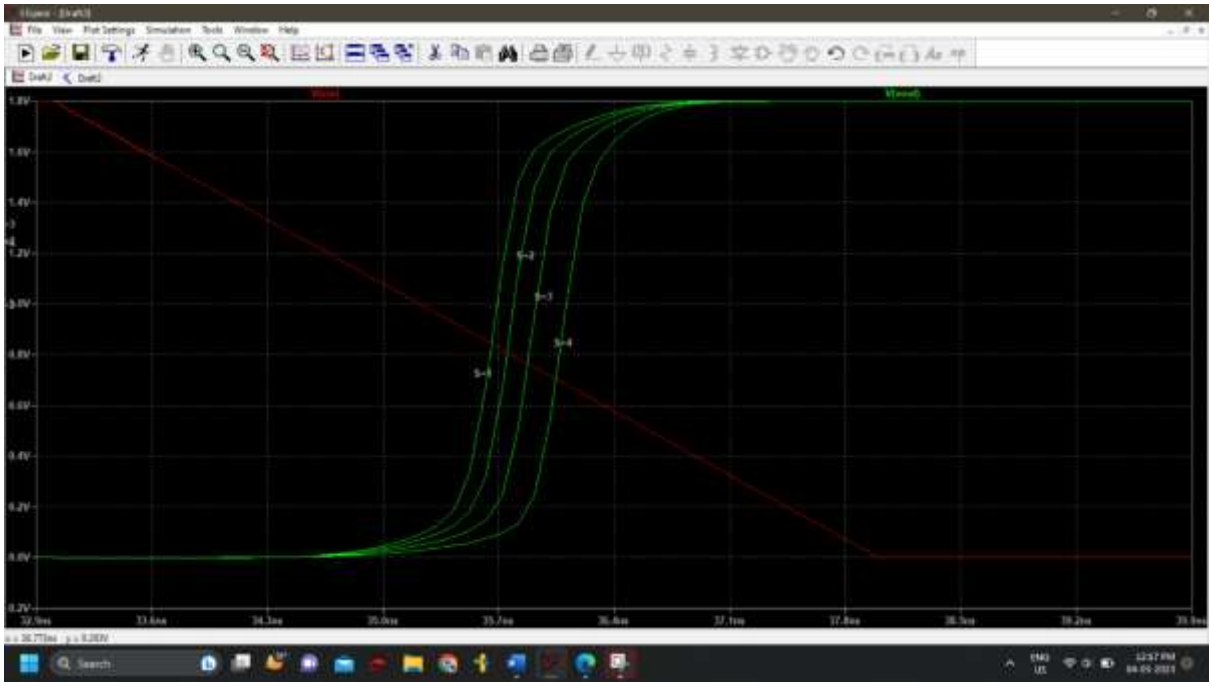
d) Transient analysis

When PMOS is sized Kp times the size of the corresponding PMOS of the minimum-sized inverter for Kp = 1,2,4, keeping the size of the NMOS the same as that of the corresponding NMOS of the minimum-sized inverter.

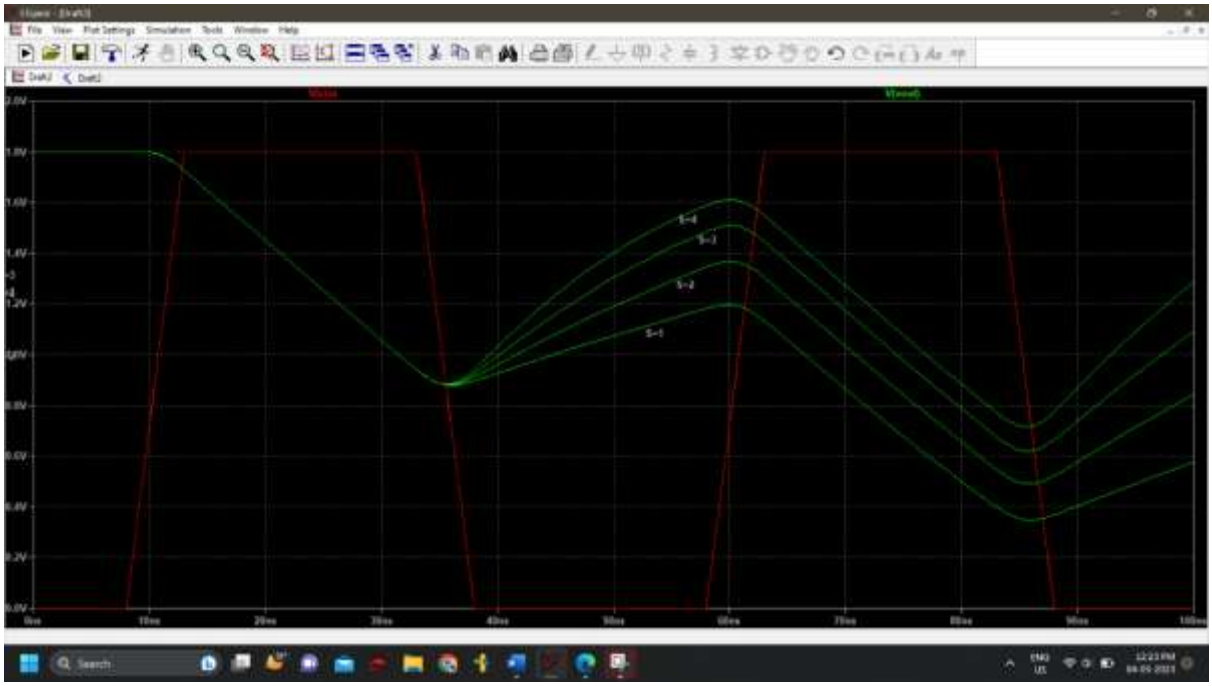
Without capacitor at output node

```
Measurement: t_hl
  step      t_hl   FROM   TO
     1      5.31521e-10 9.64719e-09 1.01787e-08
     2      5.52082e-10 9.82774e-09 1.03798e-08
     3      5.64594e-10 9.96823e-09 1.05328e-08
     4      5.57457e-10 1.00857e-08 1.06432e-08

Measurement: t_lh
  step      t_lh   FROM   TO
     1      5.16693e-10 3.58572e-08 3.63739e-08
     2      5.39519e-10 3.56547e-08 3.61942e-08
     3      5.3232e-10  3.55239e-08 3.60562e-08
     4      5.25373e-10 3.54154e-08 3.59408e-08
```



With capacitor at output node

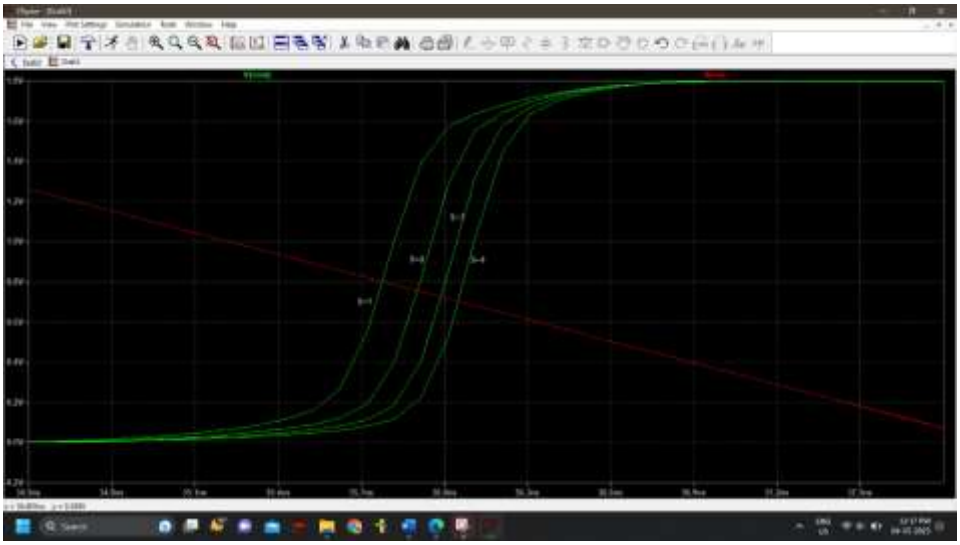


```
Measurement "t_hl" FAIL'ed

Measurement "t_lh" FAIL'ed
```

When NMOS is sized Kn times the size of the corresponding NMOS of the minimum-sized inverter for Kn = 1,2,4, keeping the size of the PMOS the same as that of the corresponding PMOS of the minimum-sized inverter.

Without capacitor

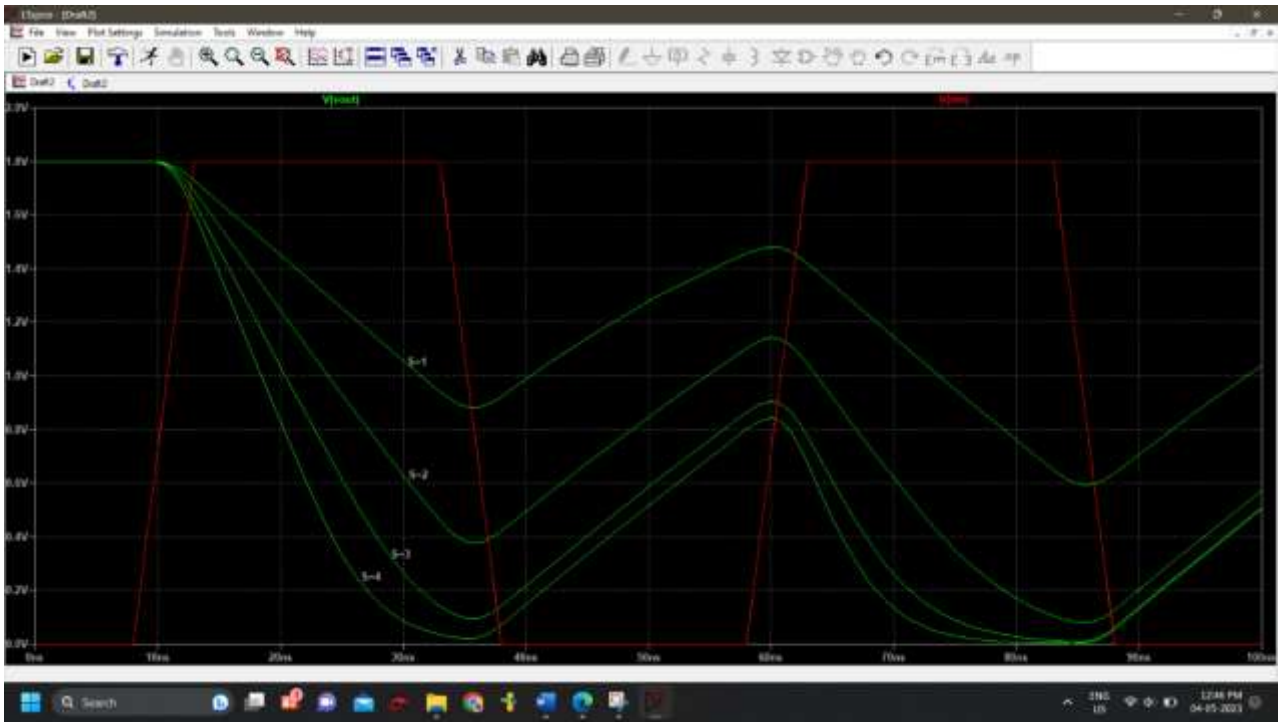


\

```
Measurement: t_hl
  step      t_hl   FROM   TO
     1      5.49713e-10 9.9379e-09  1.04876e-08
     2      5.14946e-10 9.84303e-09 1.0358e-08
     3      4.81481e-10 9.77937e-09 1.02609e-08
     4      4.52877e-10 9.73166e-09 1.01845e-08

Measurement: t_lh
  step      t_lh   FROM   TO
     1      5.42273e-10 3.55436e-08 3.60858e-08
     2      4.79771e-10 3.57049e-08 3.61847e-08
     3      4.42384e-10 3.58119e-08 3.62543e-08
     4      4.24381e-10 3.58762e-08 3.63006e-08
```

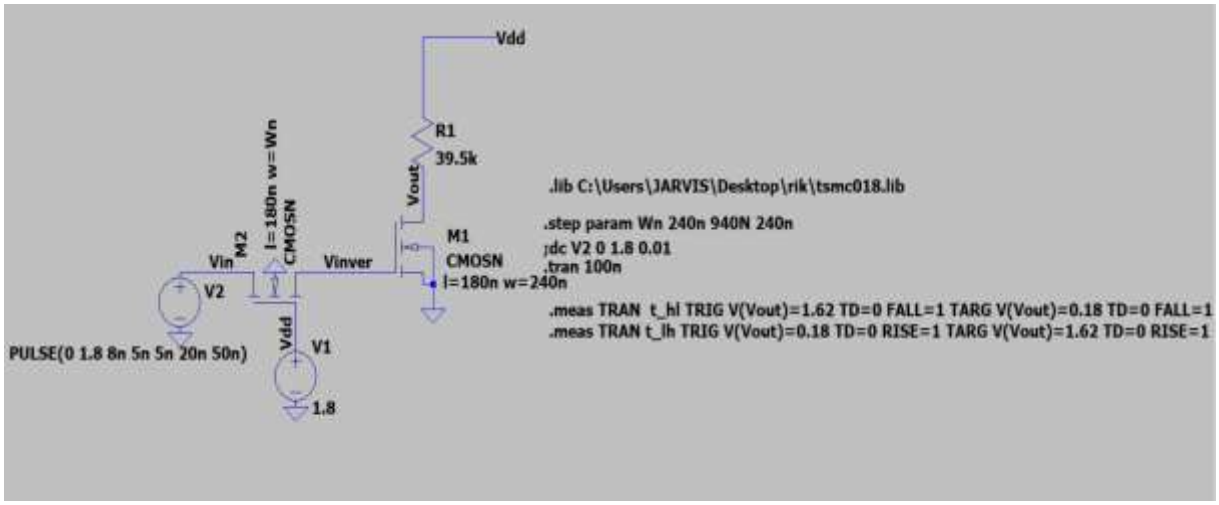
With capacitor



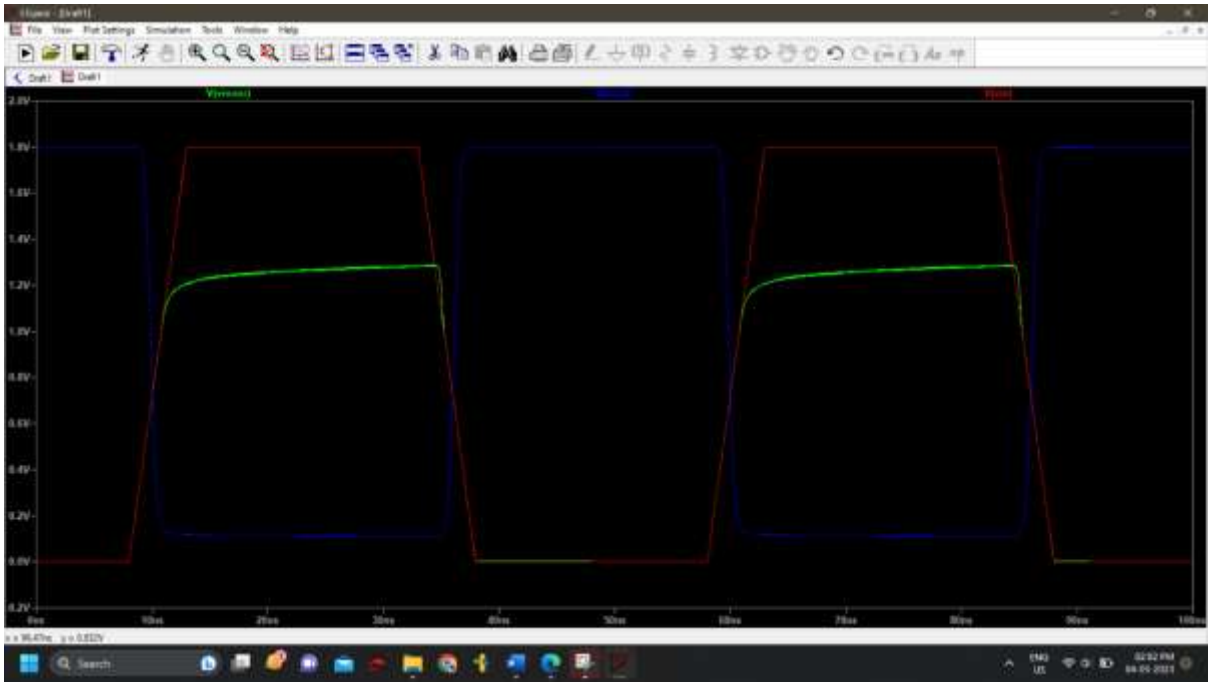
```
Measurement: t_hl
  step      t_hl   FROM   TO
     1      0      1.57354e-08 0
     2      6.55689e-08 1.40724e-08 7.96413e-08
     3      1.86163e-08 1.33046e-08 3.19209e-08
     4      1.45775e-08 1.2857e-08  2.74345e-08

Measurement "t_lh" FAIL'ed
```

e)

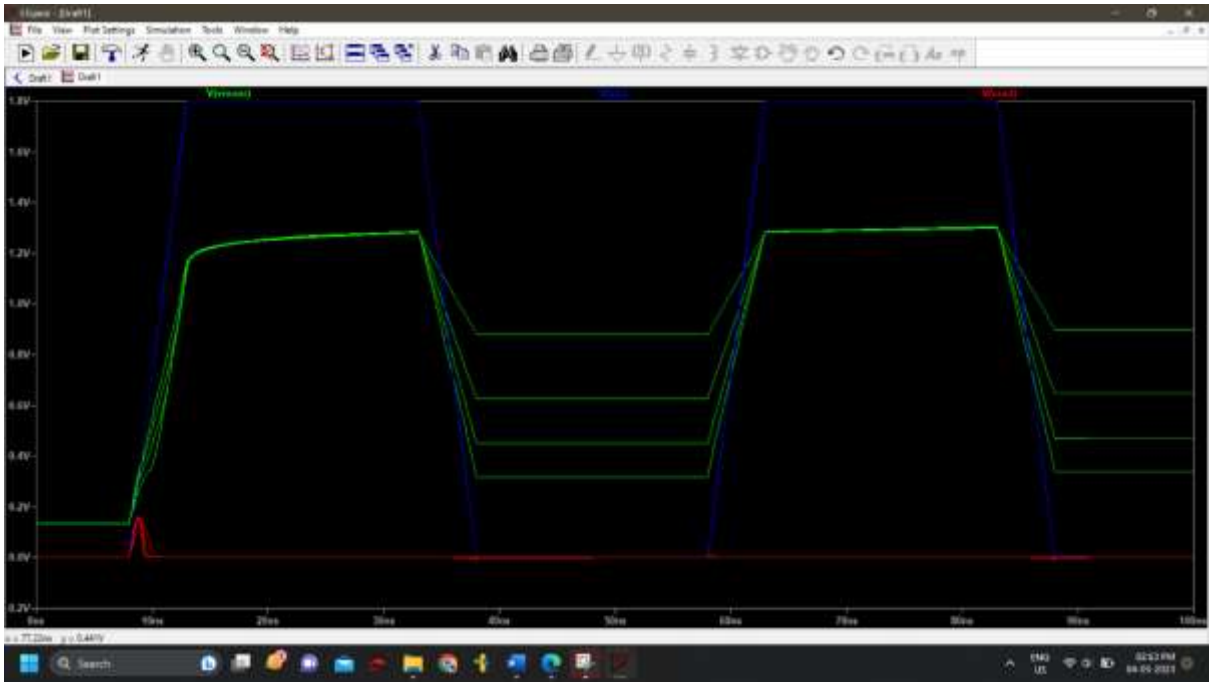


External resistance used to make the rise and fall time equal is 39.5 k-ohms



```
Measurement: t_hl
  step      t_hl   FROM   TO
     1      1.29995e-09 9.38816e-09 1.06881e-08
     2      1.29898e-09 9.38727e-09 1.06862e-08
     3      1.29847e-09 9.38686e-09 1.06853e-08
     4      1.29828e-09 9.38664e-09 1.06849e-08

Measurement: t_lh
  step      t_lh   FROM   TO
     1      1.29691e-09 3.53464e-08 3.66433e-08
     2      1.29793e-09 3.53445e-08 3.66424e-08
     3      1.29844e-09 3.53436e-08 3.6642e-08
     4      1.29874e-09 3.5343e-08  3.66418e-08
```



```
Measurement "t_hl" FAIL'ed

Measurement "t_lh" FAIL'ed
```

We are not getting any rise time or fall time because the pass transistor turns off at $V_{DD} - V_T$ which is 1.8 – 0.366 so, the output will never reach 90% of the input.