AKASH KUMAR
M.TECH PE
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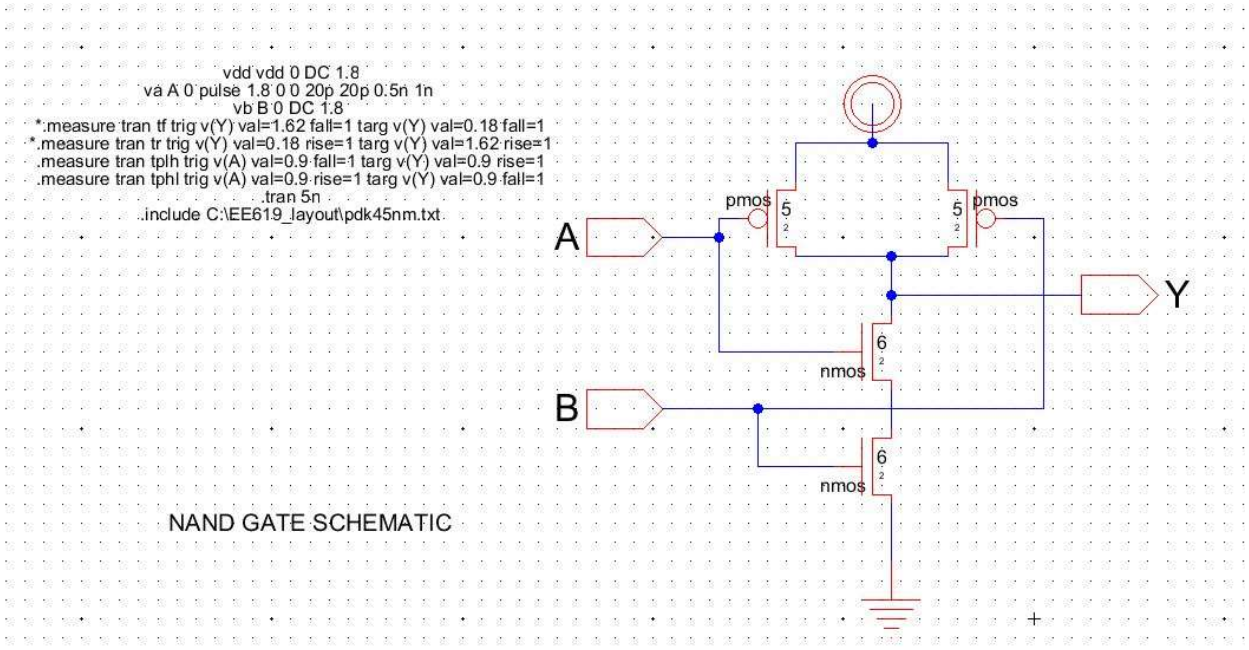
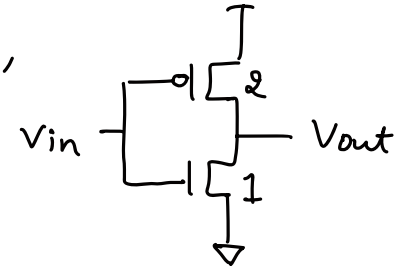
1) NAND GATE

SCHEMATIC:



TOR SIZE EXPLANATION:

For a reference inverter,



In order to equate the worst case t_{plh} and t_{phl}, we need resistance in pMOS side and nMOS side for worst case input to be same.

For NAND,

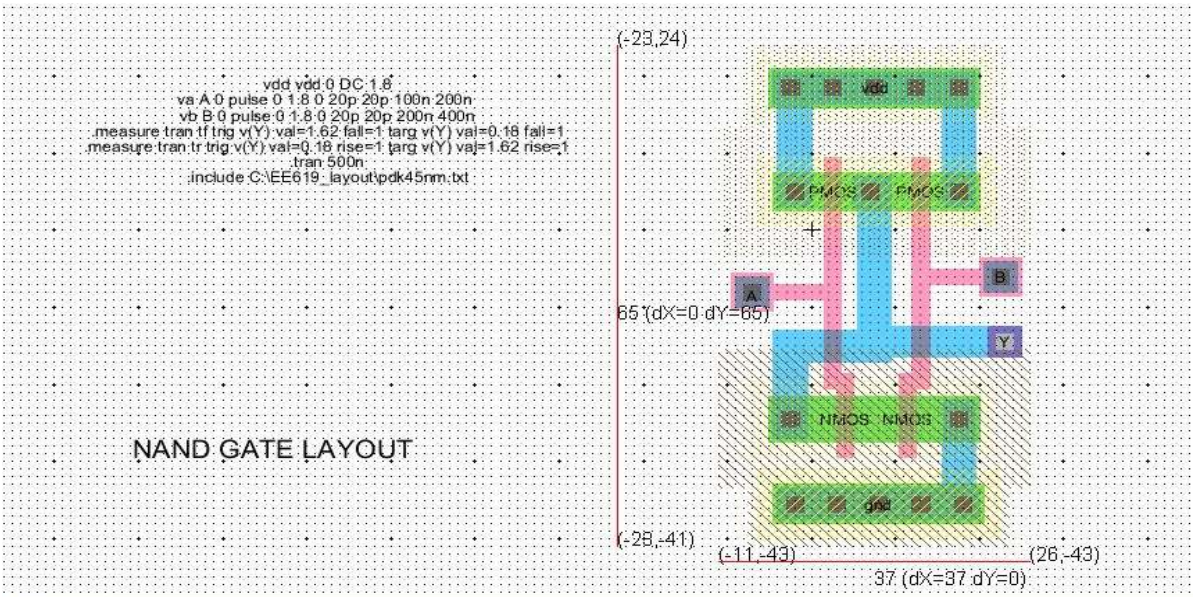
i) worst case t_{plh} :- A=0, B=1 (or) A=1, B=0.

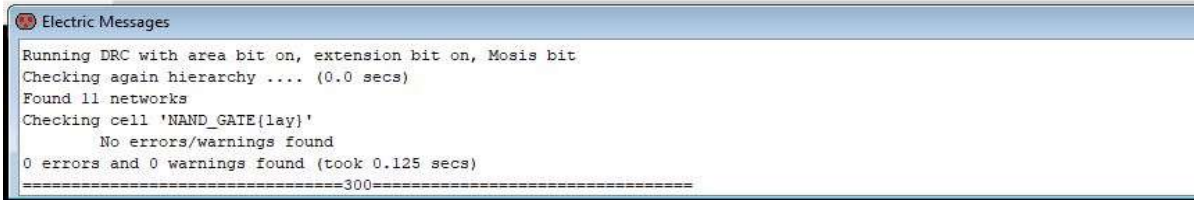
ii) worst case t_{phl} :- A=1 B=1.

We have manipulated gate sizes to match t_{plh} and t_{phl} for given inputs. Thus, we have arrived at pMOS size5 and nMOS size 6 which is in accordance with theoretical value of same size in pMOS & nMOS.

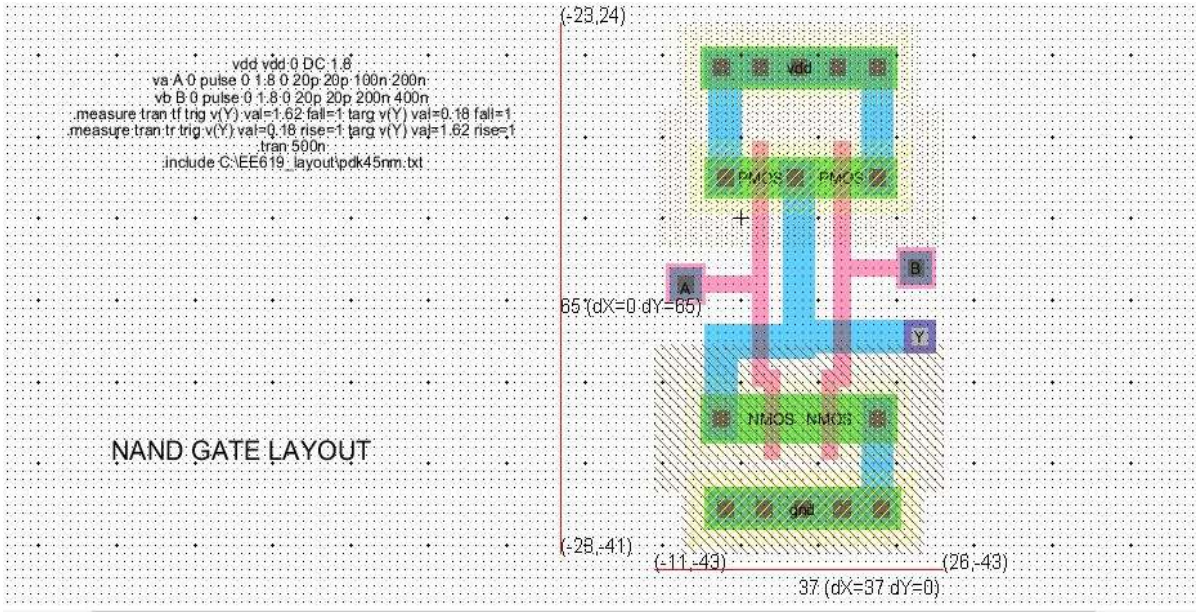
The input given to the circuit is of frequency 1GHz as specified in project problem statement.

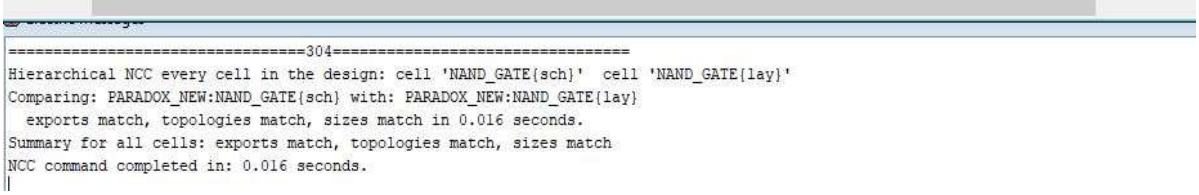
LAYOUT WITH DRC LOG:





LAYOUT WITH LVS LOG:



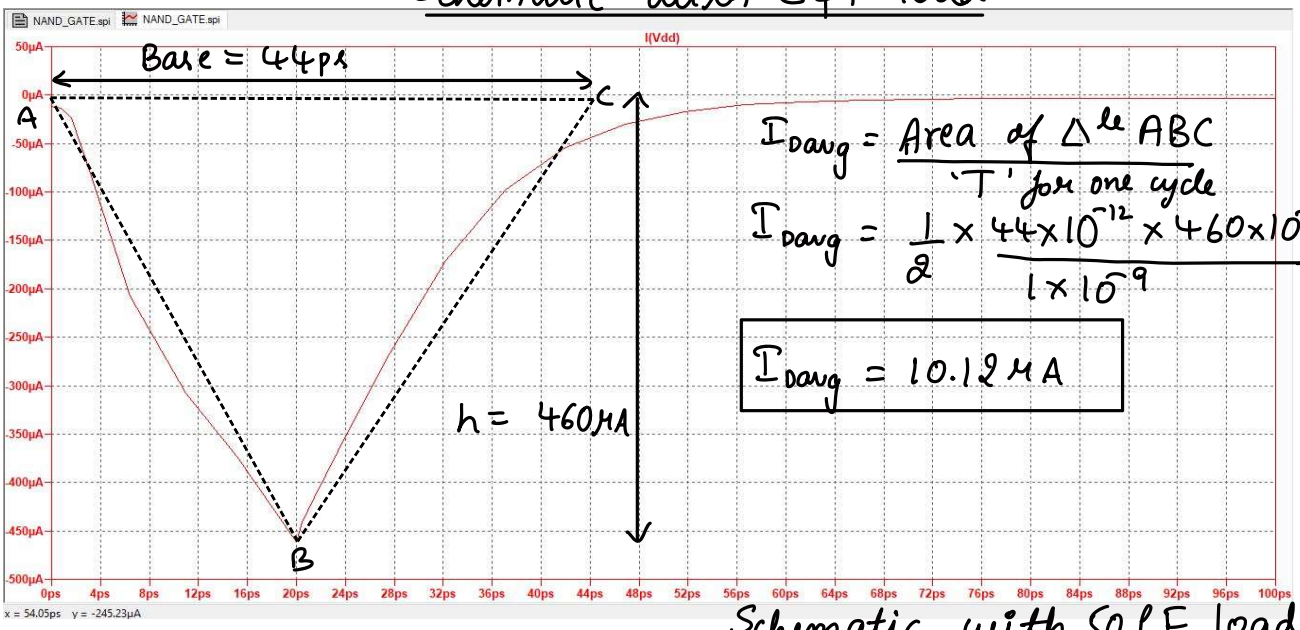


PROPAGATION DELAY:

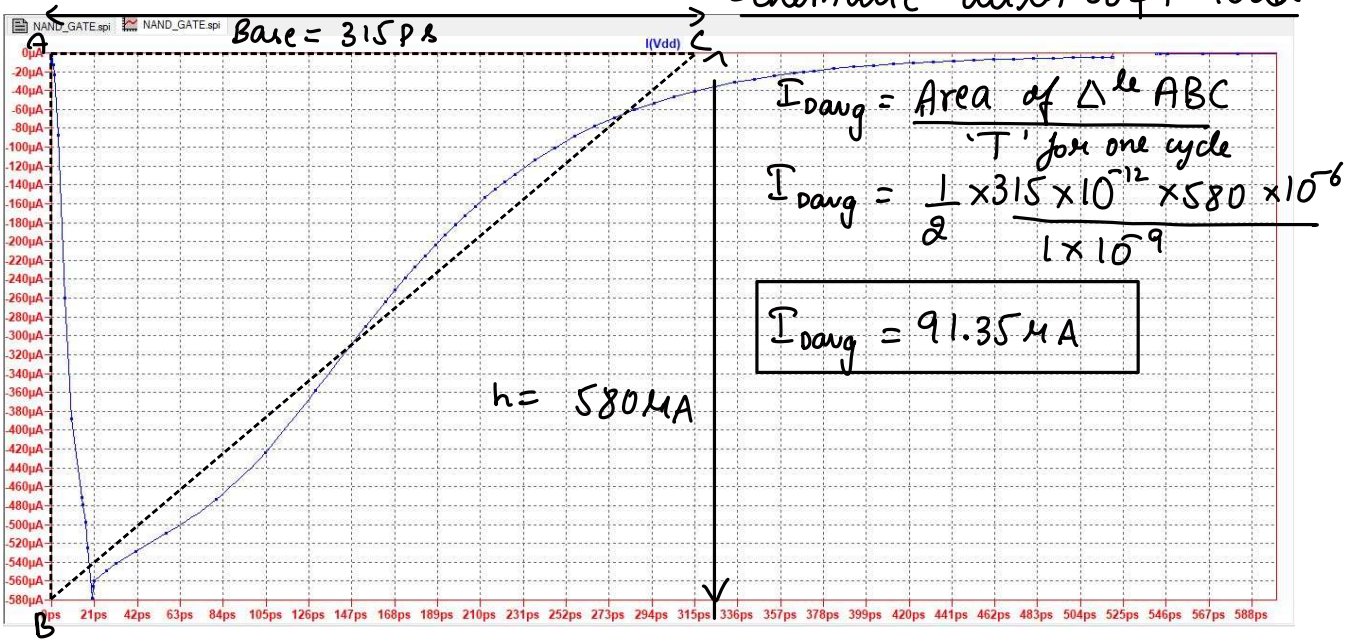
NAND	Schematic			Layout		
Load capacitance	tplh	tphl	average	tplh	tphl	average
5fF	19.9397ps	22.6598ps	21.29975ps	20.8951ps	23.8189ps	22.357ps
50fF	174.089ps	174.767ps	174.428ps	175.082ps	175.279ps	175.1805ps

POWER CONSUMPTION:

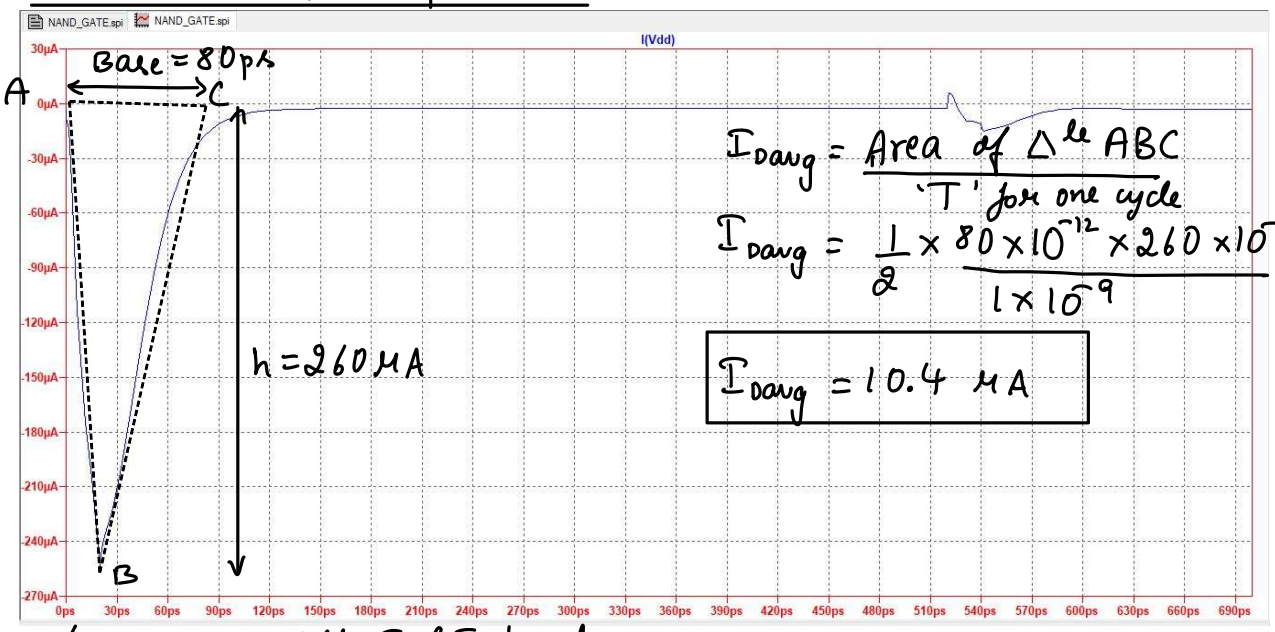
Schematic with 5fF load



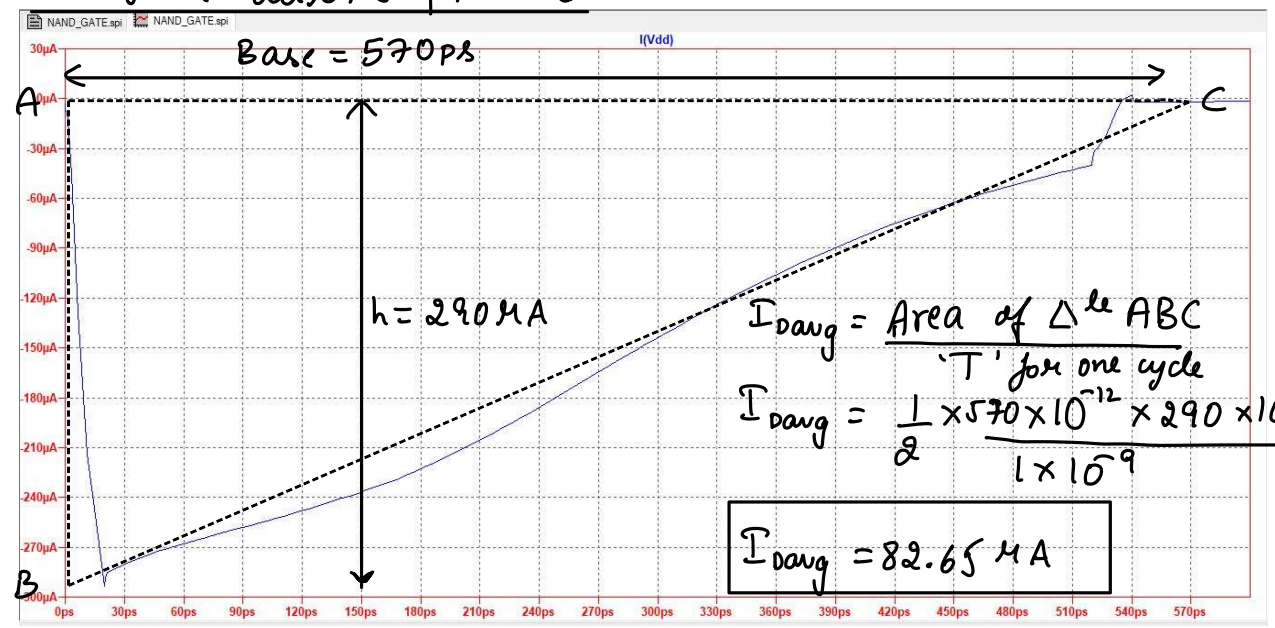
Schematic with 50fF load



Layout with 5fF load



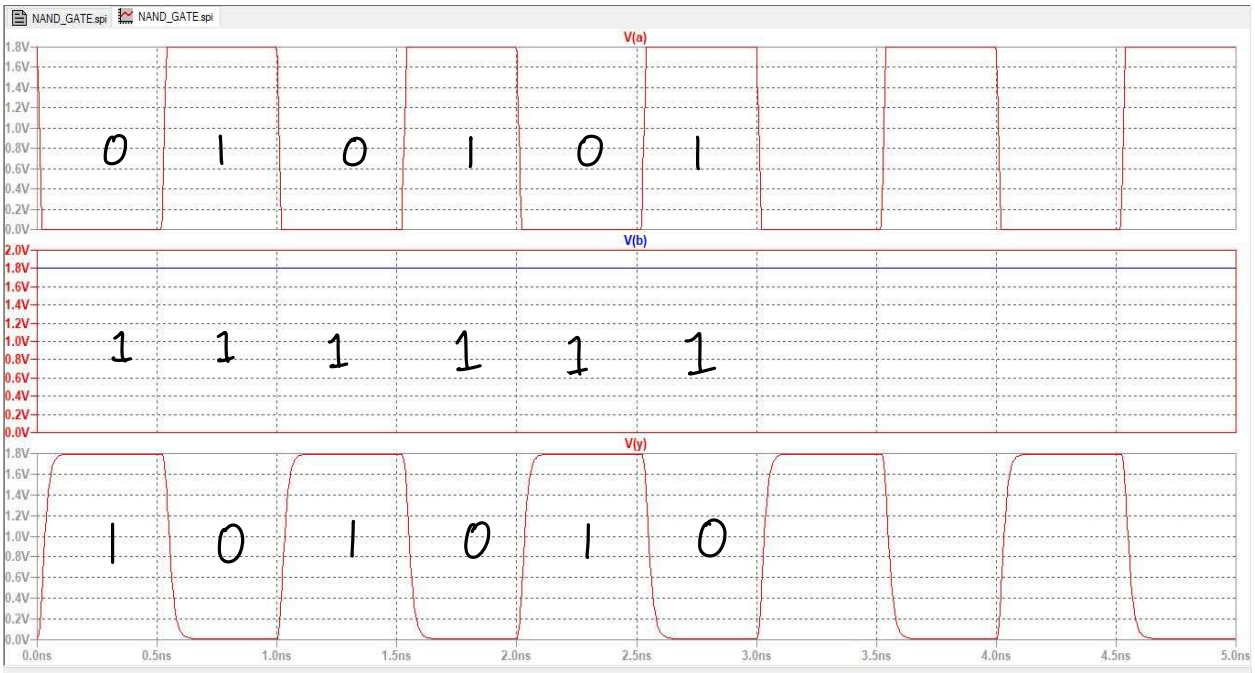
Layout with 50fF load



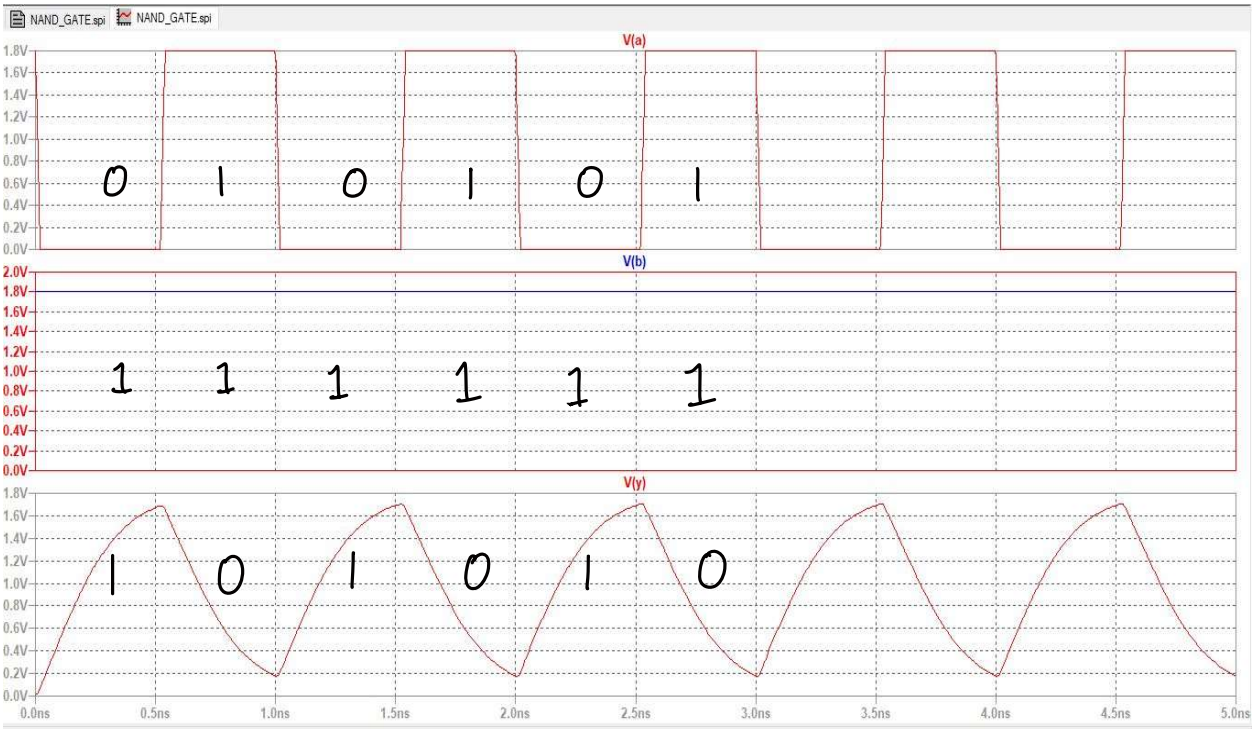
NAND	Schematic			Layout		
Load Capacitance	Average Id	Vdd	Power	Average Id	Vdd	Power
5fF	10.12 μA	1.8	18.21 μW	10.4 μA	1.8	18.72 μW
50fF	91.35 μA	1.8	164.43 μW	82.65 μA	1.8	148.7 μW

TRANSIENT I/O WAVEFORMS:

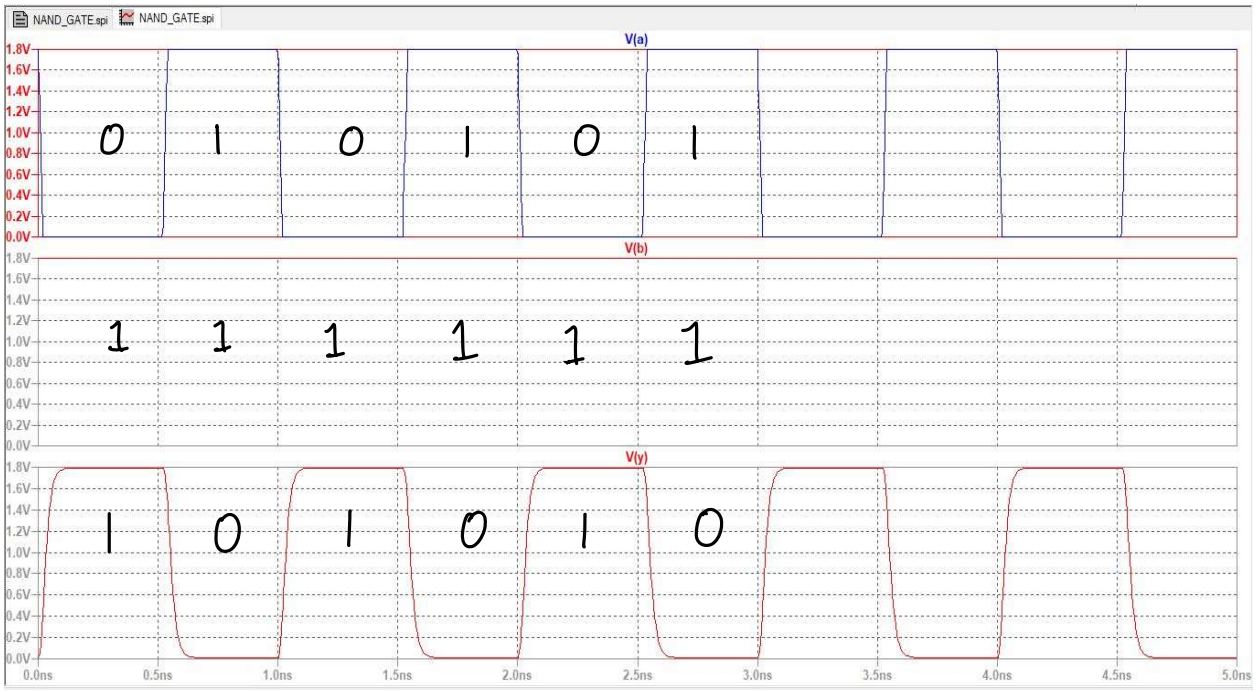
1) FOR SCHEMATIC WITH 5fF LOAD.



2) FOR SCHEMATIC WITH 50fF LOAD



3) FOR LAYOUT WITH 5fF LOAD



4) FOR LAYOUT WITH 50fF LOAD