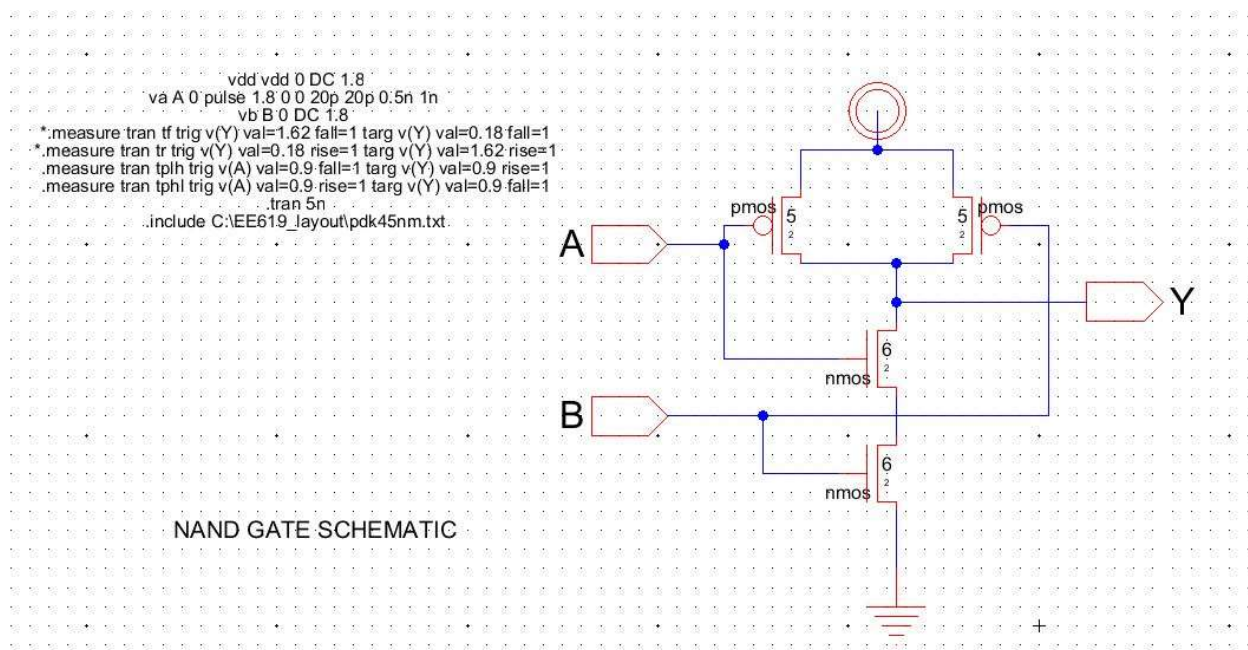


1) NAND GATE

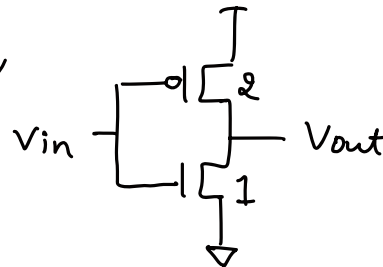
SCHEMATIC:



TOR SIZE EXPLANATION:

For a reference inverter,

In order to equate the
worst case t_{pnh} and



t_{pnl} , we need resistance in pMOS side and nMOS side for worst case input to be same.

For NAND,

i) worst case t_{pnh} :- $A=0, B=1$ (or) $A=1, B=0$.

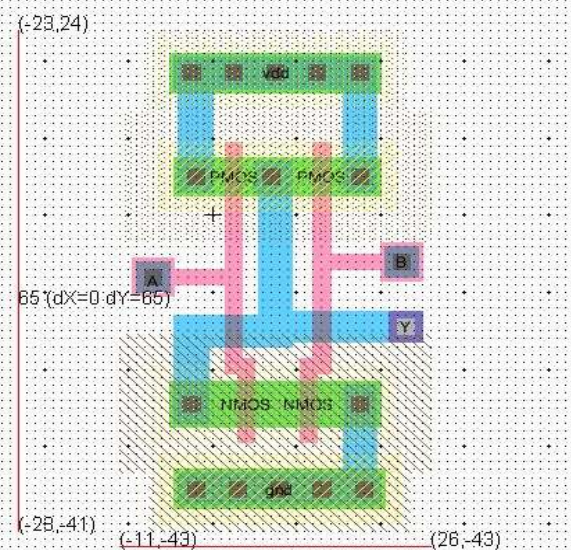
ii) worst case t_{pnl} :- $A=1, B=1$.

We have manipulated gate sizes to match t_{pnh} and t_{pnl} for given inputs. Thus, we have arrived at pMOS size 5 and nMOS size 6 which is in accordance with theoretical value of same size in pMOS & nMOS.

The input given to the circuit is of frequency 1KHz
as specified in project problem statement.

LAYOUT WITH DRC LOG:

NAND GATE LAYOUT



The diagram shows a NAND gate layout on a grid. It includes a PMOS transistor at the top and two NMOS transistors at the bottom. The inputs are labeled A and B, and the output is labeled Y. The layout is bounded by coordinates (-23,24) to (26,-43). Dimensions are given as 65 (dX=0 dY=65) and 37 (dX=37 dY=0).

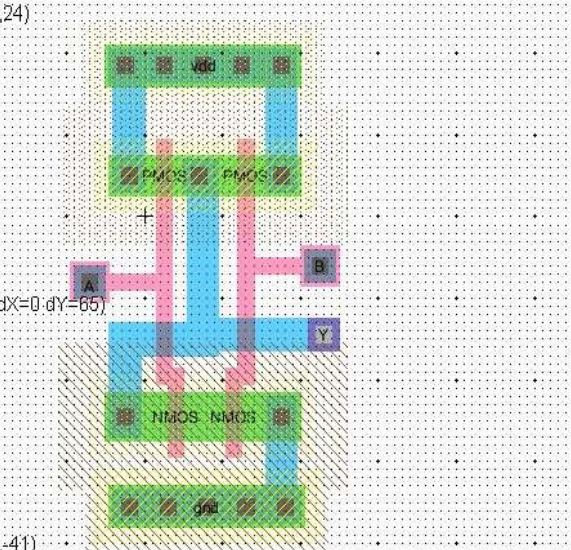
```
vdd vdd 0 DC 1.8
va A 0 pulse 0 1.8 0 20p 20p 100n 200n
vb B 0 pulse 0 1.8 0 20p 20p 200n 400n
.measure tran t1 trig v(Y) val=1.62 fall=1 targ v(Y) val=0.18 fall=1
.measure tran t2 trig v(Y) val=0.18 rise=1 targ v(Y) val=1.62 rise=1
tran 500n
include C:\EE619_layout\pdk45nm.txt
```

Electric Messages

Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy (0.0 secs)
Found 11 networks
Checking cell 'NAND_GATE{lay}'
No errors/warnings found
0 errors and 0 warnings found (took 0.125 secs)
=====300=====

LAYOUT WITH LVS LOG:

NAND GATE LAYOUT



The diagram shows a NAND gate layout on a grid. It includes a PMOS transistor at the top and two NMOS transistors at the bottom. The inputs are labeled A and B, and the output is labeled Y. The layout is bounded by coordinates (-23,24) to (26,-43). Dimensions are given as 65 (dX=0 dY=65) and 37 (dX=37 dY=0).

```
vdd vdd 0 DC 1.8
va A 0 pulse 0 1.8 0 20p 20p 100n 200n
vb B 0 pulse 0 1.8 0 20p 20p 200n 400n
.measure tran t1 trig v(Y) val=1.62 fall=1 targ v(Y) val=0.18 fall=1
.measure tran t2 trig v(Y) val=0.18 rise=1 targ v(Y) val=1.62 rise=1
tran 500n
include C:\EE619_layout\pdk45nm.txt
```

=====304=====

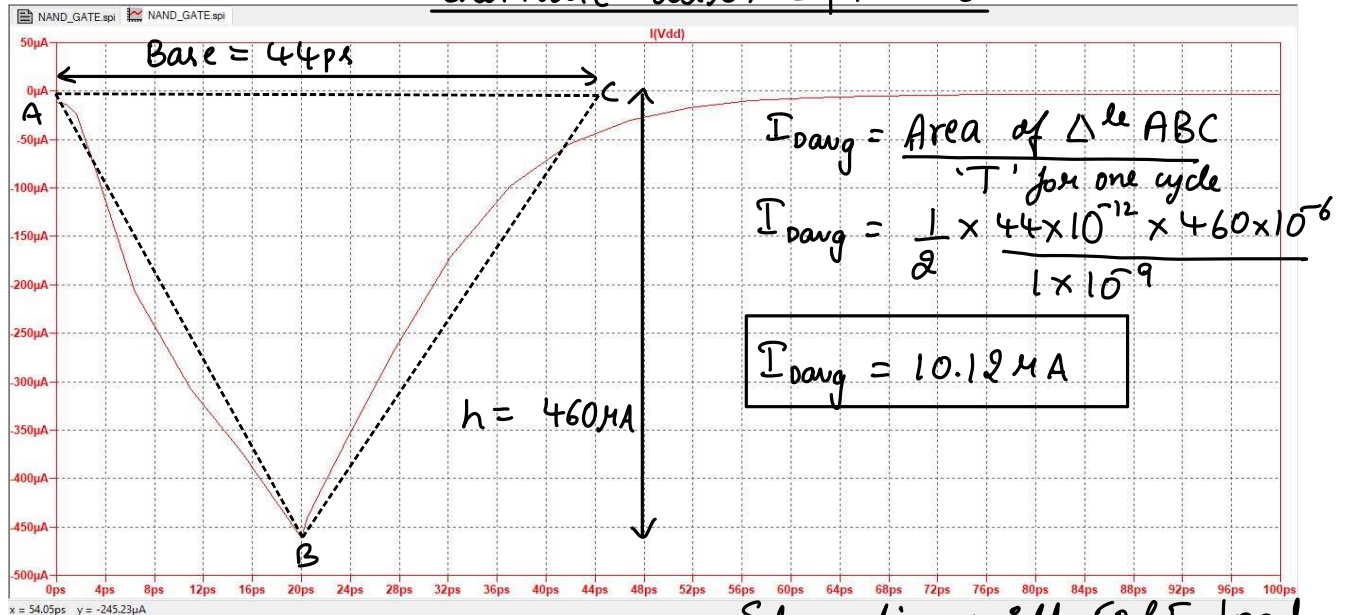
Hierarchical NCC every cell in the design: cell 'NAND_GATE{sch}' cell 'NAND_GATE{lay}'
Comparing: PARADOX_NEW:NAND_GATE{sch} with: PARADOX_NEW:NAND_GATE{lay}
exports match, topologies match, sizes match in 0.016 seconds.
Summary for all cells: exports match, topologies match, sizes match
NCC command completed in: 0.016 seconds.

PROPAGATION DELAY:

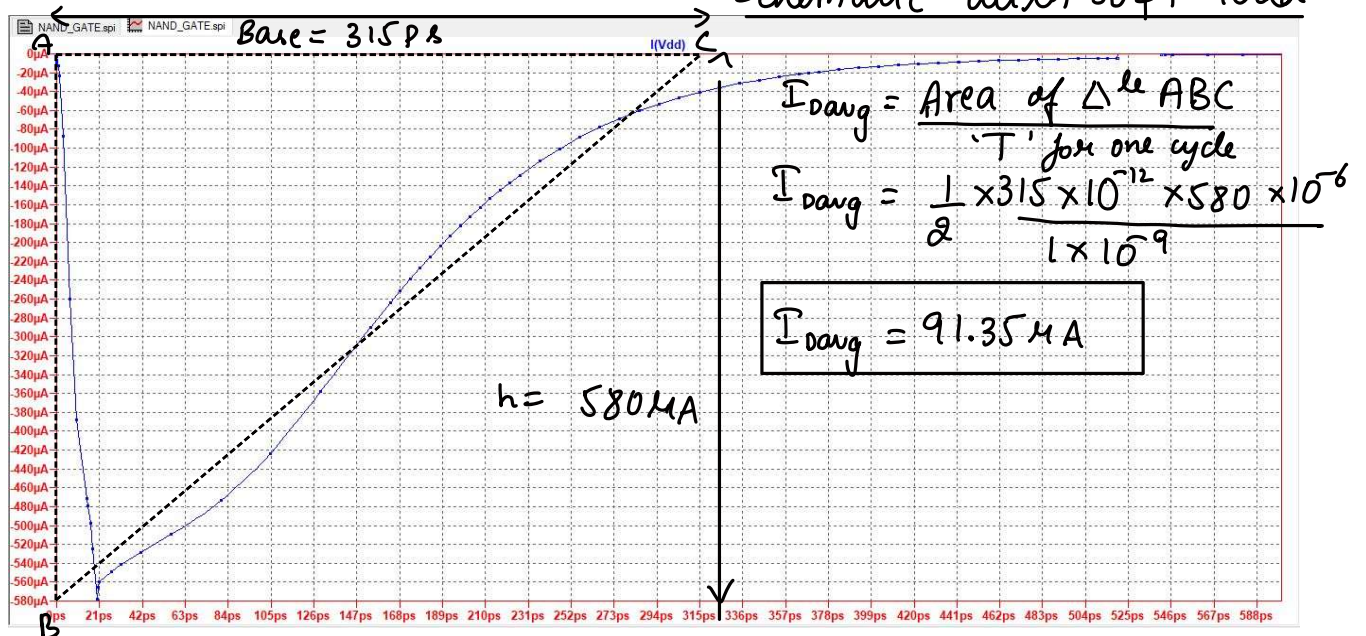
NAND	Schematic			Layout		
Load capacitance	tplh	tphl	average	tplh	tphl	average
5fF	19.9397ps	22.6598ps	21.29975ps	20.8951ps	23.8189ps	22.357ps
50fF	174.089ps	174.767ps	174.428ps	175.082ps	175.279ps	175.1805ps

POWER CONSUMPTION:

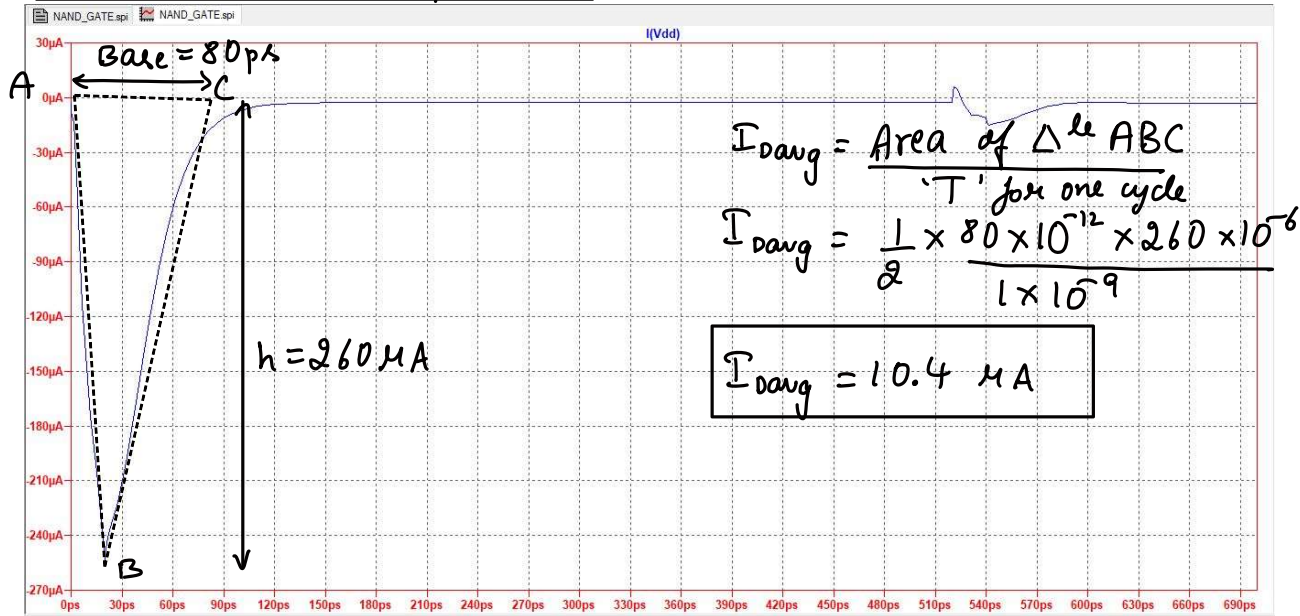
Schematic with 5fF load



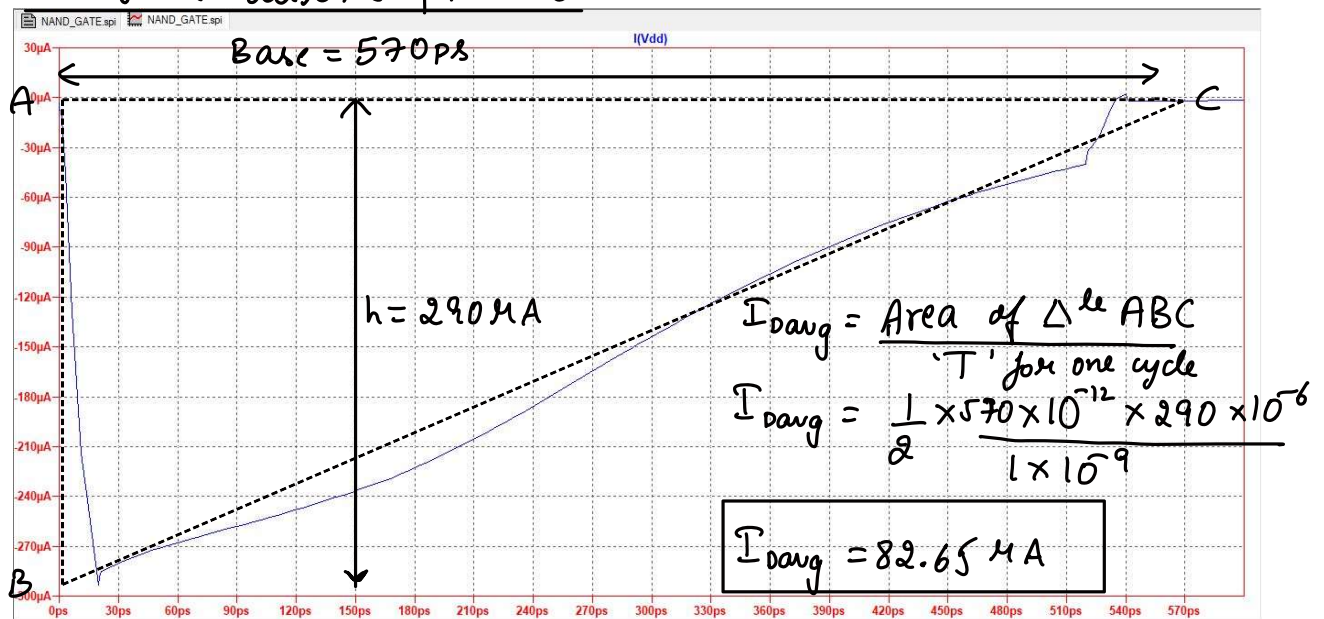
Schematic with 50fF load



Layout with 5fF load



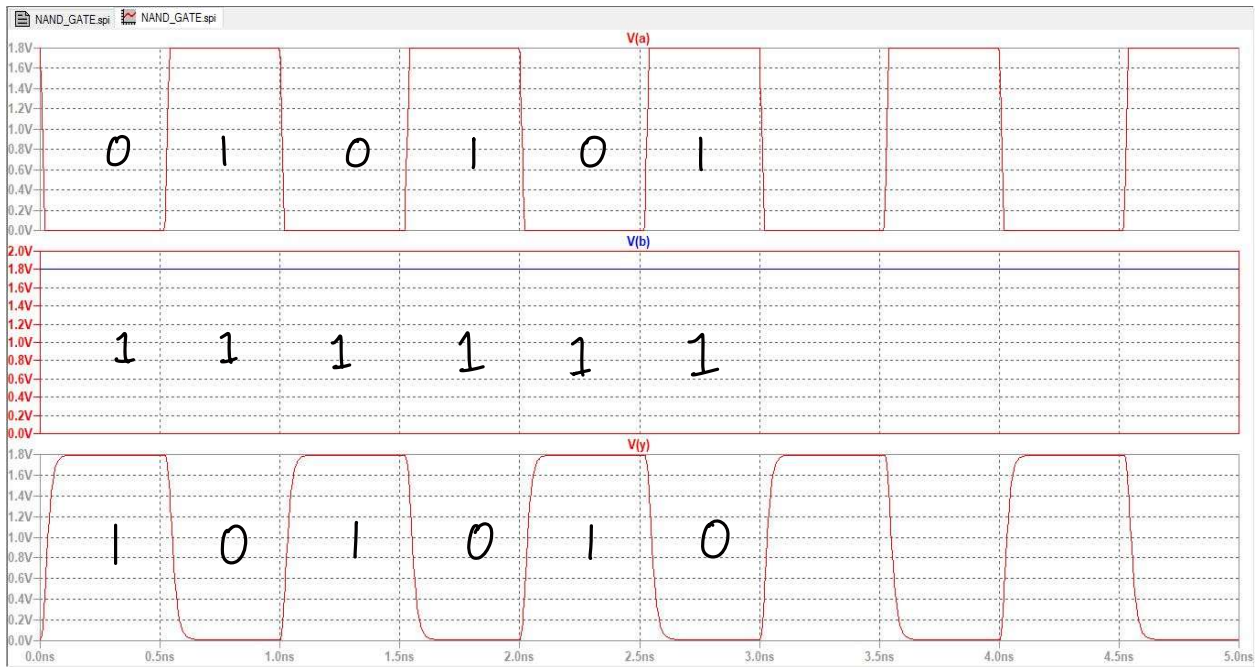
Layout with 50fF load



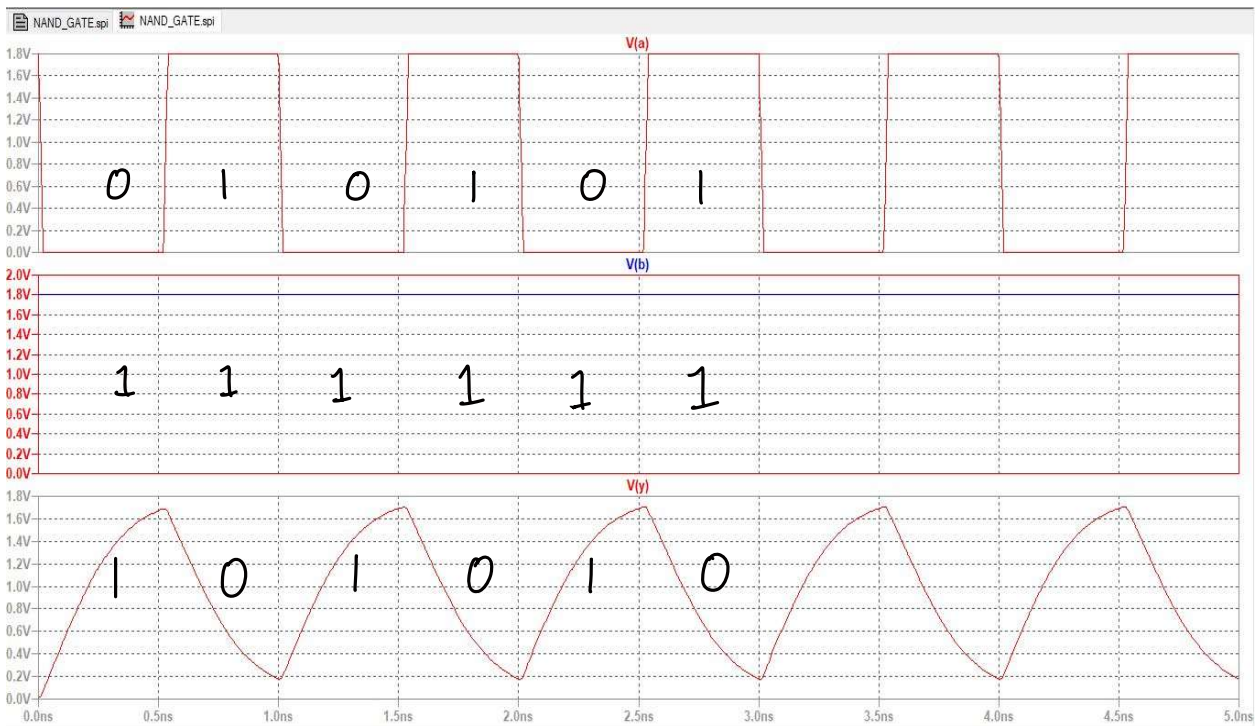
NAND	Schematic			Layout		
Load Capacitance	Average Id	Vdd	Power	Average Id	Vdd	Power
5fF	10.12 μA	1.8	18.21 μW	10.4 μA	1.8	18.72 μW
50fF	91.35 μA	1.8	164.43 μW	82.65 μA	1.8	148.7 μW

TRANSIENT I/O WAVEFORMS:

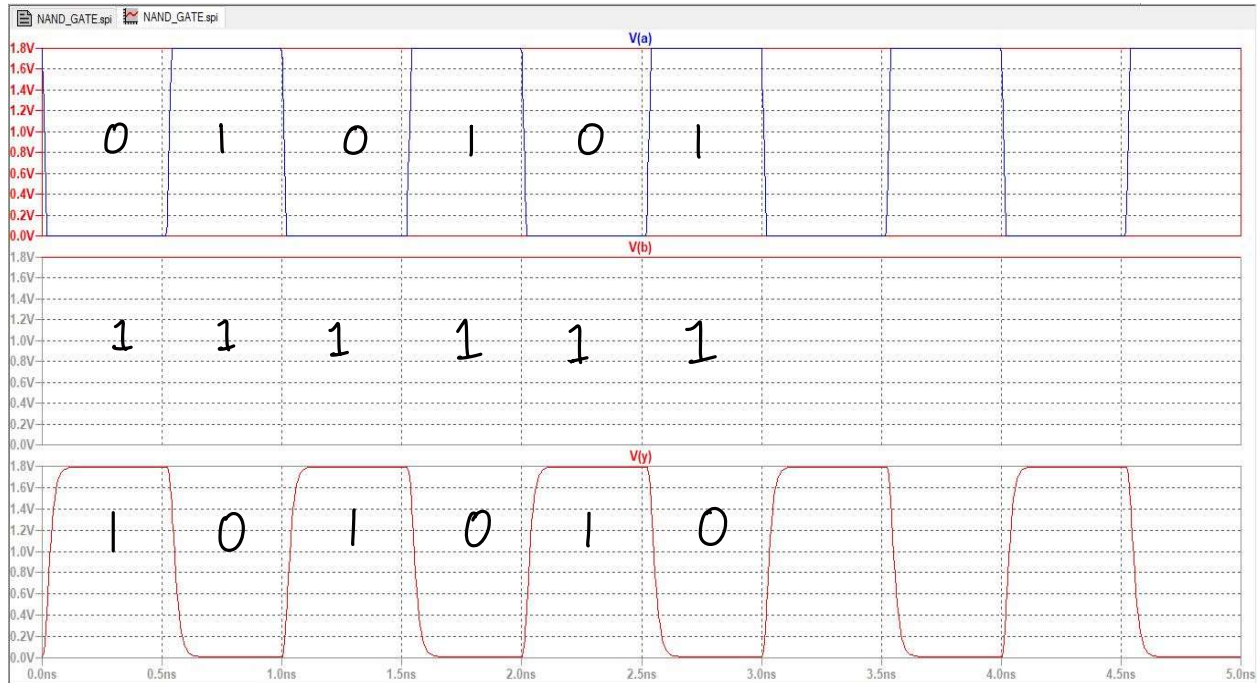
1) FOR SCHEMATIC WITH 5fF LOAD.



2) FOR SCHEMATIC WITH 50fF LOAD



3) FOR LAYOUT WITH 5fF LOAD



4) FOR LAYOUT WITH 50fF LOAD

