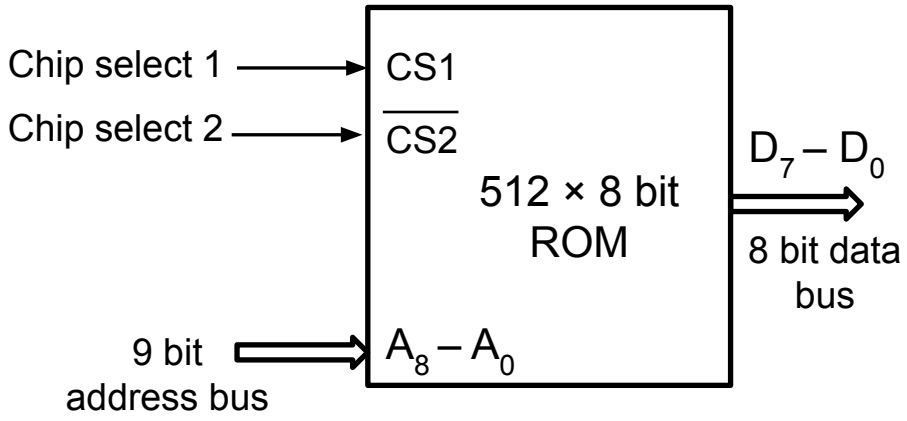
Block diagram of ROM chip



To construct a 2 KB RAM chip
How many 128 B RAM chips are required?

Big RAM chip size = 2 KB = $2^1 \times 2^{10}$ B = 2^{11} B

Available small RAM chip size = 128 B = 2^7 B

Number of 128 B RAM chips require =

$$= \frac{\text{Big RAM chip size}}{\text{Available small RAM chip size}}$$

$$= \frac{2^{11}\ \text{B}}{2^7}$$

$$= 2^4\ \text{B}$$

$$= 16$$

Design a big RAM chip using small RAM chips

To construct a 256 B RAM chip How many 128 B RAM chips are required?

Big RAM chip size = 256 B
Available small RAM chip size = 128 B

Number of 128 B RAM chips =

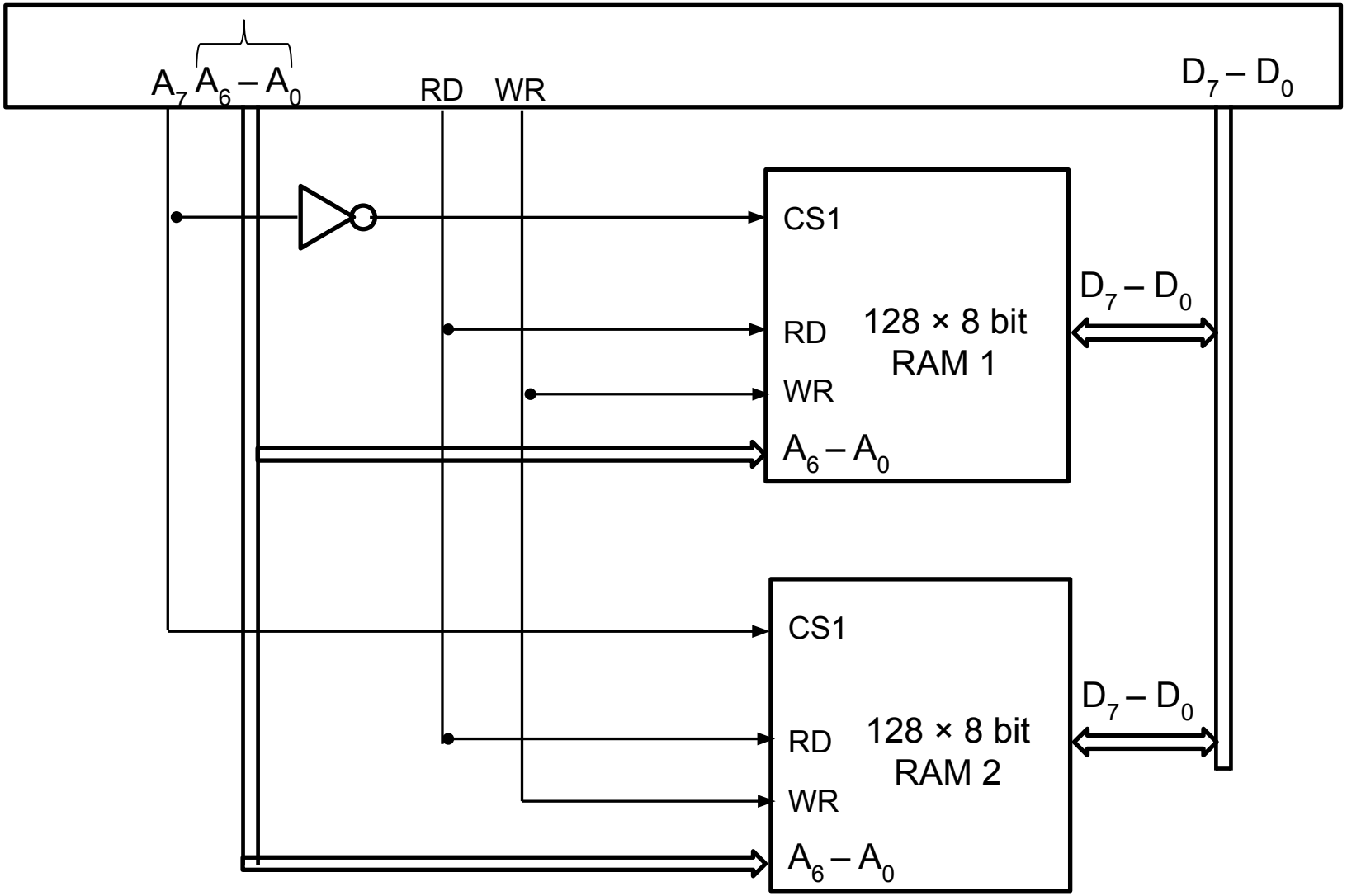
$$= \frac{\text{Big RAM chip size}}{\text{Available small RAM chip size}}$$

$$= \frac{256\ \text{B}}{128\ \text{B}}$$

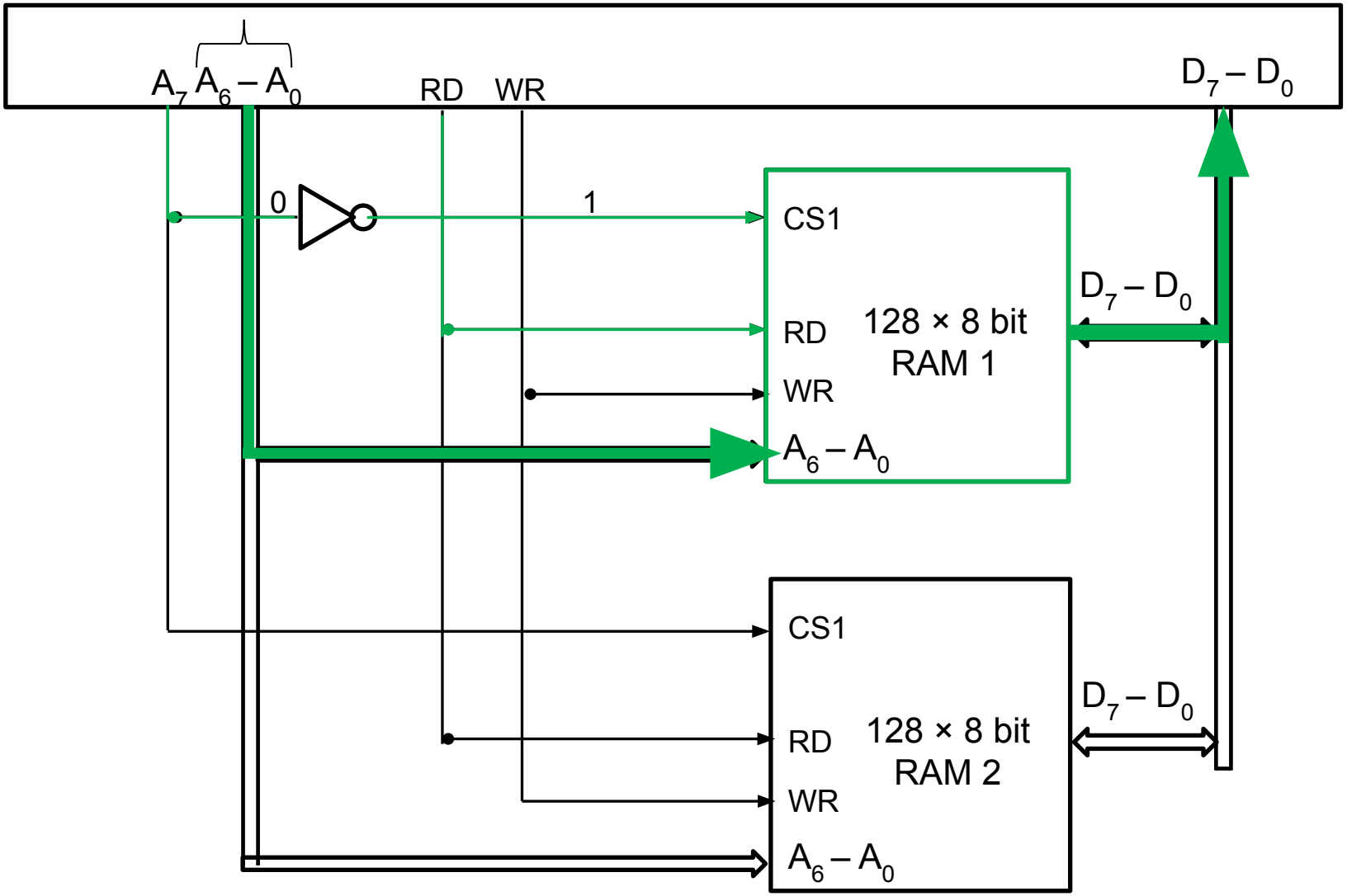
$$= 2$$

Number of Address bits for small RAM chip = 7 ($A_6 - A_0$)
Number of Address bits for big RAM chip = 8 ($A_7 - A_0$) Click here
Number of Data bits for big RAM chip and small RAM chip are same and is equal to 8 ($D_7 - D_0$)

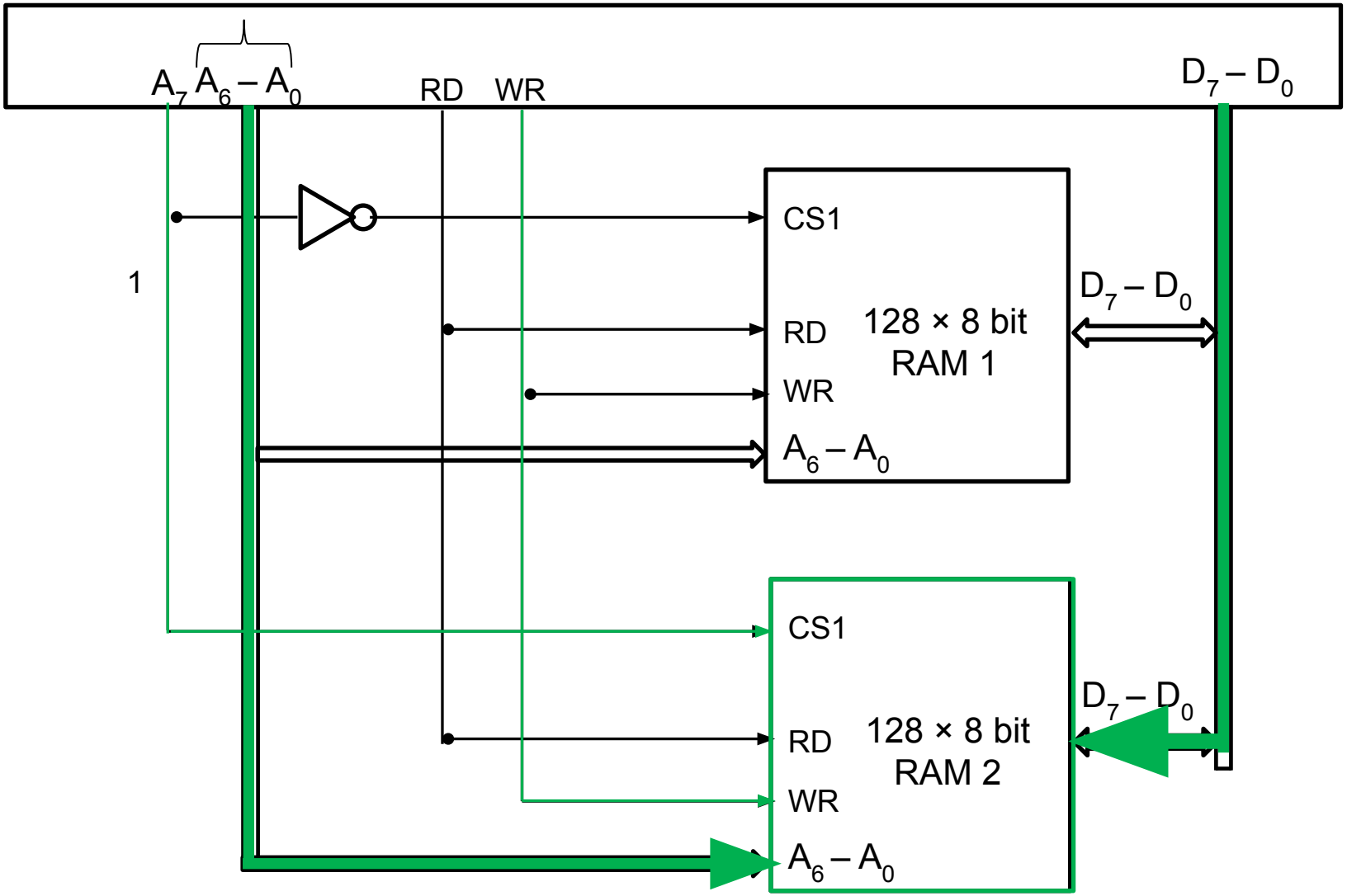
Memory connection to the CPU



Memory Read operation from RAM 1



Memory Write operation into RAM 2



Memory Address Map

Component	Hexadecimal Address	Address bus A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
RAM 1	00 – 7F	0	×	×	×	×	×	×	×
RAM 2	80 – FF	1	×	×	×	×	×	×	×

Click here

Design a big RAM chip using small RAM chips contd.

To construct a 1 KB RAM chip How many 256 B RAM chips are required?

Big RAM chip size = 1 KB = 1024 B
Available small RAM chip size = 256 B

Number of 256 B RAM chips require =

$$= \frac{\text{Big RAM chip size}}{\text{Available small RAM chip size}}$$

$$= \frac{1024\ \text{B}}{256\ \text{B}}$$

$$= 4$$

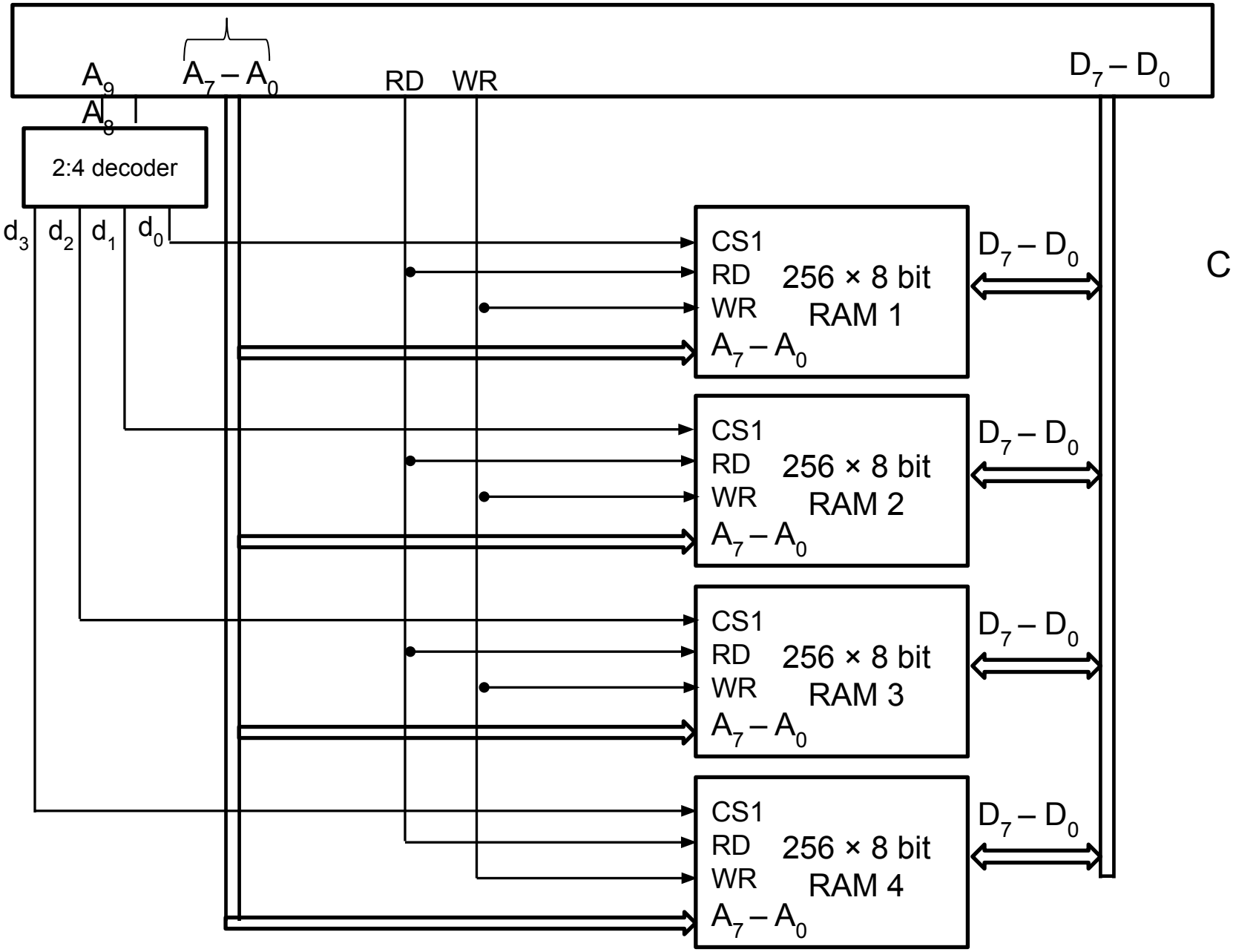
Number of Address bits for small RAM chip = 8 ($A_7 – A_0$)
Number of Address bits for big RAM chip = 10 ($A_9 – A_0$)
Number of Data bits for big RAM chip and small RAM chip are same and is equal to 8 ($D_7 – D_0$)

Memory Address Map

Component	Hexadecimal Address	Address bus A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
RAM 1	0000 – 00FF	0	0	×	×	×	×	×	×	×	×
RAM 2	0100 – 01FF	0	1	×	×	×	×	×	×	×	×
RAM 3	0200 – 02FF	1	0	×	×	×	×	×	×	×	×
RAM 4	0300 – 03FF	1	1	×	×	×	×	×	×	×	×

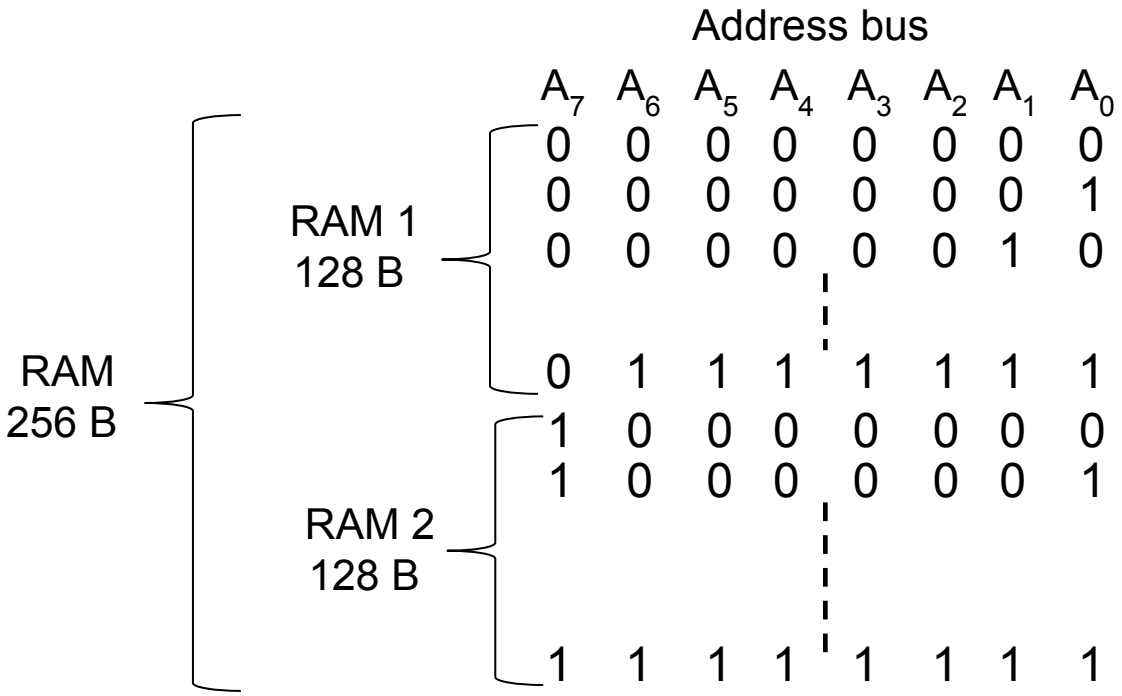
Click here

Memory connection

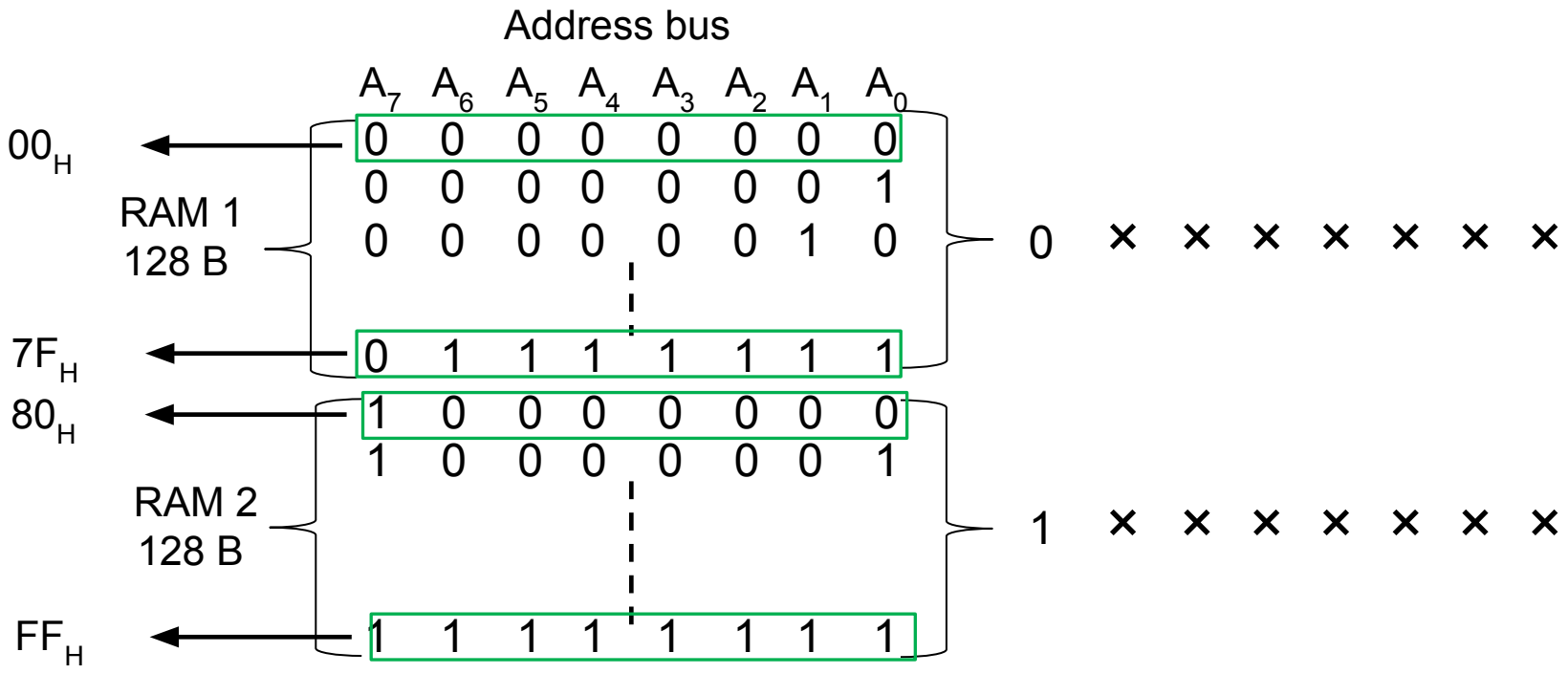


Click here

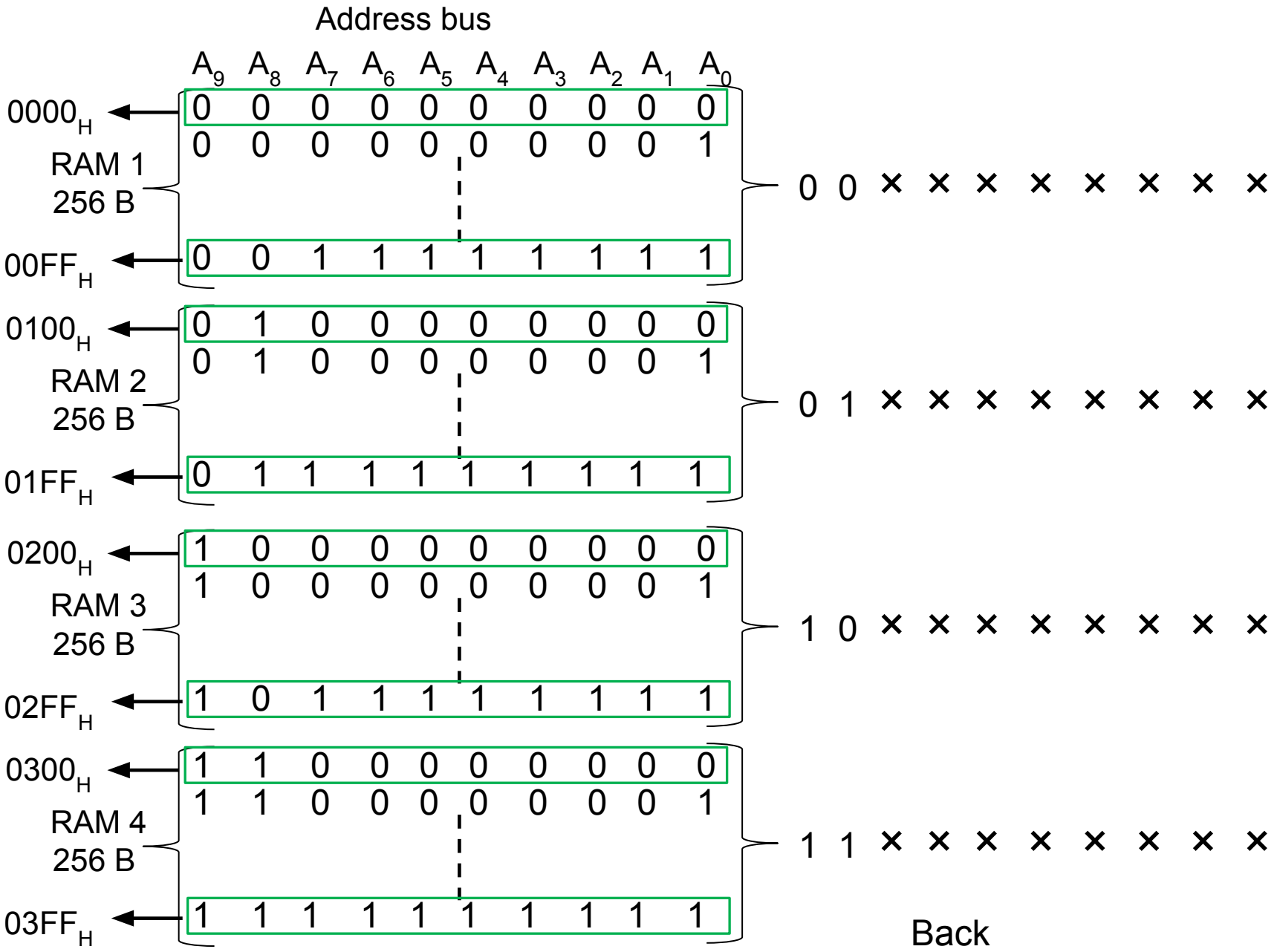
Thank You


Address bus
A7 A6 A5 A4 A3 A2 A1 A0
RAM 256 B
RAM 1 128 B
0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 1
0 0 0 0 0 0 1 0
0 1 1 1 1 1 1 1
RAM 2 128 B
1 0 0 0 0 0 0 0
1 0 0 0 0 0 0 1
1 1 1 1 1 1 1 1

Back


Address bus
A7 A6 A5 A4 A3 A2 A1 A0
00H
0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 1
RAM 1
128 B
0 0 0 0 0 0 1 0
0 × × × × × × ×
7FH
0 1 1 1 1 1 1 1
80H
1 0 0 0 0 0 0 0
1 0 0 0 0 0 0 1
RAM 2
128 B
1 × × × × × × ×
FFH
1 1 1 1 1 1 1 1

Back


Address bus
A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
0000H
0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 1
RAM 1
256 B
00FFH
0 0 1 1 1 1 1 1 1 1
0 0 × × × × × × × ×
0100H
0 1 0 0 0 0 0 0 0 0
0 1 0 0 0 0 0 0 0 1
RAM 2
256 B
01FFH
0 1 1 1 1 1 1 1 1 1
0 1 × × × × × × × ×
0200H
1 0 0 0 0 0 0 0 0 0
1 0 0 0 0 0 0 0 0 1
RAM 3
256 B
02FFH
1 0 1 1 1 1 1 1 1 1
1 0 × × × × × × × ×
0300H
1 1 0 0 0 0 0 0 0 0
1 1 0 0 0 0 0 0 0 1
RAM 4
256 B
03FFH
1 1 1 1 1 1 1 1 1 1
1 1 × × × × × × × ×
Back

Decoder Specification

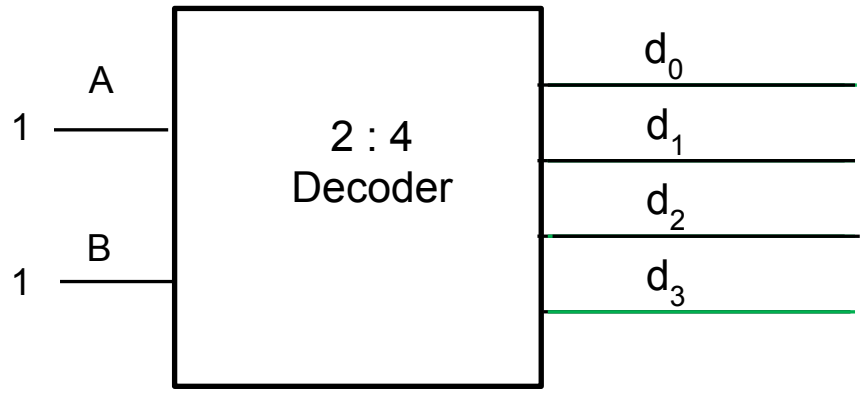
N : 2^N Decoder => N inputs and 2^N outputs

2 : 4 Decoder => 2 inputs and 4 outputs

3 : 8 Decoder => 3 inputs and 8 outputs

4 : 16 Decoder => 4 inputs and 16 outputs

Decoder



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