

The University of Texas at Dallas

Department of Electrical Engineering

EECT 6326 ANALOG INTEGRATED CIRCUIT DESIGN
“DESIGN OF FULLY COMPENSATED TWO STAGE OP-AMP &
SCHMITT TRIGGER USING IT”

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PROBLEM STATEMENT AND DESIGN SPECIFICATION

This project is aimed to implement a Schmitt trigger circuit and a single threshold comparator, both using OP-AMP, to compare their behavior in noisy environment. To do that, first I am designing an OP-AMP with the design specifications given below.

Design a two-stage differential input and single-ended output amplifier. The amplifier is to be powered from a 3.3 volts power supply. The current sources/sinks required for biasing can be derived from the given current reference using current mirrors. Use TSMC CMOS 0.35- μ m technologies to best meet the following specifications:

1. Differential voltage gain: $A_{vd} \geq 60\text{dB}$.
2. Output voltage swing range: $OVSR = V_o(\text{max}) - V_o(\text{min}) \geq 2\text{V}$.
3. Slew rate: $SR \geq 10 \text{ V}/\mu\text{s}$.
4. Input common mode range: $ICMR \geq 1.8\text{V}$.
5. Common mode rejection ratio: $CMRR \geq 70 \text{ dB}$.
6. Unity Gain-bandwidth: $GB \geq 8 \text{ MHz}$ with a 10 pF load capacitance.
7. Phase Margin: $f(GB) \geq 60^\circ$ with a 10 pF load capacitance.
8. Power dissipation: $P_{diss} \leq 1\text{mW}$.

THEORY OF OPERATION

The Schmitt trigger is a comparator circuit with two thresholds. The main difference between normal comparator and Schmitt trigger is that the later one provides a hysteresis between two thresholds. This greatly improves the performance of the circuit when there is noise in input. Image below shows this difference.

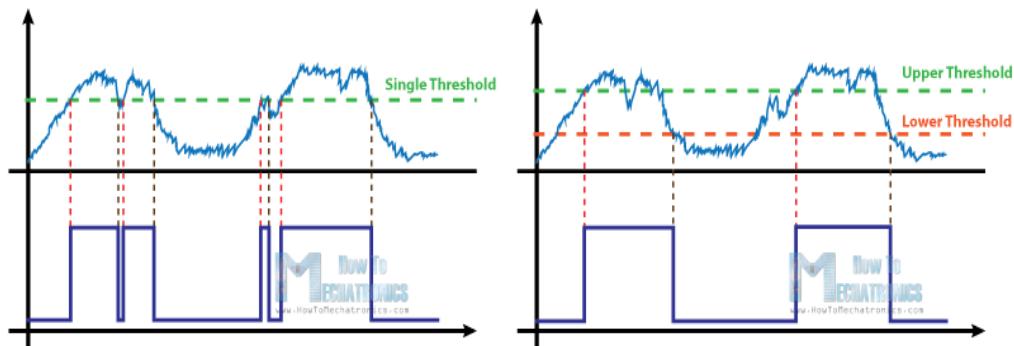


Figure 1 Comparison of performance of Single threshold comparator and Schmitt trigger in noisy input
Image source: <https://howtomechatronics.com/how-it-works/electrical-engineering/schmitt-trigger/>

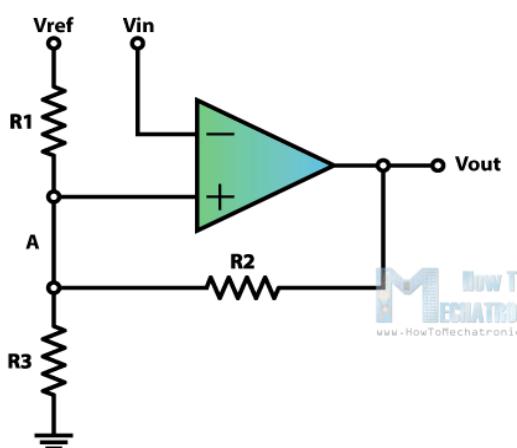


Figure 2 Schematic Diagram of Schmitt Trigger
Image source: <https://howtomechatronics.com/how-it-works/electrical-engineering/schmitt-trigger/>

This circuit has only two output states, either low or high. The voltage at point A determines the two required reference voltages.

When the output is low the resistors R2 and R3 comes in parallel to each other and Va is given as:

$$V_a = \frac{R2||R3}{R1 + R2||R3} \times V_{ref}$$

This gives us the higher threshold.

When output is low then R2 and R1 comes in parallel and Va is given as:

$$V_a = \frac{R3}{R3 + R1||R2} \times V_{ref}$$

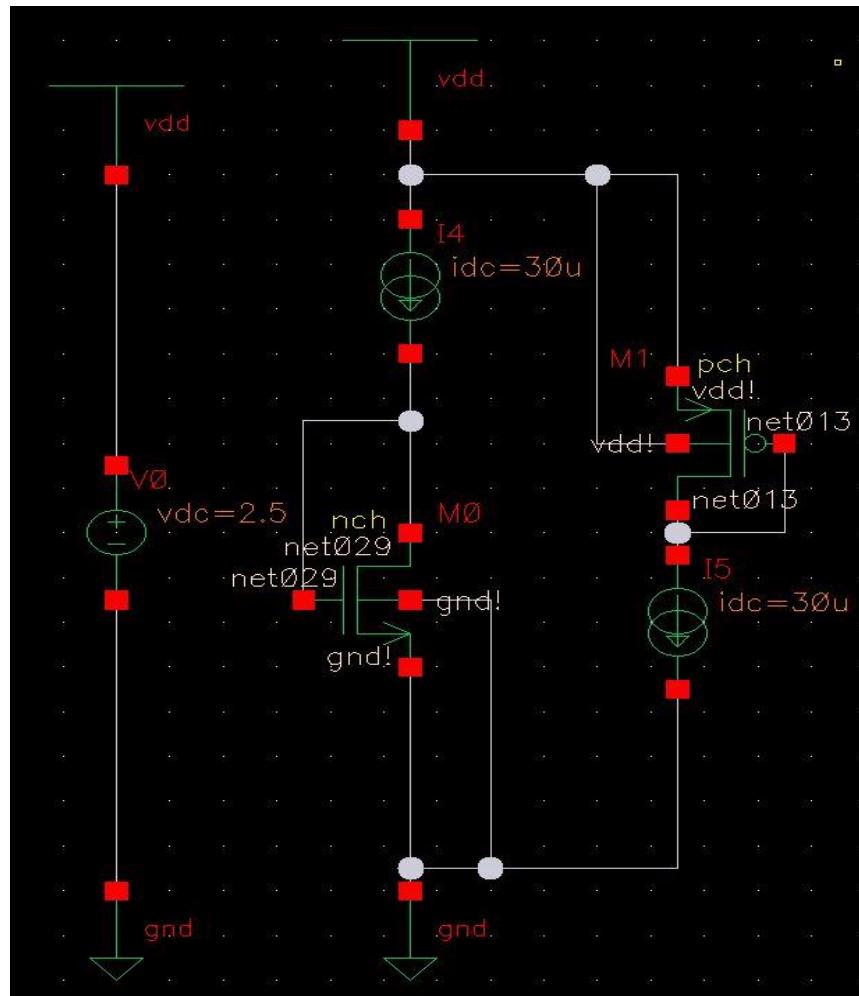
This gives us the lower threshold voltage. The values selected by me are:

R1 = R2 = R3 = 10kΩ and Vref = Vdd = 3.3 Volts.

With these values the lower threshold comes out to be 1.1V and higher threshold comes out to be 2.2V.

CALCULATION OF THRESHOLD VOLTAGES AND $\mu nCox / \mu pCox$

Before proceeding to designing of the OPAMP I needed the values of threshold voltages and process trans-conductance of the NMOS and PMOS devices. To get that, I did the following setup in Cadence.



After getting the DC operating points of these devices I got following values:

Table 1 Threshold and process trans conductance calculation

Parameter	NMOS	PMOS
$ V_{th} $	$V_{th_min} : 0.52 \text{ V}$ $V_{th_max} : 0.96 \text{ V}$	$V_{th} : 0.72\text{V}$
K_n'	$200\mu\text{A/V}$	$60\mu\text{A/V}$

DESIGN PROCEDURE

To design the Schmitt trigger the most important thing is to design the operational amplifier. Once the OPAMP is designed then Schmitt trigger can be easily implemented using it. In order to achieve required gain, we need to use two-stage amplifier. I am using Two Stage Amplifier for my design as shown below. This is my initial design. Further changes will be made if needed.

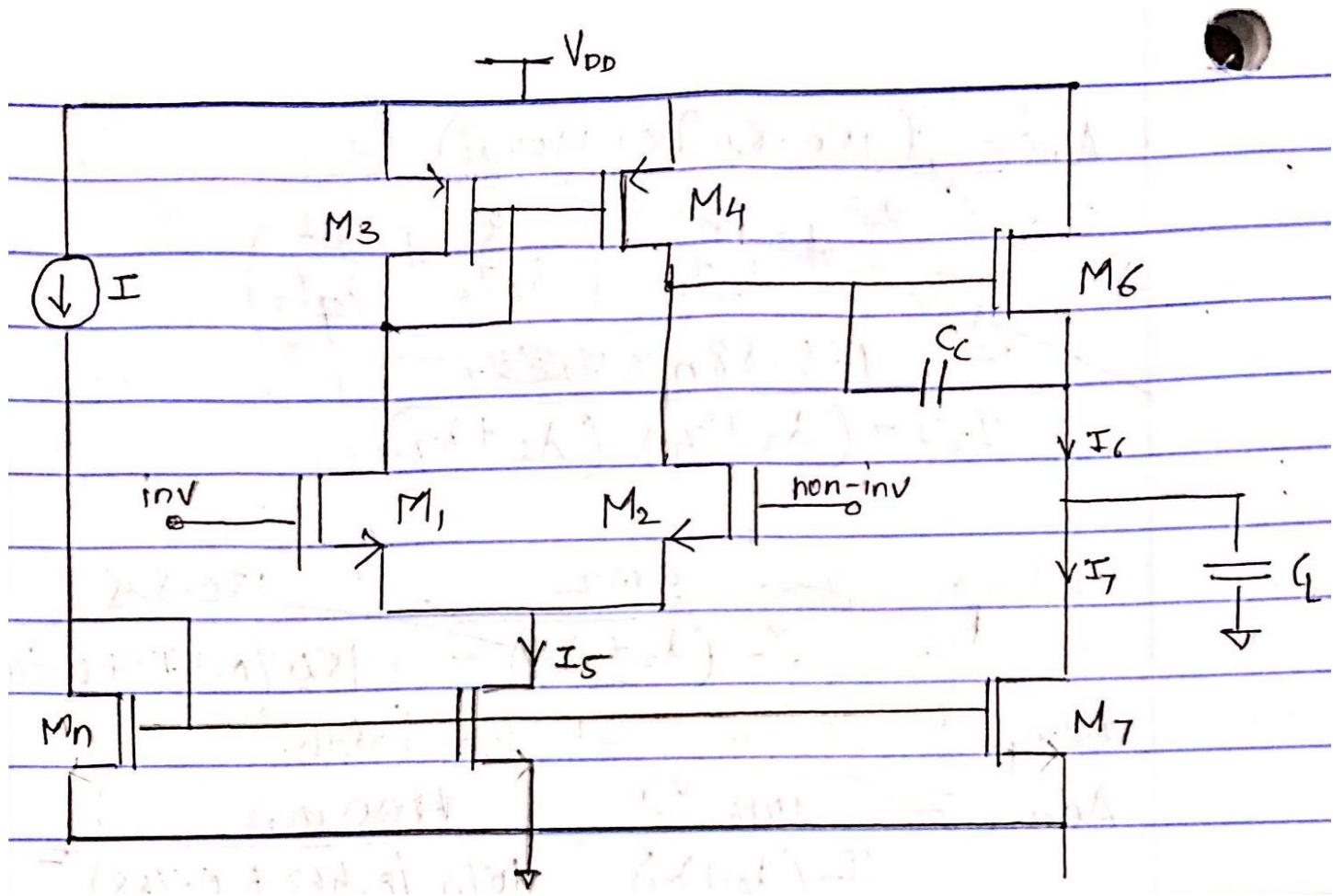


Figure 3 A Two-Stage Miller Compensated Amplifier

DESIGN OF OP-AMP:

1) For $\phi_m = 60^\circ$, $C_c \geq 0.22C_L$
 $\therefore C_c \geq 2.2\text{pF}$

Selecting $C_c = 3.0\text{pF}$

$$SR = \frac{I_S}{C_c} \therefore I_S = 3 \times 10 \times p = 30\mu A$$

2) Calculation of S_1 & S_2 :

$$g_m = 2\pi \times G_B W \times C_c = 2\pi \times 8 \text{M} \times 3 \text{p}$$

$$\therefore g_m \approx 150\mu S$$

$$S_1 = S_2 = \frac{g_m^2}{k'_n \times I_S} = \frac{(150 \cdot 8 \mu)^2}{200\mu \times 30\mu}$$

$$S_1 = S_2 \approx 4$$

3) Calculation of S_3 & S_4 :

$$S_3 = \frac{I_S}{k'_p [V_{DD} - V_{inmax} - V_{th3max} + V_{thmin}]^2}$$

$$= \frac{30\mu}{60\mu [3.3 - 3.1 - 0.72 + 0.65]^2}$$

$$\therefore S_3 = S_4 \approx 30$$

4) Calculation of S_5 :

$$V_{dsat_5} \geq V_{min} = \sqrt{2I_2} - V_{th\max}$$

$$\geq 1.3 - \sqrt{\frac{300}{200 \times 4}} - 0.95 \geq 0.05$$

$$S_5 = \frac{2I_5}{k'_n (V_{dsat_5})^2} = 120 \leftarrow \text{This is too large}$$

\therefore Increasing S_1 & S_2 to 7 from 4

$$\therefore \text{new } g_m = 204.98 \mu S$$

$$\text{Now, } V_{dsat_5} \geq 1.3 - 0.14 - 0.96 \geq 0.1$$

$$\therefore S_5 = 30 \leftarrow \text{Reasonable}$$

5) Calculation of S_6 & I_6 :

For OCMR $\geq 2V$

$$\text{deciding } V_{max} = 3.1V \text{ & } V_{min} = 0.6V$$

which is very reasonable & also satisfying
specs, $(3.1 - 0.6 = 2.5) \geq 2V$

$$\therefore V_{dsat\min} \Rightarrow 3.3 - 3.1 = 0.2V.$$

for $\phi_m = 60^\circ$, $P_2 \geq 2.2 \text{ GBW}$

$$\therefore \frac{gM_6}{C_L} = 2.2 \frac{gM_2}{C_C} \therefore gM_6 = 2.2 C_L \times \frac{gM_2}{C_C}$$

$$\therefore g_{m6} = \frac{2.2 \times 10}{3} \times 204.93 \mu$$

$$\therefore g_{m6} \approx 2.1 \text{ mS}$$

$$S_6 = g_{m6}$$

$$= \frac{k_p' V_{dsat6}}{2.1 \text{ m}} = 175$$

$$\therefore S_6 = 175$$

$$I_6 = \frac{g_{m6}^2}{2k_p' S_6} = \frac{2.1 \text{ m}^2}{2 \times 60 \mu \times 175} = 210 \mu\text{A}$$

$$\text{also } I_6 = \frac{S_6}{S_4} I_4 = 87.5 \mu\text{A}$$

\therefore taking $I_6 = I_7 = 210 \mu\text{A}$, & recalculating S_6

$$S_6 = \frac{I_6}{I_4} \times S_4 = \boxed{420 = S_6}$$

6) Calculation of S_7 :

$$S_7 = \frac{I_7}{I_5} \times S_5 = \frac{210}{30} \times 30 = 210$$

$$\therefore S_7 = 210$$

from response it is observed that required ϕ_m is not achieved. (see screen shot below).

\therefore Using Nulling resistor.

Below are the screenshots of the OP-AMP without nulling resistor and its frequency response. It was observed that the required phase margin was not achieved with this configuration.

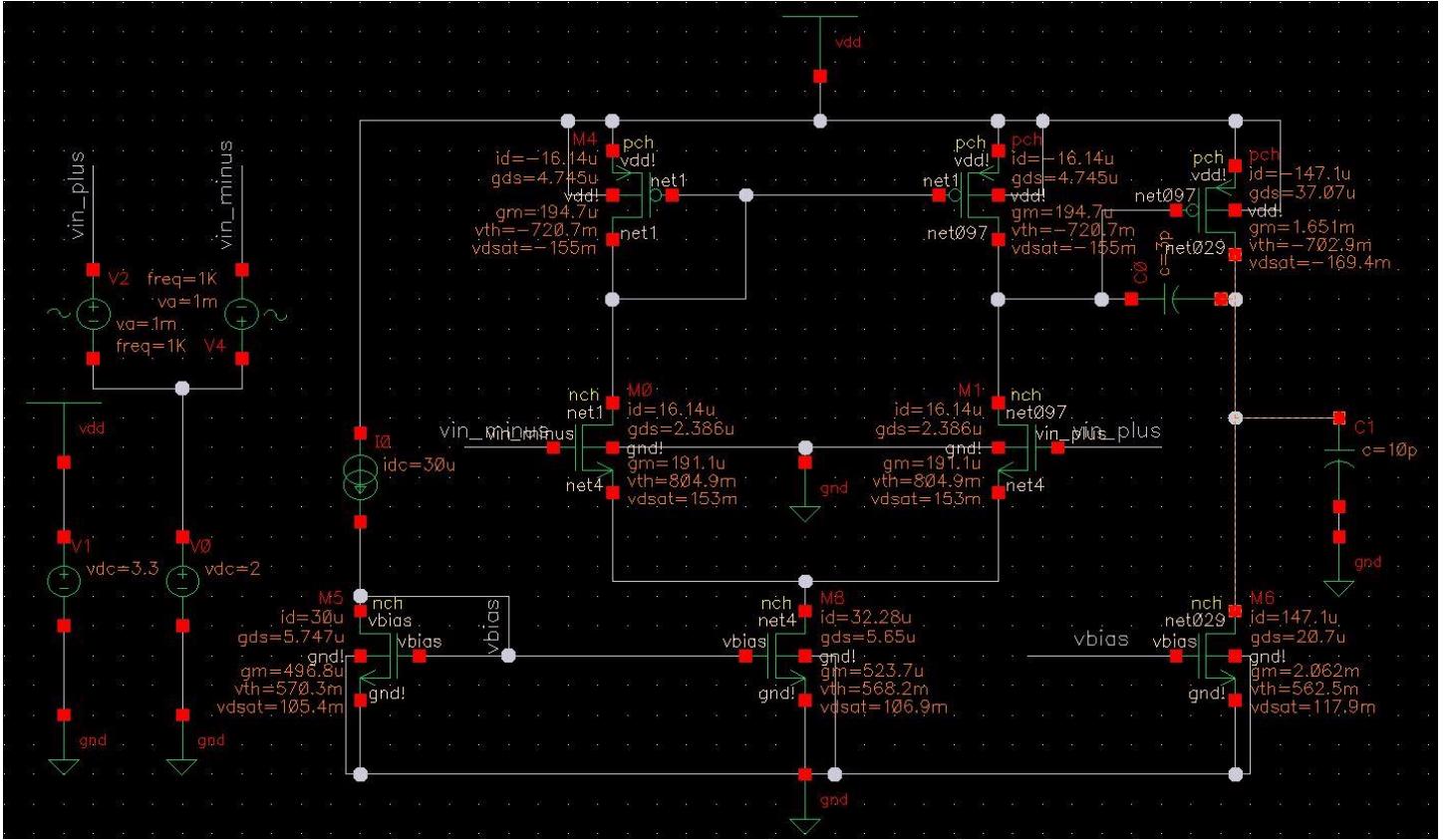


Figure 4 Schematic of OP-AMP without nulling resistor

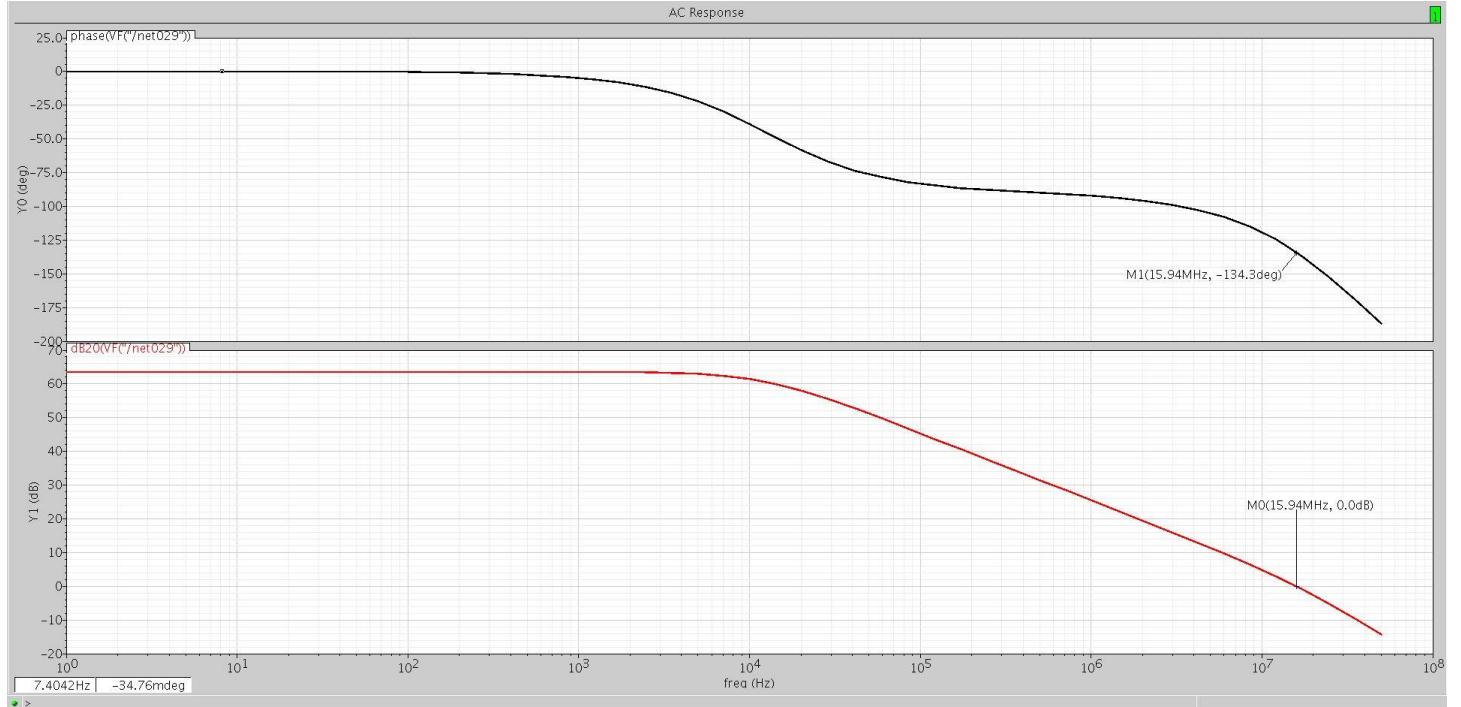
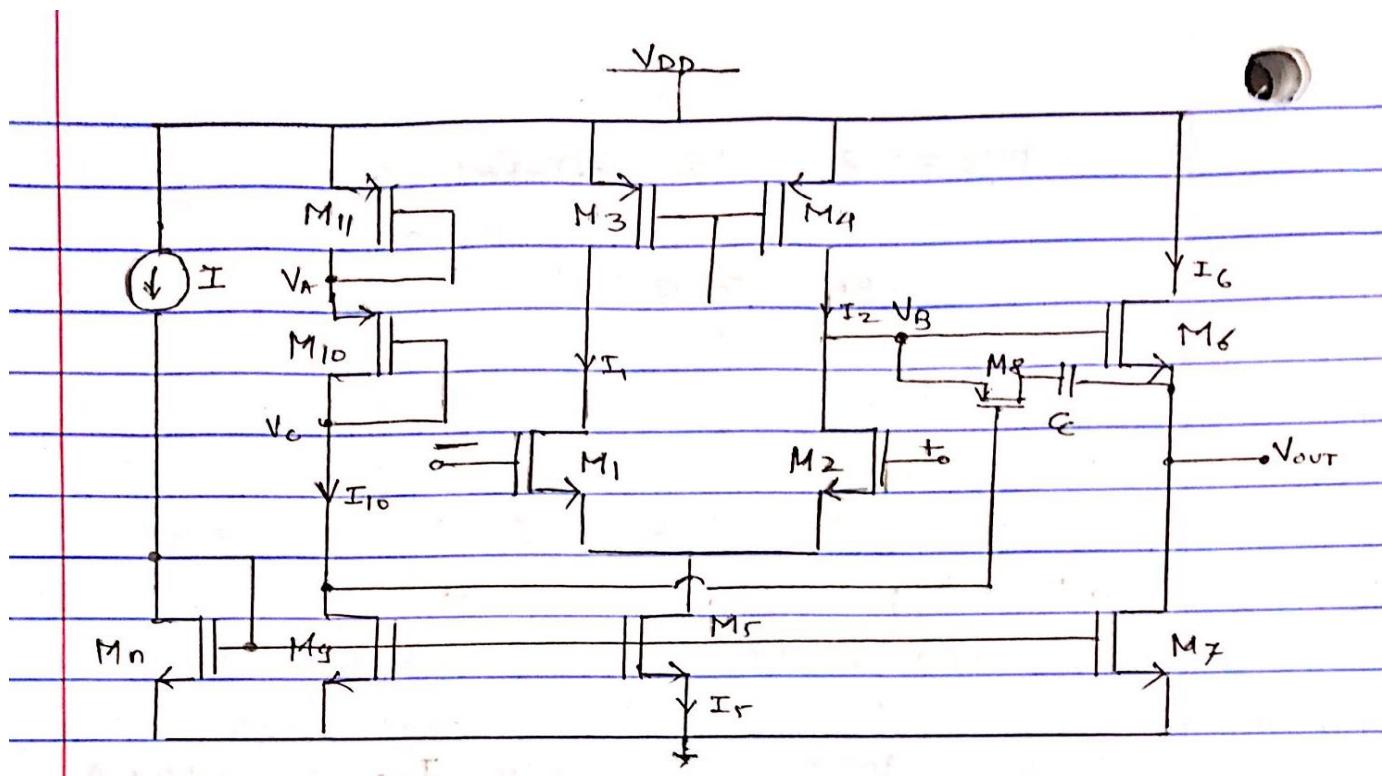


Figure 5 Frequency response of the above circuit

The phase response shows that the achieved phase margin is $\Phi_m = 180 - 134.9 = 45.1$ degree. My target was 60 degree. Therefore I changed the circuit by adding a self-biased nulling resistor using P-MOS device.

Design of the nulling resistor transistor:



R_z should be added in series with C_0 . The zero created by this resistor cancels 2nd pole if;

$$|P_z| = |z_1| \Rightarrow \frac{qmg}{c_L} = \frac{1}{R_z c_c - (c_c/gm_0)}$$

$$\therefore R_2 \text{ must be} = \frac{1}{gm_6} \left(\frac{C_c + C_L}{C_c} \right)$$

- This value of R_2 will cancel 2nd pole for only one C_L (i.e. 10 pF)
 - For making it work for all loads, Above method is used.
 - Choosing $I_g = I_{10} = I_{11} = 7.5\text{ mA}$.
if $V_A = V_B$ then desired operation is achieved.

$\therefore M_6$ & M_{11} are related by

$$S_{11} = \frac{I_{11}}{16} \times S_6 = \frac{7.5}{210} \times 420$$

$$\therefore S_{11} = 15$$

Choose $S_{10} = 1$

$$\text{Now, } S_g = \frac{I_g}{I_5} \times S_r = \frac{7.5}{30} \times 30 = 7.5 = S_g$$

After derivation, equation for S_8 turns out to be

$$S_8 = \left(\frac{C_L}{C_L + C_C} \right) \sqrt{\frac{S_{10} S_6 16}{I_{10}}}$$

$$\therefore S_8 = 25.05$$

$$\therefore S_8 \approx 25$$

After implementing this setup, schematic & AC response is as shown below

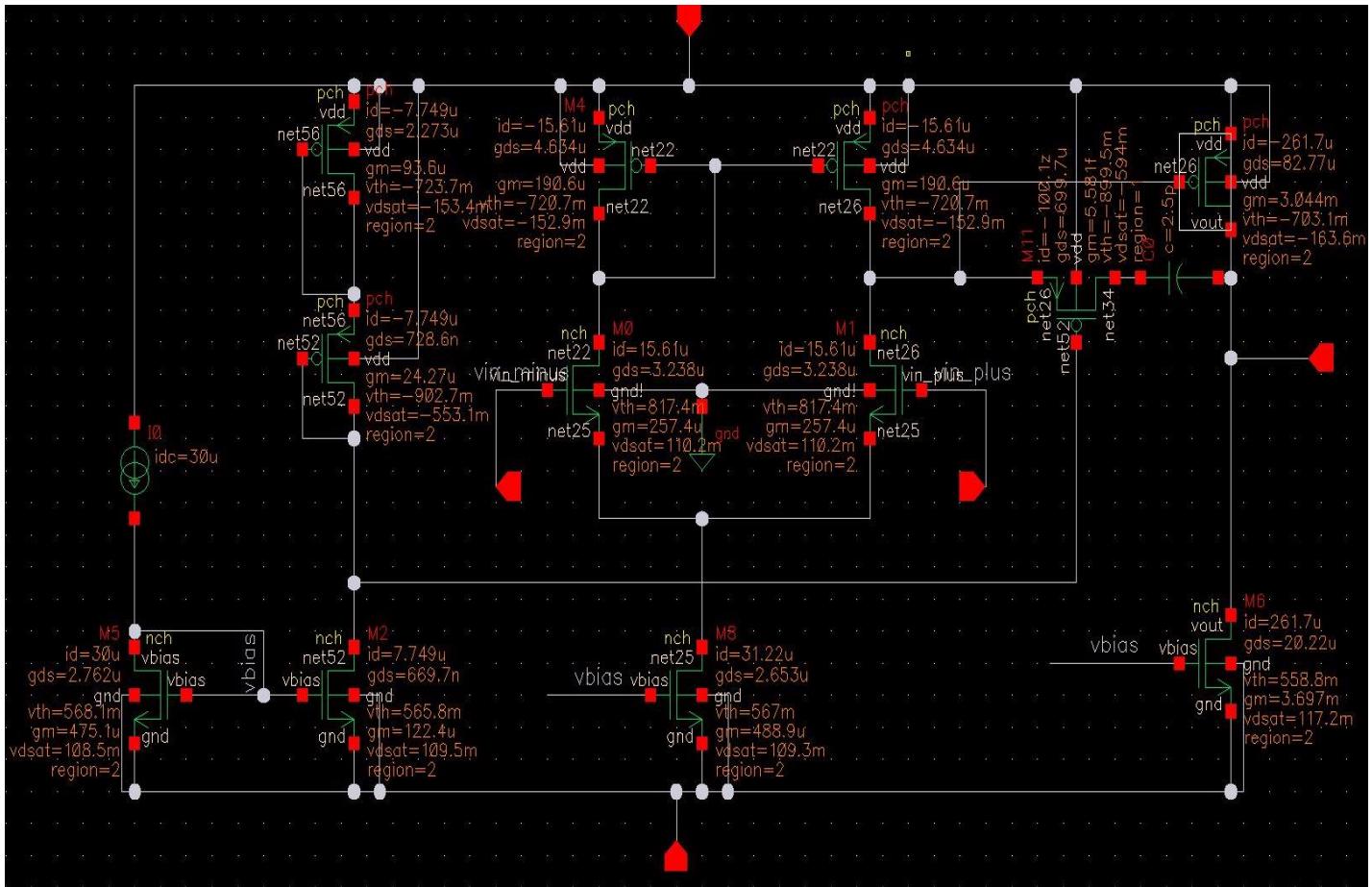


Figure 6 Schematic of OPAMP with nulling resistor

Above figure confirms that all transistors are in saturation region and circuit is operating as desired

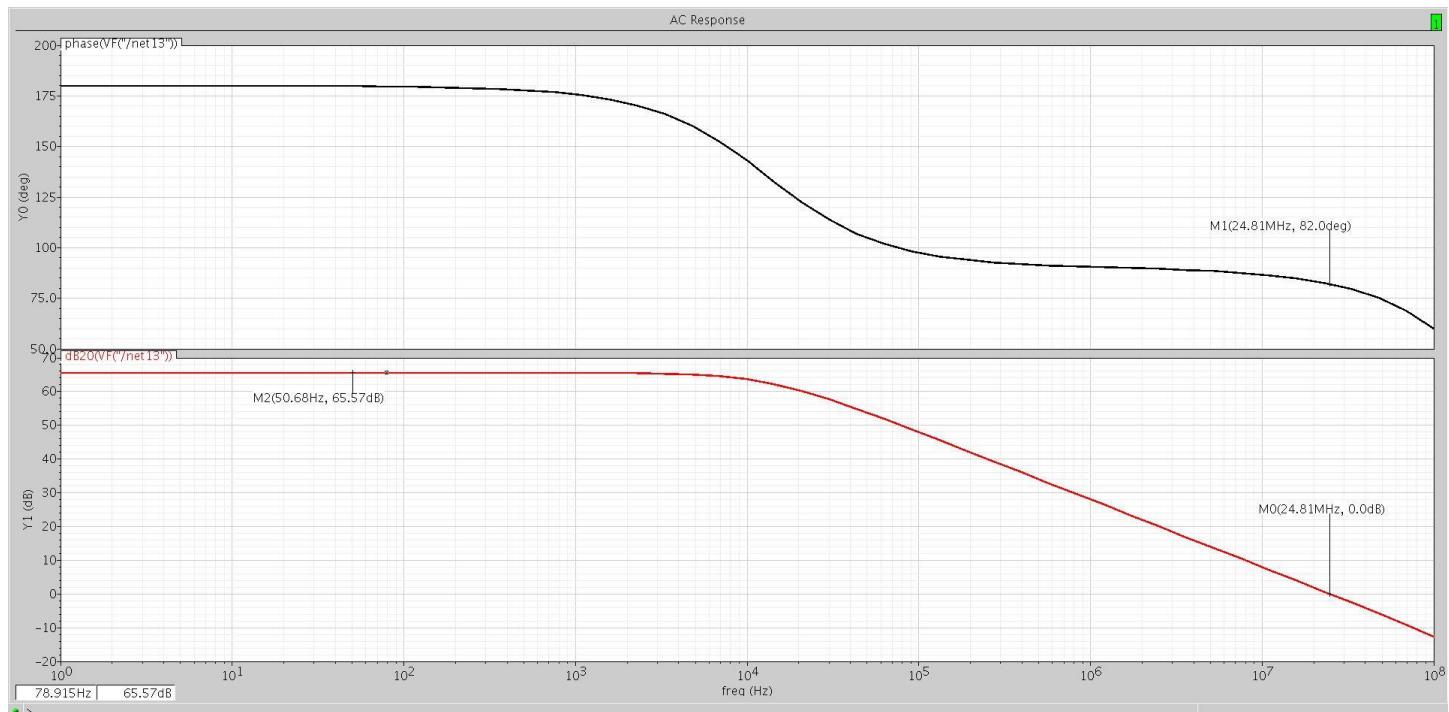


Figure 7 Frequency Response of above circuit

The frequency response shows that the **DC gain of the circuit is 65.57dB**, unity gain bandwidth is **24MHz** and phase margin **$\Phi_m = 180 - 82 = 98$ degree**. All of these are meeting or exceeding the target specification.

MEASUREMENT of CMRR

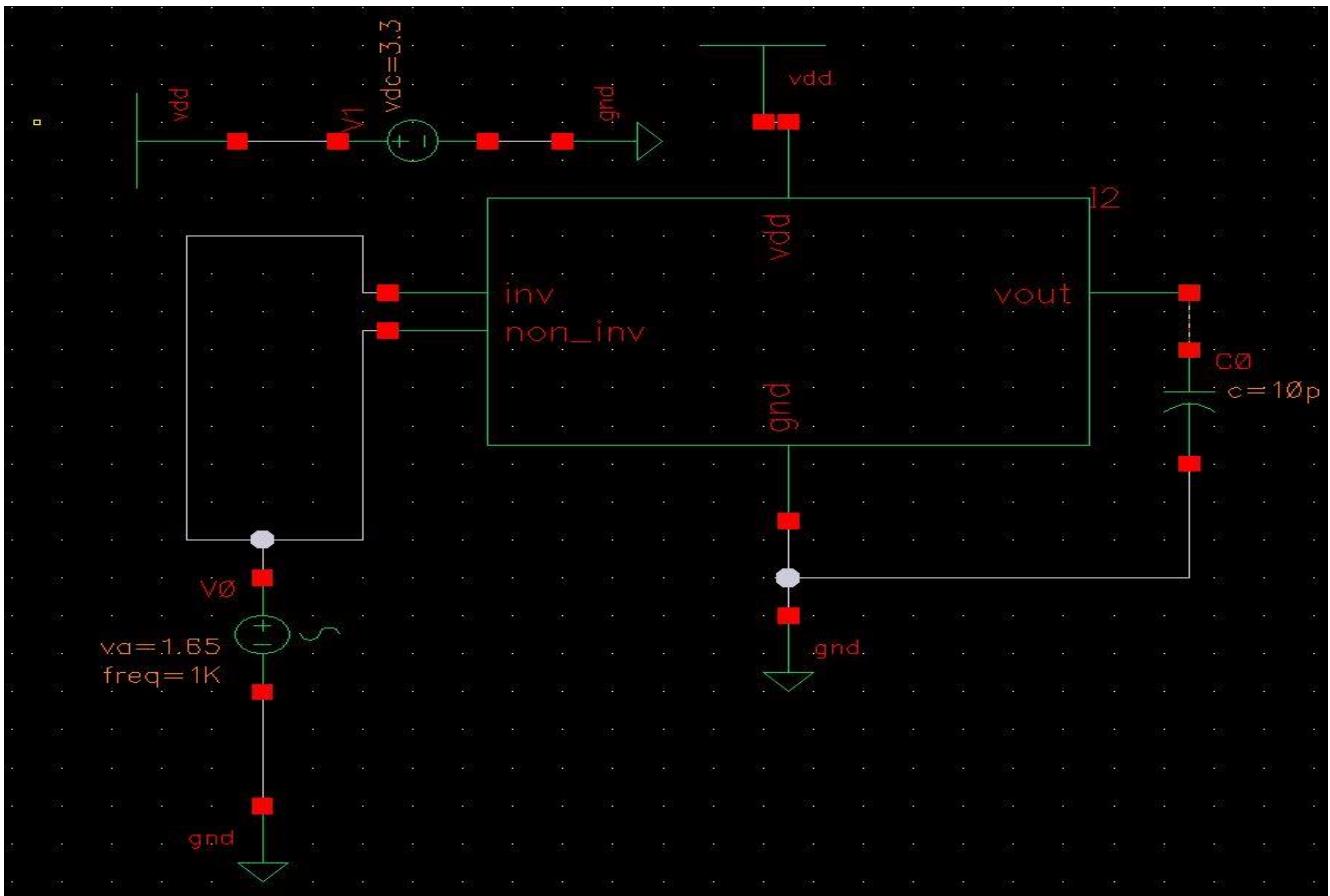


Figure 8 Setup for measuring common mode gain A_{cm}

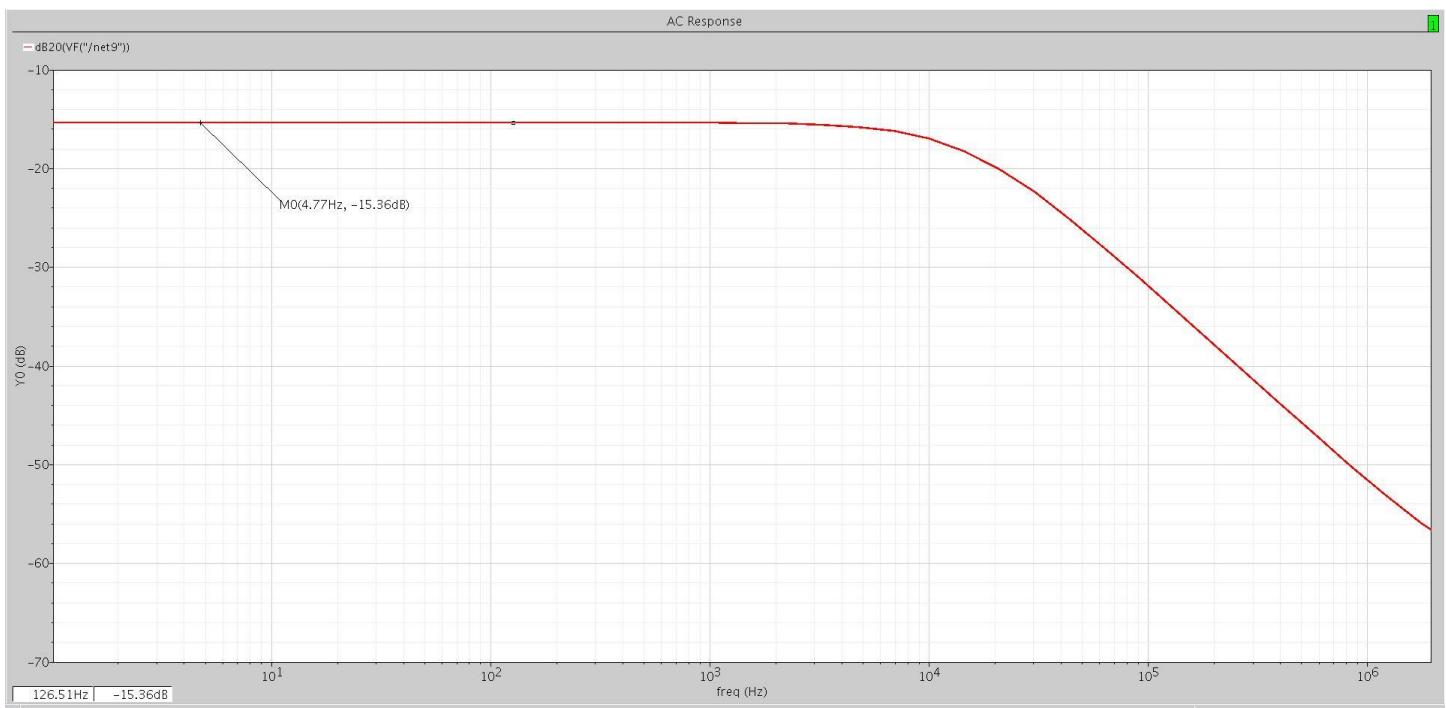


Figure 9 Common mode response

The above plot shows the common mode response of the system when set up as shown in Figure 8. We can see that the common mode gain is $A_{cm} = -15.36\text{dB}$. We have already seen that the differential mode gain A_{dm} is 65.57dB . Hence the CMRR is, $\text{CMRR} = A_{cm} - A_{dm} = 65.57 - (-15.36) = 80.9\text{dB}$, which is very excellent.

MEASUREMENT OF POWER DISSIPATION

Total current flowing through circuit according to calculation is

$$\text{Total current} = 30\mu A + 30\mu A + 7.5\mu A + 210\mu A = 277.5\mu A$$

Therefore hand calculated power dissipation is

$$P_{diss} = 3.3 \times 277.5\mu A = 0.915mW$$

After doing DC analysis in cadence, power dissipation is got from Analog environment > Tools > Result Browser > pwr > right click "Table". It was **1.012mW**

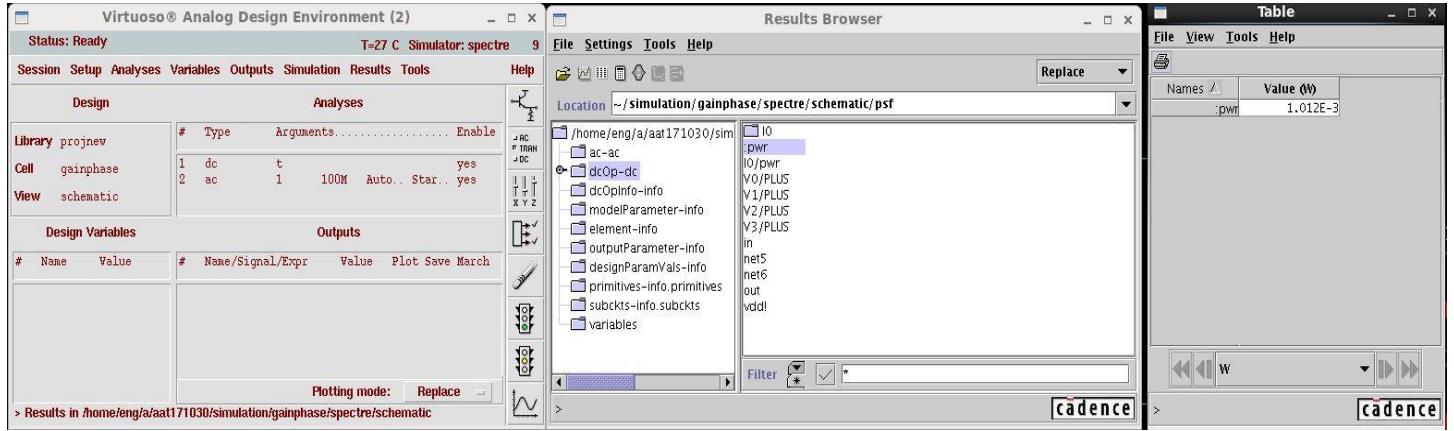


Figure 10 Measuring Power Dissipation

MEASUREMENT OF SLEW RATE

To measure the slew rate, pulse input was given as shown below

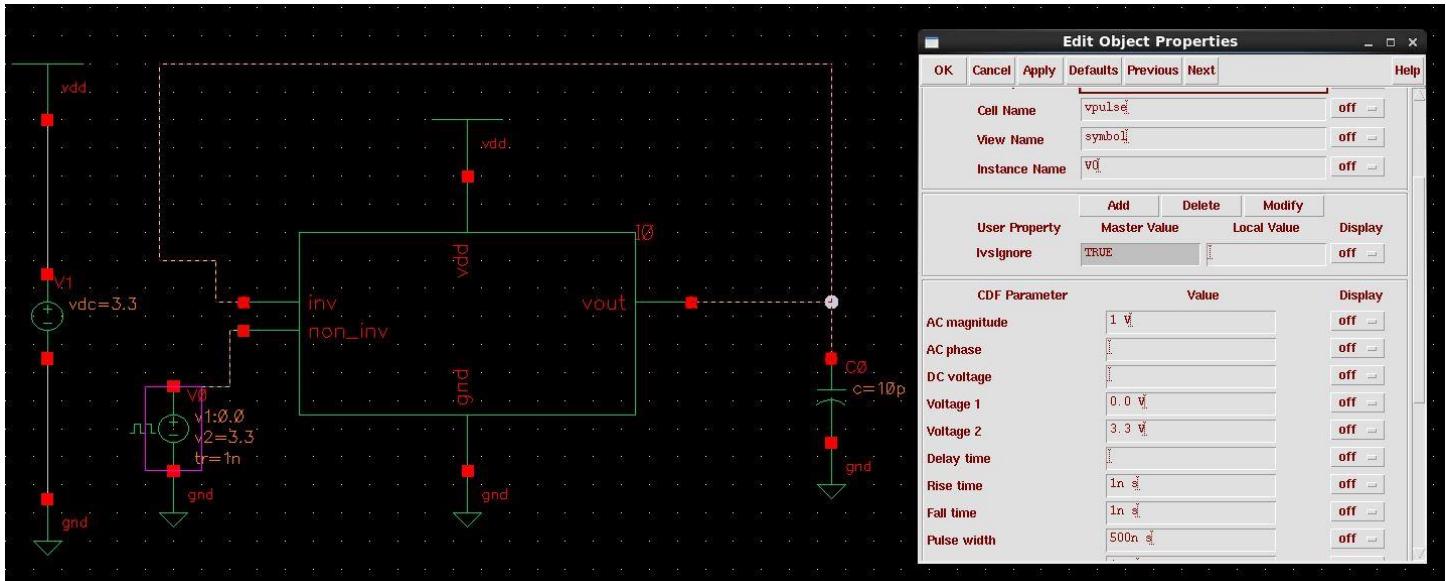


Figure 11 Setup for slew rate

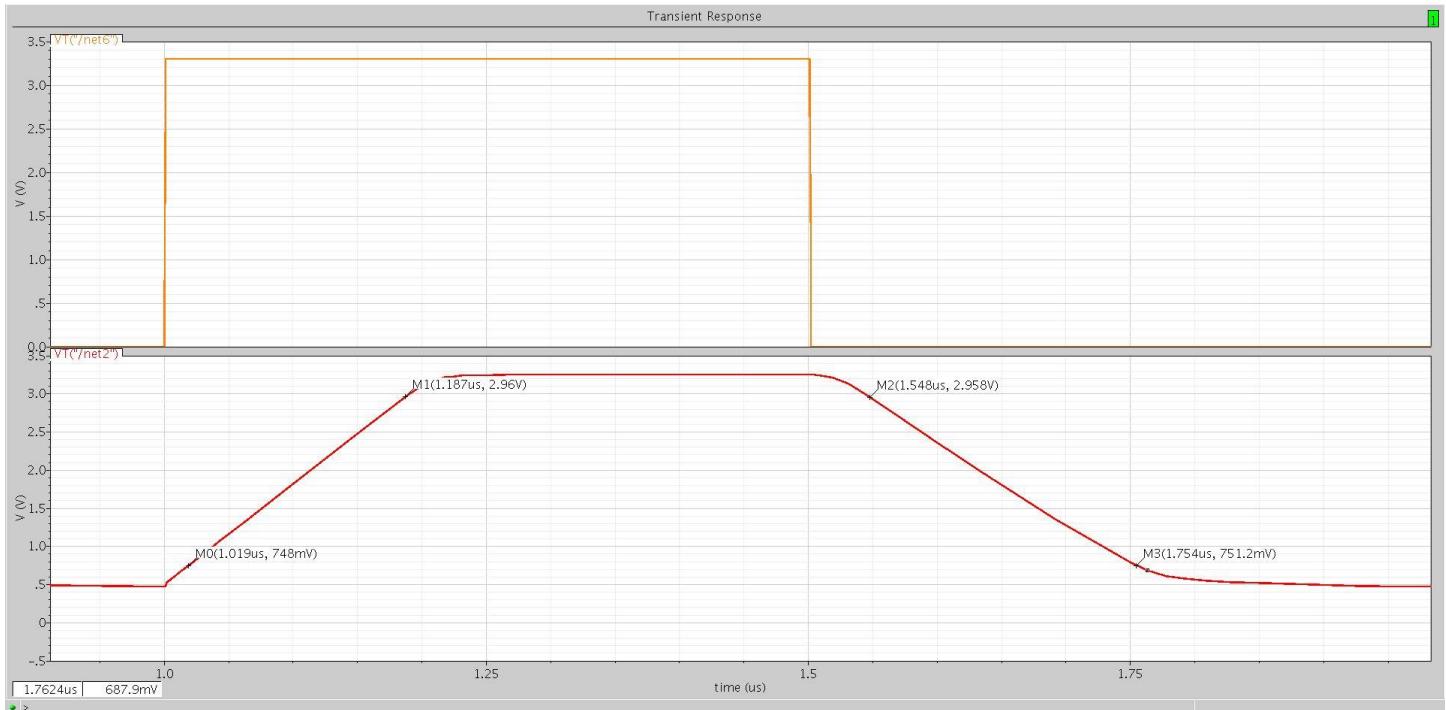


Figure 12 Transient plot of input and output

Above graph clearly shows that positive slew rate is $+SR = (2.96 - 0.748)/(1.187 - 1.019) = 13.82 \text{ V}/\mu\text{s}$ and negative slew rate is $|-SR| = (0.7512 - 0.748)/(1.754 - 1.548) = 11.045 \text{ V}/\mu\text{s}$.

The average slew rate is $\text{SR} = 12.43 \text{ V}/\mu\text{s}$ which meets the design specifications.

MEASUREMENT OF OUPUT VOLATGE SWING RANGE

* Output Voltage swing:

$$V_{out\ max} = V_{DD} - V_{dsat(6)} = 3.3 - \sqrt{\frac{2 \cdot I_6}{k'_6 S_6}}$$

$$= 3.3 - \sqrt{\frac{2 \times 210 \mu A}{60 \mu A \times 420}} = 3.17 V$$

$$V_{out(min)} = V_{dsat(7)} = \sqrt{\frac{2 I_7}{k'_7 S_7}} = \sqrt{\frac{2 \times 210 \mu A}{200 \mu A \times 210}}$$

$$= 0.1 V.$$

$$\therefore 0.1 V < V_{out} < 3.17 V$$

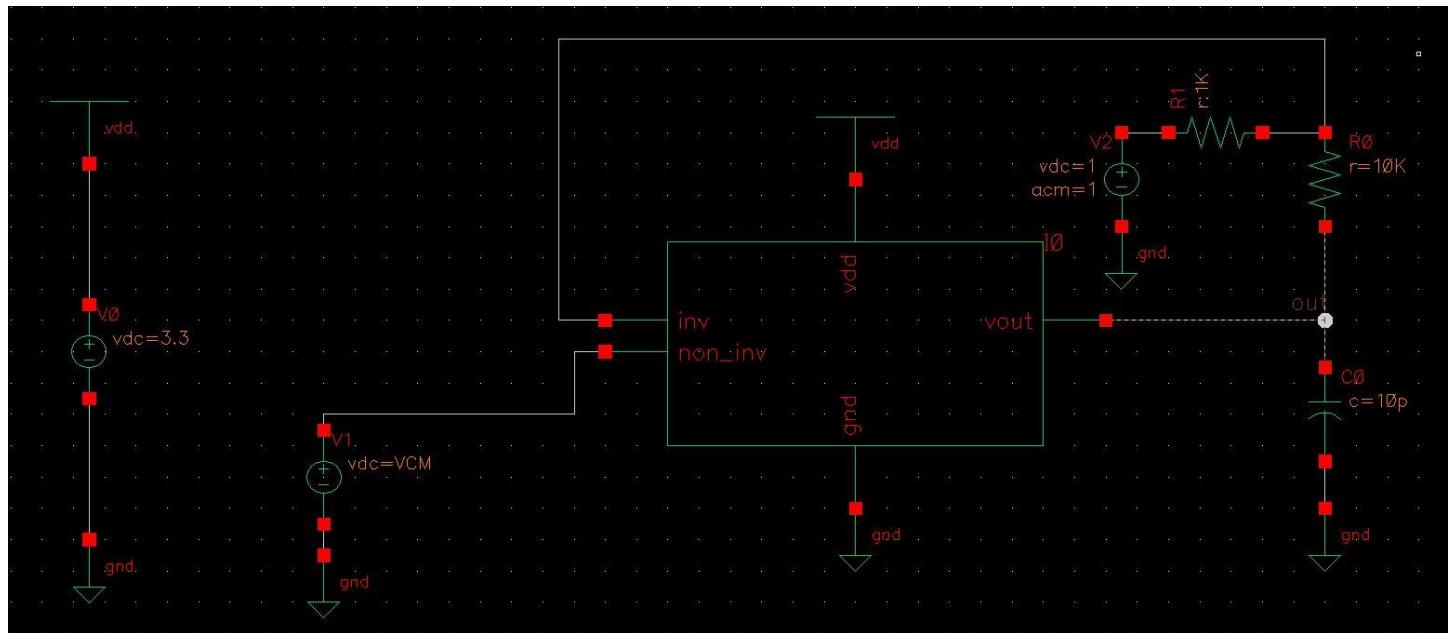


Figure 13 Setup for calculation of OVSR

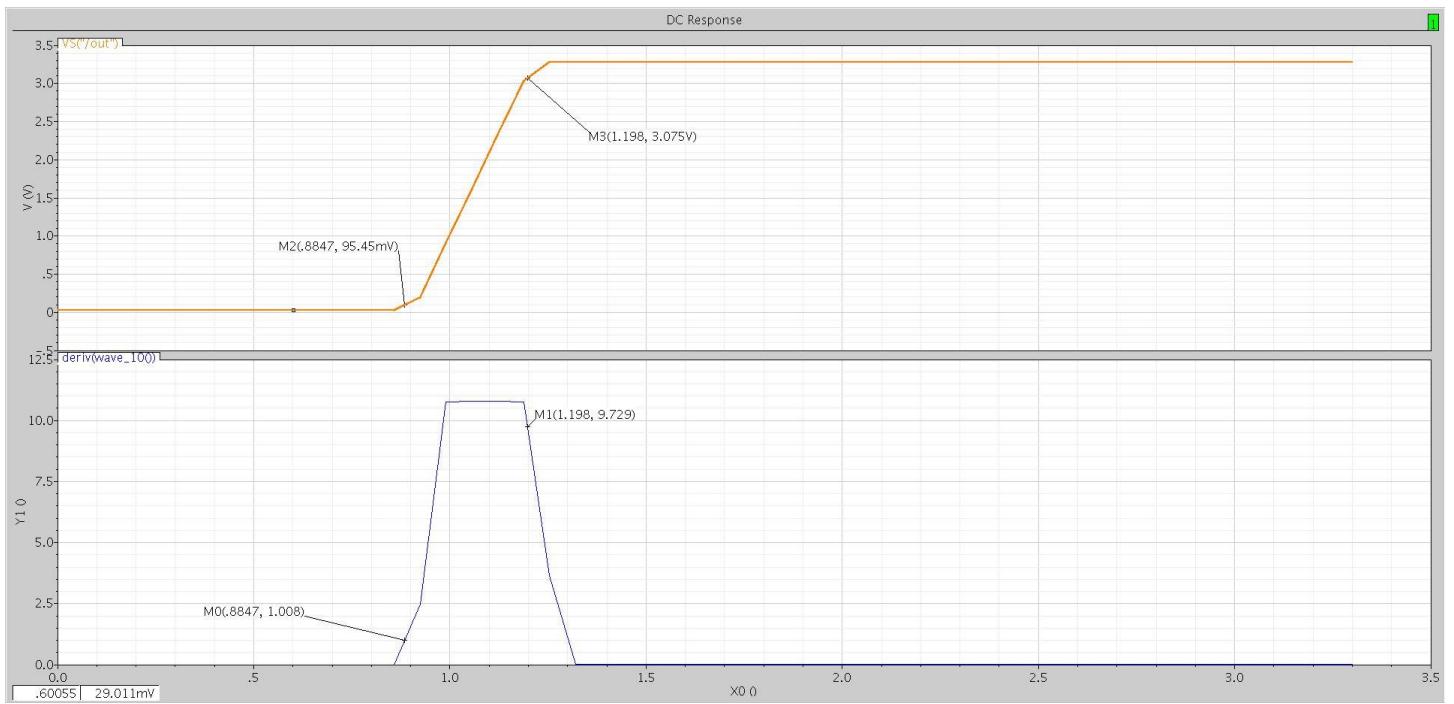


Figure 14 Plot for calculation of OVSR

Plot above is the plot of output voltage with respect to change in input common mode voltage. Plot below is the derivative of it. From the plot below we get the rising point and falling point. By keeping marker at these locations we get the OVSR from plot above. From the plot we get the OVSR to be $OVSR_{min} = 0.095V$ and $OVSR_{max} = 3.075V$.

Therefore, **$0.095V < V_{out} < 3.075V$**

MEASUREMENT OF INPUT COMMON MODE RANGE

The figures below shows the setup for calculating the ICMR and plot for it.

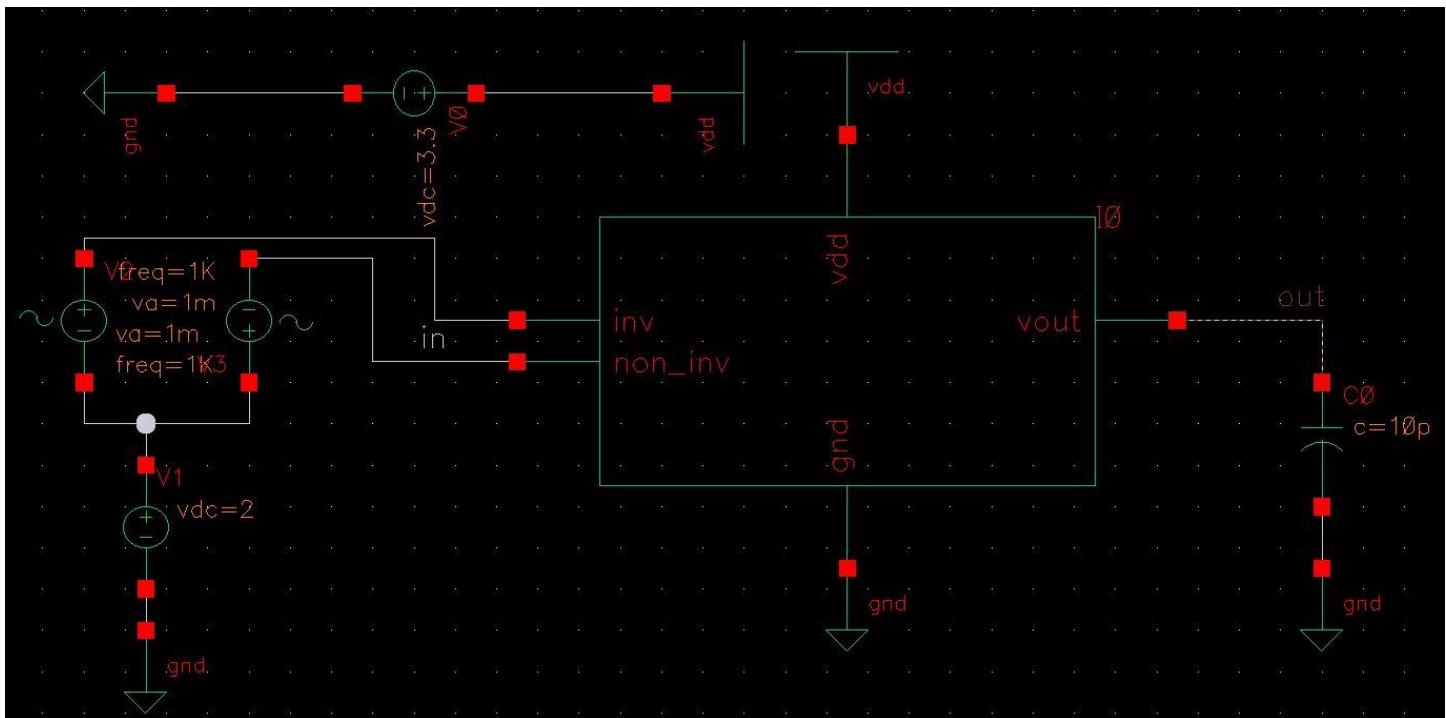


Figure 15 Setup for ICMR Calculation

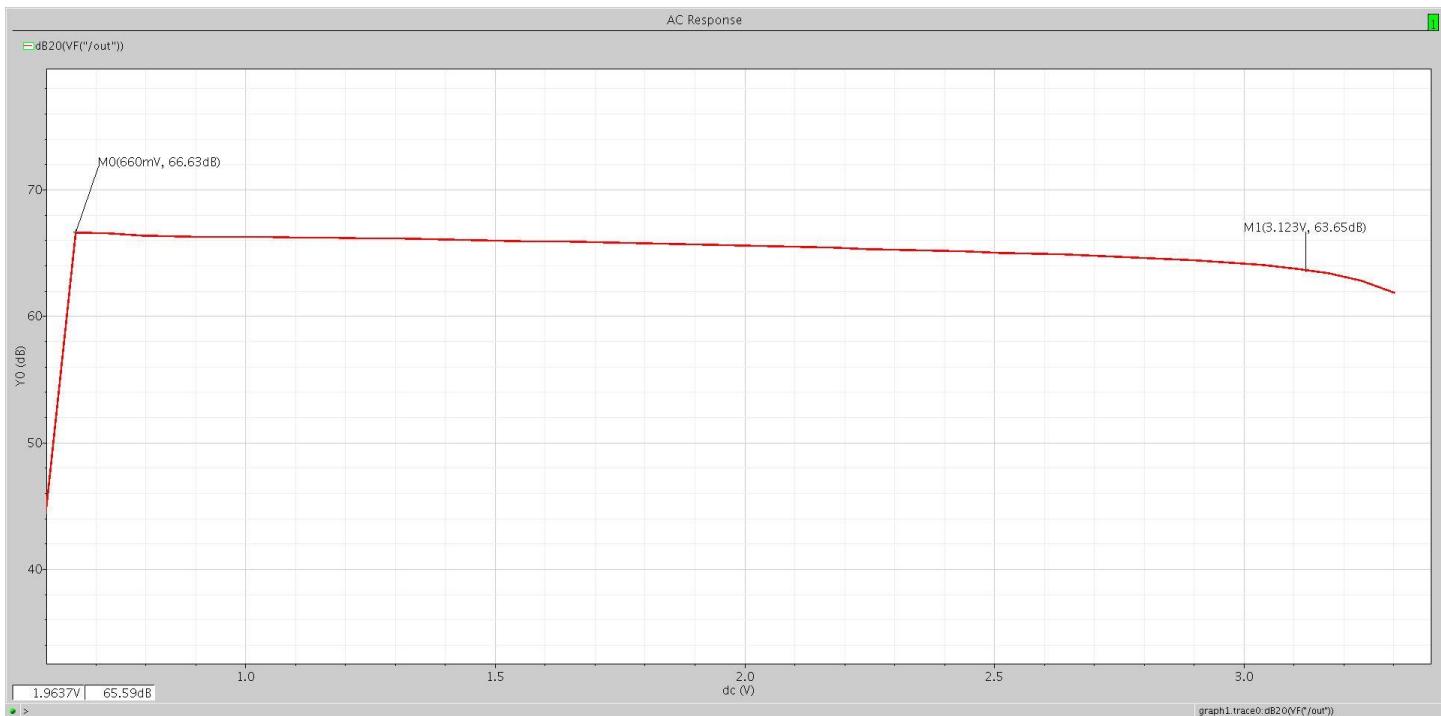


Figure 16 Plot for ICMR setup

The above plot shows that the highest gain was achieved at 0.66V and its 3dB below point is at 3.12V. Hence ICMR of the circuit is **0.66 V < ICMR < 3.12 V**.

SIMULATION / HAND CALCULATION CORELATION

Table 2 Simulation values and hand calculated values corelation

Parameter	Simulation / Target specs	Hand calculation
DC gain	65.57 dB	62 dB
Phase Margin	98 degree	60 degree
Unity Gain Bandwidth	24 Mhz	8 MHz
Slew Rate	12.43V/ μ	10V/ μ
Input Common mode range	Vin_max = 3.12 V Vin_min = 0.66 V	Vin_max = 3.1 V Vin_min = 1.2 V
CMRR	80.9 dB	>70 dB
Power Dissipation	1.012 mW	0.915 mW

Now that the OPAMP is designed as per requirement, we can easily implement Schmitt trigger using it.

IMPLEMENTATION OF SCHMITT TRIGGER USING OPAMP

Circuit below shows the schematic of the normal comparator with single reference (left) and Schmitt trigger with two thresholds (right).

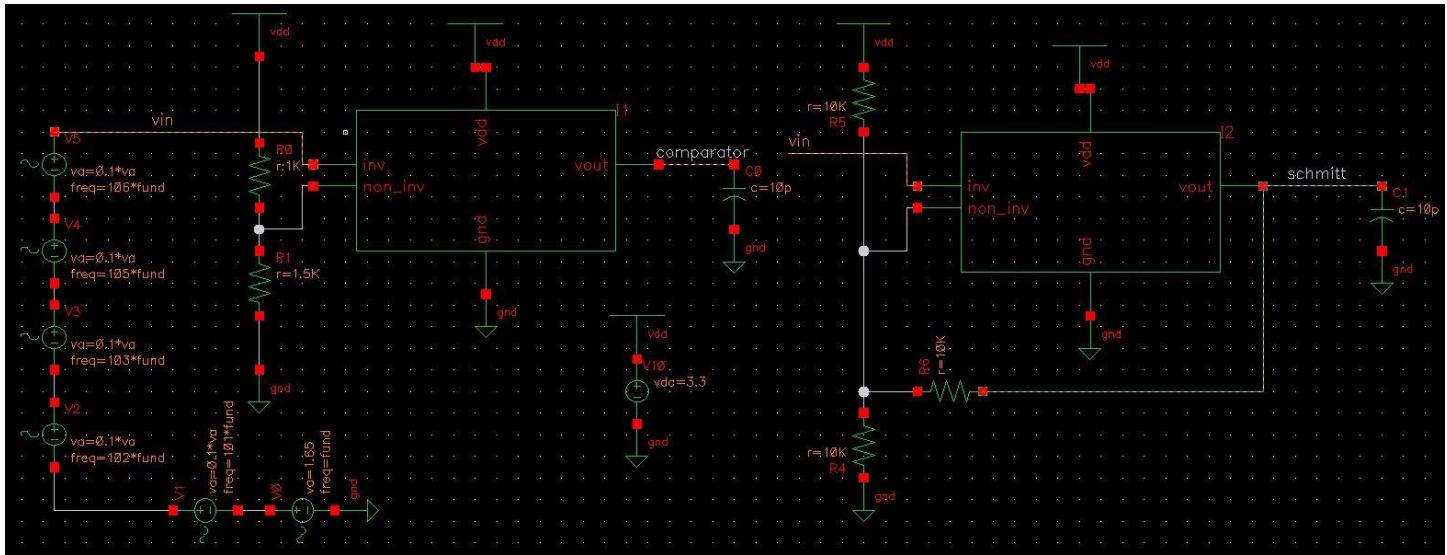


Figure 17 Implementation of Comparator and Schmitt Trigger and their comparison

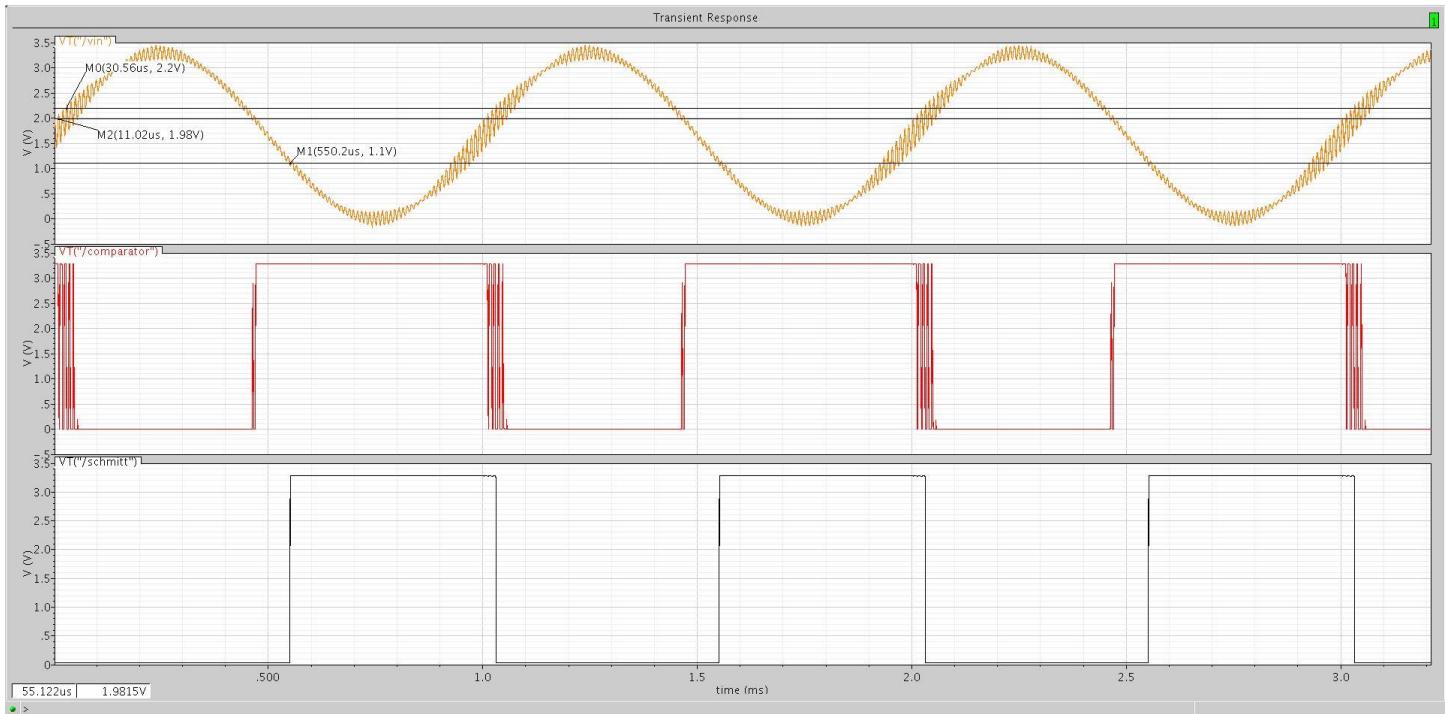


Figure 18 Response of comparator (middle) and Schmitt Trigger (bottom) for noisy input (top)

In figure 18, the top and bottom reference lines on input wave are upper and lower thresholds of Schmitt Trigger whereas the middle reference is the reference level of the comparator. From the plot we can see that when there is too much noise in the input, the comparator fails to perform well but the Schmitt trigger can avoid this noise.

DISCUSSION, SUMMARY AND OBSERVATION

In this project, a two stage fully compensated OPAMP has been designed. All specifications of the designed OPAMP are calculated and matched with the target/desired specifications. The designed OPAMP is tested by implementing it in an application, that is, Comparator and Schmitt Trigger. It has been observed that the OPAMP is meeting the requirement. Below is the list of the areas where system is going above expectations and areas where design can be improved.

Areas of great achievement:

- CMRR of 80dB (target of 70 dB)
- GBW of 24.81MHz (target of 8MHz)
- Phase margin of 98 degree (target of 60 degree)

Areas that can be improved:

- Slew Rate. Although the desired slew rate requirement was met, the slew rate of $>20V/\mu s$ is always better.
- Power consumption.

Table 3 Summary of the aspect ratios of all transistors used in the circuit

Transistor	Aspect Ratio	W (μm)	L (μm)
M1	7	0.5	7.5
M2	7	0.5	7.5
M3	30	0.5	15
M4	30	0.5	15
M5	30	0.9	27
M6	420	0.45	189
M7	210	0.9	189
M8	25	1	25
M9	7.5	0.9	6.75
M10	1	0.5	0.5
M11	15	0.5	7.5
Mn	30	0.9	27

REFERENCES

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5. D. Nedelkovski, 'What is Schmitt Trigger | How It Works', [Online] Available : <https://howtomechatronics.com/how-it-works/electrical-engineering/schmitt-trigger/>