

DSD LAB ASSESSMENT

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2 BIT COMPARATOR:

2- Bit comparator:



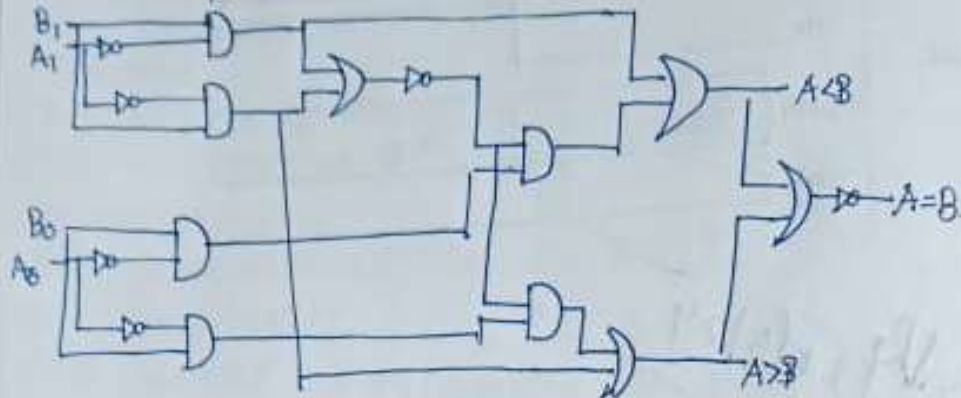
Inputs				Outputs		
A ₁	A ₀	B ₁	B ₀	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	0	1	0
1	1	0	1	1	0	0
1	1	1	0	0	0	1
1	1	1	1	0	1	0

Equation: $(A > B) : A_0 \bar{B}_1 \bar{B}_0 + A_1 \bar{B}_1 + A_1 A_0 B_0$

$(A = B) : (A_0 \oplus B_0) (A_1 \oplus B_1)$

$(A < B) : \bar{A}_1 B_1 + \bar{A}_0 B_1 B_0 + \bar{A}_1 \bar{A}_0 B_0$

circuit Diagram:



Dataflow code:

```

module comp (input [1:0] A, B, output A-less-B, A-equal-B, A-great-B);
  wire t1, t2, t3, t4, t5, t6, t7, t8;
  xnor u1 (t1, A[1], B[1]);
  xnor u2 (t2, A[0], B[0]);
  and u3 (A-equal-B, t1, t2);
  assign t3 = (~A[0]) & (~A[1]) & B[0];
  assign t4 = (~A[1]) & B[1];
  assign t5 = (~A[0]) & B[1] & B[0];
  assign A-less-B = t3 | t4 | t5;
  assign t6 = (~B[0]) & (~B[1]) & A[0];
  assign t7 = (~B[1]) & A[1];
  assign t8 = (~B[0]) & A[1] & A[0];
  assign A-great-B = t6 | t7 | t8;
endmodule
  
```

timescale 1ps/10ps

module tb-comp;

reg [1:0] A, B;

wire A-less-B, A-equal-B, A-great-B;

integer i;

comp dut (A, B, A-less-B, A-equal-B, A-great-B);

```

module beginm
  for (i=0; i<4; i=i+1)
    beginm
      A=i;
      B=i+1;
      #20;
    end
  for (i=0; i<4; i=i+1)
    beginm
      A=i;
      B=i;
      #20;
    end
  for (i=0; i<4; i=i+1)
    beginm
      A=i+1;
      B=i;
      #20;
    end
  end
endmodule

```

3).

Behavioural code:

```

module comp-behav (input [1:0] A, B, output reg A-less-B,
  A-equal-B, A-greater-B);
  always @(A) begin
    if (A==B)
      A-equal-B=1;
    else
      A-equal-B=0;
    if (A<B)
      A-less-B=1;
    else
      A-less-B=0;
    if (A>B)
      A-greater-B=1;
    else
      A-greater-B=0;
  end
endmodule

```

Gatelevel code:

module comp_gate (input [1:0] A, B, output A-less-B, A-equal-B, A-great-B);

wire t1, t2, t3, t4, t5, t6, t7, t8;

Xnor u1 (t1, A[0], B[0]);

Xnor u2 (t2, A[0], B[0]);

and u3 (A-equal-B, t1, t2);

and u4 (t3, ~A[0], ~A[1], B[0]);

and u5 (t4, ~A[1], B[1]);

and u6 (t5, ~A[0], B[1], B[0]);

or u7 (A-less-B, t3, t4, t5);

and u8 (t6, ~B[0], ~B[1], A[0]);

and u9 (t7, ~B[1], A[1]);

and u10 (t8, ~B[0], A[1], A[0]);

or u11 (A-great-B, t6, t7, t8);

endmodule

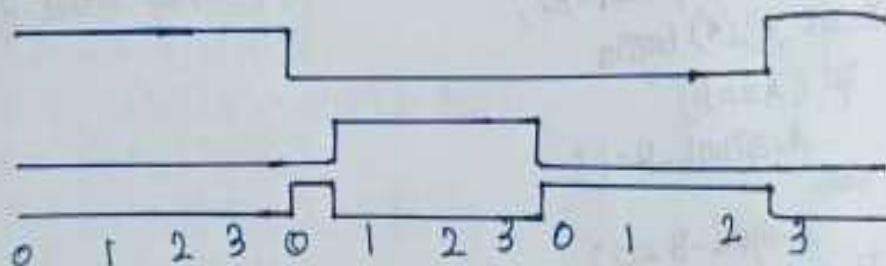
op:

A	00	01	10	11	00	01	10	11	01	10	11	00
B	01	10	11	00	01	10	11	00	01	10	11	00

A-less-B

A-equal-B

A-great-B



C:\Users\akash\OneDrive\Desktop\Zot-comparator\Zot-comparator.vi (Zot-comparator)

File Edit View Tools Bookmarks Window Help

C:\Users\akash\OneDrive\Desktop\Zot-comparator\Zot-comparator.vi (Zot-comparator) - Default



```
1 // FGA projects using Verilog VLSI
2 // dependent.com : FGA projects, Verilog projects, VLSI projects
3 // Verilog code for 2-bit comparator
4 module comparator_2bit (A, B, output A_less_B, A_equal_B, A_greater_B);
5     wire temp1, temp2, temp3, temp4, temp5, temp6, temp7, temp8;
6     // A = B output
7     and a1(temp1, A[0], B[0]);
8     and a2(temp2, A[1], B[1]);
9     and a3(A_equal_B, temp1, temp2);
10    // A less than B output
11    xor x1(temp3, A[0], B[0]);
12    xor x2(temp4, A[1], B[1]);
13    and a4(temp5, B[1], temp3);
14    and A_less_B(temp6, temp5, temp4);
15    // A greater than B output
16    xor x3(temp7, A[0], B[0]);
17    xor x4(temp8, A[1], B[1]);
18    and a5(temp9, A[0], temp7);
19    and A_greater_B(temp8, temp9, temp4);
20 endmodule
21 timescale 10 ps 10 ps
22 // FGA projects using Verilog VLSI
23 // dependent.com
24 // Verilog testbench code for 2-bit comparator
25 module tb_comparator;
26     reg [1:0] A, B;
27     wire A_less_B, A_equal_B, A_greater_B;
28     comparator_2bit A_less_B, A_equal_B, A_greater_B;
29     // device under test
30     comparator_2bit A_less_B, A_equal_B, A_greater_B;
31     initial begin
32         $display("Initial Values");
33         begin
34             A = 0;
35             B = 0;
36             $display("A = 0, B = 0");
37         end
38         $display("Initial Values");
39         begin
40             A = 1;
41             B = 0;
42             $display("A = 1, B = 0");
43         end
44         $display("Initial Values");
45         begin
46             A = 0;
47             B = 1;
48             $display("A = 0, B = 1");
49         end
50         $display("Initial Values");
51         begin
52             A = 1;
53             B = 1;
54             $display("A = 1, B = 1");
55         end
56     end
57 endmodule
```



Project - C:\Users\akash\OneDrive\Desktop\Zbit-comparator\Zbit-comparator -- C:\Users\akash\OneDrive\Desktop\Zbit-comparator\Zbit-comparator.v - Default

File	Status	Type	Date/Modified	Ln#
zbit-comparator.v	✓	Verilog	0 10/03/2024 08:24:11...	

```
1 module comparator_behavioural(input [3:0] A, B, output reg [3:0] i_equal, i_greater);
2
3     always @(*) begin
4         if (A == B)
5             i_equal = 1;
6         else
7             i_equal = 0;
8         if (A < B)
9             i_less = 1;
10        else
11            i_less = 0;
12        if (A > B)
13            i_greater = 1;
14        else
15            i_greater = 0;
16    end
17 endmodule
18
19 `timescale 10 ps / 1 ps
20 module tb_comparator;
21     reg [3:0] A, B;
22     wire [3:0] i_equal, i_less, i_greater;
23     integer i;
24     comparator_dut A_B_A_less_B_i_equal_B_i_greater(B);
25     initial begin
26         for (i = 0; i < 10; i++)
27             begin
28                 A = i;
29                 B = i + 1;
30                 #10;
31             end
32         for (i = 0; i < 10; i++)
33             begin
34                 A = i;
35                 B = i;
36                 #10;
37             end
38         for (i = 0; i < 10; i++)
39             begin
40                 A = i + 1;
41                 B = i;
42                 #10;
43             end
44     end
45 endmodule
```

Transcript

```
# Reading pref.tcl
# Loading project Zbit-comparator
```

ModelSim

