DSD LAB ASSESSMENT

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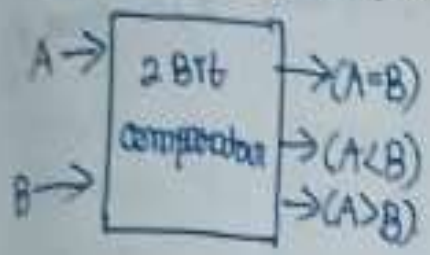
REGN NO:23BCE2029

2 BIT COMPARATOR:

2- Bit comparator:



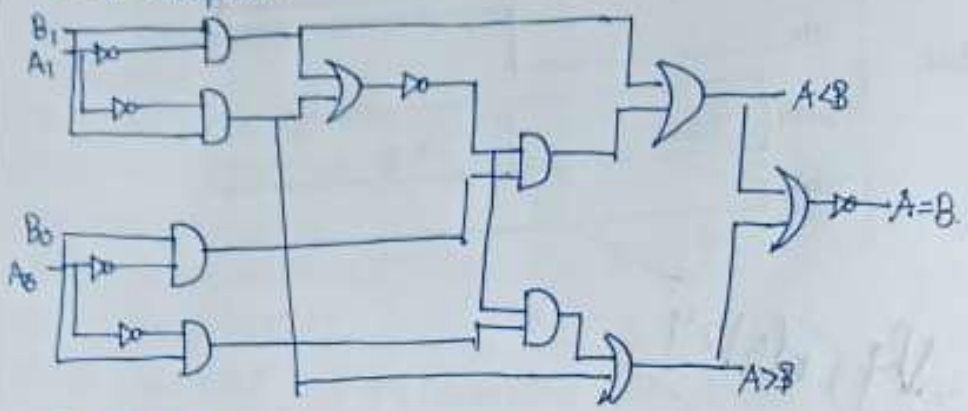
Inputs				outputs		
A_1	A_0	B_1	B_0	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

Equation: $(A>B): A_0\overline{B_1}\,\overline{B_0} + A_1\overline{B_1} + A_1A_0B_0$

$(A=B): (A_0 \odot B_0)(A_1 \odot B_1)$

$(A<B): \overline{A_1}B_1 + \overline{A_0}B_1B_0 + \overline{A_1}\,\overline{A_0}B_0$

Circuit Diagram:



Dataflow code:

```
module comp (input [1:0] A, B, output A_less_B, A_equal_B, A_great_B);
wire t1, t2, t3, t4, t5, t6, t7, t8;
xnor u1 (t1, A[1], B[1]);
xnor u2 (t2, A[0], B[0]);
and  u3 (A_equal_B, t1, t2);
assign t3 = (~A[0]) & (~A[1]) & B[0];
assign t4 = (~A[1]) & B[1];
assign t5 = (~A[0]) & B[1] & B[0];
assign A_less_B = t3|t4|t5;
assign t6 = (~B[0]) & (~B[1]) & A[0];
assign t7 = (~B[1]) & A[1];
assign t8 = (~B[0]) & A[1] & A[1] & A[0];
assign A_great_B = t6|t7|t8;
endmodule
```

```
timescale 1ps/1ps
module tb_comp;
reg [1:0] A, B;
wire A_less_B, A_equal_B, A_great_B;
integer i;
comp dut (A, B, A_less_B, B, A_equal_B, A_great_B);
```

```
initial begin
    for (i=0; i<4; i=i+1)
    begin
      A=i;
      B=i+1;
      #20;
    end
    for (i=0; i<4; i=i+1)
    begin
      A=i;
      B=i;
      #20;
    end
    for (i=0; i<4; i=i+1)
    begin
      A=i+1;
      B=i;
      #20;
    end
end
endmodule
```

3). Behavioural code:

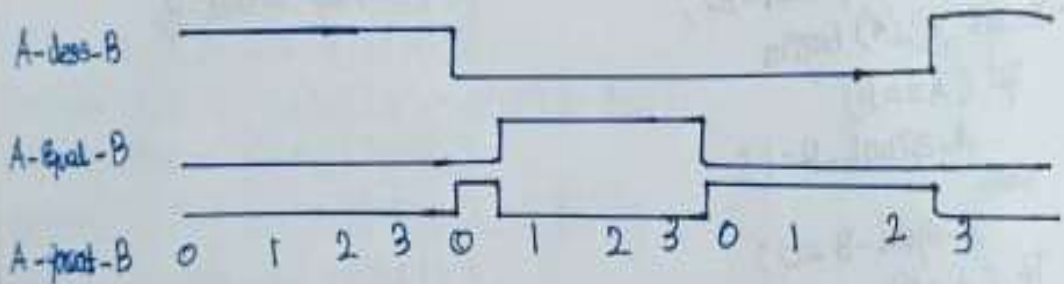
```
module comp_behav ( input [1:0] A,B, output reg A_less_B,
A_equal_B, A_greater_B);
  always @(*) begin
    if (A==B)
      A_equal_B=1;
    else
      A_equal_B=0;
    if (A<B)
      A_less_B=1;
    else
      A_less_B=0;
    if (A>B)
      A_great_B=1;
    else
      A_great_B=0;
  end
endmodule
```

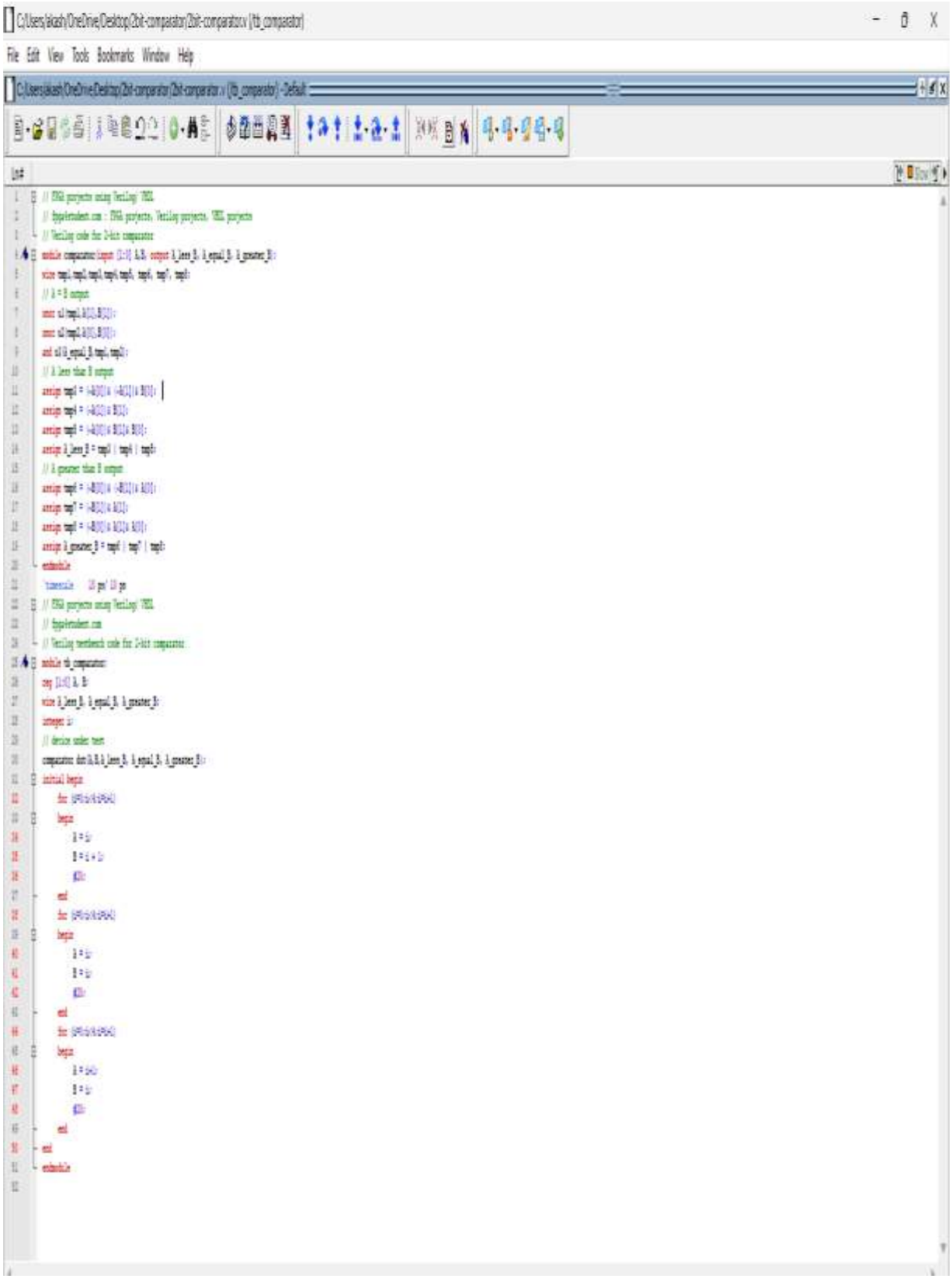
Gatelevel code:

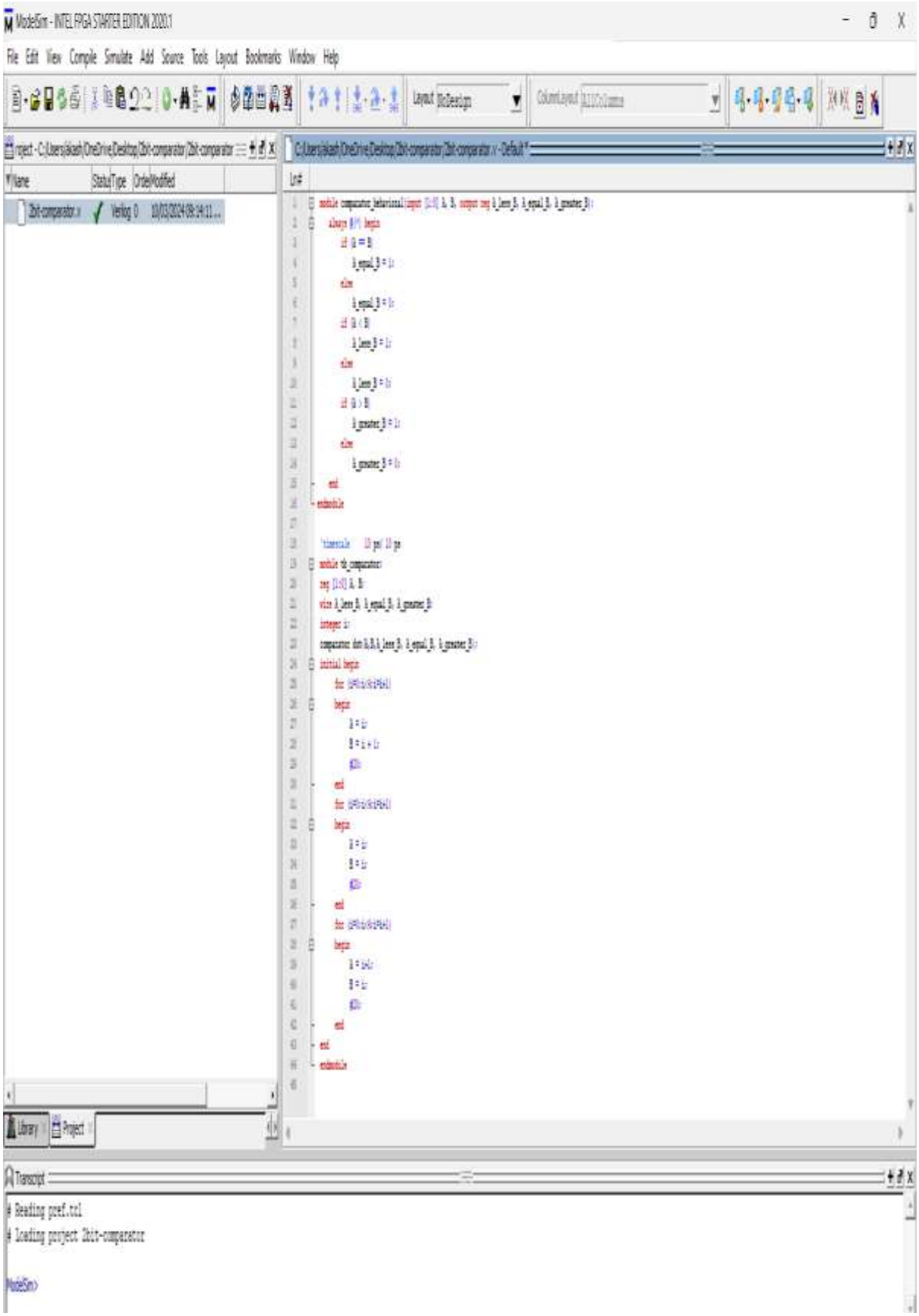
```
module comp_gate (input [1:0] A, B, output A_less_B, A_equal_B, A_great_B);
    wire t1,t2,t3,t4,t5,t6,t7,t8;
    xnor U1 (t1, A[1], B[1]);
    xnor U2 (t2, A[0], B[0]);
    and  U3 (A_equal_B, t1,t2);
    and  U4 (t3, ~A[0], ~A[1], B[1]);
    and  U5 (t4, ~A[1], B[1]);
    and  U6 (t5, ~A[0], B[1], B[0]);
    or   U7 (A_less_B, t3,t4,t5);
    and  U8 (t6, ~B[0], ~B[1], A[0]);
    and  U9 (t7, ~B[1], A[1]);
    and  U10 (t8, ~B[0], A[1], A[0]);
    or   U11 (A_great_B, t6,t7,t8);
endmodule
```

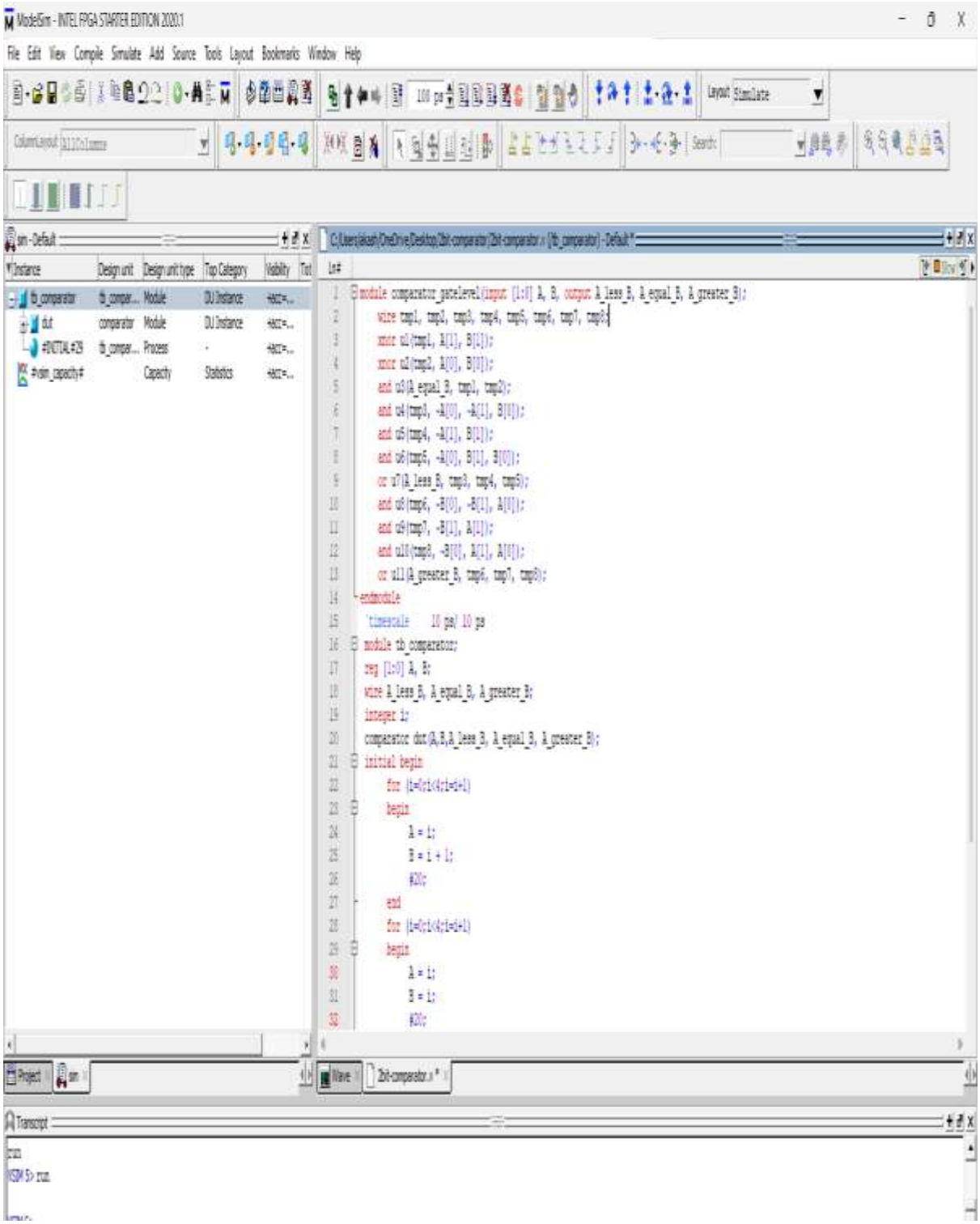
O/P:

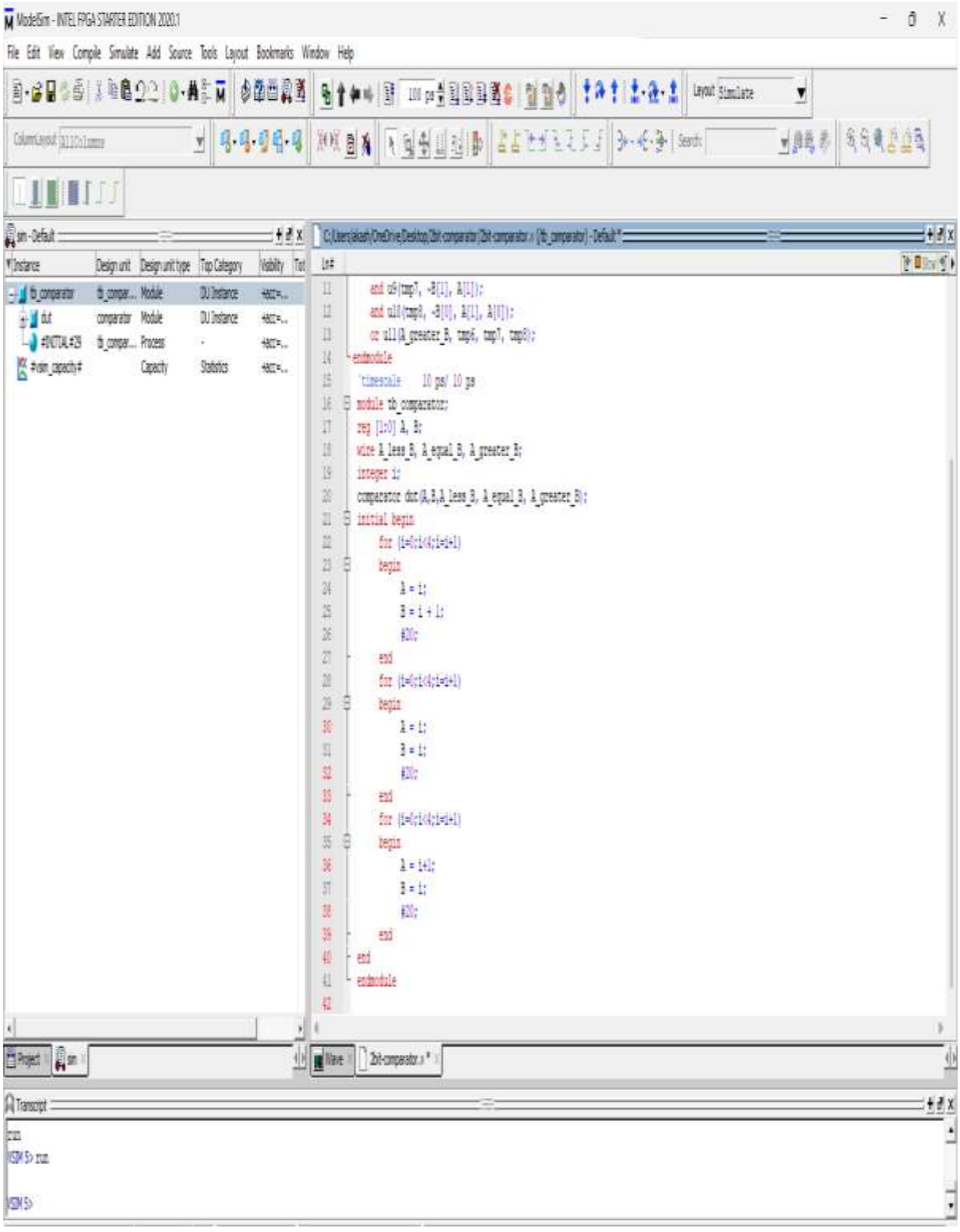
A	00	01	10	11	00	01	10	11	01	10	11	00
B	01	10	11	00	01	10	11	00	01	10	11	



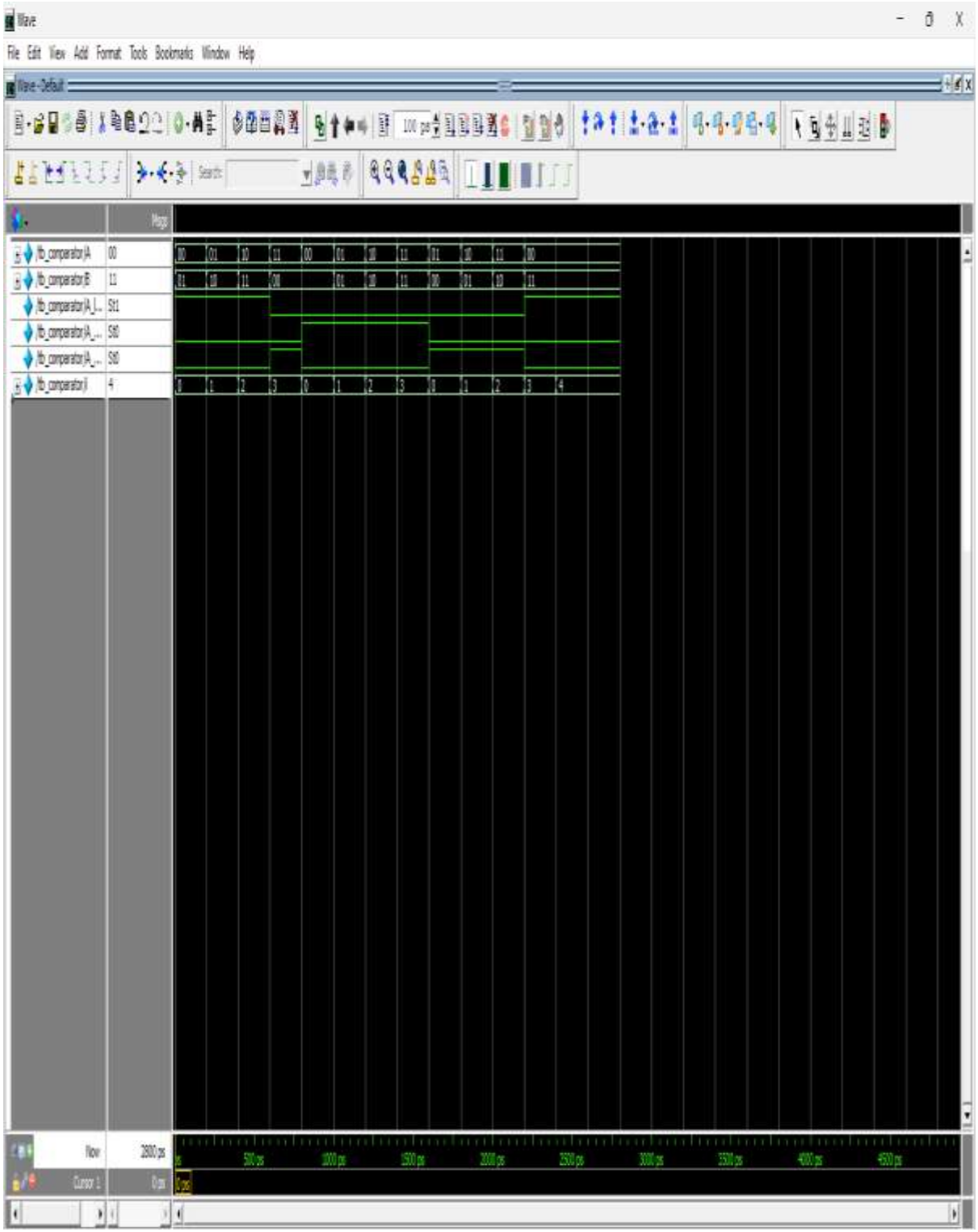



ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
Transcript
Reading pref.tcl
Loading project 2bit-comparator
ModelSim>


ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
sim - Default
Instance
Design unit
Design unit type
Top Category
Visibility
tb_comparator
dut
#INITIAL#29
#vsim_capacity#
Module
Process
Capacity
Statistics
Project
sim
Wave
2bit-comparator.v *
Transcript
VSIM 5> run
module comparator_gatelevel(input [1:0] A, B, output A_less_B, A_equal_B, A_greater_B);
wire tmp1, tmp2, tmp3, tmp4, tmp5, tmp6, tmp7, tmp8;
xnor u1(tmp1, A[1], B[1]);
xnor u2(tmp2, A[0], B[0]);
and u3(A_equal_B, tmp1, tmp2);
and u4(tmp3, ~A[0], ~A[1], B[0]);
and u5(tmp4, ~A[1], B[1]);
and u6(tmp5, ~A[0], B[1], B[0]);
or u7(A_less_B, tmp3, tmp4, tmp5);
and u8(tmp6, ~B[0], ~B[1], A[0]);
and u9(tmp7, ~B[1], A[1]);
and u10(tmp8, ~B[0], A[1], A[0]);
or u11(A_greater_B, tmp6, tmp7, tmp8);
endmodule
`timescale 1ns/ 10 ps
module tb_comparator;
reg [1:0] A, B;
wire A_less_B, A_equal_B, A_greater_B;
integer i;
comparator dut(A,B,A_less_B, A_equal_B, A_greater_B);
initial begin
for (i=0;i<4;i=i+1)
begin
A = i;
B = i + 1;
#20;
end
for (i=0;i<4;i=i+1)
begin
A = i;
B = i;
#20;




```
    end else if(temp7, ~B[1], A[1]);
    end else if(temp8, ~B[0], A[1], A[0]);
    or all(A_greater_B, temp6, temp7, temp8);
endmodule
`timescale    10 ps/ 10 ps
module tb_comparator;
reg [1:0] A, B;
wire A_less_B, A_equal_B, A_greater_B;
integer i;
comparator dut(A,B,A_less_B, A_equal_B, A_greater_B);
initial begin
    for (i=0;i<4;i=i+1)
    begin
        A = i;
        B = i + 1;
        #20;
    end
    for (i=0;i<4;i=i+1)
    begin
        A = i;
        B = i;
        #20;
    end
    for (i=0;i<4;i=i+1)
    begin
        A = i+1;
        B = i;
        #20;
    end
end
endmodule
```


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Msgs
/tb_comparator/A
/tb_comparator/B
/tb_comparator/A_l...
/tb_comparator/A_...
/tb_comparator/A_...
/tb_comparator/i
00
11
St1
St0
St0
4
Now
2800 ps
Cursor 1
0 ps