

↳ PCB - Printed Circuit Board

↳ Bus:

Minute Cu lines running from 8086 processor to other components

↳ 64 KB of memory
(4 ICs)

↳ In btwn processor & memory

↳ memory interface circuits
(6 ICs)

Pin Configuration: (Dual Inline package)

- 40 pins \Rightarrow 5 categories

① Address / Data bus \Rightarrow 16 bit data line

$AD_0 - AD_{15}$ 20 bit address line
 $A_{16} - A_{19}$

Form factor - Size of IC made small

Address & Data is multiplexed

Address & Data not used at same time

So, combined / multiplexed address & data lines

$AD_0 - AD_{15}$ - both address & data

1st bus cycle - Address 2nd " " - Data } Time multiplexed

$A_{16} - A_{19}$ - Solely for address

② Status signals

Status of operation (ALU) is shown in status reg.

- III by, what status of 8086 MP from external source is reflected in S pins
- It is multiplexed with address lines
 - 1st bus cycle : Address
 - 2nd " : Status (external comm.)

A₁₆ / S₃

A₁₇ / S₄

A₁₉ / S₆

$\overline{\text{BHE}}$ / S₇

S ₄	S ₄ / S ₃
0	0 \Rightarrow ES of memory being used by proc
0	1 \Rightarrow SS executed
1	0 \Rightarrow CS executed
1	1 \Rightarrow DS executed

From this, we can identify

Inst. fetch \Rightarrow CS

Data " \Rightarrow DS

S₅ : If interrupt flag is enabled

\hookrightarrow 1 or 0

flag register \Rightarrow IF

If $IF = 0 \Rightarrow S_5 = 0$

$IF = 1 \Rightarrow S_5 = 1$

S₆ : Always 0 \Rightarrow default

Buses under control of processor

If any external device wishes to comm.

with proc directly



At this time, S6 will be in high impedance state (neither low nor high)

[S7 later]

③ Control signals

Controls comm b/wn proc & memory/I/O

1) MN/MX [Only i/p control signal]

Min mode & Max mode



normal ope



multiple processors

(1 processor)

In 8086, multiple cores can't be connected,

but, co-processor (8087) can be ".

At that time, max mode is enabled

↓
floating pt operation

MN/MX is an i/p signal



1 \Rightarrow minimum mode

0 \Rightarrow maximum mode

Pin no: 33



I/P pin for MN/MX \rightarrow complemented

2) ALE

Address Latch Enable

To show that address is carried

\Rightarrow It is o/p signal

1 \Rightarrow carries address [AD₀-AD₁₅, A₁₆-A₁₉]
0 \Rightarrow orw

- Tells external devices

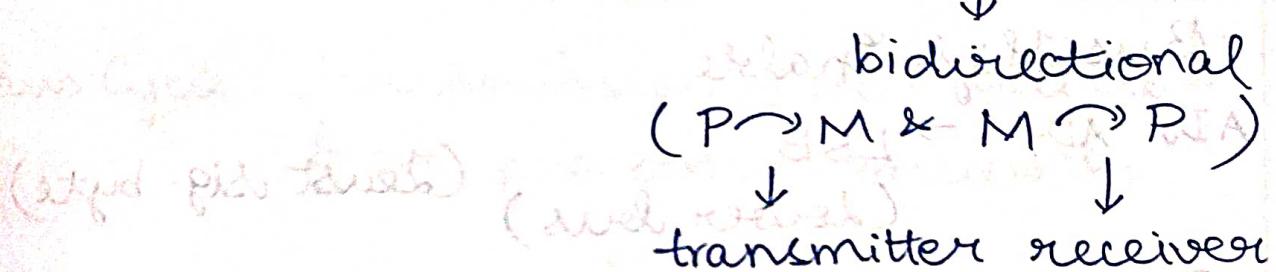
3) M/IO (Pin 28)

- Proc. can comm. with memory and I/O
- It is O/P Signal
 - ↳ 1 \Rightarrow memory
 - ↳ 0 \Rightarrow input/output device

M/IO

4) DT/R

Type / Direction of comm. in Data Bus



Read : Receiver

Write : Transmitter (For entire ope)

- It is O/P Signal

1 \Rightarrow transmitter

0 \Rightarrow receiver

5) RD:

- Read bus cycle

(Covered later)

- Out signal

↳ start pt of read bus cycle

↳ Only start timing

6) WR:

- Write bus cycle

- Start pt of write bus cycle

- Out signal

D DEN:

- Data Enable for enabling buffers during read
- $M \rightarrow P$
- To enable buffers \Rightarrow Only for read

- Out signal

↓
Bus Data fetched from
external devices

8) BHE:

- Bus High Enable

$AD_0 - AD_7 \rightarrow LSB$

(Lower bus) (Least sig. byte)

$AD_8 - AD_{15} \rightarrow MSB$

(High Bus) (Most sig. byte)

Multiplexed

Byte wide ope \Rightarrow No need high bus

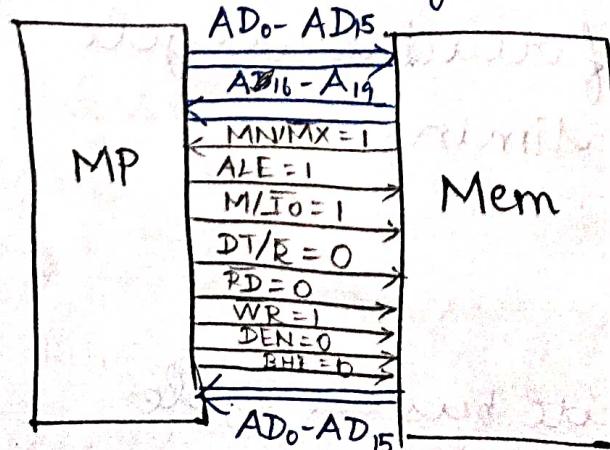
Word " " " \Rightarrow Both bus needed

- Usually only lower bus is enabled

- Using BHE, high bus is enabled

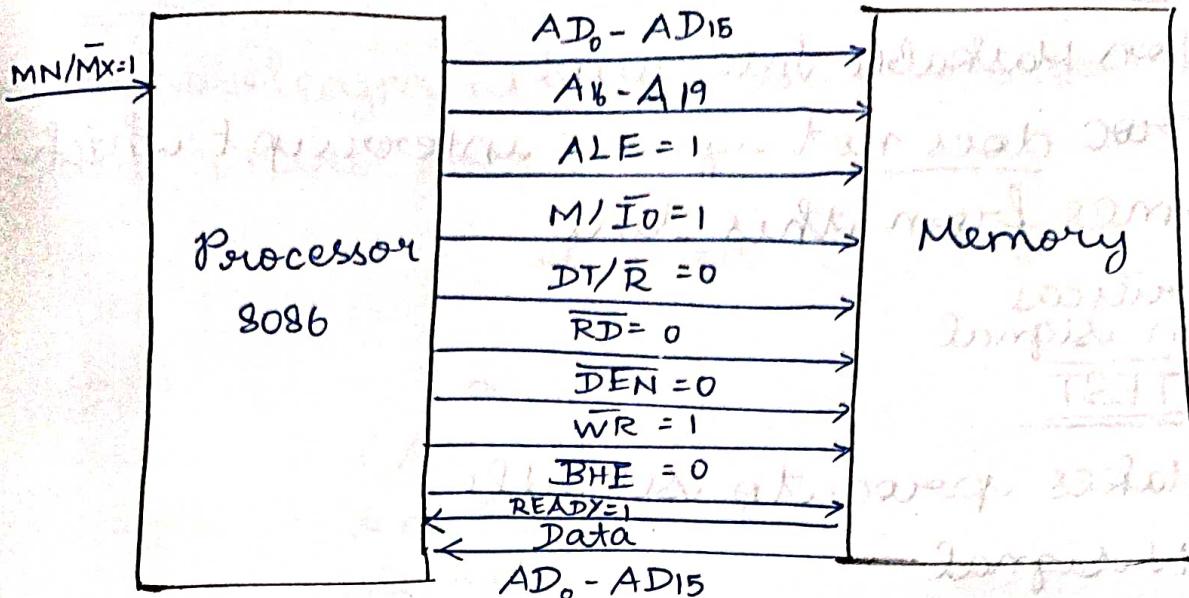
$I/P \Rightarrow 0 \Rightarrow$ high bus enabled

$O/P \Rightarrow 1 \Rightarrow$ high bus ~~disabled~~ enabled



To read a word
in min mode

$MN/M\bar{X}=1 \quad \overline{WR}=1$
 $ALE=1$ (dbt) $\overline{DEN}=0$
 $M/I\bar{O}=1 \quad \overline{BHE}=0$
 $DT/\overline{R}=0 \quad \overline{RD}=0$



Bus Cycle : Transmission of bus cycle to & from processor & memory

9) READY:

\rightarrow memory ready to perform opes
(Only signal from mem to proc.)

④ Interrupt signals:

1) INTR (Pin 18)

In signal

Sends from ext. device to proc.

2) INTA

- Out at ext. interrupt source generated
- Reply to request
- Interrupt acknowledgement
 - \rightarrow Proc. ignored interrupt ($IF = 0$) \Rightarrow Do not disturb
 - $0 \Rightarrow$ Proc. accepts interrupt

3) NMI:

- Non Maskable Interrupt
- Proc. does not ignore interrupt which comes from this line
- Critical
- IN signal

4) TEST:

- Makes proc. to sit idle
- IN signal
- 0: Hold
 - 1: Idle state (Pause proc.)
 - 0: Resume operation

5) RESET:

- Resets processors
- IN signals

NOTE:

All interrupt signals except INTA is IN signal

⑤ DMA:

- Direct Memory Access
- External device communicates to mem. through processor

① HOLD:

- Take over bus (by external device)
- IN signal
- Once sent, bus under control of ext. device

2) HLDA :

- acknowledgement given by processor to take control over bus

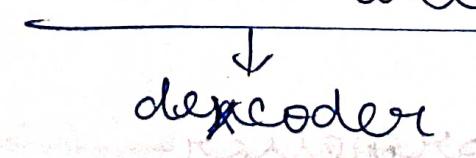
40 pins

20 pins
(Address & data signals)

Addl Data	Status	Control	Interrupt	DMA
AD ₀ - AD ₁₅ A ₁₆ - A ₁₉	S ₃ - S ₇	READY MN/MX' ALE' MIO' DT/R' RD' WR' DEN' BHE'	INTR INTA' NMI TEST' RESET	HOLD HLDA

24-31 holds different signals in MAX mode

Bus Admittation: (Max mode operations)

S₀, S₁, S₂ go to bus controller which generates
8 lines
8 lines : 

decoder

Sq'	S1'	So'	Signal
0	0	0	INTA'
0	0	1	IORC'
0	1	0	IOWC'
0	1	1	HLT
1	0	0	MRDC'
1	0	1	MRDC'
1	1	0	MWTC'

IORC':

G/P O/P read operation

IOWC':

I/O write operation.

MRDC': (100)

Instruction fetch.

MRDC': (101)

} Memory Read

Data Segment fetch

MWTC':

Write to data segment

LOCK:

Locks other processor

If a processor does not want to share info

QSi QSo, code \Rightarrow Status of inst. queue

0 0 - No ope

0 1 - First byte

1 0 - Queue empty

1 1 - 2nd byte

- whether proc. can pre-fetch instructions
& place in inst. queue

REQU

RQ/GT_i

RQ/GT₀

start

burst

Request

More than 1 device

Grant

can connect

↑ priority
11 signals produced by bus controller

RQ/GT₀

HOLD

RQ/GT_i

HLDA

LOCK

WR

S₂

M/I_O

S₁

DT/R

S₀

DEN

QS₀

ALE

QS₁

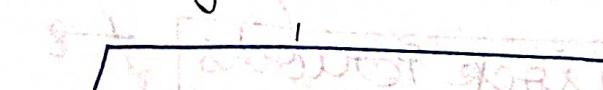
INTA

Max mode

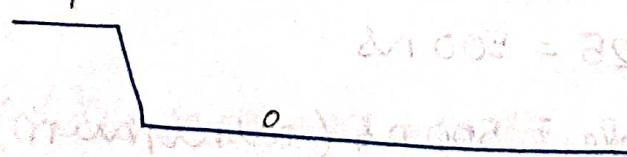
Min mode

Timing diagram:

M/I_O



DT/R

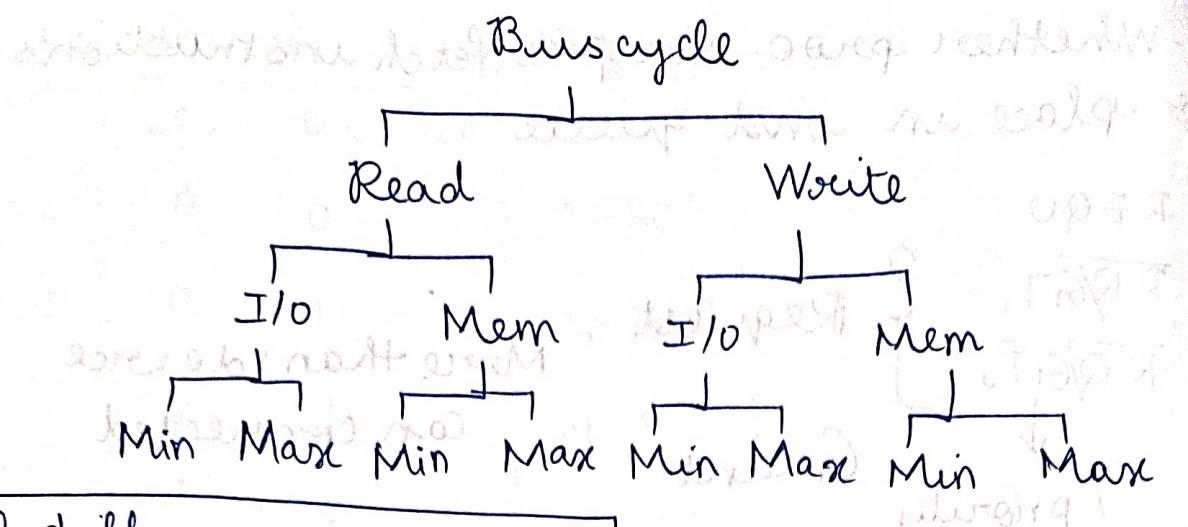


AD₀ - AD₁₅



=> mix of
0's & 1's

Bunch of lines representation



8 different bus cycles are there

Timing diagram: Representation of bus cycle

8086 \leftarrow 5/8/10 MHz frequency

$$\text{Clock period} = \frac{1}{F}$$

$$T = \frac{1}{F}$$

Ex:

for 8 MHz MP

$$T = \frac{1}{8 \text{ MHz}}$$

$$T = 125 \text{ ns}$$

1 Bus Cycle = 4 Clock Periods

Ex:

$$4 \times 125 = 500 \text{ ns}$$

1 buscycle = 500 ns (minimum)

(Any read or write operation)

If memory is slow, waiting time is also added.

- Based on Read & Write, we have address lines, which carries address & data

↓

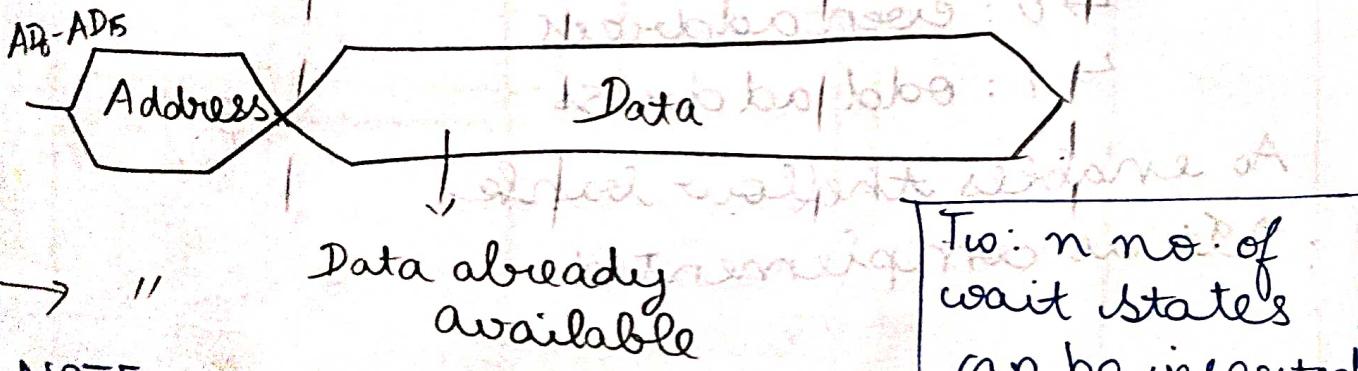
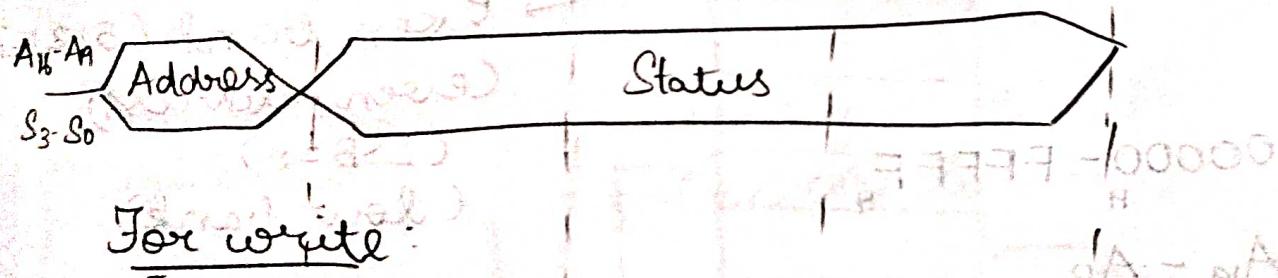
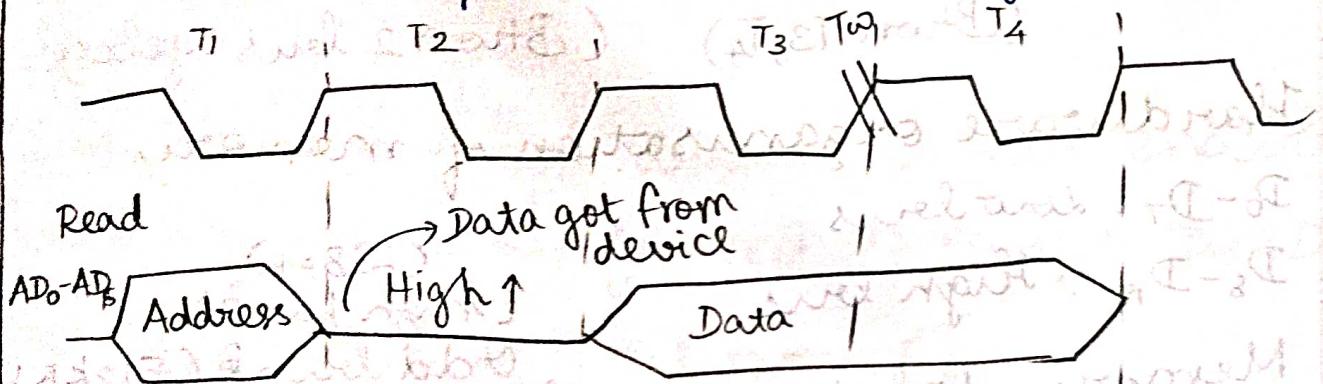
Level of data bus changes $\rightarrow AD_0 - AD_{15}$ is in

- In 2nd clock period, proc. is idle

(↑ impedance state)

- In 1st clock period - address carried

- In 3rd clock period, data is given



NOTE:

If external device is not ready, wait state is incorporated btwn T_3 & T_4 .

Ex: Wait for 2 clock periods

$$\text{wait time} = 2 \times 125 = \underline{\underline{250 \text{ ns}}}$$

Wait state : Clock period

- Idle state : ~~Processor does not use bus~~
- Between 2 bus cycles
 - Processor does not use bus
 - Represented using clock cycles
- Wait states
- Between asserted - between T_3 , T_4 (Btwn 2 bus cycles)
 - Between asserted - between T_4 , T_5 (Btwn 2 bus cycles)

Hardware organisation of memory :

$D_0 - D_7$: Low bus

$D_8 - D_{15}$: High bus

Memory split into

(LSB = 1)

(high bank)

Odd bank (512KB)

Even bank (512KB)

(even address)

(LSB = 0)

(low bank)

00000 - FFFFF_H

$A_{19} - A_0$

↳ 0 : even address

↳ 1 : odd address

A_0 enables the (low bank)

\Rightarrow It is complemented

1115

(Diagram refer)

BHE used for enabling high bank

$A_{19} - A_1$ connected to both ICs (low & high bank)

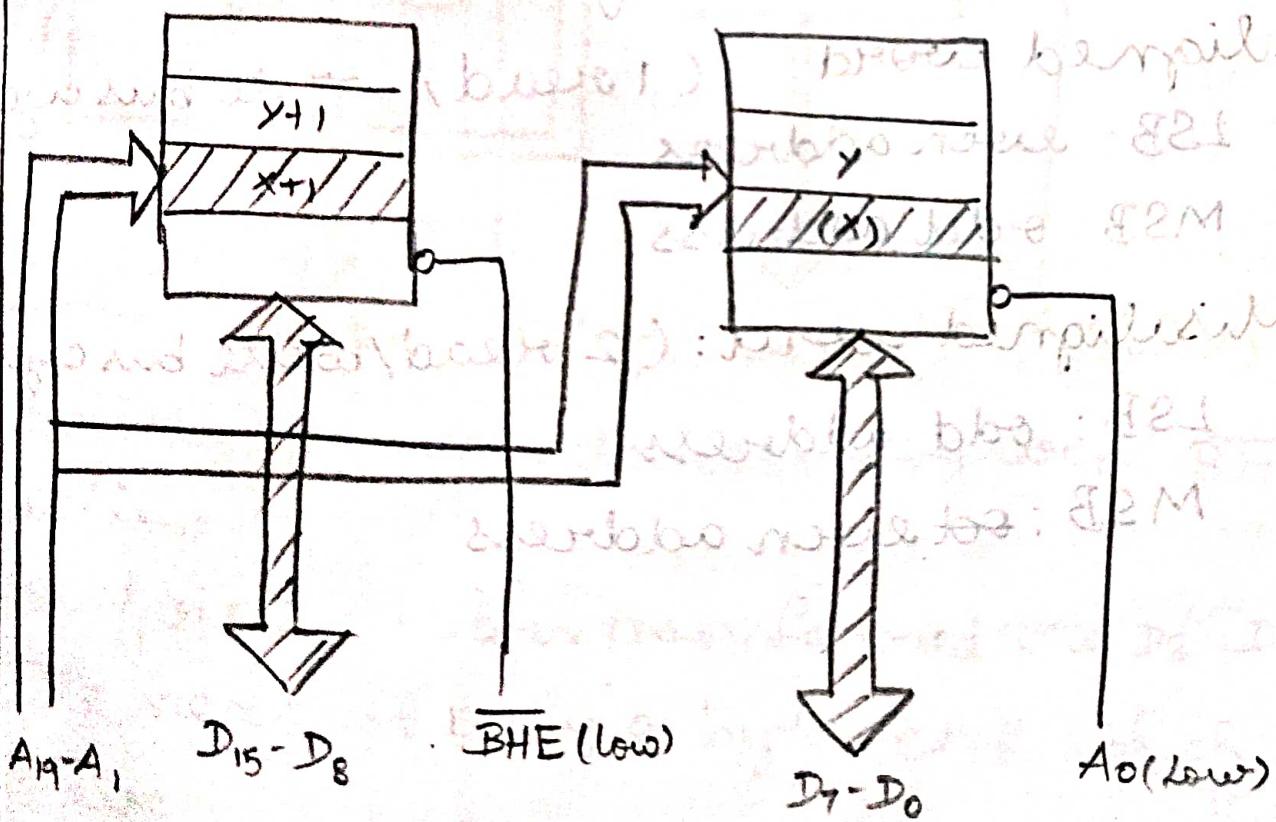
$D_7 - D_0 \Rightarrow$ low bus

$D_{15} - D_8 \Rightarrow$ high bus

To transfer a byte: (from low bus)

- A₀ is low
- So, Low bus is enabled
- So, the data from low bank is transferred to D₇-D₀.
- Also BHE does not enable High bus
- A₁₉-A₁ is transferred to both banks.
- But, as the high bank is not enabled no data is transferred through D₁₅-D₈.

Fetch word from memory:



45|A2

MSB LSB

D₈ - D₁₅ D₀ - D₇

To fetch: a word from 11114

- ↳ 11114 is even address
- ↳ A₀ is active low, which enables low bank
- ↳ Data (A₂) is transferred to D₀ - D₇
- ↳ Considers the next address : 11115, which is odd address
- ↳ BHE is low, which activates high bank
- ↳ Data (45) is transferred to D₈ - D₁₅

Aligned word:

LSB: even address
(1 read/write bus cycle)

MSB: odd address

Misaligned word:

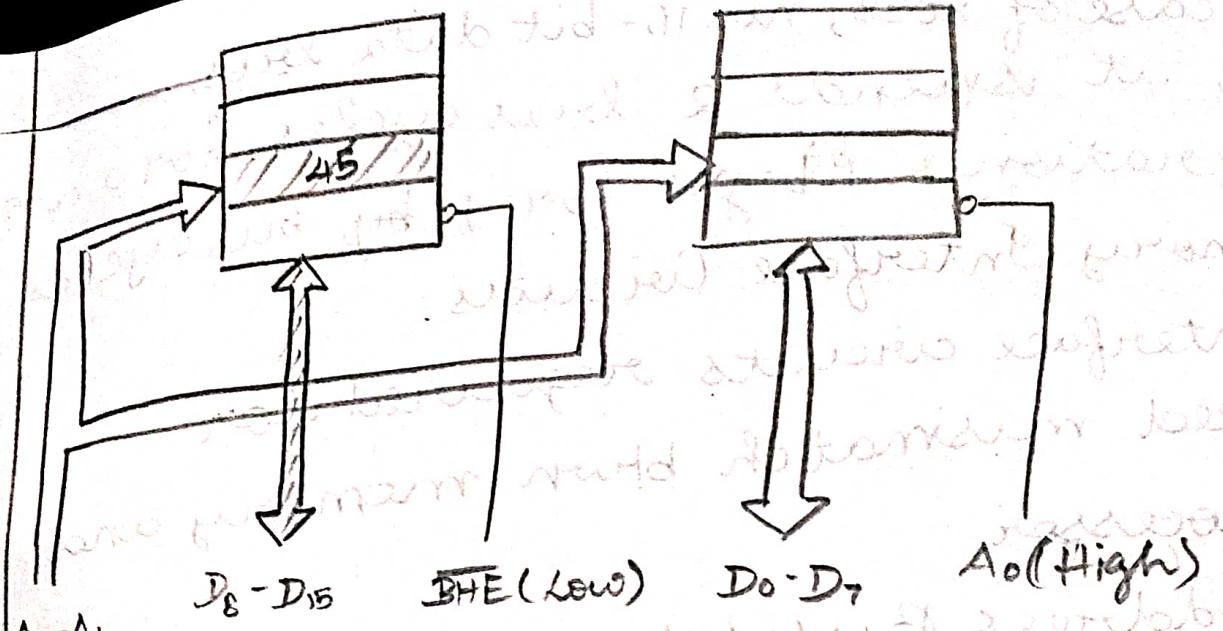
LSB: odd address
(2 read/write bus cycles)

MSB: even address

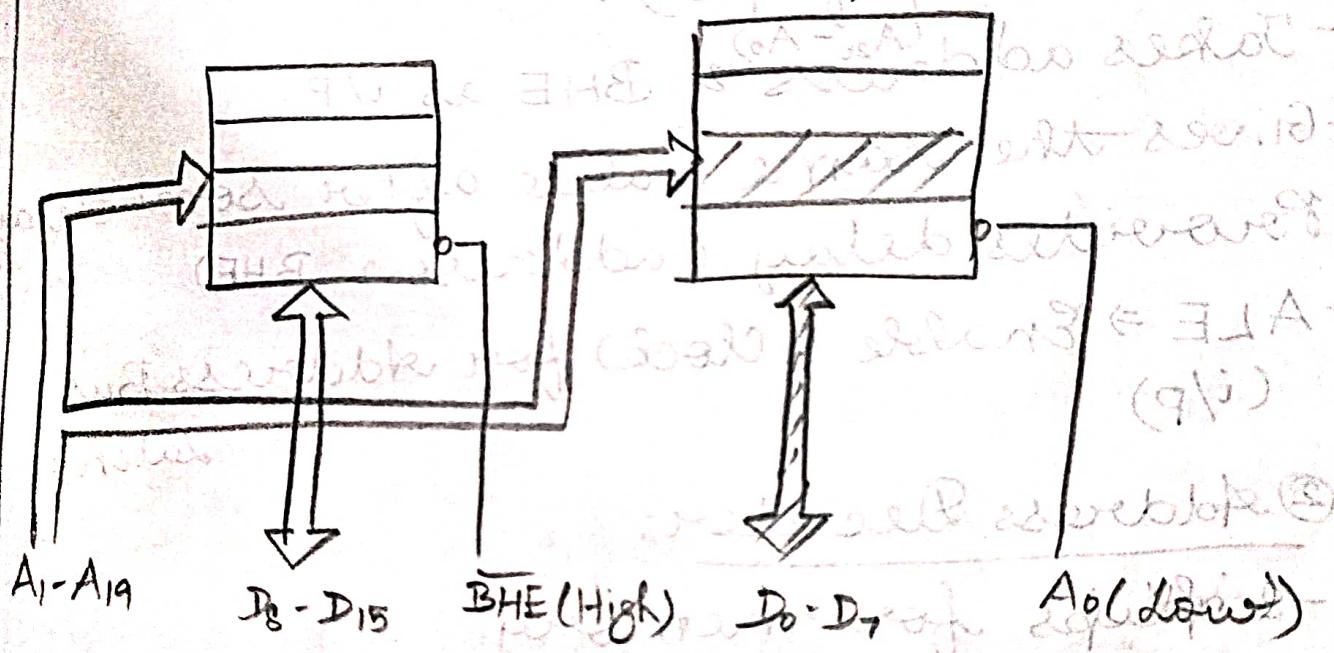
MSB	LSB
68	
45	
A2	
11114	

4568 next.

0815



45 - 68



Firstly, as odd address is given, BHE is low.

So, firstly LSB is transferred to D₈-D₁₅. The next is only a byte fetch which is even.

D₀-D₇ uses tag block pins.

In case of 8088, no 16-bit data bus,
so, it spends 2 bus cycles for a word
operation & 1 byte for 1 byte bus cycles

Memory Interface Circuits:

- Interface circuits required for speed mismatch b/w memory and processor

① Address Bus Latch:

- Latch (Flip flops)
- Takes address $(A_{20} - A_0)$ & BHE as i/p
- Gives the same value after some delay
- Provides delay (address & BHE)
- ALE \Rightarrow Enable (Clock) for Address Bus (i/p)

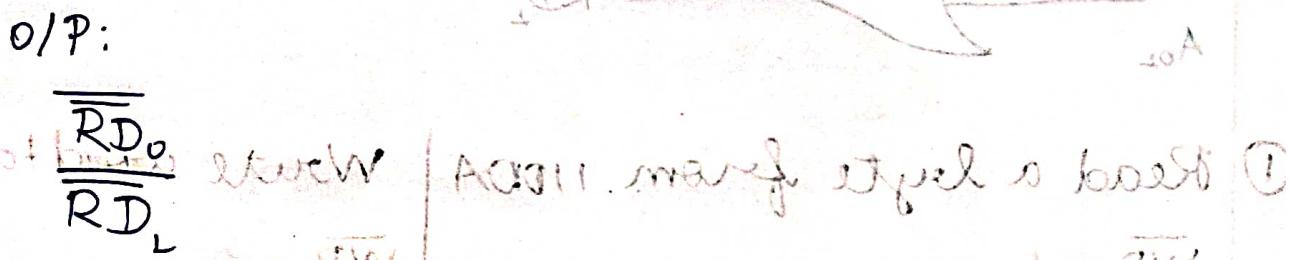
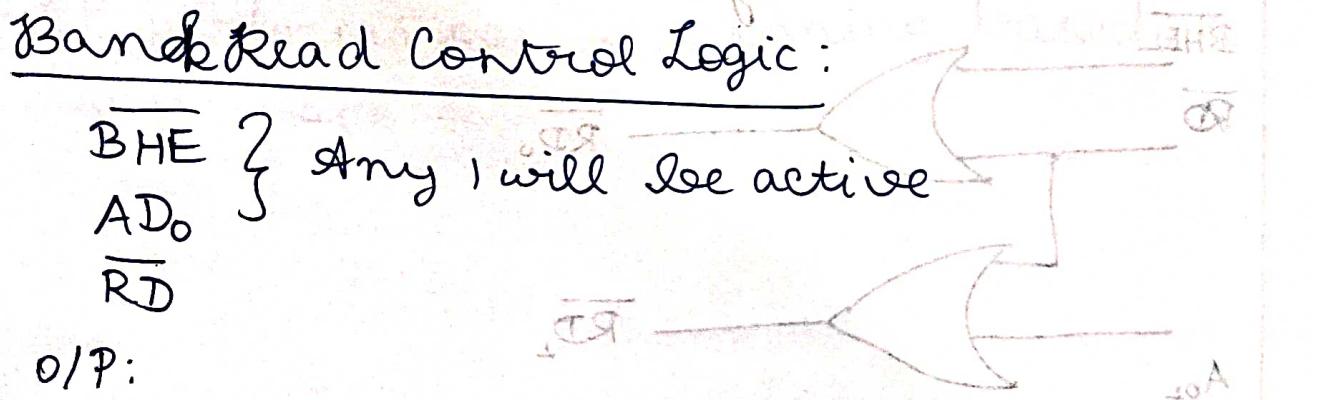
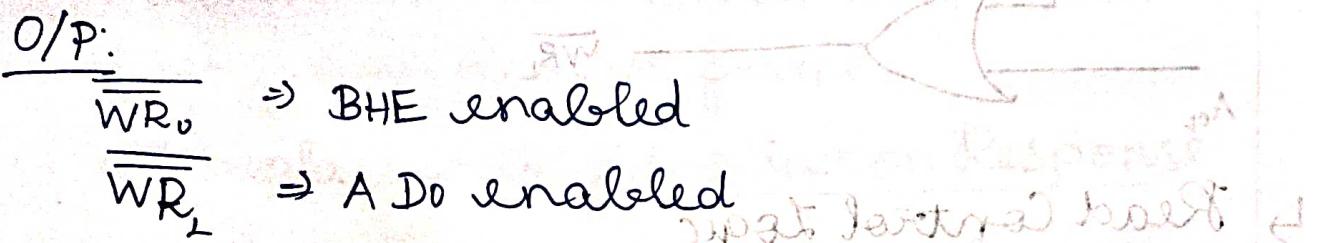
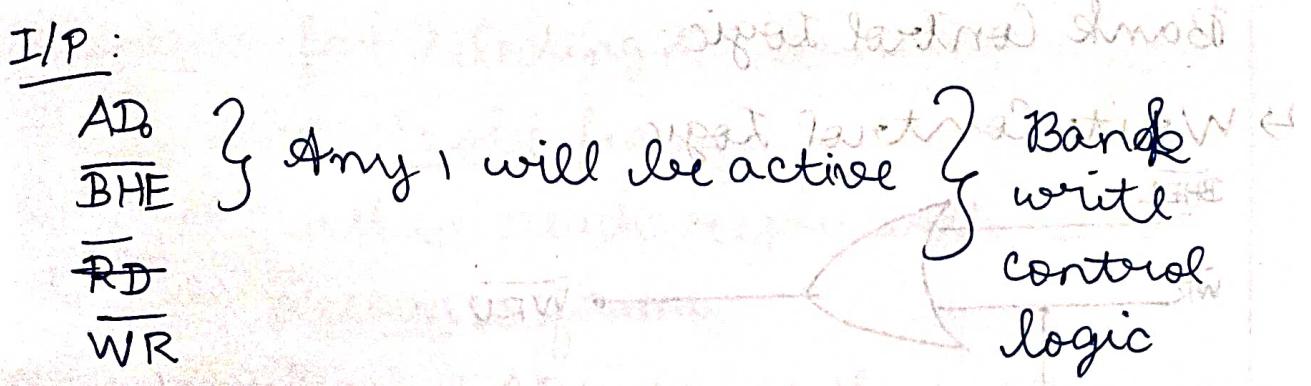
② Address Decoder:

- 8 chips for memory
- byte : 1 memory
- word : 2 memory
- Reduce power consumption
- Input : $AD_{17} - AD_9$
- Output : $\overline{CE}_0 - \overline{CE}_7$

only 1 will get enabled
- 3×8 decoder

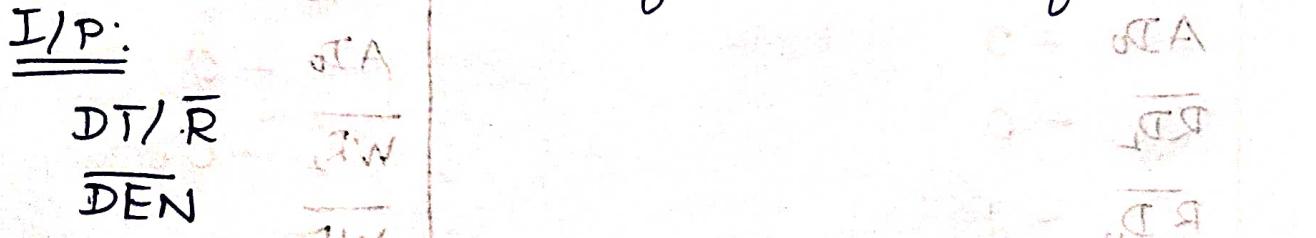
③ Bank Control Logic:

Bank \rightarrow Odd
 \rightarrow Even

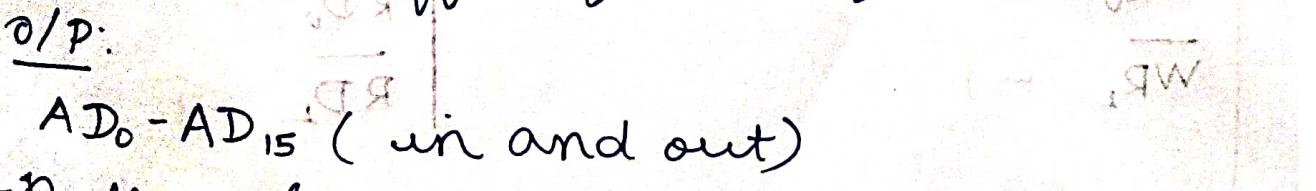


④ Data Bus Transceiver Buffer:

- Control direction of data transfer



- Acts as buffer for delay

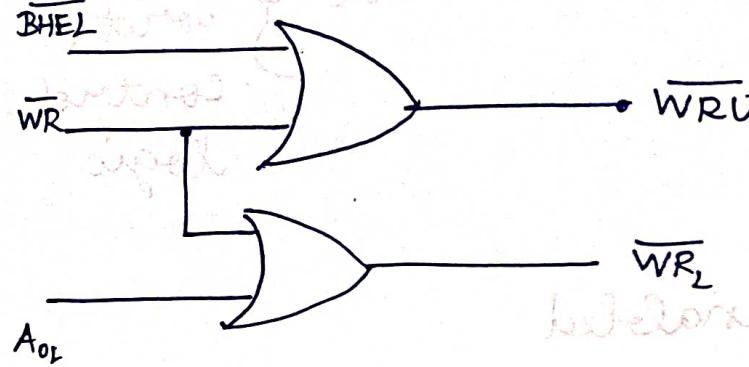


AD₀ - AD₁₅ (in and out)

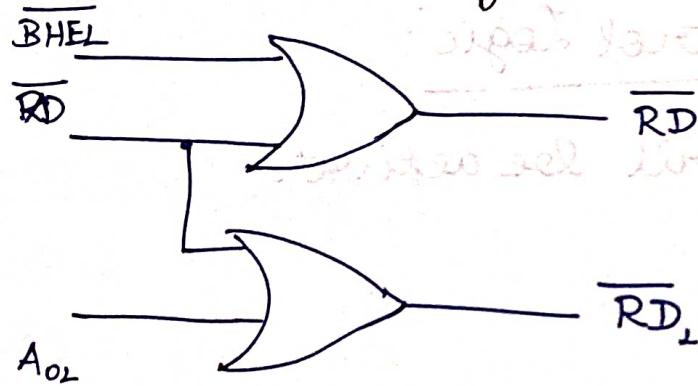
- Buffer: storage medium like flip flops

Bank Control Logic:

Write Control Logic:



Read Control Logic:



① Read a byte from 1100A

$$\overline{WR} = 1$$

$$\overline{RD} = 0$$

$$\overline{BHE} = 1$$

$$AD_0 = 0$$

$$\overline{RD}_U = 0$$

$$\overline{RD}_V = 1$$

$$\overline{WR}_U = 1$$

$$\overline{WR}_L = 1$$

Write word to 1100A

$$\overline{WR} = 0$$

$$\overline{RD} = 1$$

$$\overline{BHE} = 0$$

$$AD_0 = 0$$

$$\overline{WR}_U = 0$$

$$\overline{WR}_L = 0$$

$$\overline{RD}_U = 1$$

$$\overline{RD}_L = 1$$

(This bank has 1100A - 1101A)

Bank of 16K bits, maximum operating speed?

Technique for Selecting AP : Scanning

- ↳ Node sends Probe frame
 - ↳ All APs within reach reply with Probe Response frame
 - ↳ Node selects 1 AP & sends that AP an Association Request frame
 - ↳ AP replies with Association Response
- AP performs passive scanning based on Beacon frame