26) Changes to sPentium compared to its predecessory 1) Cache: The predecessors like 8086 used a single 816 cache that was shared b/w data and instructions. This could lead to data intense programs running out of cache for instructions. This is solved by having two 8 KB caches One bor data and one for instructions.
Also, has 64 bits data bus, which allows it to redd

2) Memory

2) Memory Has 4MB of memory similar to predesuon Themsemory is divided into 8 banks which can be scleded using Bark Froble Signals. Unlike 8086, the parity check is built in. also, Address is also checked for parity When APCHK is logic O, the addessus are not valid and the execution is stopped.

16) () () It has been replied

3

3) Timing and olds Halade A ca 3) Branch prediction.
Pentium implements branch prebetching using branch prediction. This allows the enecution of the branch instruction in one clock cycle if the prediction is correct (most of thetime or three dock cycles it items. 4) Super o calar archi tecture. Pentium has three execution units 1) A coprocessor to execute floating point instructions eg: FADD ST, ST(2) 25 A U-pipe amountion unit to one wite integer instructions (primary) 3) A V-pipe enecution unit to execute integer instructions (slower) This means 3 instruction when independent

can be simultaneously executed

coprocuor Upine

eg: FADD ST, ST(2), MOV AX, 5

MOU BX,6

ony

won

5) A 64 bit data bus This allows the processor to read either a bit byte (8 bits) doubleword (32 bits) or a

awad word (64 bits)

based on the Bank Enables chosen This contributes a faster throughput and also allows longer bloating point

numbers and instructions.

		173 7	A CONTRACTOR OF THE PARTY OF TH	
10	Feature	13	15	i 7
,,)	Cores	2-4-40	4-6	6-8
	Threads	4-878	8-12	12-16
	Cache	32mB L3	64 MB L3	256 MB L3
	Over clocking	Not available	in K scies thin	in K series Chips
	Turbo boost	No	Yes 9 9	Yes
	Hypen threading	No	Yes	Yes
	Power consumption	35W-65WTO	65-95 W TOP	65-125 N
	308 30075			1DP

Features of intel 13,15,17 chips i3: used for low power intensive work loads like web browsing and office usage. used for higher Thensive north like 73: profesioral wo software with the grant of the section of the i7: for high and gaminy and scientific triod computing. Over clocking: Increasing the clock speed over the base frequency, this directly increases the -16 throughput, usually done monvally. MB L3 Tarko Boost: This is a beatone which auto matrally L series increases the clock brequery over the hips base level, based on the aroount of nortload.

Hyper threading:

Divides a physical core into two logical throats, hence into parallelising it and improving the through put.

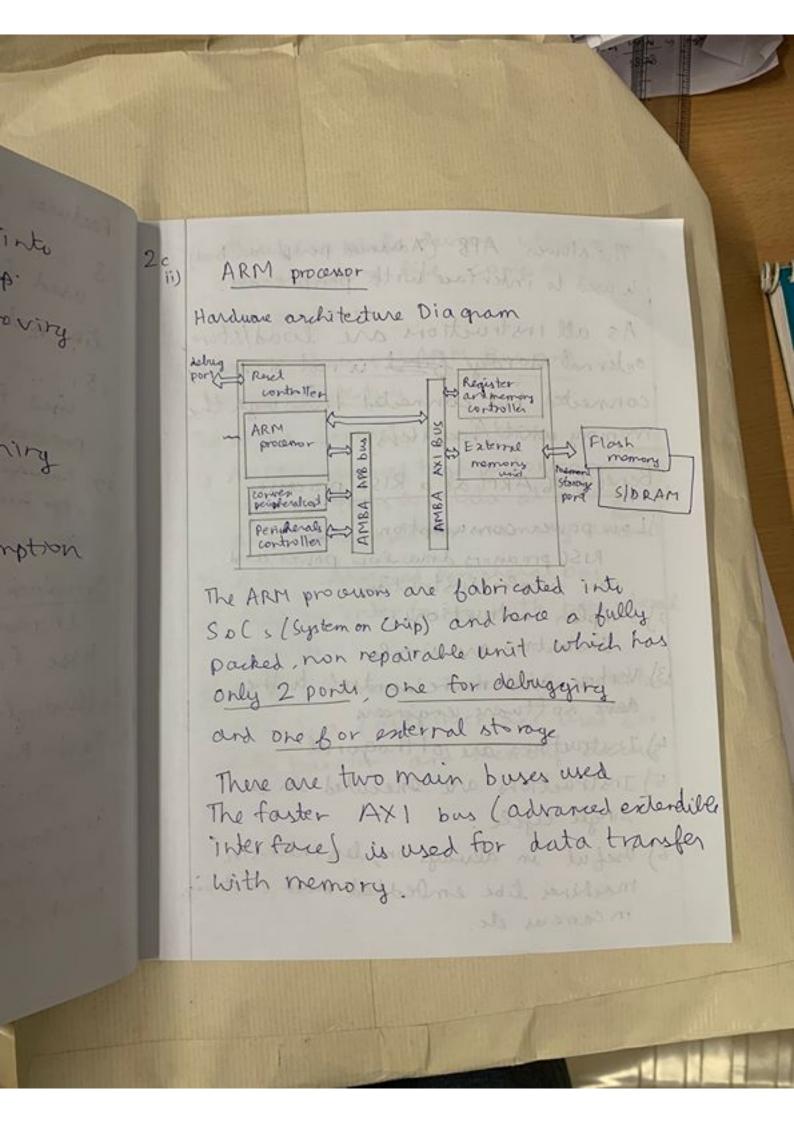
This takes advantage of parallelisation and pipelining

Power consamption:

Interms of power consumption and head produced

13 L 15 L 17

applicate promoned dools all as



The slower APB (Advanced peripheral bus) is used to interface with peripherals.

As all instructions are load/stone enternal storage first is not directly connected but connected through the memory unit (requirens)

Benefits of ARM as a RISC processor

1) Low power consumption:

RISC processors draw-low power and use simples instruction,

2) Simpler instructions:

Instructions are simple

- 3) Verbose and more control to the
- 4) Instructions are ofthogoral
- 5) Instructions are enecuted in a single cycle.
- 6) Useful in always on, less intensine machines like embedded moch electroniq. in cameras etc.

& buy stone edly

And in mobile devices which greatly improve battery life compared to CISC processors.

Salient features of ARM Bus and Memory Architecture

The AMBA consists of 3 buses

- 1) AHPB advanced high performance, bus
 This bus transfers data at a high rate
 and hence used for memory accen.
- 2) APB Advanced peripheral boy Used for interfacing with peripheral devices.
- 3) AXI Advanced Extendible Intertace. This is a bout interface used for data transfer and memory acress.

wing.