Dear Students,

Following are the details about the textbooks you have to refer for CA I.

Portions: Unit I & II

COs covered: CO1 & CO2

INTRODUCTION : Fundamental Components of Embedded Systems - Challenges for Embedded Systems - Examples -Programming Languages - Recent Trends in Embedded Systems - Architecture of Embedded Systems

Book: Sriram V Iyer, Pankaj Gupta , "Real-time Systems Programming", Tata McGraw-Hill Publishing Company Limited Chapter 1

Embedded Design Life Cycle - Development Environment

Book: Arnold S Berger , "Embedded Systems Design - An Introduction to Processes, Tools and Techniques", Elsevier Chapter 1, 2

MEMORY AND INTERRUPTS : Types of Memory - Direct Memory Access - Common Memory problems - validating memory contents - Interrupts - Interrupt Service Routines

Book: Sriram V Iyer, Pankaj Gupta , "Real-time Systems Programming", Tata McGraw-Hill Publishing Company Limited Chapter 3, 4, 5

Memory Testing (Self study)

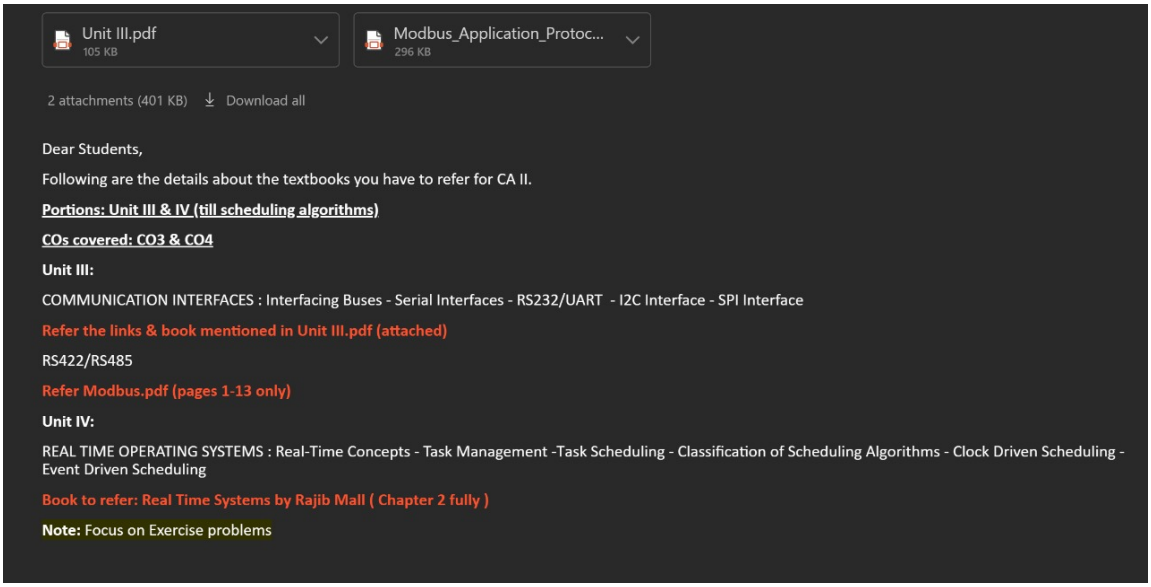
https://barrgroup.com/embedded-systems/how-to/memory-test-suite-c

UNIT 1

1. Design Challenges in Embedded System
2. Selection of a Processor
3. Significance of Co-Design and Co-Verification Process
4. Embedded Design life Cycle - Scenario based
5. Hardware/Software Partitioning
6. Components of a Embedded System(less important)

UNIT 2

1. Volatile Keyword - Significance
2. Interrupt Service Routine
3. Re-entrancy
4. Myths related to Memory Management - 4
5. Write Operation - Read Operation - Timing Diagram
6. Guidelines to be followed for ISR
7. Incorrect Handling of Interrupts and resolve issue - debugging ISR



UNIT - 3

1. SPI - Master Slave Configuration
2. Data Transfer on I2C Bus
3. Consider two DTEs such as two PCs connected via RS232 (DB9 connector) using null modem cable. Draw the null modem cable connection to demonstrate full hand shaking.
4. Choose appropriate communication protocol for a given scenario

Dear Students,

Following are the details about the textbooks you have to refer to for CA III.

Portions: Unit I - Unit V

COs covered: CO1 - CO5

Unit IV:

Resource Sharing – Priority Inheritance Protocol - Priority Ceiling Protocol

Book to refer:

Chapter 3 - Real Time Systems by Rajib Mall

Unit V:

VALIDATION AND DEBUGGING : Host and Target Machines - Validation Types and Methods - Host Testing - Host- Based Testing Setup - Target Testing - Remote Debuggers and Debug Kernels - ROM Emulator - Logical Analyzer Background Debug Mode - In-Circuit Emulator

Books to refer:

Chapter 12 - Sriram V Iyer, Pankaj Gupta , "Real-time Systems Programming", Tata McGraw-Hill Publishing Company Limited, New Delhi, 2006
Chapter 6,7&8 - Embedded Systems Design: An Introduction to Processes, Tools, and Techniques by Arnold S. Berger

UNIT - 4

1. Deadlock and Chain Blocking issues in Priority Inheritance Protocol(PIP)
2. Cyclic Scheduling - What is the major cycle,frame size and feasible schedule
3. Event Driven - Check if schedulable by RMA,DMA,and EDF and draw schedules
4. Given a scenario of tasks and resources after time t and some operations what is the priority of the tasks in PIP
5. List types of real time tasks and discuss characteristics of them
6. Explain constraints to be checked to decide frame size
7. Explain the operation of Priority Inheritance Protocol to resolve priority inversion? Highlight the issues of Priority Inheritance Protocol when sharing critical resources among real time tasks using examples ? Show how Priority Ceiling Protocol overcomes those drawbacks?

UNIT - 5

1. Explain ROM Emulator in target System testing
2. Salient features of logic analyzer tool? Advantages and limitations
3. What are limitations of host testing and why host testing when it has limitations compared to target testing
4. Significance of Debug Kernels and compare with other target testing tools
5. Show how Host testing is used to effectively debug an embedded system
6. Discuss the embedded system tools used for target testing and debugging when the system is in stable condition