



PSG COLLEGE OF TECHNOLOGY, COIMBATORE -4. F 22416

16 Pages

Roll No.	Name of the Student	Signature of the Student	Signature of the Invigilator				
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Branch & Semester	BE CSE	5	Test No. 3 Date 22.10.2024				
Course Code	19Z502	Title Microprocessors and Interfacing					
Faculty Use	Marks Scored				Grand Total (Out of.....)	Faculty Signature	
	Qn.	a	b	c			
	1	5					5
2	6	5	5	10	26	31	✓

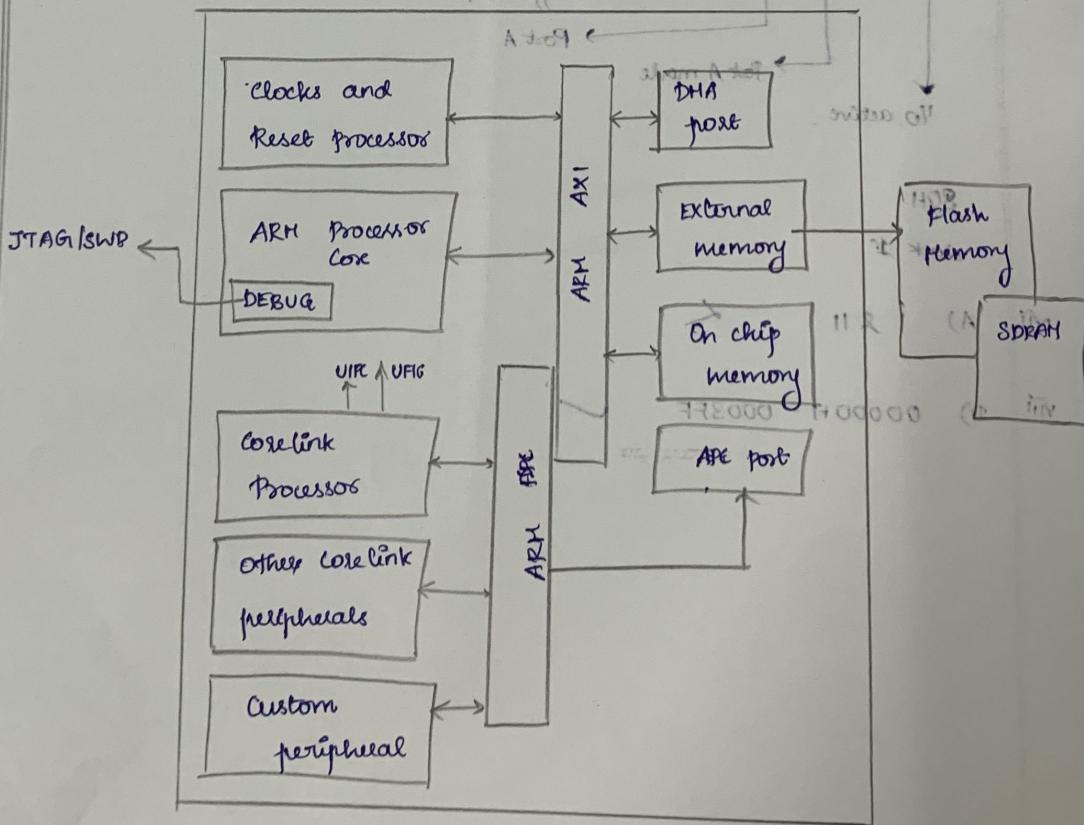
- 2 a.
- D) ARM ✓
 - Protected ✓
 - A) 16 threads ✓
 - B) Turbo boost ✓
 - B) Analog-to-digital conversion. ✗
 - 8, 32 ✓
 - C) It has built-in Ethernet ✓

2.c.

ii)

Hardware architecture diagram of ARM processor

(Advanced RISC machine) processors.



clock → To synchronize. The more faster the clock cycle, the more no of instructions per second increases.

Reset → To re initialize the processor.

ARM processor core → The heart of the processor to process instructions and perform operations.

DEBUG → To rectify the code.

JTAG (Joint Test Action Group)

Core link processor → has UPI, and UFLC for fast processing

Peripherals → The external devices connected to it. e.g.

Keyboard, mouse, etc.

AXI → Extensible Interface.

DMA → Direct Memory Access

External memory → Use Flash memory and SDRAM

On chip memory → SoC

benefits as RISC processor: (Reduced Instruction Set Computer)

* It has simple, small set of instructions

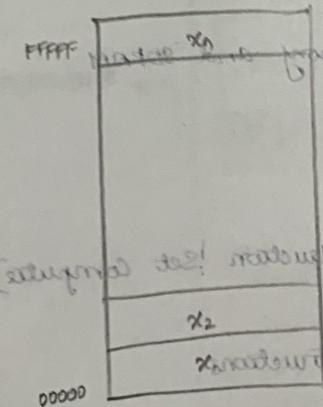
* Each instruction takes one clock cycle.

* Consumes less power.

- * Faster than CISC with advantages of → short
- * simple pipelining, not complex
- * Simple Hardware Implementation at → short
- * Easy to Implement and Debug
- * More code required to implement tasks
- * Efficient utilization by less power and resource consumption.
- * High performance.

Salient features of ARM Bus and Memory Architecture:

ARM memory



- * It has effective memory management.
- * Memory locations are contiguous.
- * With k bits of address bus, 2^k memory locations can be derived.

In addition to built-in memory,

now days we have external memories like SRAM, EEPROM, flash etc. which can be used.

ARM Processor

Salient features of ARM memory & bus:

- * ARM v7 (32-bit)
- * ARM v8 (64-bit), following needs of real applications
- * High performance
- * Low power consumption.

AMBA

(Advanced Microcontroller Bus Architecture)

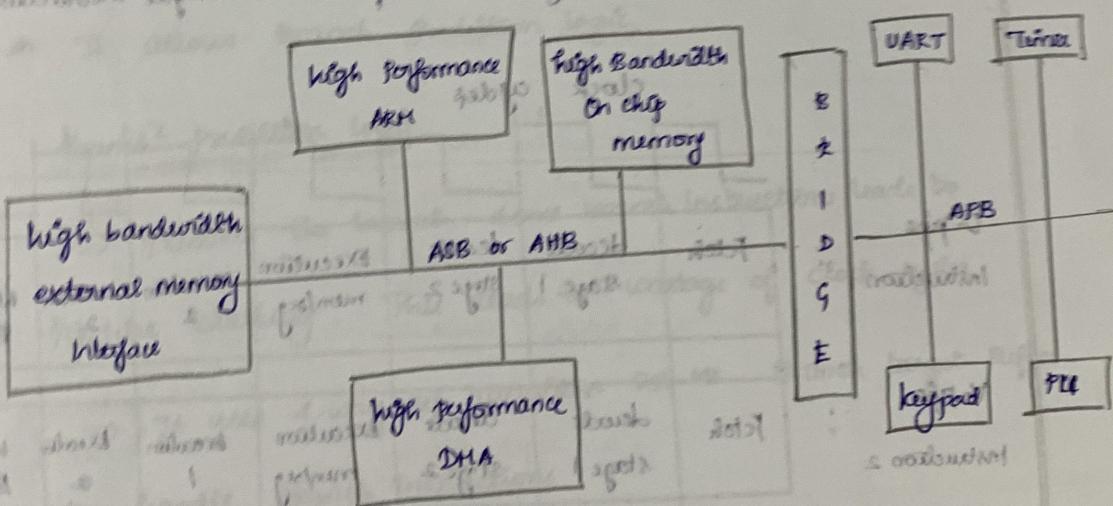


ABB → Used for simple cost effective design

AHB → Used for High performance and high clock
synthesized design

APB → Used for low power & speed. Low power consumption
design.

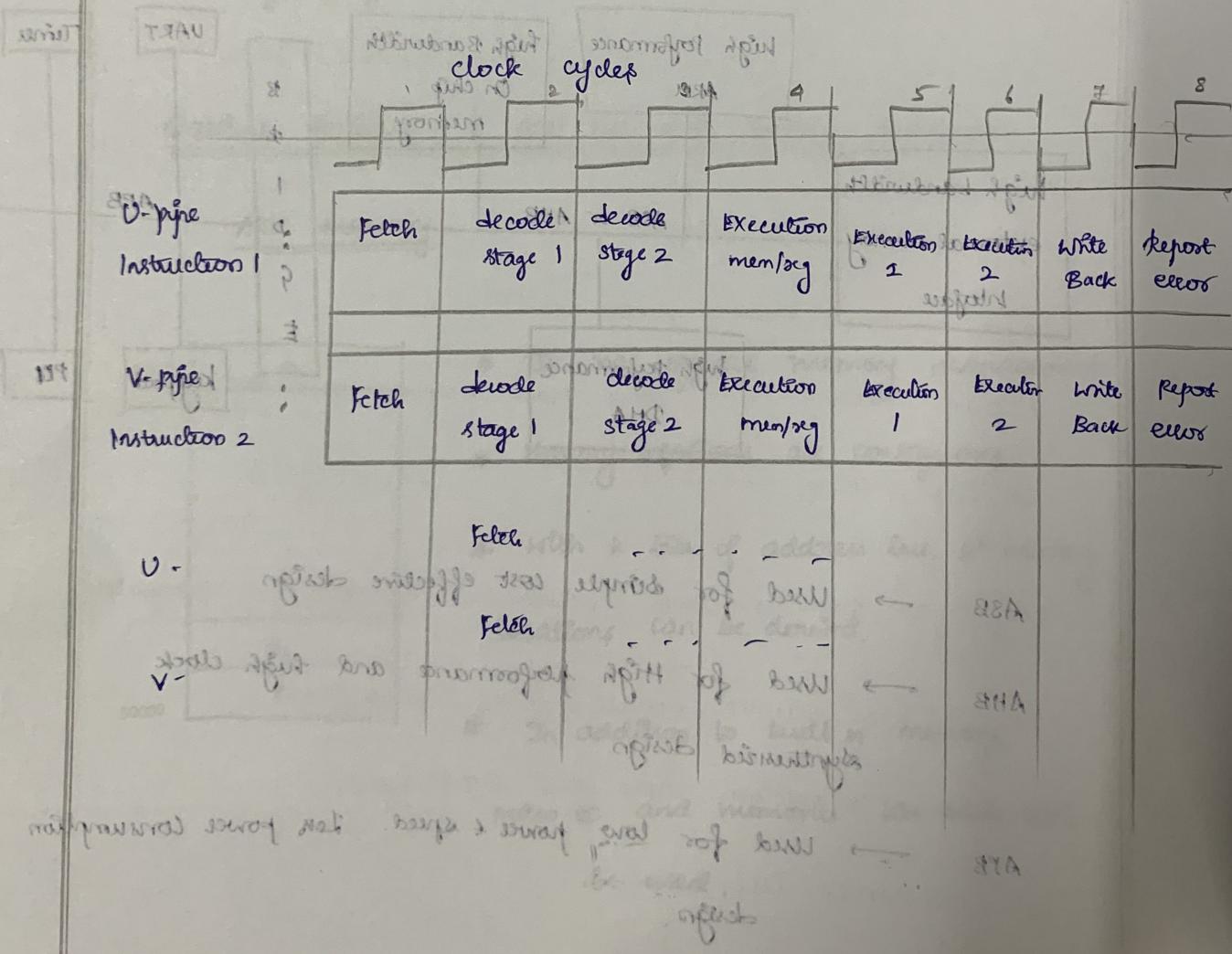
2 b

Improvements in Pentium Processor's Performance

- * It has super scalar architecture where 2 or more instructions can be done parallelly (in a) single clock cycle. It promotes parallelism, which improves efficiency & throughput.
- It has U-pipe and V-pipe:

U-pipe → used for all instructions

V-pipe → can only be used for some simple instructions.



- * It has 5 stages of pipeline (fetch, decode, execute, write back, report error)
- * Both U and V pipe performs all these stages in same clock cycle.
- * It has additionally Floating Point Unit. Which has 3 stage pipeline.
- * It has 64 bit data bus, and 32 bit address bus.
- * It allows Branch Prediction logic.

Branch Prediction logic

⇒ Predicts the branch. Some branch instructions leads to Pipeline stalling. This leads to wastage of clock cycles.

⇒ It uses 4-way set associative 256 KB Branch target Buffer to handle branch instructions.

⇒ It predicts the Branch Instructions (CALL, JMP, RET) before they lead to stalling

⇒ Uses 4-bit of history data for prediction.

⇒ Has conditional & unconditional branch

5	6	7
8	9	10
:		
21		
28		
29		

27	28	29

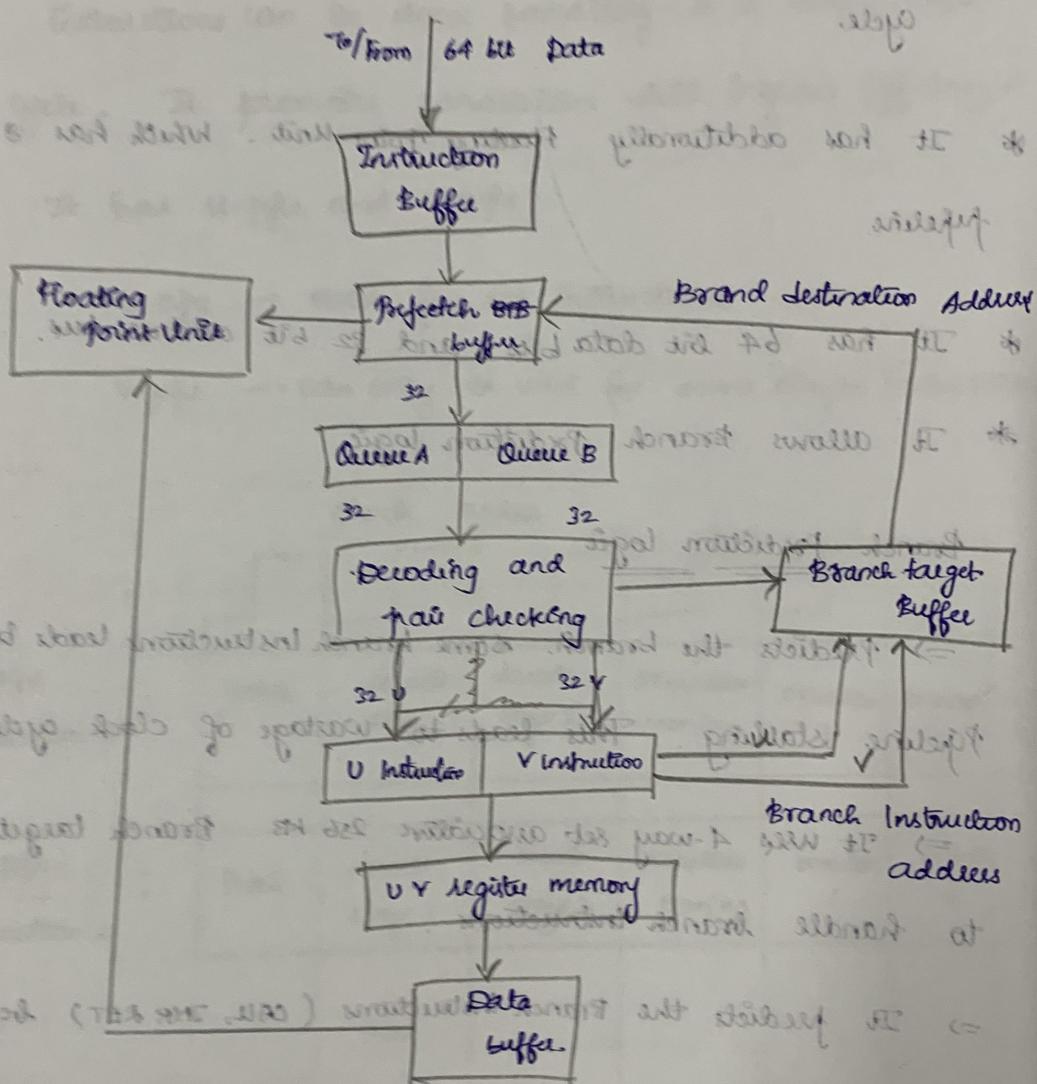
After Branch

5	21	24	29

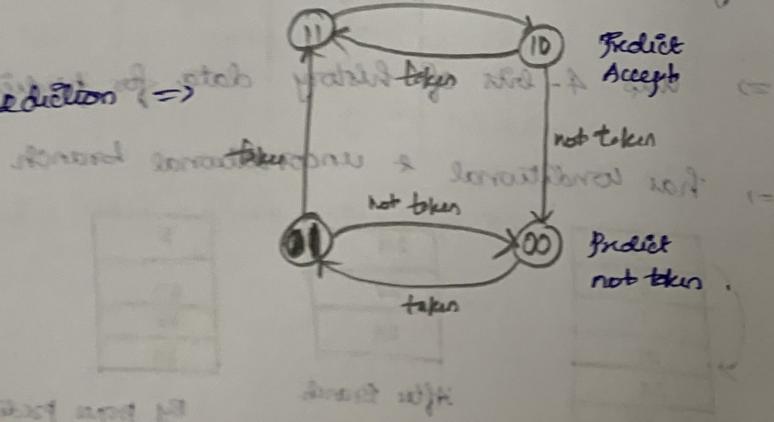
By Probe prediction

- * Has separate instruction and data buffer to avoid contention (if both are needed at a time)

Block diagram of Pentium Processor



Branch prediction \Rightarrow



P3, I5, I7 (hardware & software)

2 b
ii)

P3	I5	I7
* Used for low end applications	* Used for mid-range daily use computer	* Used for high-end where high processing power is needed
* 4 threads	* 4 threads	* 8 threads
* 3 - 4 MB cache	* 3 - 8 MB cache	* 4 - 8 MB cache
* Clock cycle 8 GHz 1.8 - 3.5 GHz	* Clock cycle 1.9 - 3.8 GHz	* Clock cycle 2.6 - 3.7 GHz
* dual core - 2 cores	* quad core 4, 2 or sometimes 6	* Cores = 6, 8, +
* does not support turbo boost	* Supports turbo-boost	* Supports turbo-boost
+ does not support virtualization technology	+ Supports virtualization technology	+ Supports virtualization technology
+ does not support Intel vPro	+ does not support Intel vPro	+ Supports Intel vPro
+ eg : documentation, watching video etc	+ eg: web browsing, word processing, spreadsheets, etc.	+ eg: graphic designing, video editing, gaming, etc.