LOGIC ANALYSER

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INTRODUCTION

- **Design verification** is vital in the embedded system design process.
- Possible choice for verification - **simulate** the system
- High-level model - simulation is fast - **not accurate**.
- **Runtime information** is extremely important.
- Necessary to **debug and validate** the system.
- Logic Analyzer - capable of showing **the relationship** and timing among many **different signals** in a **digital system**.

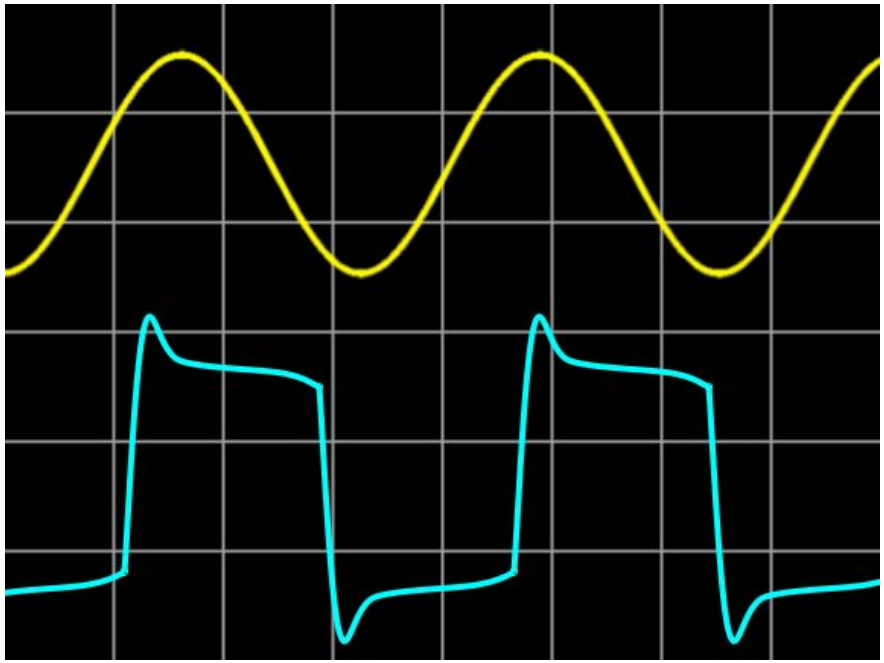
FEATURES

- Recording Several Input Channels.
- Complex Digital Triggering
- Mixed-Signal Capability
- Portability
- Ease of Data Navigation
- Quick Digital Measurements
- Decode and Search Transmitted Data

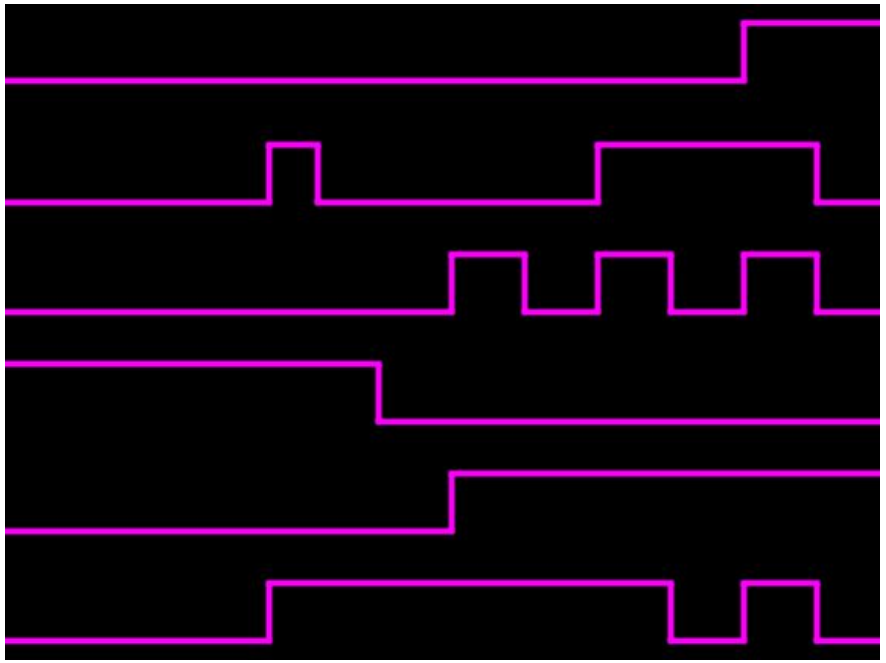
FORM FACTORS

- **Portable logic analyzers** - have the more traditional "test equipment" form factor, often larger than most workbench oscilloscopes.
- **Modular logic analyzers** - rack- or PC-mounted cards that slide into a mainframe or backplane.
- **PC-based logic analyzers** rely on computers to perform the heavy lifting of displaying and analyzing the captured data.

HOW LOGIC ANALYZER IS DIFFERENT FROM OSCILLOSCOPE ?



Example of an **oscilloscope** displaying a sine wave and overshoot on **two channels**

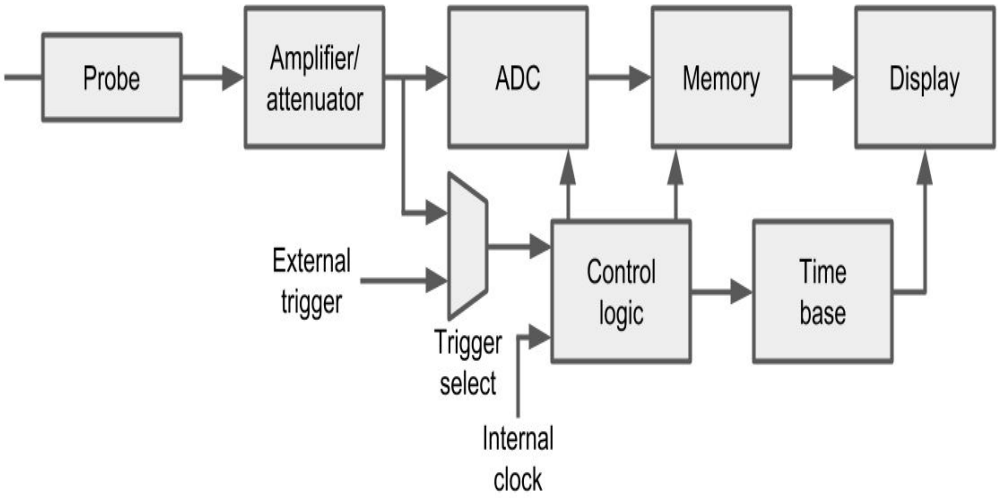


Example of a **logic analyzer** displaying digital signals on **six channels**

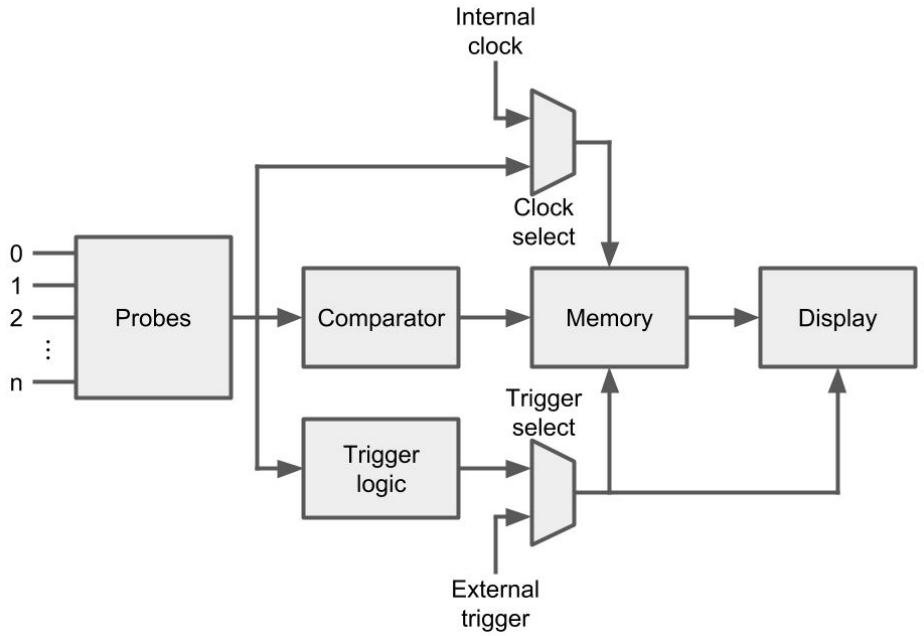
OSCILLOSCOPE	LOGIC ANALYZER
Channels - Few	Channels - Many
Resolution - High	Resolution - Low
Measurement type - Analog	Measurement type - Digital
Store and Display - Repeatedly	Store and Display - Record
Real-time features FFT	Real-time features - Protocol analyzers
Simple threshold - Steady waveform	Complex triggering - capture and filter data

BLOCK DIAGRAM

OSCILLOSCOPE



LOGIC ANALYZER



SAMPLING MODES

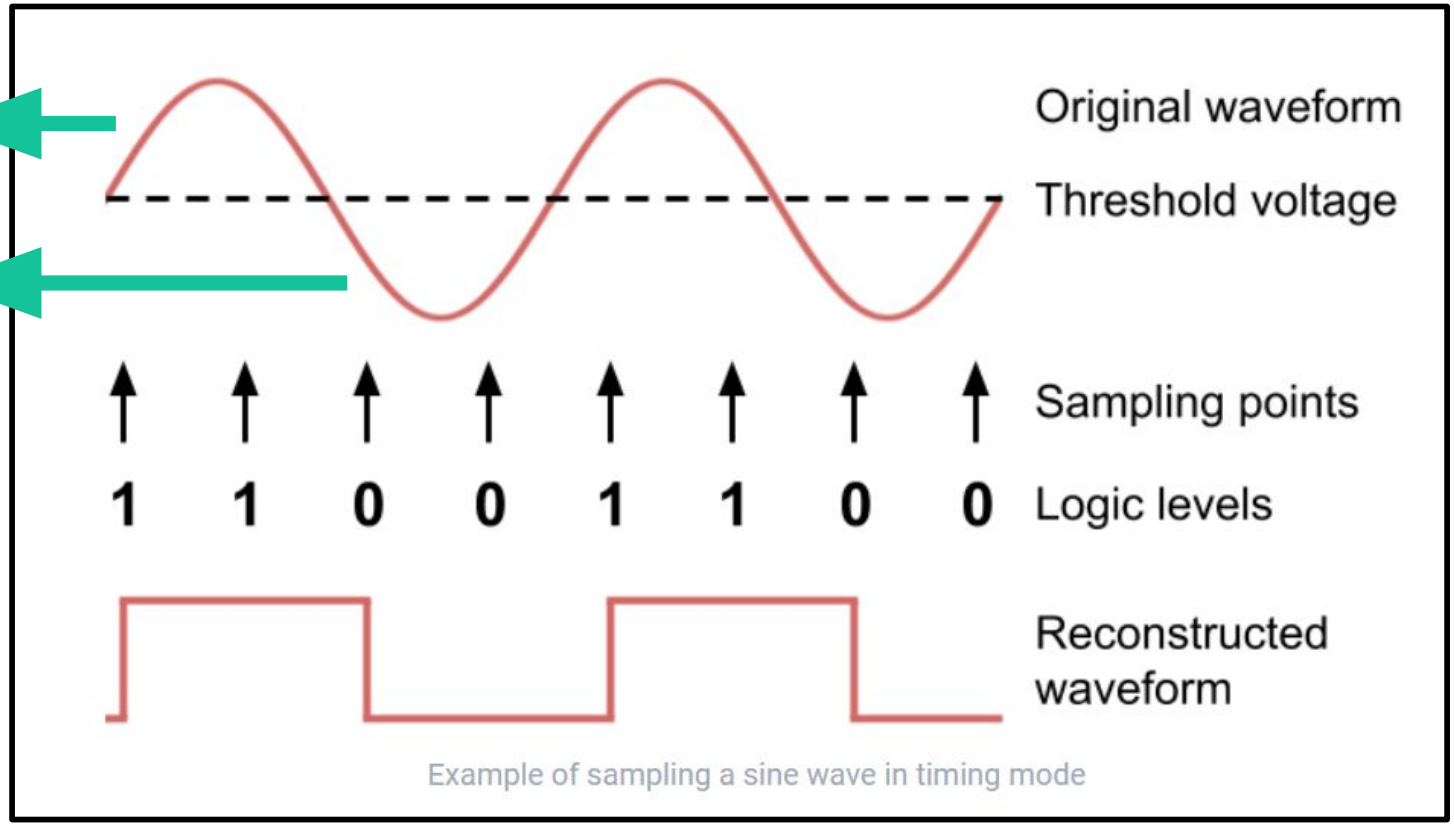
Most logic analyzers have two methods of capturing and displaying data:

- Timing mode
- State mode

TIMING MODE

Higher than the threshold voltage

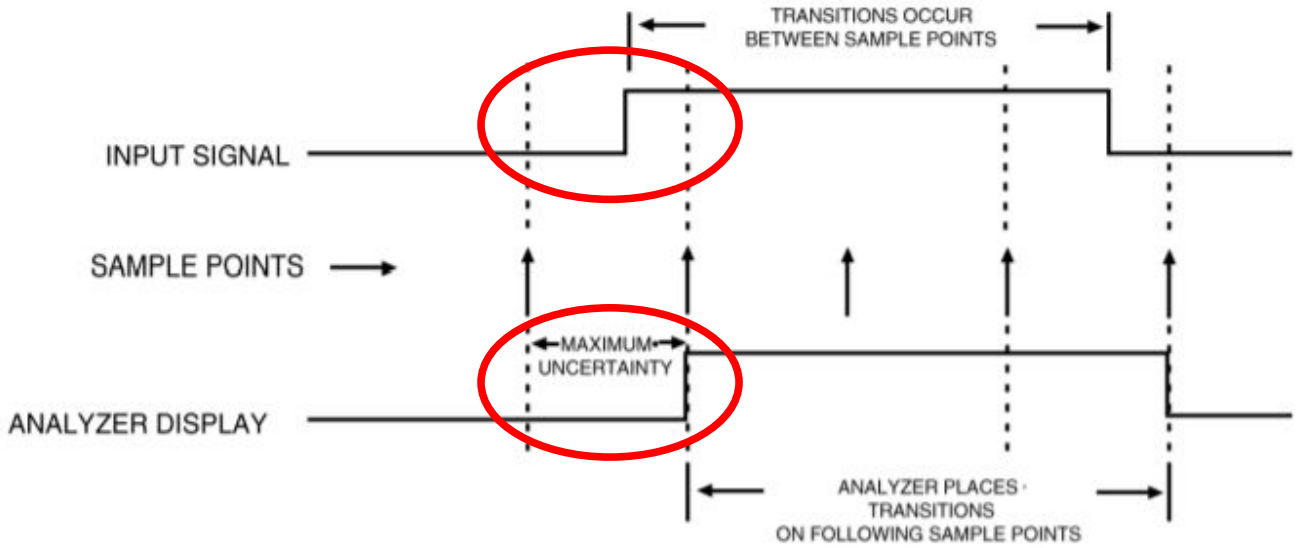
Lower than the threshold voltage



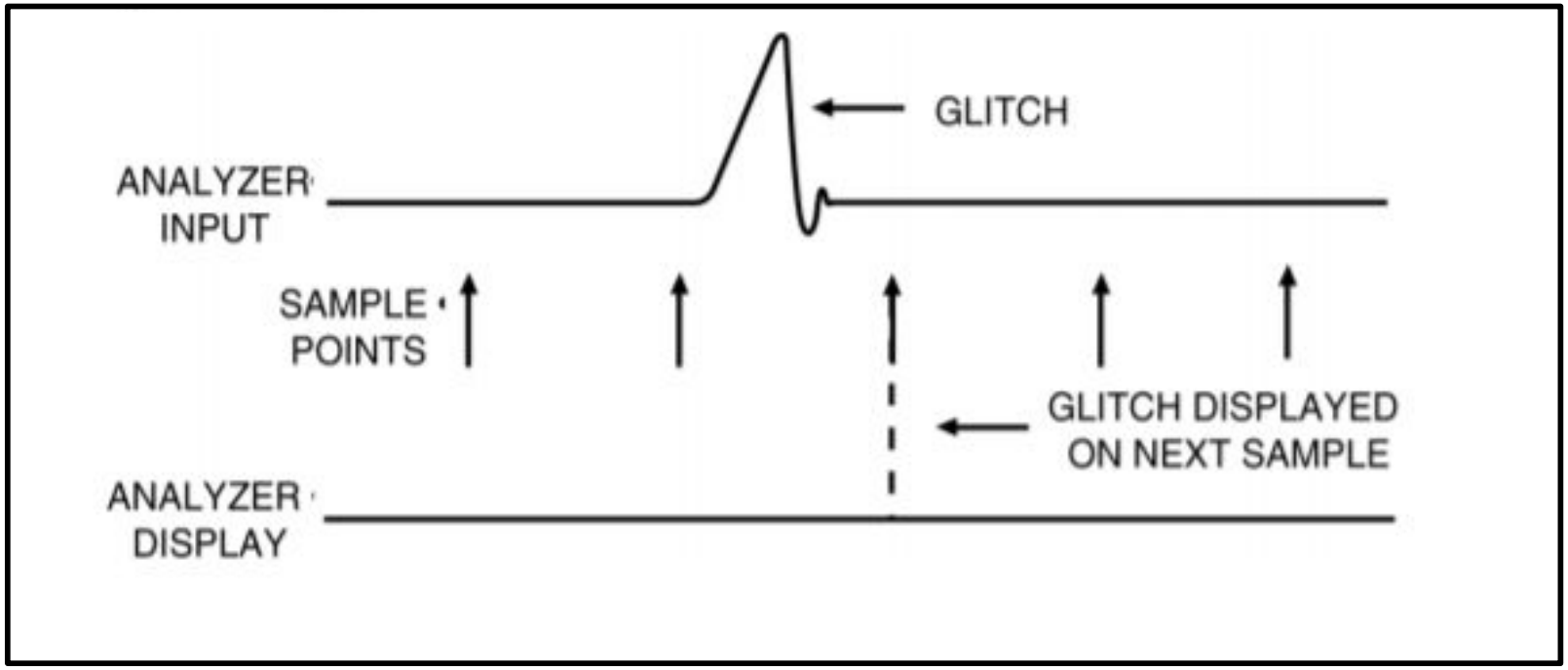
Example of sampling a sine wave in timing mode

AMBIGUITY

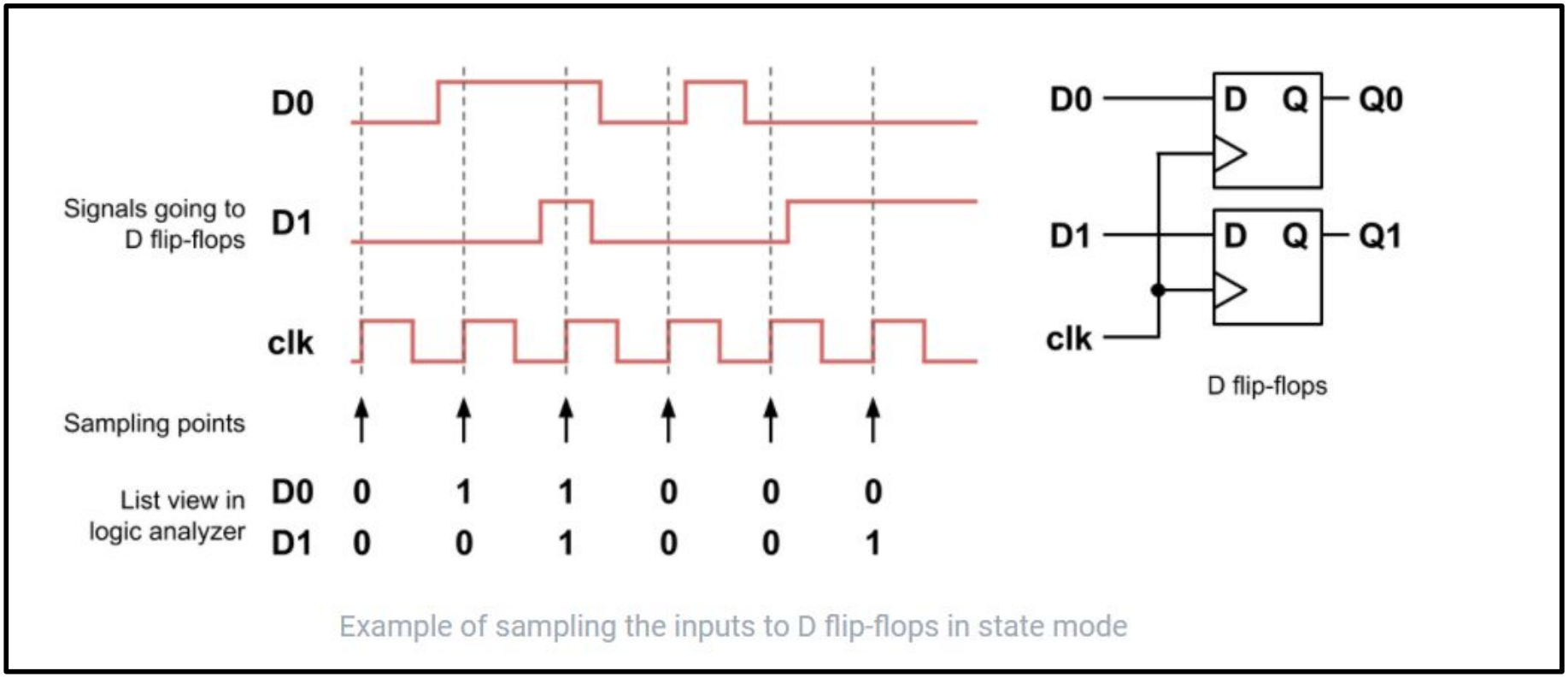
Figure 2.4 Timing analyzer sampling an input line



GLITCH CAPTURE



STATE MODE

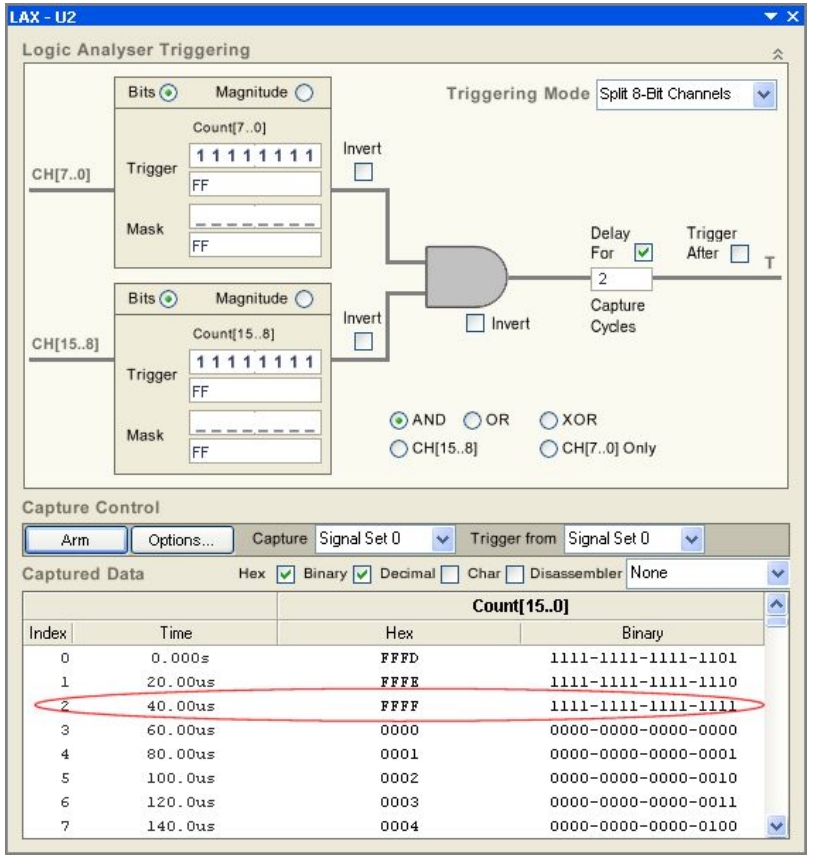


Example of sampling the inputs to D flip-flops in state mode

DIFFERENCES

- The **timing analyzer** has an **internal clock** to control sampling, so it **asynchronously** samples the system under test. A **state analyzer synchronously** samples the system since it gets its sampling clock from the system.
- State analyzer to check "**what**" happened on a bus
- Timing analyzer to see "**when**" it happened.
- State analyzer generally displays data in a **listing** format.
- Timing analyzer displays data as a **waveform** diagram.

TRIGGERS


LAX - U2
Logic Analyser Triggering
Bits
Magnitude
Triggering Mode
Split 8-Bit Channels
Count[7..0]
CH[7..0]
Trigger
11111111
FF
Mask
FF
Invert
Delay For
Trigger After
T
2
Capture Cycles
Invert
Bits
Magnitude
Count[15..8]
CH[15..8]
Trigger
11111111
FF
Mask
FF
Invert
AND
OR
XOR
CH[15..8]
CH[7..0] Only
Capture Control
Arm
Options...
Capture
Signal Set 0
Trigger from
Signal Set 0
Captured Data
Hex
Binary
Decimal
Char
Disassembler
None
Count[15..0]
Index
Time
Hex
Binary
0 0.000s FFFD 1111-1111-1111-1101
1 20.00us FFFE 1111-1111-1111-1110
2 40.00us FFFF 1111-1111-1111-1111
3 60.00us 0000 0000-0000-0000-0000
4 80.00us 0001 0000-0000-0000-0001
5 100.0us 0002 0000-0000-0000-0010
6 120.0us 0003 0000-0000-0000-0011
7 140.0us 0004 0000-0000-0000-0100

TRIGGERS

- Triggers are the basic mechanisms for **selectively controlling which part of the execution history** the logic analyzer reports.
- The trigger system is among the **most complex** hardware circuitry.
- The trigger system also must be able to deal with **various combinations of the address, data, and status information**.

SPECIFYING A TRIGGER

- One of the most difficult tasks for a software developer is to **correctly set up the trigger condition** for a logic analyzer so that the event of interest can be isolated and captured.

- The trigger system also can be used as a **toggle switch**.

- The logic analyzer's trigger system is usually arranged around the concept of **resources and state transitions**.

TRIGGER RESOURCES

- **Think of resources as logic variables. A resource might be assigned to a condition of the system.**
- EXAMPLES :

ADDRESS = 0x5555AAAA.

ADDRESS != 0x5555AAAA

0x50000000 <= ADDRESS <= 0x50000010

(0x50000000 <= ADDRESS <= 0x50000010) !

ADDRESS = 0x500XXXXX

TRIGGER RESOURCES (cntd)

- To create a range resource,

RESOURCE1 (0x50000000 <= ADDRESS) and RESOURCE2 (ADDRESS <= 0x50000010)

- It is possible to assign trigger resources to the **data bus bits and to the status bus bits.**

IF (ADDRESS=0xAAAAAAAA) AND (DATA=0x0034) AND (STATUS=WRITE) THEN TRIGGER

HOW TRIGGERS WORKS

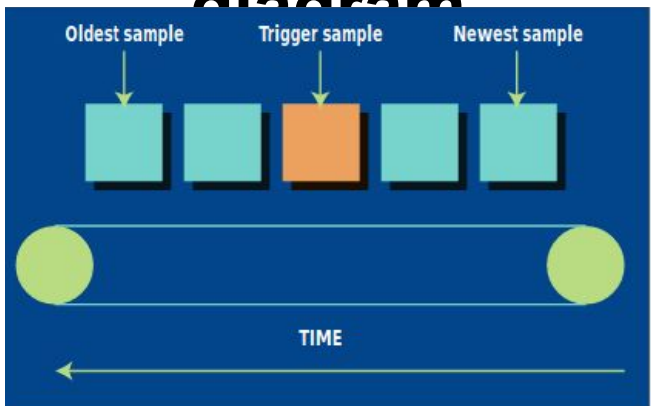
- The logic analyzer is a **passive device.**

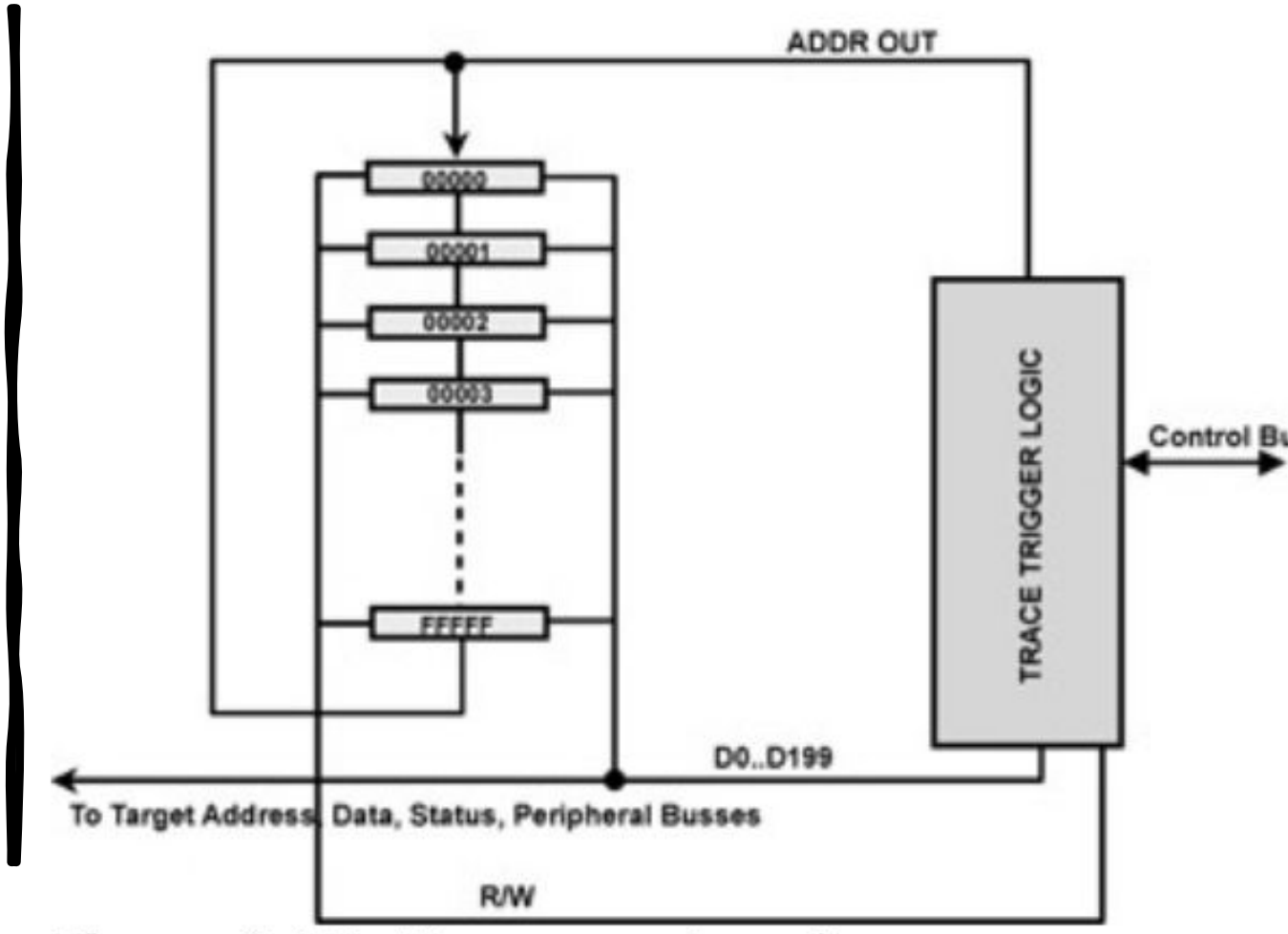
- It **records the signals** that appear on the microprocessor busses while the processor runs normally.

- The trigger capabilities of a logic analyzer can be used to **record the instruction and data flow at some point** in the program execution flow.

Schematic representation of a logic analyzer trace and trigger system

Memory system diagram





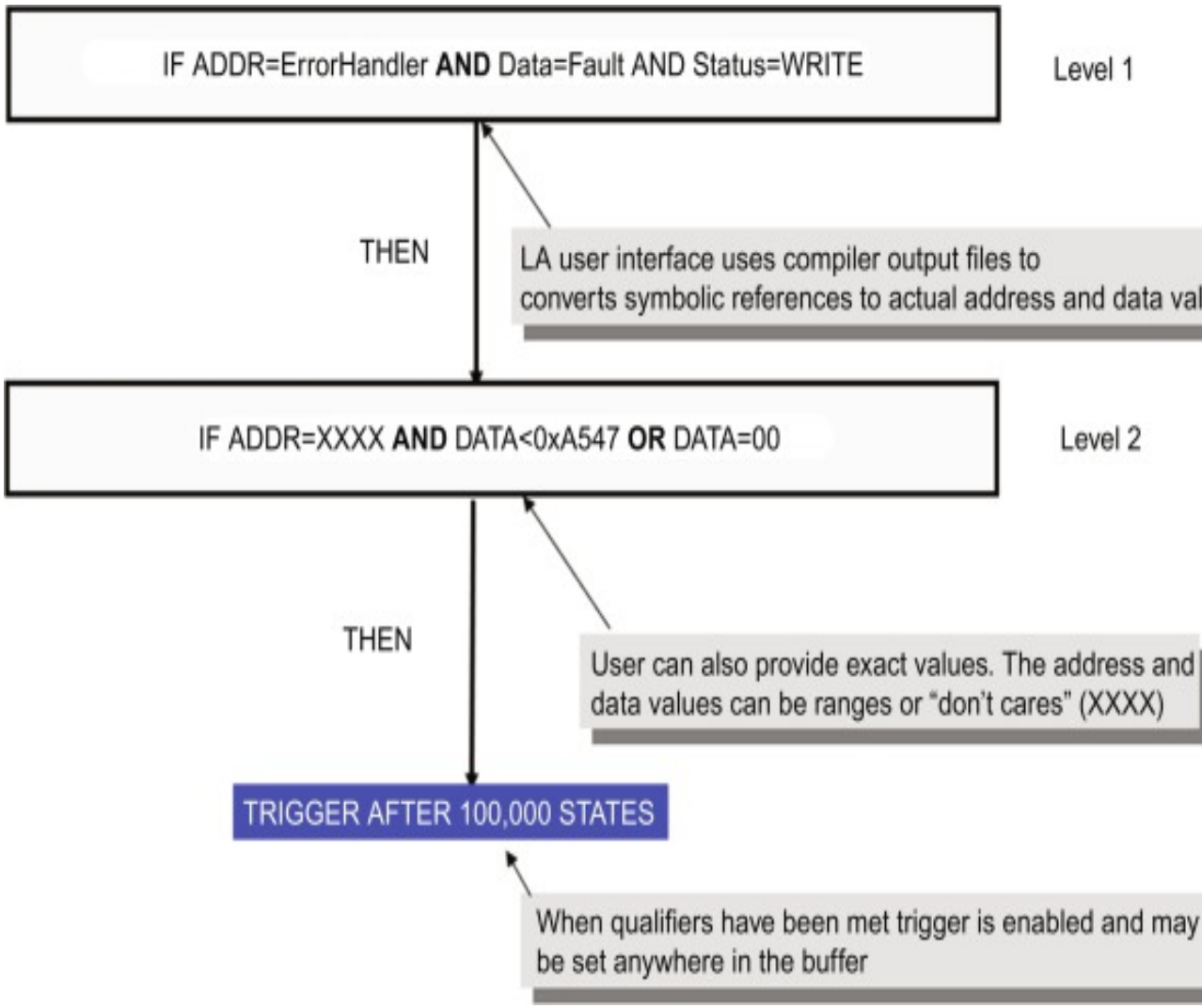
STATE TRANSITIONS

- Sometimes specifying address, data, and status values, even with the capability of defining complicated patterns, is just **not enough**.

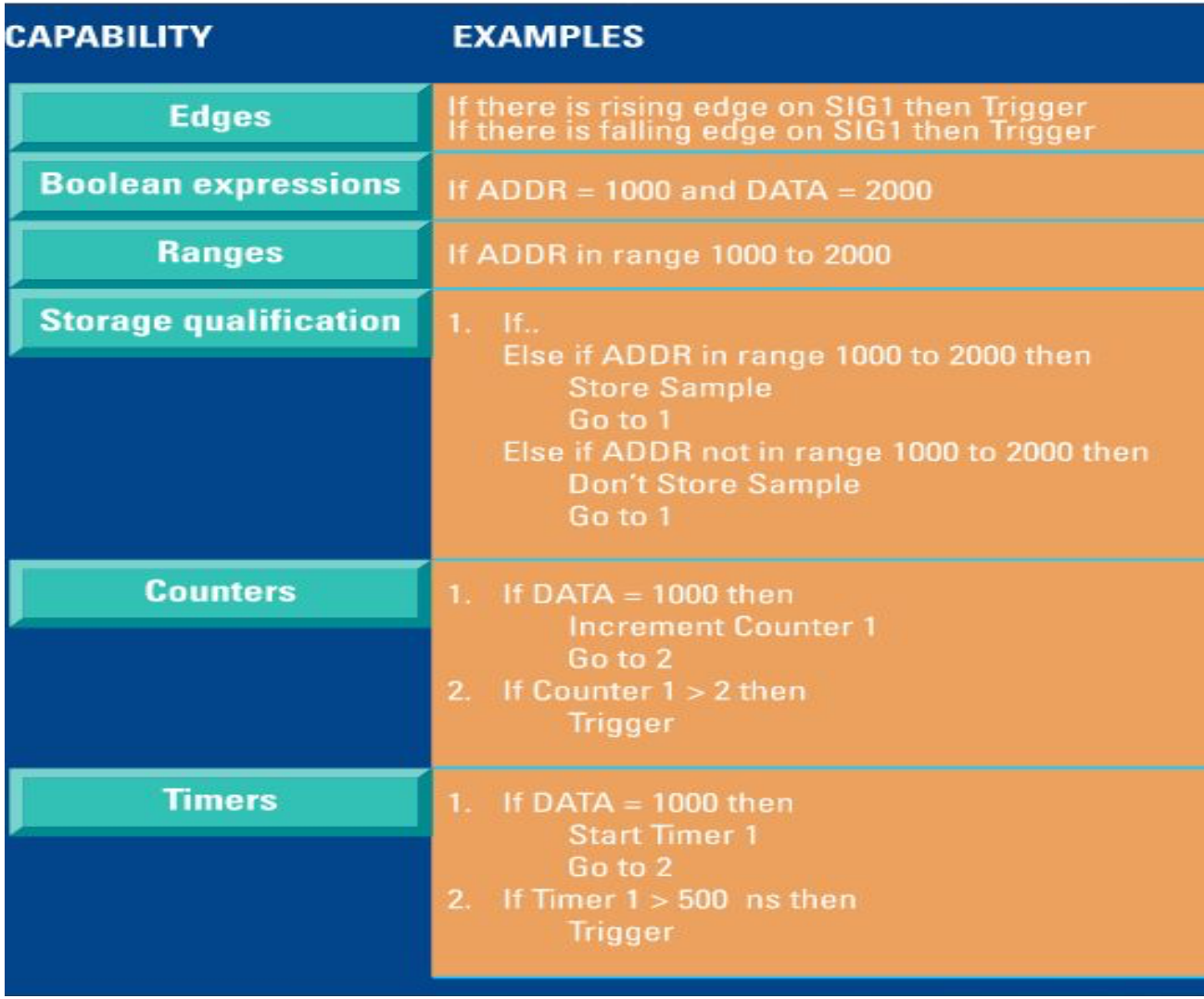
- This is where the **state transition trigger capability** can be used .

- With trigger sequencing, the resources have been combined to provide a **triggering capability that depends on the path taken through the code**.

Triggering a logic analyzer after a sequence of trigger states.



Logic Analyser Triggering Capabilities



CAPABILITY	EXAMPLES
Edges	If there is rising edge on SIG1 then Trigger If there is falling edge on SIG1 then Trigger
Boolean expressions	If ADDR = 1000 and DATA = 2000
Ranges	If ADDR in range 1000 to 2000
Storage qualification	1. If.. Else if ADDR in range 1000 to 2000 then Store Sample Go to 1 Else if ADDR not in range 1000 to 2000 then Don't Store Sample Go to 1
Counters	1. If DATA = 1000 then Increment Counter 1 Go to 2 2. If Counter 1 > 2 then Trigger
Timers	1. If DATA = 1000 then Start Timer 1 Go to 2 2. If Timer 1 > 500 ns then Trigger

APPLICATIONS OF LOGIC ANALYZER

- Logic analyzers are widely used to develop and **debug electronic logic** circuits,
- They display traces of **multiple logic channels** and reveal the circuit operation,
- Logic analyzers are test instruments that are widely used for testing **complex digital or logic circuits**.
- Timing measurements

  Measure the timing of signals to find out conflicts or timing problems
- Assistance on analysis

  It provides **additional analysis to bus signals** or protocol to simplify the development cycle.
- Bug finder

  Logic analyzer can be used for **error tracing** or finding error bugs.

ADVANTAGES OF LOGIC ANALYZER

- It supports measurements of **multiple channels** commonly not supported by oscilloscope. This is very useful in debugging microprocessor or microcontroller based boards. Normally logic analyzer supports **16 or more** channels. Advanced logic analyzers even support **300 channels.**
- High performance
- Lower costs
- Easy to carry
- Convenient to use
- Extendibility

DISADVANTAGES OF LOGIC ANALYZER

- It does not focus on **analog characteristics** of the signal and their specific values.
- Hence it is not suited for such **analog measurements** unlike oscilloscope.
- Logic analyzer is used for **digital** measurements.

REFERENCES

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- https://www.ijert.org/research/logic-analyzer-IJERTV1IS3155.pdf
- **Embedded Systems Design: An Introduction to Processes, Tools, and Techniques by Arnold S. Berger**

THANK YOU !!!