CA Test 1 & 2
2019 Regulations

PSG COLLEGE OF TECHNOLOGY, COIMBATORE - 641 004
Department of Computer Science and Engineering
BE CSE & SEMESTER V
CONTINUOUS ASSESSMENT TEST I Date: 08.08.2024
19Z502 - MICROPROCESSORS AND INTERFACING

Time: 1 Hour 30 minutes. **Maximum Marks: 50**

INSTRUCTIONS:

1. Answer **ALL** questions. Each Question carries 25 Marks.
2. In each question, subdivision **a** carries total of 5 marks (one mark for each question), subdivisions **b(i)** and **b(ii)** carries 5 marks each and subdivision **c** carries 10 marks each.
3. Course Outcome Table:

Qn. 1	CO 1

Qn.2	CO 2

1. **a** **(5 x 1 mark = 5 marks)**

i. In 8086 microprocessor, for a PUSH instruction after each execution of the instruction, the stack pointer is

A) Incremented by 1 B) Decrement by 1
B) Incremented by 2 D) Decremented by 2

ii. Identify the instructions with correct syntax

I MOV DS,1000 immediate addressing wont work
II NEG BL
III CBW BL cbw only for AX/AL
IV SHR BX, CL

A) II and IV only B) II only C) I and II only D) I, II and III only

iii. The size of each segment in 8086 is

A) 64KB B) 24KB C) 128 KB D) 256 KB

wrong question, A is not a decimal, can convert hexadecimal to decimal

iv. Given an number 9AH (in hexadecimal format). Show how it's represented in Unpacked BCD and packed BCD format. Show the output in binary form.

packed -> putting two numbers in 1 byte
unpacked -> putting one number in 1 byte

F) The program that follows implements a delay loop.

```
MOV CX, 0280H
DLY:  DEC CX
      JNZ DLY
NXT: …
```

(280)_16 -> (640)_10
640 - 1 = 639

How many times (in decimal) does the JNZ DLY instruction jumps to DLY label?

(2 x 5 marks = 10 marks)

b.

i. Sketch the software architecture of 8086 processor and explain its register organization.

ii. List the types addressing modes available in 8086. Explain the various memory operand addressing modes of 8086 with appropriate example.

(1 **x 10 marks = 10 marks)**

c. An array of 16-bit numbers is saved in memory location starting from 2000. The size of the array (16-bit number) is stored in location 2500 and 2501. There will be exactly one element repeated in the array. Write an assembly language program to **f**ind the repeated element in the array and save it (16-bit number) in location 2502 and 2503.

For Example:

Input: **Output:**

Memory location	Values (HEX)	Value in Decimal
2000	06	6
2001	00	
2002	00	0
2003	00	
2004	01	257
2005	00	
2006	00	257
2007	01	
Memory location	**Values (HEX)**	**Value in Decimal**
2500	06	4
2501	00	

Memory location	Values (HEX)	Value in Decimal
2502	00	257
2503	01	

2. **a.** **(5 x 1 mark = 5 marks)**

i. Identify the output signal/s of 8086 from the following

A) $M/\overline{IO}$ B) HLDA C) READY D) INTR

ii. Pick the TRUE statement/s from the following.

I. Switching RESET to logic 0 initializes the internal registers of the MPU.

II. LOCK' is an input signal which is used to lock out processor from using the bus.

III. NMI is the interrupt request with highest priority and cannot be masked by software.

A) I only B) II and III only C) I and III only D) I and II only

iii. What does status code S4S3 = 01 mean in terms of memory segment being accessed by microprocessor?

A) Extra Segment B) Code Segment C) Data Segment D) Stack Segment

iv. How many minimum and maximum number of idle states that can be inserted in a 8086 microprocessor ? 0 to infinity

v. What is the duration of the bus cycle in the 8088 microprocessor if the clock is 5 MHz and three wait states are inserted ? 7

b. **(2 x 5 marks = 10 marks)**

i. Compare 8088 and 8086 microprocessor for maximum and minimum mode of operation.

ii. Demonstrate with a diagram on how a misaligned word is transferred from memory to 8086 processor, using the concept of memory bank. Identify all the signals involved in this process ?

2 mem read cycle, 8bit data bus for misaligned rather than 16 bit usual

(1 x 10 marks = 10 marks)

c. Consider a byte 45_{16} is written to memory address $0A00D_{16}$ of an 8086 based microcomputer operating in minimum mode. What type of bus cycle does the processor uses for this interaction? Illustrate that with a timing diagram.

draw timing diagram, show signals, give bin values of address,
show what values are transferred,
what is present in A0 A1 A2 etc pins

Answer key:

1. a. 1. D
1. a. 2. A
1. a. 3. A
1. a. 4. Incorrect Question: BCD is used only for numbers 0 to 9. Unpacked BCD (as 16 bits) and packed BCD (as 8 bits)
1. a. 5. 0280H is 640 in decimal…however, when CX is 0, jump will not be executed, so 639 times

2.a.1. A and B
2.a.2. C (I and III only)
2.a.3. D (Stack Segment)
2.a.4. Idle states can't be inserted in a read/write bus cycle. Only wait states can be inserted. Max. idles states - no limit, as long as READY signal is active low, the idle states are inserted.
2.a.5. 200ns * (4 +3) = 1400ns