CSC 137 Homework #6

6.1 a) Single-cycle data path

0.8ns + 0.8ns + 1.1ns + (0.05 x 3)ns =

2.85ns

max clock frequency $= \frac{1}{2.85ns} = .350877 Hz$

$= 350 MHz$

b) multi-cycle data path

(0.05 + 0.05 + 0.05) + (1.1) + 0.3 + 0.6

$= 2.15ns$

max clock frequency $= \frac{1}{2.15ns} = .465116278 Hz$

$= 465 MHz$

c) pipe-liked data path

(4 x 0.15) + 0.8 + (3 x 0.15) + 0.8 + (2 x 0.15) +

1.1 + 0.15 = 4.2ns

max clock frequency $\frac{1}{4.2ns} = 0.23809523 Hz$

$= 238 MHz$

6.2 A+B = Delay of 1

Path 1 — A+B+C @ combinational logic 2 = Delay of 1

Path 2 — A+B+C±D combinational logic 3 = Delay of 1

A+B+C±D combinational logic 3 to register

= Delay of 1

Total Delay = 4

Total Delay = 13

Speed up $S = \frac{\text{Path 1 time}}{\text{Path 2 time}}$ $\frac{4}{13} = 0.3$

Speed up by 0.3 units

Extra credit -

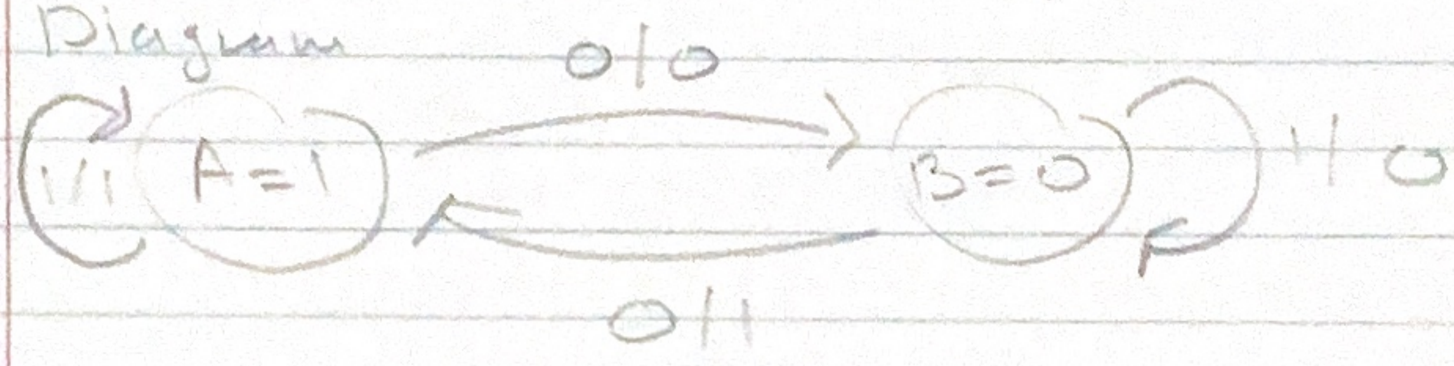
previous o/p	present i/p	present o/p
0	0	1
0	1	0
1	0	0
1	1	1

o/p are only 0/1 so assume A = 1 state
B = 0 state

A frequency o/p = 1
B frequency o/p = 0

x/y = i/p/o/p = present i/p / present o/p

Diagram



State Transition Table

Present State	New State x=0	New State x=1	o/p x=0	o/p x=1
A	B	A	0	1
B	A	B	1	0

PS	IP	NS	Or	Y
1	1	1	1	1
1	0	0	0	0
0	1	0	0	0
0	0	1	1	1

o/p = EX NOR Gate