We take the following as given: the input voltage V_{in}; the circuit constants V_{CC}, R_1 and R_2; and the BJT parameters β, $V_{BE,\text{on}}$ and $V_{CE,\text{sat}}$. We now show how equations (1) to (7) define three operating modes for the BJT, called OFF, ACTIVE and SATURATED, and derive expressions for V_{BE}, I_B, I_C and V_{CE} in each mode.

Conditions	Mode	Behavior: Derivation and Reasons
$V_{\text{in}} < V_{BE,\text{on}}$	OFF	$V_{BE} = V_{\text{in}}$ from BJT input model (3) $I_B = 0$ from BJT input model (3) $I_C = 0$ from BJT output model (5) $V_{CE} = V_{CC}$ from output loop KVL (2)
$V_{\text{in}} > V_{BE,\text{on}}$ $V_{CE} > V_{CE,\text{sat}}$	ACTIVE	$V_{BE} = V_{BE,\text{on}}$ from BJT input model (4) $I_B = \frac{V_{\text{in}} - V_{BE,\text{on}}}{R_1}$ from input loop KVL (1) $I_C = \beta I_B$ from BJT output model (6) $V_{CE} = V_{CC} - I_C R_2$ from output loop KVL (2)
$V_{\text{in}} > V_{BE,\text{on}}$ $V_{CE} \not> V_{CE,\text{sat}}$	SATURATED	$V_{CE} = V_{CE,\text{sat}}$ from BJT output model (7) $I_C = \frac{V_{CC} - V_{CE,\text{sat}}}{R_2} \equiv I_{C,\text{sat}}$ from output loop KVL (2) $V_{BE} = V_{BE,\text{on}}$ from BJT input model (4) $I_B = \frac{V_{\text{in}} - V_{BE,\text{on}}}{R_1}$ from input loop KVL (1)

Table 1: BJT operating modes.

Note that $I_{C,\text{sat}}$, which is called the saturation current, is the maximum value of I_C among all the modes. In contrast, $V_{CE,\text{sat}}$ is the minimum value of V_{CE}. After some practice, you are expected to recall and evaluate th derivation for each mode by looking at a circuit diagram like Fig. 1 or Fig. 3.

Load Line Method

Analyze a circuit graphically by plotting the I-V characteristics of both subcircuits together.

The I-V characteristic of the load subcircuit represents all the (V,I) values at which it can operate. Likewise, the source subcircuit's I-V characteristic represents all of its possible (V,I) values. Therefore, when you plot both I-V characteristics together on the same I-V plane, their point of intersection is the (V,I) value at which both subcircuits operate together. For this reason, the intersection is called the operating point.

We can use this insight to analyze a circuit graphically. Finding the operating point in this way is called the load line method. (Confusingly, the source I-V characteristic is known as the load line because it intersects the load I-V characteristic.) Table 5 below shows two examples for the test circuit in Fig. 1 with different load subcircuits, a resistor and current source, respectively.

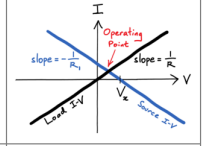
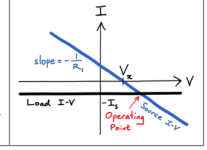
Circuit	Schematic	Load Line Method Plot
Fig. 1 with Resistor as Load Subcircuit		
Fig. 1 with Current Source as Load Subcircuit		

Table 5: Load line method examples.

Notice that, when the load subcircuit is a resistor, the operating point is in the upper-right quadrant, so the source subcircuit is delivering power ($P < 0$) and the load subcircuit is absorbing power ($P > 0$). But when the load subcircuit is a current source, the operating point is in the lower-right quadrant, so the source subcircuit is absorbing power ($P > 0$) and the load subcircuit is delivering power ($P < 0$).

Conditions	Mode	Behavior under Linear Model
$V_{GS} < V_{TH}$	OFF	$I_D = 0$
$V_{GS} > V_{TH}$ $V_{DS} > V_{GS} - V_{TH}$	ACTIVE	$I_D = k(V_{GS} - V_{TH})^2$
$V_{GS} > V_{TH}$ $V_{DS} < V_{GS} - V_{TH}$	OHMIC	$I_D = k(V_{GS} - V_{TH})V_{DS}$

Table 1 : NMOS transistor operating modes.

Figure 7

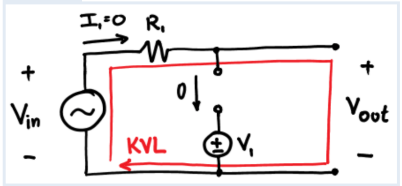


Fig. 7: Diode c

When $V_{\text{in}} < V_1 + V_{\text{on}}$ in Fig. 1, the diode is OFF and is replaced by an open circuit in this figure. Now, we apply KVL to obtain: $V_{\text{in}} = I_1 R_1 + V_{\text{out}}$. Note that $I_1 = 0$ since R_1 is not part of a complete circuit. Therefore, $V_{\text{out}} = V_{\text{in}}$.

Figure 8

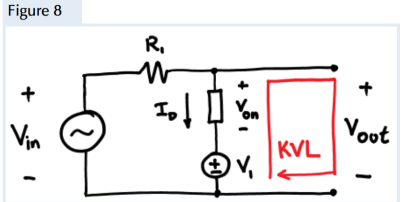


Fig. 8: Diode clipper with the diode ON.

When $V_{\text{in}} > V_1 + V_{\text{on}}$ in Fig. 1, the diode is ON and is replaced by an element with voltage drop V_{on} in this figure. Now, we apply KVL to obtain: $V_1 + V_{\text{on}} = V_{\text{out}}$. Therefore, $V_{\text{out}} = V_1 + V_{\text{on}}$.

Combining the results from Fig. 7 and Fig. 8 gives

$$V_{\text{out}} = \begin{cases} V_{\text{in}}, & \text{if } V_{\text{in}} < V_1 + V_{\text{on}}, \\ V_1 + V_{\text{on}}, & \text{if } V_{\text{in}} > V_1 + V_{\text{on}}. \end{cases} \tag{2}$$

Power on the I-V Plane

Power is absorbed in two quadrants of the I-V plane and delivered in the other two.

We extend the formula for power to the case of nonstandard labeling by reversing its sign to account for switching the relative orientation of the voltage polarity and current arrow labels.

$$P = \begin{cases} VI, & \text{under standard labeling,} \\ -VI, & \text{under nonstandard labeling.} \end{cases} \tag{1}$$

The I-V plane spans the axes on which an I-V characteristic is plotted. In Table 4 below, we use equation (1) to identify the sign of P in each quadrant under both standard and nonstandard labeling. We determine whether power is being delivered or absorbed in each quadrant, depending on whether it is a load or source subcircuit.

Labeling	Subcircuit Type	Sign of P by I-V Plane Quadrant
Standard Labeling	Load Subcircuit	$P = VI$ (+) ABSORBING; $P = VI$ (−) DELIVERING; $P = VI$ (+) ABSORBING; $P = VI$ (−) DELIVERING
	Source Subcircuit	$P = -VI$ (−) DELIVERING; $P = -VI$ (+) ABSORBING; $P = -VI$ (−) DELIVERING; $P = -VI$ (+) ABSORBING
Nonstandard Labeling	Load Subcircuit	$P = VI$ (−) DELIVERING; $P = VI$ (+) ABSORBING; $P = VI$ (−) DELIVERING; $P = VI$ (+) ABSORBING
	Source Subcircuit	$P = -VI$ (+) ABSORBING; $P = -VI$ (−) DELIVERING; $P = -VI$ (+) ABSORBING; $P = -VI$ (−) DELIVERING

Table 4: Signs of P on the I-V plane.

$$G = \frac{V_{CE,\text{sat}} - V_{CC}}{V_{\text{in}}^* - V_{BE,\text{on}}} \tag{1}$$

The constant output voltages V_{CC} in OFF mode and $V_{CE,\text{sat}}$ in SATURATED mode are explained by the behavior of V_{CE} in those modes. The transition input voltage $V_{BE,\text{on}}$ between OFF and ACTIVE is the boundary between the conditions on V_{in} in those modes.

At the transition input voltage between ACTIVE and SATURATED, the BJT obeys the behavior of both of these modes. In particular, we follow these steps to derive V_{in}^*:

$$I_C = I_{C,\text{sat}} = \frac{V_{CC} - V_{CE,\text{sat}}}{R_2} \quad \text{SATURATED mode } I_C \text{ formula}$$

$$I_B = \frac{I_C}{\beta} \quad \text{from ACTIVE mode } I_C \text{ formula}$$

$$V_{\text{in}}^* = V_{\text{in}} = V_{BE,\text{on}} + I_B R_1 \quad \text{from ACTIVE mode } I_B \text{ formula}$$

The overall expression is:

$$V_{\text{in}}^* = V_{BE,\text{on}} + \frac{R_1}{\beta R_2}(V_{CC} - V_{CE,\text{sat}}), \tag{2}$$

where V_{CC}, R_1 and R_2 are known circuit constants and β, $V_{BE,\text{on}}$ and $V_{CE,\text{sat}}$ are known BJT parameters. Substituting equation (2) into equation (1), gives another formula for the gain of the common emitter amplifier:

$$G = -\frac{\beta R_2}{R_1} \tag{3}$$

Figure 1

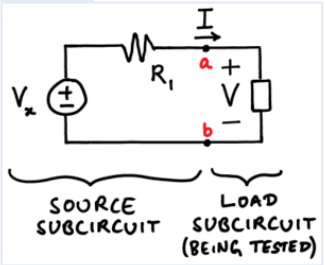
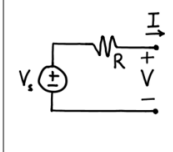
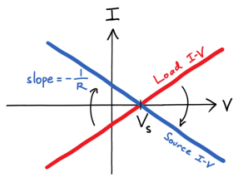
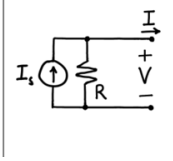
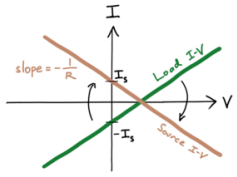


Fig. 1: Test circuit. The voltage source V_x and the resistor $R1$ form the fixed part of the test circuit and we say they comprise the source subcircuit. The element being tested is interchangeable and we say it forms the load subcircuit. Typically, the source subcircuit delivers electrical energy to the load subcircuit, but this is not always the case. V is the voltage drop from terminal a to terminal b and I is the current from a to b through the load subcircuit.

Source I-V Characteristics

A source I-V characteristic has an equal but opposite slope compared to the equivalent load I-V characteristic.

If a combination of elements is in the source subcircuit instead of the load subcircuit, then V and I are in nonstandard labeling. This difference occurs because the current arrow label of I points out of the top terminal of the source subcircuit but into the top terminal of the load subcircuit. Therefore, the source I-V characteristic is a vertically flipped copy of the equivalent load I-V characteristic.

Subcircuit	Schematic	I-V Characteristic	Explanation
Voltage Source and Resistor in Series (Source)			The source I-V characteristic is a line with slope $-1/R$ and V-intercept of V_s. It is flipped vertically compared to the equivalent load I-V characteristic.
Current Source and Resistor in Parallel (Source)			The source I-V characteristic is a line with slope $-1/R$ and I-intercept of I_s. It is flipped vertically compared to the equivalent load I-V characteristic.

ıts in source subcircuit.

Figure 7

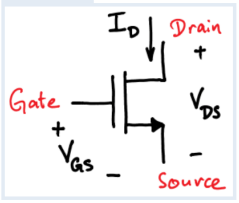


Fig. 7: The circuit symbol for an NMOS transistor. The input voltage V_{GS} drops from gate to source. (Note that $V_{GS} = V_G$ in Fig. 3 and Fig. 4 since the body and source terminals are grounded in those diagrams.) On the output side, I_D flows into the drain and V_{DS} drops from drain to source. Notice that the NMOS transistor symbol incorporates the symbol for a capacitor to signify the gate's capacitative properties.

If the input V_{GS} is fixed, an output I-V characteristic can be traced relating I_D to V_{DS}. Varying V_{GS} therefore produces a family of curves. We model the operation of an NMOS transistor by dividing the I-V space into 3 modes, OFF, ACTIVE and OHMIC, and fitting linear equations to each I-V curve in each mode.

Figure 9

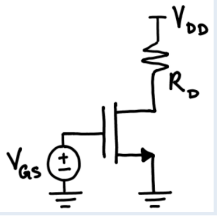


Fig. 9: NMOS transistor connected a Thévenin subcircuit. You can apply the load line method to analyze an NMOS transistor connected to a Thévenin subcircuit, consisting of V_{DD} and R_D. Intersect the NMOS output I-V characteristic in Fig. 8 with the Thévenin subcircuit's I-V characteristic to find the operating point (V_{DS}, I_D) and the mode which it represents.

Figure 6

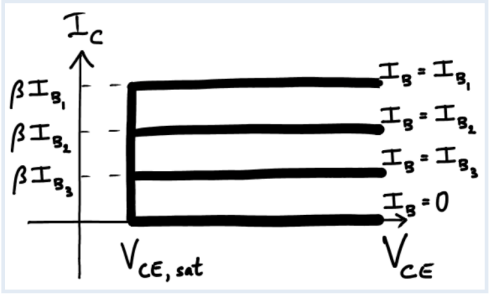
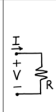
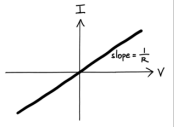
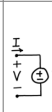
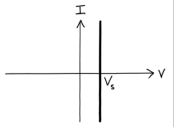
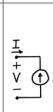
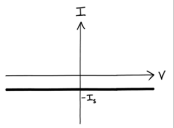
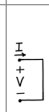
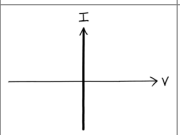
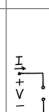
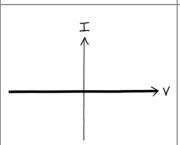


Fig. 6: Model for output I-V characteristic. In this model, all the I-V curves start from $I_C = 0$ and $V_{CE} = V_{CE,\text{sat}}$, called the saturation voltage. If $I_B = 0$, the curve is $I_C = 0$ for all $V_{CE} \geq V_{CE,\text{sat}}$. If $I_B > 0$, then $I_C = \beta I_B$ for all $V_{CE} > V_{CE,\text{sat}}$. The typical value of $V_{CE,\text{sat}}$ for a silicon BJT is 0.2 V.

From this model, we draw the following conclusions about the output loop of a common emitter circuit:

$$\text{If } I_B = 0, \text{ then } I_C = 0. \quad (5$$
$$\text{If } I_B > 0 \text{ and } V_{CE} > V_{CE,\text{sat}}, \text{ then } I_C = \beta I_B. \quad (6$$
$$\text{Otherwise, } V_{CE} = V_{CE,\text{sat}}. \quad (7$$

Element	Schematic	I-V Characteristic	Explanation
Resistor			A resistor R satisfies Ohm's law $I = V/R$, so its I-V characteristic goes through the origin and has slope $1/R$.
Voltage Source			A voltage sour maintains a fix drop and can current, so its characteristic line at $V = V_s$.
Current Source			A current sour maintains a fix and can allow voltage drop, characteristic horizontal line Note that there negative sign current arrow and I_s are in directions.
Short Circuit			A short circuit connection be terminals. The circuit maintai voltage drop a allow any curr V characteristi vertical line at Notice that a s behaves identi zero voltage s $V_s = 0$ V.
Open Circuit			An open circu absence of a c between two t The open circu maintains zerc and can allow voltage drop, characteristic horizontal line Notice that an circuit behave identically to current source with $I_s = 0$ A.

Load I-V Characteristics

A load subcircuit consisting of sources and resistors has a linear I-V characteristic.

The load subcircuit may consist of more than one element in series and/or parallel combinations. The load I-V characteristic can be obtained from the elements' I-V characteristics using KVL and KCL. In fact, if the load subcircuit consists of sources and resistors only, the load I-V characteristic must be linear, as illustrated by the examples below.

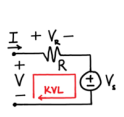
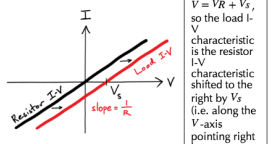
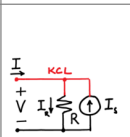
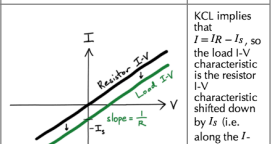
Subcircuit	Schematic	I-V Characteristic	Explanation
Voltage Source and Resistor in Series (Load)			KVL implies that $V = VR + V_s$, so the load I-V characteristic is the resistor I-V characteristic shifted to the right by V_s (i.e. along the V-axis pointing right by an amount $+V_s$).
Current Source and Resistor in Parallel (Load)			KCL implies that $I = IR - I_s$, so the load I-V characteristic is the resistor I-V characteristic shifted down by I_s (i.e. along the I-axis pointing up by an amount $-I_s$).

Table 2: I-V characteristics of combinations of circuit elements in load subcircuit.

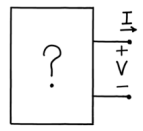
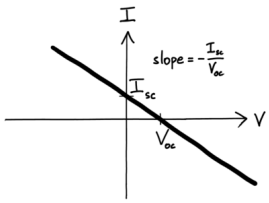
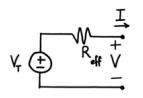
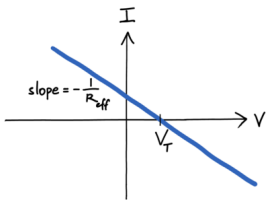
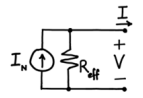
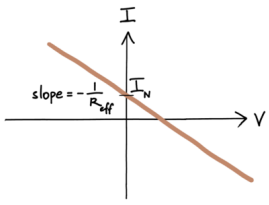
Subcircuit	Schematic	I-V Characteristic	Explanation
Unknown subcircuit			Any subcircuit containing exclusively sources and resistors has a linear I-V characteristic. This line has V-intercept equal to V_{oc} since $I_{oc} = 0$, and it has I-intercept equal to I_{sc} since $V_{sc} = 0$. Therefore, the slope is $-I_{sc}/V_{oc}$.
Thévenin subcircuit			This line is the I-V characteristic of a voltage source and resistor in series.
Norton subcircuit			This line is the I-V characteristic of a current source and resistor in parallel.

Figure 5

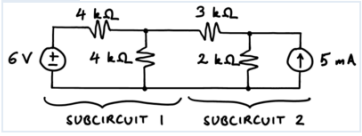


Fig. 5: Circuit consisting of two subcircuits. Either of the known subcircuits can be replaced by a simpler Thévenin or Norton equivalent without changing the behavior of the other known subcircuit.

The table below gives example procedures for determining the Thévenin and Norton equivalents of the two subcircuits in Fig. 5.

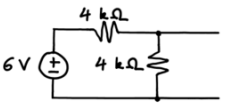
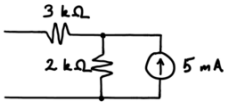
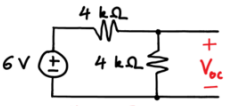
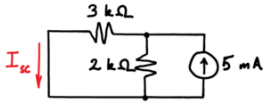
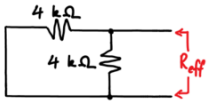
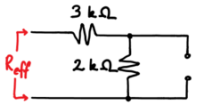
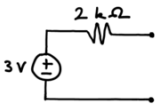
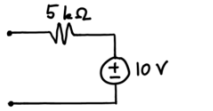
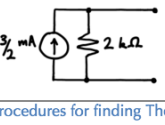
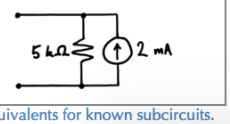
Step	Subcircuit 1	Subcircuit 2
Draw known subcircuit		
Find one of the values VT, IN or $Reff$	 VOLTAGE DIVIDER $V_{Th} = V_{oc} = 3$V	 CURRENT DIVIDER $I_N = I_{sc} = 2$ mA
Find another value out of VT, IN or $Reff$	 RESISTORS IN PARALLEL $R_{eff} = 4\text{k}\Omega \| 4\text{k}\Omega = 2\text{k}\Omega$	 RESISTORS IN SERIES $R_{eff} = 3\text{ k}\Omega + 2\text{k}\Omega = 5\text{ k}\Omega$
Find the remaining value VT, IN or $Reff$	$IN = \frac{V_T}{R_{eff}} = \frac{3\text{ V}}{2\text{ k}\Omega} = \frac{3}{2}$ mA	$VT = IN\text{Reff} = (2\text{ mA})(5\text{ k}\Omega) = 10$ V
Draw Thévenin equivalent		
Draw Norton equivalent		

Table 3: Example procedures for finding Thévenin and Norton equivalents for known subcircuits.