Offset Ideal Model

Diode circuits can often be analyzed using linear models.

The offset ideal model approximates the nonlinear I-V characteristic in Fig. 3 as a piecewise linear graph with a threshold voltage parameter V_{on}. The typical value for a silicon diode is $V_{on} = 0.7$ V.

Figure 4

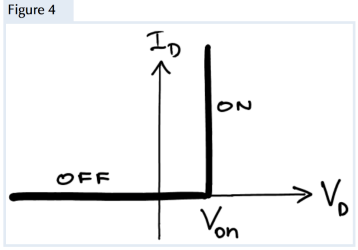


Fig. 4: Offset ideal model I-V characteristic of a diode. If $V_D < V_{on}$, we approximate $I_D = 0$. Otherwise, if $I_D > 0$, we approximate $V_D = V_{on}$. These two regions define two diode states, called OFF and ON.

Within each diode state, the diode can be replaced with a simpler linear element. If the diode is OFF, it can be replaced by an open circuit which has $I_D = 0$ and can have any value of V_D. Otherwise, the diode is ON and it can be replaced by an element with fixed voltage drop $V_D = V_{on}$ and any value of I_D.

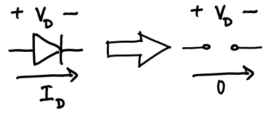
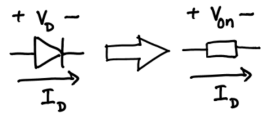
Condition	State	Behavior	Replacement Rule
$V_D < V_{on}$	OFF	$I_D = 0$	
$I_D > 0$	ON	$V_D = V_{on}$	

Table 1: Diode states and replacement rules.

Figure 7

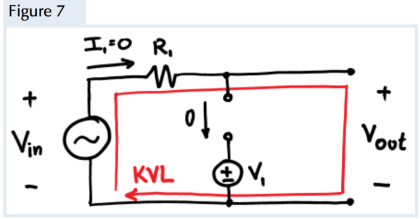


Fig. 7: Diode clipper with the diode OFF. When $V_{in} < V_1 + V_{on}$ in Fig. 1, the diode is OFF and is replaced by an open circuit in this figure. Now, we apply KVL to obtain: $V_{in} = I_1 R_1 + V_{out}$. Note that $I_1 = 0$ since R_1 is not part of a complete circuit. Therefore, $V_{out} = V_{in}$.

Figure 8

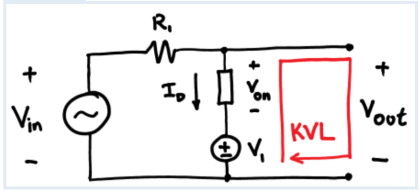


Fig. 8: Diode clipper with the diode ON. When $V_{in} > V_1 + V_{on}$ in Fig. 1, the diode is ON and is replaced by an element with voltage drop V_{on} in this figure. Now, we apply KVL to obtain: $V_1 + V_{on} = V_{out}$. Therefore, $V_{out} = V_1 + V_{on}$.

Combining the results from Fig. 7 and Fig. 8 gives

$$V_{out} = \begin{cases} V_{in}, & \text{if } V_{in} < V_1 + V_{on}, \\ V_1 + V_{on}, & \text{if } V_{in} > V_1 + V_{on}. \end{cases} \tag{2}$$

Figure 4

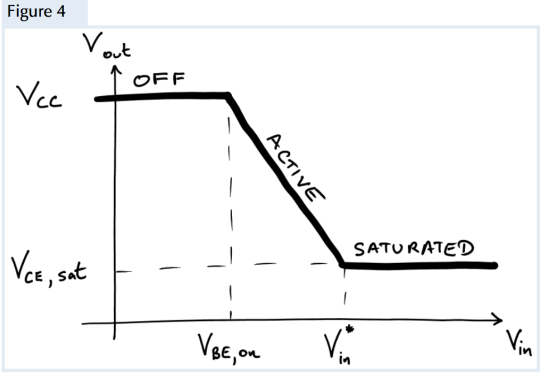


Fig. 4: Amplifier input-output characteristic. V_{out} is constant at V_{CC} in the OFF mode, linearly decreasing in the ACTIVE mode and constant at $V_{CE,sat}$ in the SATURATED mode. The transition from OFF to ACTIVE happens at $V_{in} = V_{BE,on}$ and the transition from ACTIVE to SATURATED happens at $V_{in} = V_{in}^*$, derived as (2) below.

The fact that a diode allows current to flow in only one direction means that it can rectify a sinusoidal voltage waveform by blocking its negative part.

Figure 2

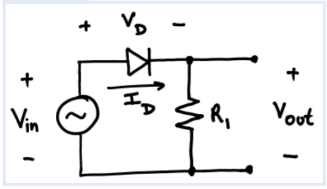


Fig. 2: Half-wave rectifier. A half-wave rectifier circuit consists of a diode in series with a resistor. The input voltage V_{in} is applied across the diode and the resistor. The output voltage V_{out} is taken across the resistor.

Figure 4

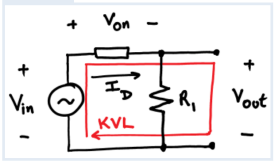


Fig. 4: Half-wave rectifier with the diode ON. When $V_{in} > V_{on}$ in Fig. 1, the diode is ON and is replaced by an element with voltage drop V_{on} in this figure. Now, we apply KVL to obtain: $V_{in} = V_{on} + V_{out}$. Therefore, $V_{out} = V_{in} - V_{on}$.

Combining the results from Fig. 3 and Fig. 4 gives

$$V_{out} = \begin{cases} 0, & \text{if } V_{in} < V_{on}, \\ V_{in} - V_{on}, & \text{if } V_{in} > V_{on}. \end{cases} \tag{1}$$

We take the following as given: the input voltage V_{in}; the circuit constants V_{CC}, R_1 and R_2; and the BJT parameters β, $V_{BE,on}$ and $V_{CE,sat}$. We now show how equations (1) to (7) define three operating modes for the BJT, called OFF, ACTIVE and SATURATED, and derive expressions for V_{BE}, I_B, I_C and V_{CE} in each mode.

Conditions	Mode	Behavior: Derivation and Reasons
$V_{in} < V_{BE,on}$	OFF	$V_{BE} = V_{in}$ from BJT input model (3) $I_B = 0$ from BJT input model (3) $I_C = 0$ from BJT output model (5) $V_{CE} = V_{CC}$ from output loop KVL (2)
$V_{in} > V_{BE,on}$ $V_{CE} > V_{CE,sat}$	ACTIVE	$V_{BE} = V_{BE,on}$ from BJT input model (4) $I_B = \dfrac{V_{in} - V_{BE,on}}{R_1}$ from input loop KVL (1) $I_C = \beta I_B$ from BJT output model (6) $V_{CE} = V_{CC} - I_C R_2$ from output loop KVL (2)
$V_{in} > V_{BE,on}$ $V_{CE} \not> V_{CE,sat}$	SATURATED	$V_{CE} = V_{CE,sat}$ from BJT output model (7) $I_C = \dfrac{V_{CC} - V_{CE,sat}}{R_2} \equiv I_{C,sat}$ from output loop KVL (2) $V_{BE} = V_{BE,on}$ from BJT input model (4) $I_B = \dfrac{V_{in} - V_{BE,on}}{R_1}$ from input loop KVL (1)

Table 1: BJT operating modes.

Note that $I_{C,sat}$, which is called the saturation current, is the maximum value of I_C among all the modes. In contrast, $V_{CE,sat}$ is the minimum value of V_{CE}. After some practice, you are expected to recall and evaluate the derivation for each mode by looking at a circuit diagram like Fig. 1 or Fig. 3.

$$G = \frac{V_{CE,sat} - V_{CC}}{V_{in}^* - V_{BE,on}} \tag{1}$$

The constant output voltages V_{CC} in OFF mode and $V_{CE,sat}$ in SATURATED mode are explained by the behavior of V_{CE} in those modes. The transition input voltage $V_{BE,on}$ between OFF and ACTIVE is the boundary between the conditions on V_{in} in those modes.

At the transition input voltage between ACTIVE and SATURATED, the BJT obeys the behavior of both of these modes. In particular, we follow these steps to derive V_{in}^*:

$$I_C = I_{C,sat} = \frac{V_{CC} - V_{CE,sat}}{R_2} \quad \text{SATURATED mode } I_C \text{ formula}$$

$$I_B = \frac{I_C}{\beta} \quad \text{from ACTIVE mode } I_C \text{ formula}$$

$$V_{in}^* = V_{in} = V_{BE,on} + I_B R_1 \quad \text{from ACTIVE mode } I_B \text{ formula}$$

The overall expression is:

$$V_{in}^* = V_{BE,on} + \frac{R_1}{\beta R_2}(V_{CC} - V_{CE,sat}), \tag{2}$$

where V_{CC}, R_1 and R_2 are known circuit constants and β, $V_{BE,on}$ and $V_{CE,sat}$ are known BJT parameters. Substituting equation (2) into equation (1), gives another formula for the gain of the common emitter amplifier:

$$G = -\frac{\beta R_2}{R_1} \tag{3}$$

Figure 5

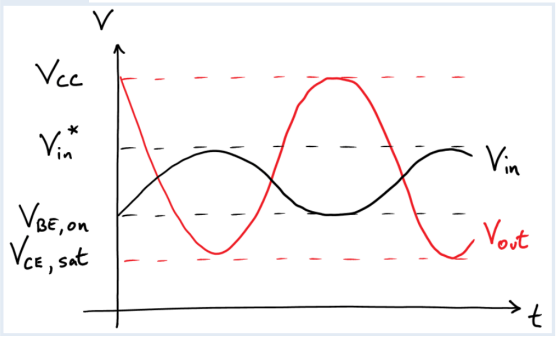


Fig. 5: Voltage signal amplification. If V_{in} is a signal between $V_{BE,\text{on}}$ and V_{in}^*, then V_{out} is an amplified and inverted copy that exists between V_{CC} and $V_{CE,\text{sat}}$.

Figure 6

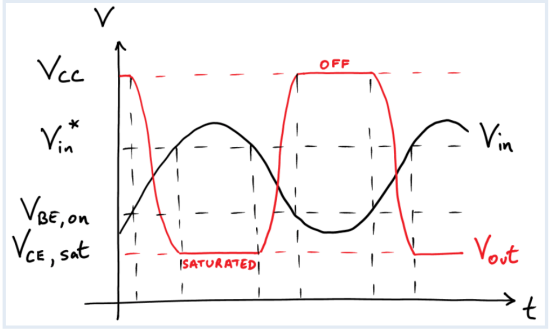


Fig. 6: Voltage signal amplification with clipping. If V_{in} is a signal that goes below $V_{BE,\text{on}}$ and above V_{in}^*, then V_{out} is an amplified and inverted copy that is clipped at V_{CC} above and $V_{CE,\text{sat}}$ below.

Conditions	Mode	Behavior under Linear Model
$V_{GS} < V_{TH}$	OFF	$I_D = 0$
$V_{GS} > V_{TH}$ $V_{DS} > V_{GS} - V_{TH}$	ACTIVE	$I_D = k(V_{GS} - V_{TH})^2$
$V_{GS} > V_{TH}$ $V_{DS} < V_{GS} - V_{TH}$	OHMIC	$I_D = k(V_{GS} - V_{TH})V_{DS}$

Table 1: NMOS transistor operating modes.

Figure 9

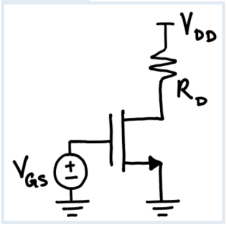


Fig. 9: NMOS transistor connected a Thévenin subcircuit. You can apply the load line method to analyze an NMOS transistor connected to a Thévenin subcircuit, consisting of V_{DD} and R_D. Intersect the NMOS output I-V characteristic in Fig. 8 with the Thévenin subcircuit's I-V characteristic to find the operating point (V_{DS}, I_D) and the mode which it represents.

Figure 7

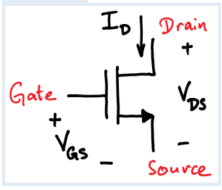


Fig. 7: The circuit symbol for an NMOS transistor. The input voltage V_{GS} drops from gate to source. (Note that $V_{GS} = V_G$ in Fig. 3 and Fig. 4 since the body and source terminals are grounded in those diagrams.) On the output side, I_D flows into the drain and V_{DS} drops from drain to source. Notice that the NMOS transistor symbol incorporates the symbol for a capacitor to signify the gate's capacitative properties.

If the input V_{GS} is fixed, an output I-V characteristic can be traced relating I_D to V_{DS}. Varying V_{GS} therefore produces a family of curves. We model the operation of an NMOS transistor by dividing the I-V space into 3 modes, OFF, ACTIVE and OHMIC, and fitting linear equations to each I-V curve in each mode.

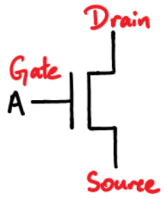
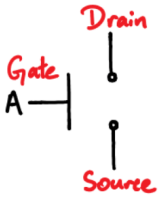
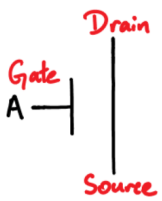
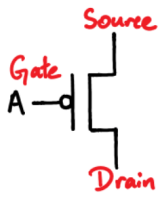
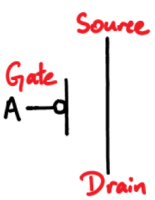
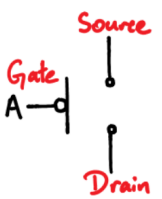
MOSFET Type	Logic Circuit Symbol	$A = 0$ Approximation	$A = 1$ Approximation
NMOS			
PMOS			

Table 1: MOSFET logic circuit symbols and approximations.

The logic circuit symbol for an NMOS transistor (shown above in Table 1) is slightly different to its analog circuit symbol. In a logic circuit, an NMOS transistor is always drawn with the drain terminal at the top and the source terminal at the bottom. In contrast, the logic circuit symbol for a PMOS transistor is always drawn with the source terminal at the top and the drain terminal at the bottom. The PMOS transistor symbol includes a bubble at the gate terminal that represents logical inversion (to be explained below). Note also that the input A labeled at the gate terminal of each MOSFET in Table 1 is a logical value. When $A = 0$, the voltage at the gate terminal is close to ground; when $A = 1$, the gate terminal voltage is close to V_{DD}.

Recall that the energy stored by a capacitor is $0.5CV^2$ J. Thus, each time a MOSFET's output goes from 0 to 1 and back to 0, the load capacitance charges and discharges with $0.5CV_{DD}^2$ J of energy. An additional $0.5CV_{DD}^2$ J is wasted during each cycle due to inefficient charging. (Charging a capacitor efficiently requires the applied voltage to be increased gradually, but this would be too slow for high-performance electronics.) Therefore, a MOSFET consumes a total of CV_{DD}^2 J of energy every time its output completes a full cycle. If the MOSFET switches at a rate of f Hz (i.e. cycles per second), then its power consumption is fCV_{DD}^2 W.

We now extend this analysis to an entire chip. Suppose the chip contains n MOSFETs but only a proportion a of them are actively switching output at any time on average. Then the average number of switching MOSFETs on the chip is na, where the proportion a is known as the activity factor. Finally, if C is the MOSFETs' average load capacitance and f is the cycling frequency of the chip, the power consumption of the chip is:

$$P = nafCV_{DD}^2 \quad (1)$$