	VHDL	Verilog
Concept / syntax	Pascal, Ada Not case sensitive	C language, case sensitive
Strong typing	Yes (Restrictive types)	No (Implicit conversations)
Other hierarchy	Yes [Separate entity/arch]	No
Focus	Safe language, focus to catch as many errors as possible early	Language focused on writing models quickly
Separate Packaging	YES Packages	YES Include files
Gate level modelling	Very Good FPGA library support	Built in primitives, UDPs, Better availability of ASIC library support

Conditional statements

If then /else /elsif

if- else (priority),
case,
casex