Simulation and Synthesis

- The design that is specified and entered as described earlier is simulated for functionality and fully debugged.
- Translation of the debugged design into the corresponding hardware circuit (using an FPGA or an ASIC) is called "synthesis."
- The circuits realized from them are essentially direct translations of functions into circuit elements.

→ Variety of software tools are available

→ Xilinx } simulate designs
→ Modelsim

→ Leonardo Spectrum & Mentor Graphics } obtains synthesized circuit

3.5 COMMENTS

It is a healthy practice to comment a design description liberally – as with any other program. Comments are incorporated in two ways. A single line comment begins with "//" and ends with a new line – for example

```
module d_ff (Q, dp, clk); //This is the design description of a D flip-flop.

//Here Q is the output.

// dp is the input and clk is the clock.
```

One can incorporate multiline comments also without resorting to "//" at every line. For such multiline comments "/*" signifies the beginning of a comment and "*/" its end. All lines appearing between these two symbol combinations are together treated as a single block comment – for example

```
module d_ff (Q, dp, clk);
```

```
/*  This module forms the design description of a d_flip_flop wherein
    Q is the output of the flip-flop ,
    dp is the data input and
    clk the clock input*/
```

Multiline comments cannot be nested. For example, the following comment is not valid.

/*The following forms the design description of a D flip-flop /*which can be modified to form other types of flip-flops*/ with clock and data inputs.*/

A valid alternative can be as follows: -

/*The following forms the design description of a D flip-flop (which can be modified to form other types of flip-flops) with clock and data inputs.*/