

ELITE PROJECT REPORT

On

JK Master Slave Experiment at Virtual Lab

SUBMITTED BY

AKASH JHA

AC - 405

MUSKAN KUMAR SHARMA

AD - 423

B.Sc (Honors) Electronics

SUBMITTED TO

**Dr. RAVNEET KAUR
Ms. Gauri Ghai**



**Department of Electronics
Acharya Narendra Dev College
University of Delhi, Delhi, India**

CERTIFICATE

This is to certify that the project entitled “**JK Master Slave Experiment at Virtual Lab**” has been undertaken under the **ELITE** scheme of **ACHARYA NARENDRA DEV COLLEGE, UNIVERSITY OF DELHI** and has been implemented in the Electronic Laboratory. This work has not been submitted anywhere earlier, partially or fully

Supervisor

Dr. Ravneet Kaur

Supervisor

Ms. Gauri Ghai

Principal

Prof. Ravi Toteja

Date:

ACKNOWLEDGEMENT

We wish to express our sincere gratitude to our DBT Star College Teacher Coordinator **Dr. Ravneet Kaur and Ms. Gauri Ghai**, for providing us an opportunity to do our internship and project work.

We sincerely thank **Prof. Amit Garg, Prof. Anju Agrawal, Dr. Vishal Dhingra, Dr. Udaibir Singh, Dr. Monika Bhattacharya, and Mr. Dinesh Kumar** for their guidance and encouragement in carrying out this project work.

We also wish to express our gratitude to support staff members who rendered their help for the successful completion of our project.

We also thank our **Principal Prof. Ravi Toteja** for providing us the opportunity to embark on this project.

INTRODUCTION

Virtual Labs nowadays have become an integral part of college life. This Covid-19 pandemic taught us very well that the practical part of college learning could be done through online platforms like the virtual lab.

In this pandemic, students who enrolled in the batch of 2020-23 have completed half of the degree practical in online mode, so it was pretty well known the importance of the virtual labs.

But still, not all the offline practicals were available on the various virtual lab platforms. So, it was decided to take an initiative to develop some unavailable labs on the online mode.

Virtual Labs have lower costs and provide a better learning experience for students at a fraction of the cost.

It was decided to develop the virtual lab on “**JK Master Slave Circuits using elementary gates**”. All the module material is written using HTML (the standard markup language for Web pages) and CSS (the language we use to style an HTML document).

It is believed that this virtual lab will help students to learn about the conceptual, theoretical as well as practical aspect of the work of “JK Master-Slave Flip-Flop”.

JK MASTER-SLAVE

The Master-Slave Flip-Flop is basically a combination of two JK flip-flops connected together in a series configuration. Out of these, one acts as the “**master**” and the other as a “**slave**”. The output from the master flip flop is connected to the two inputs of the slave flip flop whose output is fed back to inputs of the master flip flop.

In addition to these two flip-flops, the circuit also includes an inverter. The inverter is connected to clock pulse in such a way that the inverted clock pulse is given to the slave flip-flop. In other words if CP=0 for a master flip-flop, then CP=1 for a slave flip-flop and if CP=1 for master flip flop then it becomes 0 for slave flip flop.

What is the importance of JK master slave flip flop?

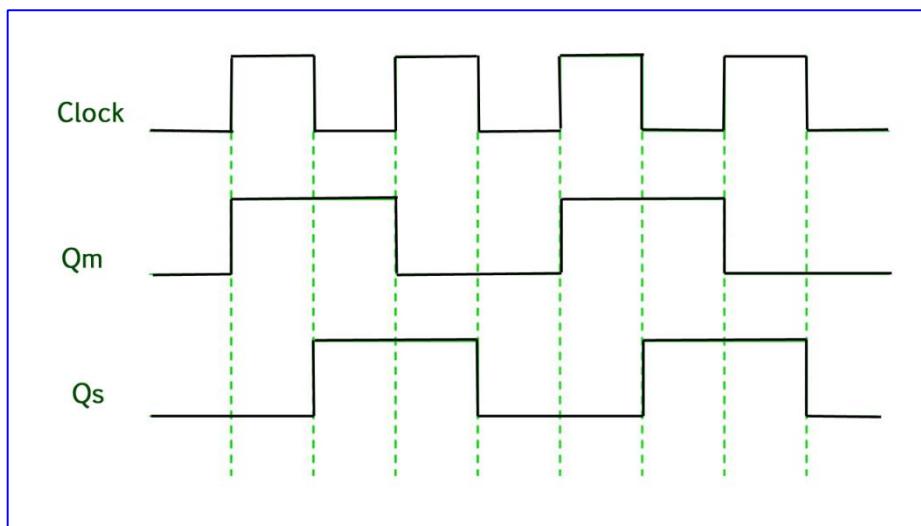
Race Around Condition In JK Flip-flop

For J-K flip-flop, if $J=K=1$, and if $\text{clk}=1$ for a long period of time, then Q output will toggle as long as CLK is high, which makes the output of the flip-flop unstable or uncertain. This problem is called race around condition in J-K flip-flop. This problem (Race Around Condition) can be avoided by ensuring that the clock input is at logic “1” only for a very short time. This introduced the concept of Master Slave JK flip flop.

Working of a master slave flip flop –

1. When the clock pulse goes to 1, the slave is isolated; J and K inputs may affect the state of the system. The slave flip-flop is isolated until the CP goes to 0. When the CP goes back to 0, information is passed from the master flip-flop to the slave and output is obtained.
2. Firstly the master flip flop is positive level triggered and the slave flip flop is negative level triggered, so the master responds before the slave.
3. If $J=0$ and $K=1$, the high Q' output of the master goes to the K input of the slave and the clock forces the slave to reset, thus the slave copies the master.
4. If $J=1$ and $K=0$, the high Q output of the master goes to the J input of the slave and the Negative transition of the clock sets the slave, copying the master.
5. If $J=1$ and $K=1$, it toggles on the positive transition of the clock and thus the slave toggles on the negative transition of the clock.
6. If $J=0$ and $K=0$, the flip flop is disabled and Q remains unchanged.

Timing Diagram of a Master flip flop –



1. When the Clock pulse is high the output of master is high and remains high till the clock is low because the state is stored.
2. Now the output of master becomes low when the clock pulse becomes high again and remains low until the clock becomes high again.
3. Thus toggling takes place for a clock cycle.
4. When the clock pulse is high, the master is operational but not the slave thus the output of the slave remains low till the clock remains high.
5. When the clock is low, the slave becomes operational and remains high until the clock again becomes low.
6. Toggling takes place during the whole process since the output is changing once in a cycle.

This makes the Master-Slave J-K flip flop a Synchronous device as it only passes data with the timing of the clock signal.

CODE

HTML CODE:-

```
<!DOCTYPE html>
<html lang="en">

<head>
    <link href="https://vjs.zencdn.net/7.17.0/video-js.css"
rel="stylesheet" />
    <meta name="viewport" content="width=device-width,
initial-scale=1.0">
    <link rel="shortcut icon"
href="../../../../../../images/vlab-logo.png" type="image/x-icon">

    <title>
        JK master slave
    </title>
    <link rel="stylesheet" href="JK.css" />
</head>

<body>
    <header>
        <div>
            <!--  -->
            

            <h1>V-Lab @ ANDC</h1>
        </div>
        <ul class="navigation">
            <li><a href="../../index.html">Home</a></li>
            <li><a href="../../index.html#labs_section">Labs</a></li>
            <li><a href="../../index.html#team">Team</a></li>
            <li><a href="https://www.andcollege.du.ac.in/" target="_blank" rel="noopener noreferrer">College Website</a>
            </li>
        </ul>
    </header>
    <div class="exp-heading">
        <h1>To design JK Master-Slave Flip-Flop design using elementary gates.</h1>
    </div>
    <nav>
        <div class="boxq">
            <a class="internal_link" href="#aim">
                <br>
            Aim</a>
        </div>
        <div class="boxq">
            <a class="internal_link" href="#theory">
                <br>
                    Theory</a>
            </div>
            <div class="boxq">
                <a class="internal_link" href="#procedure">
                    <br>
                        Procedure</a>
                </div>
                <div class="boxq">
                    <a class="internal_link" href="#animation">
                        <br>
                            Animation</a>
                    </div>
                    <div class="boxq">
                        <a class="internal_link" href="#simulator">
                            <br>
                                Simulator</a>
                        </div>
                        <div class="boxq">
                            <a class="internal_link" href="#observation">
                                <br>
                                    Observations</a>
                            </div>
                            <div class="boxq">
                                <a class="internal_link" href="#result">
                                    <br>
                                        Result</a>
                            </div>
                            <div class="boxq">
```

```

        <a class="internal_link" href="#precaution">
            <br>
            Precaution</a>
        </div>
        <div class="boxq">
            <a class="internal_link" href="#references">
                <br>
                References</a>
            </div>
        </nav>
        <section id="exp">
            <div class="container">
                <div class="box" id="aim">
                    <div class="title">
                        <h2 class="heading">Aim</h2>
                    </div>
                    <div class="desc1">
                        <p class="desc">To design JK Master-Slave Flip-Flop
design using elementary gates.</p>
                    </div>
                </div>
                <div class="box" id="apparatus">
                    <div class="title">
                        <h2 class="heading">Apparatus</h2>
                    </div>
                    <div class="desc1">
                        <ol class="desc">
                            <li>One 74LS10(3-input-nand gate) IC</li>
                            <li>Three 74LS00(2-input-nand gate) IC</li>
                            <li>Two 5 Volt supply volatge</li>
                            <li>One Clock and one not gate/inverter</li>
                        </ol>
                    </div>
                </div>
                <div class="box" id="theory">
                    <div class="title">
                        <h1 class="heading">Principle</h1>
                    </div>
                    <p class="desc">
                        Master Slave is a type of JK flip flop in which race around
condition problem is removed. In this flip flop there is two stage first
stage is Master and second is Slave.
                    </p>
                    <h1 class="desc-heading">Race Around Condition</h1>
                    <p class="desc">

```

Race around Condition: Toggling more than once within a clock cycle.

<div class="desc">

Race around condition can be avoided by

<ol class="desc">

- Master Slave Topology
- $tp < \Delta t < T$
- Edge Triggering

<p>where,</p>

→ tp = pulse width

→ Δt = time interval equal to the propagation delay through two NAND gates

→ T = Time period of the pulse

</div>

</p>

<h1 class="desc-heading">How the race around condition is removed?</h1>

<p class="desc">

As shown in above Figure there is a clock(CLK) which is connected to first stage(Master) and via inverter to second stage(Slave) i.e., if clock is 1 then first stage gets 1 and second stage gets 0.
 When clock is 1 at that instant stage 1 is on and stage 2 is off and when 0, stage 1 is off and stage 2 is on. And due to this action the output of first stage transferd to stage 2 when first stage is off and second stage is on and hence the race around condition is removed.

</p>

<div class="text-center my-2 py-2" style="font-size: 25px; background-color: rgba(244, 246, 248, 0.514);>

Truth Table

<table class="table table-hover table-bordered">

<thead>

<tr>

<th scope="col">clk</th>

<th scope="col">J</th>

<th scope="col">K</th>

<th scope="col">Q</th>

```

                <th scope="col">Qn</sup></th>
            </tr>
        </thead>
        <tbody>
            <tr>
                <th>&uarr;</th>
                <td>0</td>
                <td>0</td>
                <td colspan="2">Previous</td>
            </tr>
            <tr>
                <th>&uarr;</th>
                <td>0</td>
                <td>1</td>
                <td>0</td>
                <td>1</td>
            </tr>
            <tr>
                <th>&uarr;</th>
                <td>1</td>
                <td>0</td>
                <td>1</td>
                <td>0</td>
            </tr>
            <tr>
                <th>&uarr;</th>
                <td>1</td>
                <td>1</td>
                <td colspan="2">Toggle</td>
            </tr>
        </tbody>
    </table>
</div>
<div class="desc">
    <h2>Formula:-</h2>
    <p>To find next state <br> Q(n+1) = J*Q'(n) + K'*Q(n)</p>
    <p>Where,</p>
    <ul>
        <li>Q(n) &rArr; Previous state or output of JK master slave</li>
        <li>Q(n+1) &rArr; Next state or output of JK master slave</li>
        <li>J,K &rArr; Inputs of JK master slave</li>
    </ul>
</div>
<div class="desc">
    <h2>Working:-</h2>

```

```

<ol>
    <li>Master is positive level triggered and Slave is negative level triggered</li>
        <li>When clock pulse is one master is activated and slave is deactivated, when clock pulse goes to zero master deactivates and slave activates.</li>
            <li>For different combination of JK Truth Table shown above</li>
        </ol>
    </div>
    </div>

    <div class="box" id="procedure">
        <div class="title">
            <h2 class="heading">Procedure</h2>
        </div>
        <div class="desc1">
            <ol type="1" class="desc">
                <li> To design JK Master-Slave there is requirement of one 3-input nand gate IC(74LS10) and three 2-input nand gate IC(74LS00).</li>
                <li> Connect the circuit as shown in figure.</li>
                <li> Connect 5V supply to the circuit.</li>
                <li> Turn on the supply and write the reading.</li>
                <li> And verify it from the Truth-Table.</li>
            </ol>
        </div>
    </div>
    <div class="box" id="animation">
        <div class="title">
            <h2 class="heading">Animation</h2>
        </div>
    </div>
</section>
<!-- VideoJS to beautify video player --&gt;
&lt;script src="https://vjs.zencdn.net/7.17.0/video.min.js"&gt;&lt;/script&gt;
&lt;/body&gt;

&lt;/html&gt;
</pre>

```

View of page

V-Lab @ ANDC

Home Labs Team College Website

To design JK Master-Slave Flip-Flop design using elementary gates.

Aim Theory Procedure Animation Simulator Observations Result Precaution References

Aim

To design JK Master-Slave Flip-Flop design using elementary gates.

Apparatus

1. One 74LS10(3-input-nand gate) IC
2. Three 74LS00(2-input-nand gate) IC
3. Two 5 Volt supply volatge
4. One Clock and one not gate/inverter

Principle

Master Slave is a type of JK flip flop in which race around condition problem is removed. In this flip flop there is two stage first stage is Master and second is Slave.

JK Master-Slave Flip-Flop Circuit Diagram

How the race around condition is removed?

As shown in above Figure there is a clock(CLK) which is connected to first stage(Master) and via inverter to second stage(Slave) i.e., if clock is 1 then first stage gets 1 and second stage gets 0.

CONCLUSION

In this project the implementation of the “JK Master-Slave Flip-Flop using basic elementary Gates” is successfully carried out using HTML and CSS.

By observing the results obtained it can be concluded that Virtual Lab for JK Master-Slave Flip-Flop has been developed successfully using HTML and CSS.

The User-Interface of the Virtual Lab is kept easy and simple to which students can adapt easily.

All the information uploaded on Virtual Lab is correct and error-free. All the information is short and to the point. Thus making the Vlab more compact and time worthy.