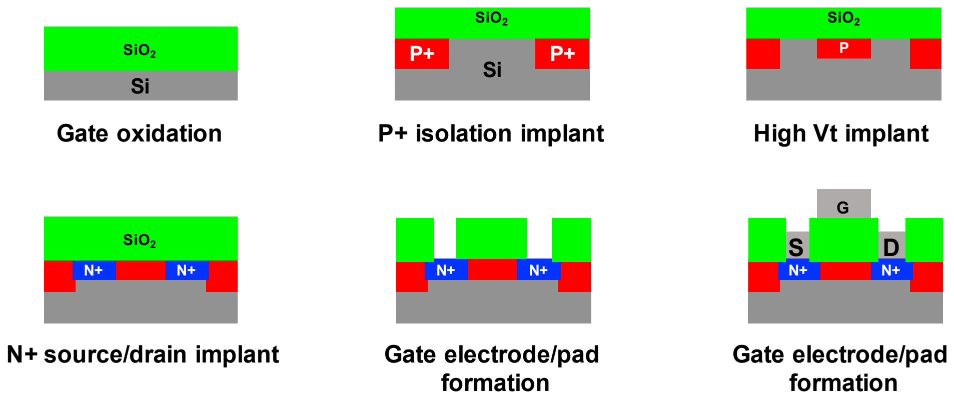
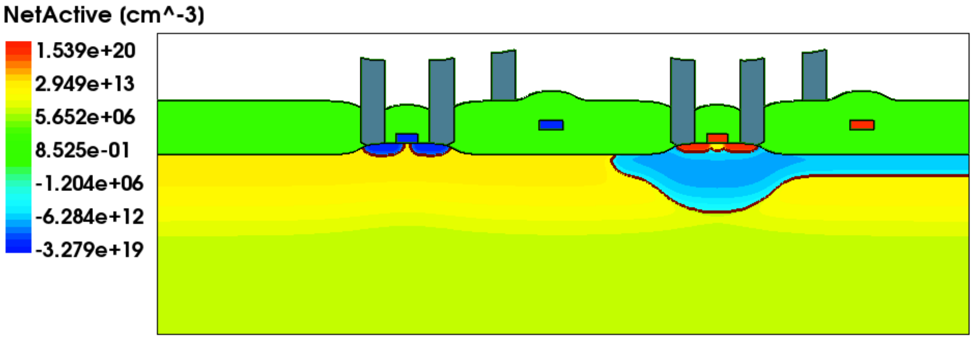
Process Flow and TCAD

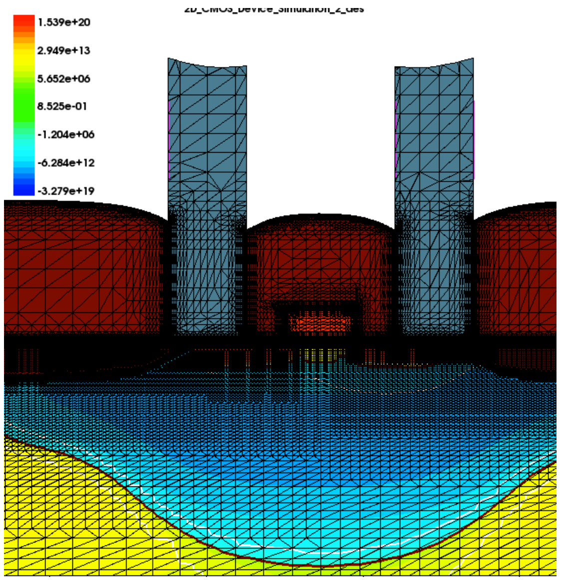
NMOS Process Flow



2D Sentaurus Simulation



Simulated NMOS with Grid



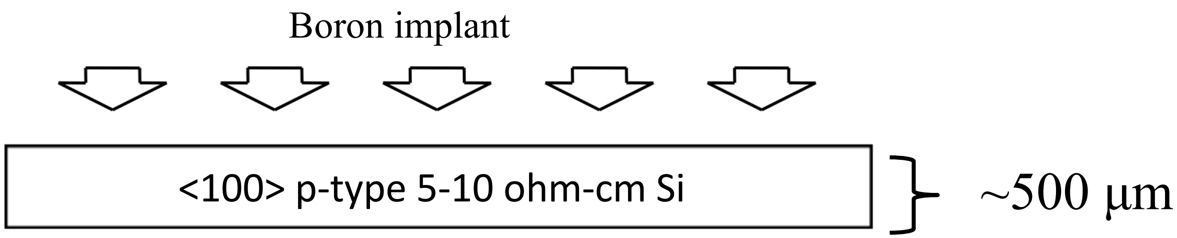
Stanford | ENGINEERING
Electrical Engineering

Outline

1. The EE312 NMOS process, step-by-step
   – Masks and process flow
   – Cross sections and SEMs/micrographs

2. Technology CAD: Sentaurus
   – Oxidation, implant/anneal simulations
   – 1D simulation examples

NMOS Process Flow



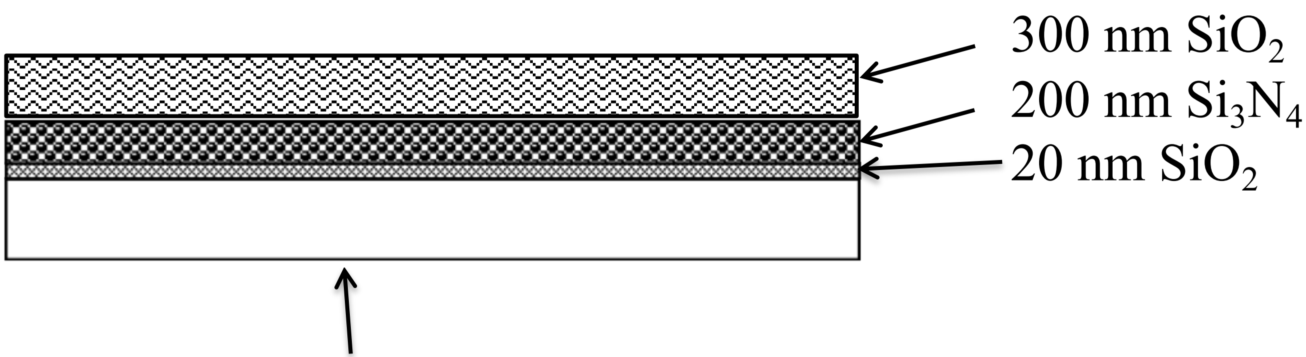
V_T adjust implant

Species: B_{11}^{+}

Dose: 4E13 cm^{-2}

Energy = 100keV

7 deg tilt



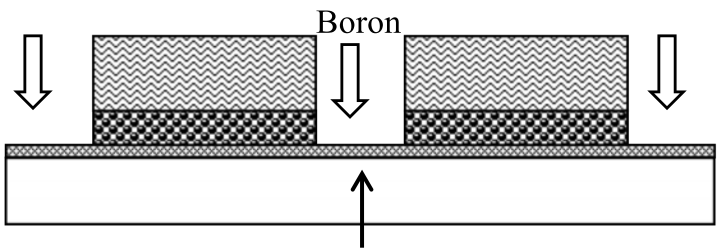
There's oxide/nitride here, too
But omitted for brevity

Pad formation for LOCOS

Thermal Oxidation @ 850°C 15min in H_2O

LPCVD Nitride Dep 45 min. @ 785°C

NMOS Process Flow



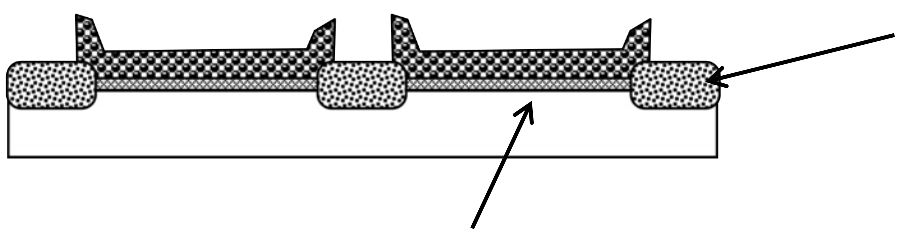
This is where isolation will be

Photomask #1: Isolation

P+ Isolation Implant

B_{11}^{+}; Dose: $1\text{x}10^{15}$ cm^{-2};

Energy 30 keV; 7^{o} tilt

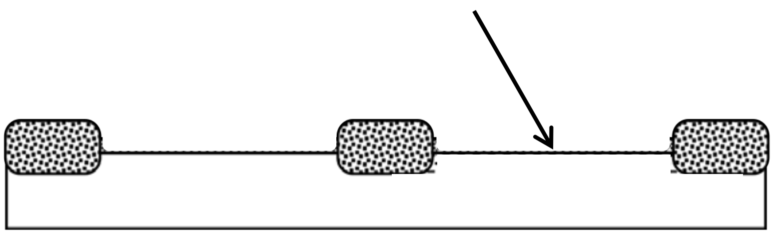


Field Oxidation

1000°C in H_2O for 1hr 45 min

540nm SiO_2

This is where NMOSFET will be



Active area formation

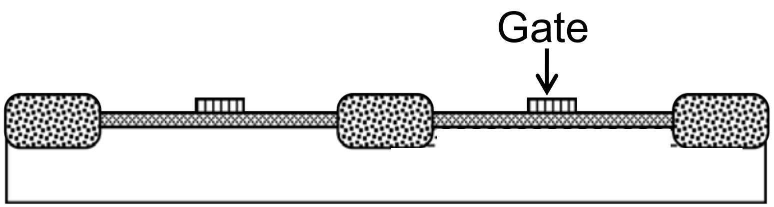
Pad nitride/oxide strip

Kooi Oxidation @ 850°C in H_2O 15min

Grows ~20nm SiO_2

Strip oxide grown in active area

NMOS Process Flow



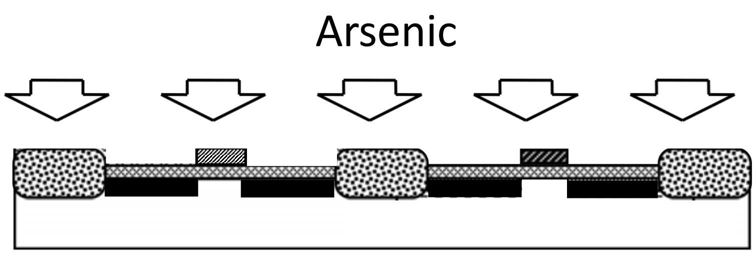
Gate Oxidation

900°C Dry O_2 20 min. ~10nm

LPCVD poly-Si deposition

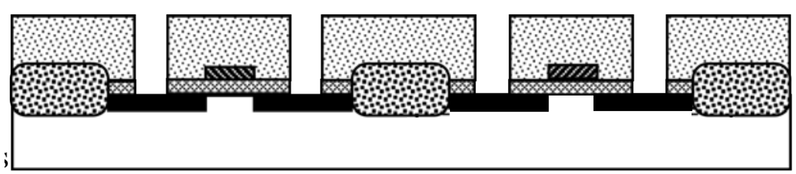
45min at 560°C, ≈ 200nm

Photomask #2: Gate definition



Source/Drain Arsenic Implant

50 keV, As^{75}, 2 x10^{15} cm^{-2}



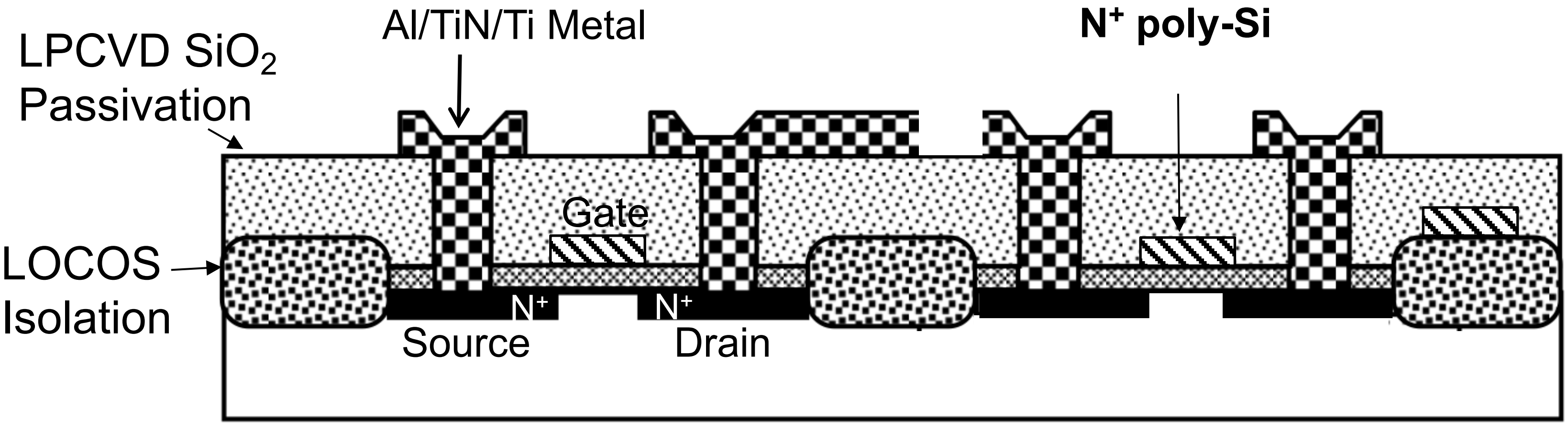
LTO Deposition

LPCVD @ 400°C, ≈ 600nm

LTO densification 30min. H_2O @ 950°C

Mask #3 – Contact Holes

FINAL DEVICE STRUCTURE



Al/TiN/Ti Metal Deposition
Mask 4 to define metal pattern
Metal Dry Etch

Forming gas anneal (H_2 diluted in N_2)
400°C for 10 minutes
Reduces surface states at oxide/silicon interface

Outline

1. The EE312 NMOS process, step-by-step
   – Masks and process flow
   – Cross sections and SEMs/micrographs

2. Technology CAD: Sentaurus
   – Oxidation, implant/anneal simulations
   – 1D simulation examples

What is Sentaurus Process?

- Three dimensional process simulation program
  - Evolved from TSUPREM4 (originally developed at Stanford during 70s and 80s)
  - Together with Sentaurus Device, widely used for TCAD simulation in semiconductor industry
  - Applications: CMOS, memory, solar cells, analog/RF devices, image sensor, etc.

- Simulates
  - Accurately simulates oxidation, ion-implantation, diffusion
  - Approximately simulates etching, deposition, epitaxy

- Output: thickness of layers, dopant distribution, certain electrical properties

Using Sentaurus Process

- Create file containing processing info and output statements with sprocess commands using Emacs, VI or any of your favorite text editor. Do not use software like Word or Pages.

- To run the simulation at the command prompt, type:

  sprocess <filename>

- Output is in file named <filename>.tdr

Creating a Sentaurus Process Input File

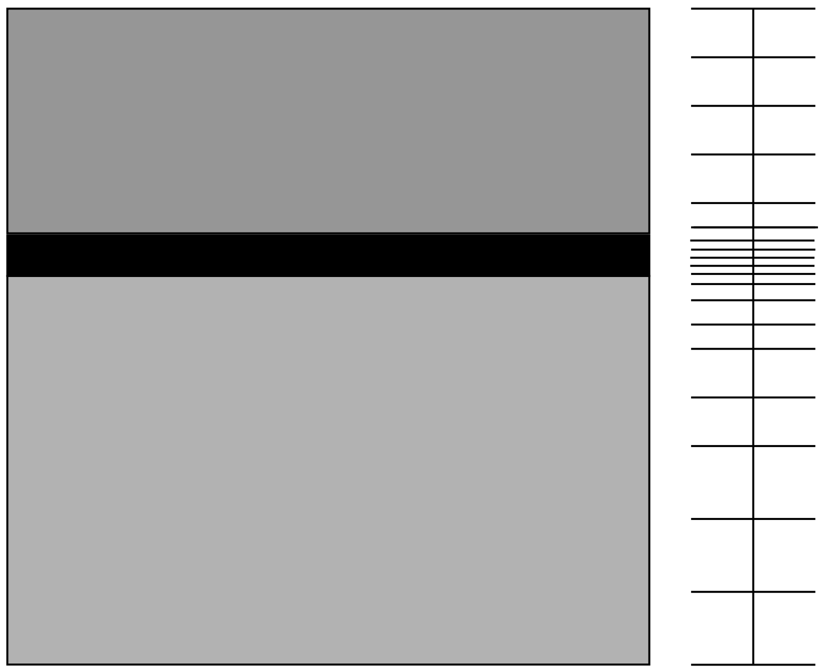
- > *Defining Initial 1D Grid*
  - line x location=0.0 spacing=1<nm> tag=SiTop
    line x location=10<nm> spacing=2<nm>
    line x location=300<nm> spacing=10<nm>
    line x location=2.0<um> spacing=0.2<um>tag=SiBottom
- > *Defining Initial Simulation Domain*
  - region Silicon xlo=SiTop xhi=SiBottom
- > *Initializing the Simulation*
  - Init concentration=1.0e15<cm-3> field=Boron
  - Init tdr=xxx
- > *Setting up a Meshing Strategy*
  - mgoals min.normal.size=3<nm> normal.growth.ratio=1.4
- > *Process steps*
  - Diffusion
    Diffuse temperature=900<C> time=10<min> O2 ramprate=10<C/min>
  - Implantation
    Implant Boron energy=45<keV> dose=5e15<cm-2> tilt=0<degree> rotation=0<degree>

Creating a Sentaurus Process input file

- *> Output commands*
  - Save structure file
    struct tdr=file
  - Print the material interfaces, most useful for examining layers
  - Sheet resistance and p-n junction depth
    SheetResistance

Using Sentaurus Process in 1-D mode: gridding

We will use Sentaurus Process in 1-D mode, and grid the structure; *e.g.*, in the x-direction



- Denser grid in areas where a lot of action occurs and where precision of information is important
- *e.g.*, thin layers, areas with steep dopant profiles

Example Sentaurus Input File

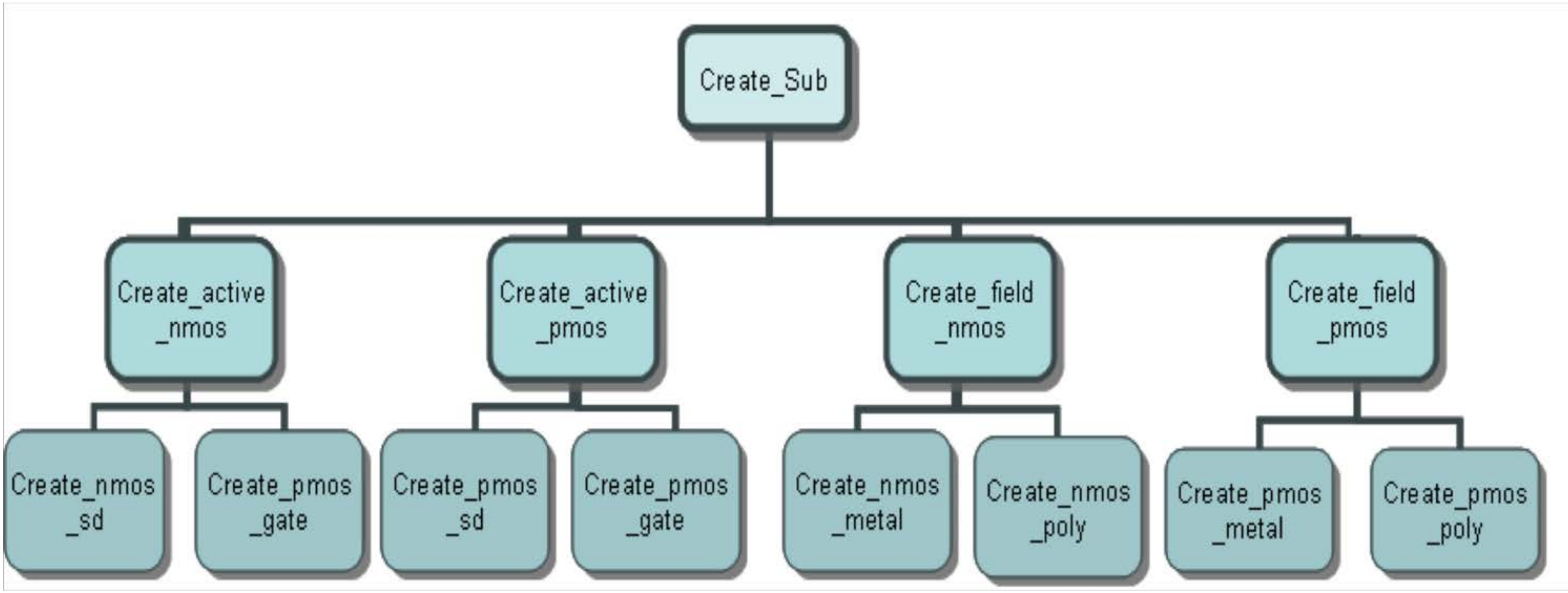
```
# 1D grid definition

line x  location=0.0     spacing=1<nm> tag=SiTop
line x  location=20<nm> spacing=2<nm>
line x  location=100<nm>        spacing=10<nm>
line x  location=600<nm>        spacing=20<nm>
line x  location=1<um>   spacing=50<nm>
line x  location=4.0<um>        spacing=0.2<um> tag=SiBottom

# Initial simulation domain

region Silicon xlo=SiTop        xhi=SiBottom

# Initialize the simulation

init concentration=8.0e14<cm-3> field=Phosphorus

# setting for automatic meshing

mgoals min.normal.size=3<nm> max.lateral.size=0.2<um> normal.growth.ratio=1.4

# Blanket implant
implant species=Phosphorus Silicon gaussian
implant Phosphorus energy=100<keV> dose=3.5e12<cm-2> tilt=0<degree> rotation=0<degree>

SetPlxList {Phosphorus_Implant}
WritePlx Blanket_AsImplant.plx

# Grow 500nm field oxide

diffuse temperature=800<C>      time=35<min>    ramprate=5.714<C/min>
diffuse temperature=1000<C>     time=10<min>    O2
diffuse temperature=1000<C>     time=100<min>   H2O
diffuse temperature=1000<C>     time=10<min>    O2
diffuse temperature=1000<C>     time=35<min>    ramprate=-5.714<C/min>

SetPlxList {PActive}
WritePlx Blanket_Annealed.plx

struct tdr=field_ox
```

Another Example Sentaurus Input File

```
# Initialize Substrate

region Silicon xlo=SubTop xhi=SubBottom
init concentration=1e+15<cm-3> field=Phosphorus wafer.orient=100

# Global Mesh settings for automatic meshing in newly generated layers
# -----------------------------------------------------------------

mgoals normal.growth.ratio=1.1 min.normal.size=5<nm> max.lateral.size=0.2<um>

# BF2 Implant
implant species=BF2 Silicon gaussian
implant BF2 dose=5e15 energy=45.0<keV> tilt=0 rotation=0

SetPlxList {PTotal Boron_Implant}
WritePlx as_implant.plx

struct smesh=asimplant

# Implant Anneal
diffuse temperature=950<C> time=30<min>
SheetResistance y=0.0

# Deposit Aluminum
deposit material=Aluminum thickness=0.6<um>

SetPlxList {PActive PTotal BActive BTotal}
WritePlx anealed950.plx

layers
SheetResistance

struct tdr=diode950

exit
```

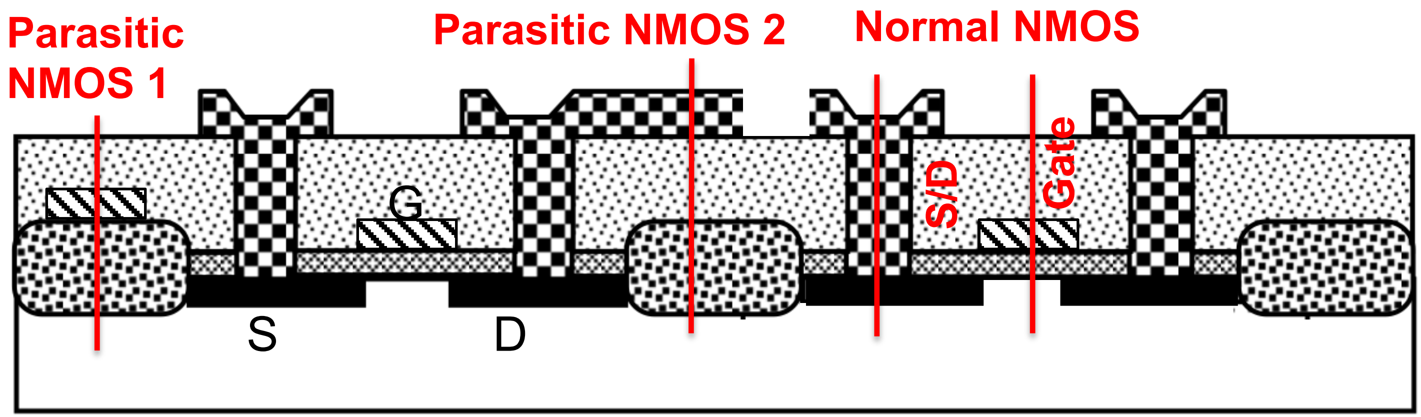
Hierarchy of Sentaurus Files

Example from EE410 (CMOS)



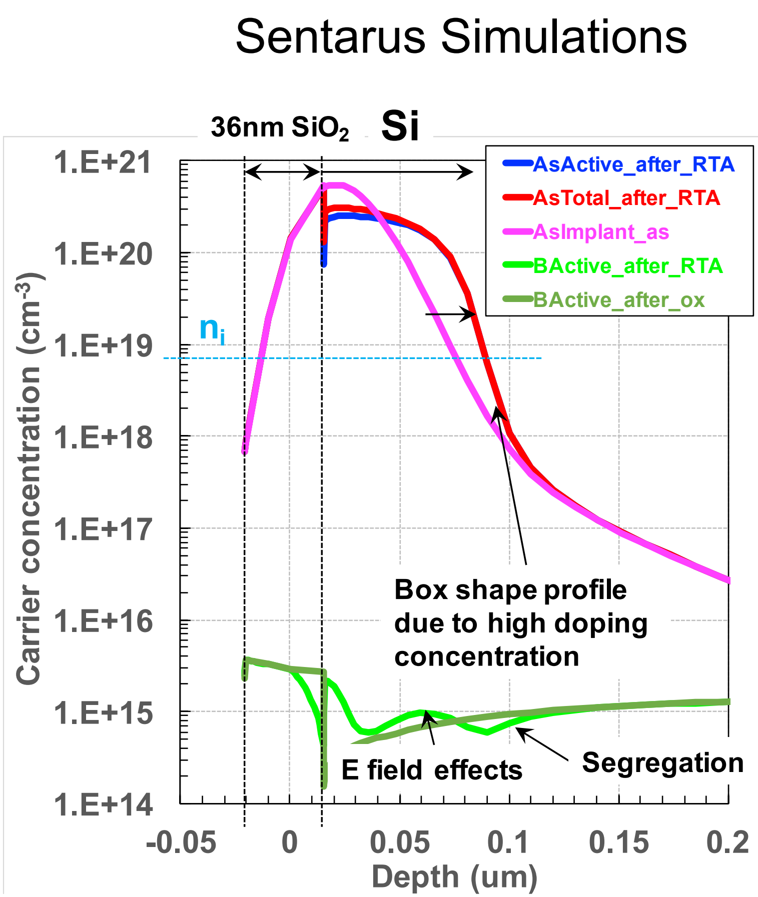
Create sub-structures (use *init* to load structure and *struct* to save structure) and reuse them

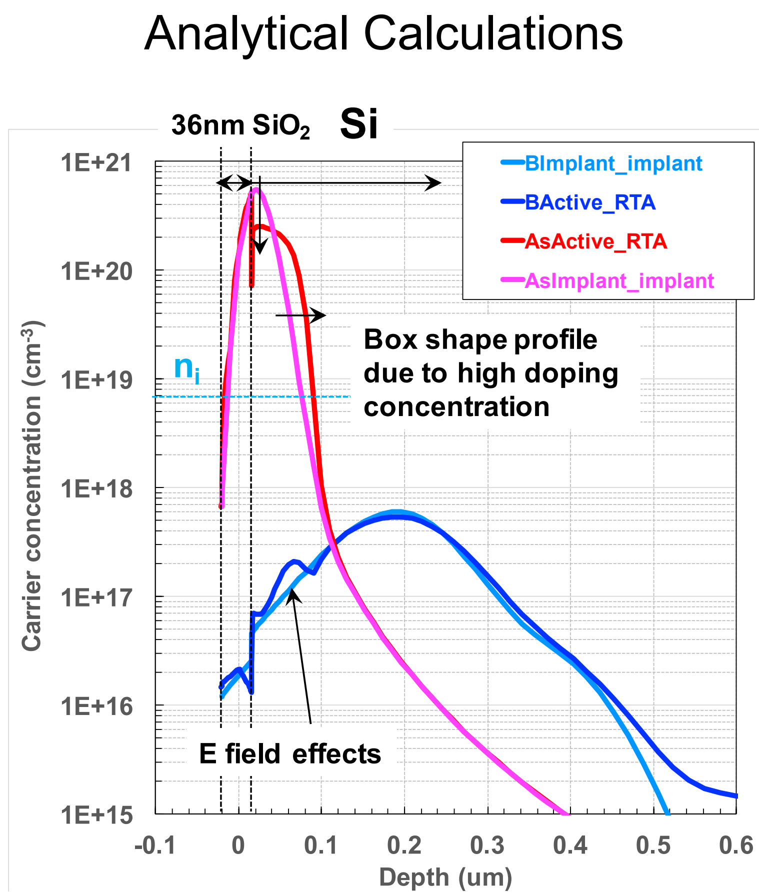
Cross-Sections to be Simulated



1. **Analytical calculations based on EE212**
    a) Various oxide thicknesses (take into account thickness loss during etching and use proper model for different oxides)
    b) Ion implanted and final diffused profiles
    c) Junction depths
    d) Sheet resistance of junctions and poly-Si gate
        - Mobility is a function of doping density. Use either Irwin's curves or analytical model given in text books, for example in Pirret's book.
        - Note that mobility in poly-Si is lower. Assume half that of crystalline Si.
        - Dopant diffusivity in poly-Si is several orders of magnitude higher than crystalline Si
    e) Threshold voltages of active and parasitic MOSFETs.
2. **Sentaurus simulations on the same topics as in 1**
    - Use simulated value of N_A and then use analytical equation for V_T
3. **Comparison between analytical calculations and simulations**

Example: NMOS S/D Profiles (2017)





Useful tips

- Create sub-structures (use *init tdr=xxx* to load structure and *struct tdr=xxx* to save structure)
- Skip steps (freckle etch) and ignore effects (layer undercutting) that Sentaurus Process cannot simulate
- Do not simulate furnace cycles below 800° C
- Use gaussian or 2-gaussian implant profiles instead of pearson profiles for all implants
- Sentaurus Process does not simulate threshold voltage

Process and Device Modeling Paper

(Submitted by each student: Individual effort)

Simulations (by Sentaurus Process, etc.) and analytical **calculations** of the structures (e.g. thickness, doping profile, ...) and electrical parameters (e.g. sheet resistance, threshold voltage, ...) that should result from the process flow you are following in the Lab.

Contents: *Less than 10 pages* of main body. It should be written similar to a paper published in a Journal, e.g., IEEE TED. Any supporting material should go in an appendix.

Schedule **1 copy** of the paper will be due on **February 15, 2019**

Grading
Completeness of information 10%
Quality of presentation 10%
Innovations and others 5%

Check details on the report format etc. on the web page

Writing the report

- Don't spend your time trying to get your hand calculations to match your Sentaurus Process results
- There is no need to describe the process in detail. However, you should Include major process parameters simulated.
- Include models and values of parameters used in calculations.
- Describe your methodology.
- Please mention the model name you have used in the simulationsas the results may vary with different models.
- Focus on differences between hand calculations and Sentaurus Process results and explain why they are different