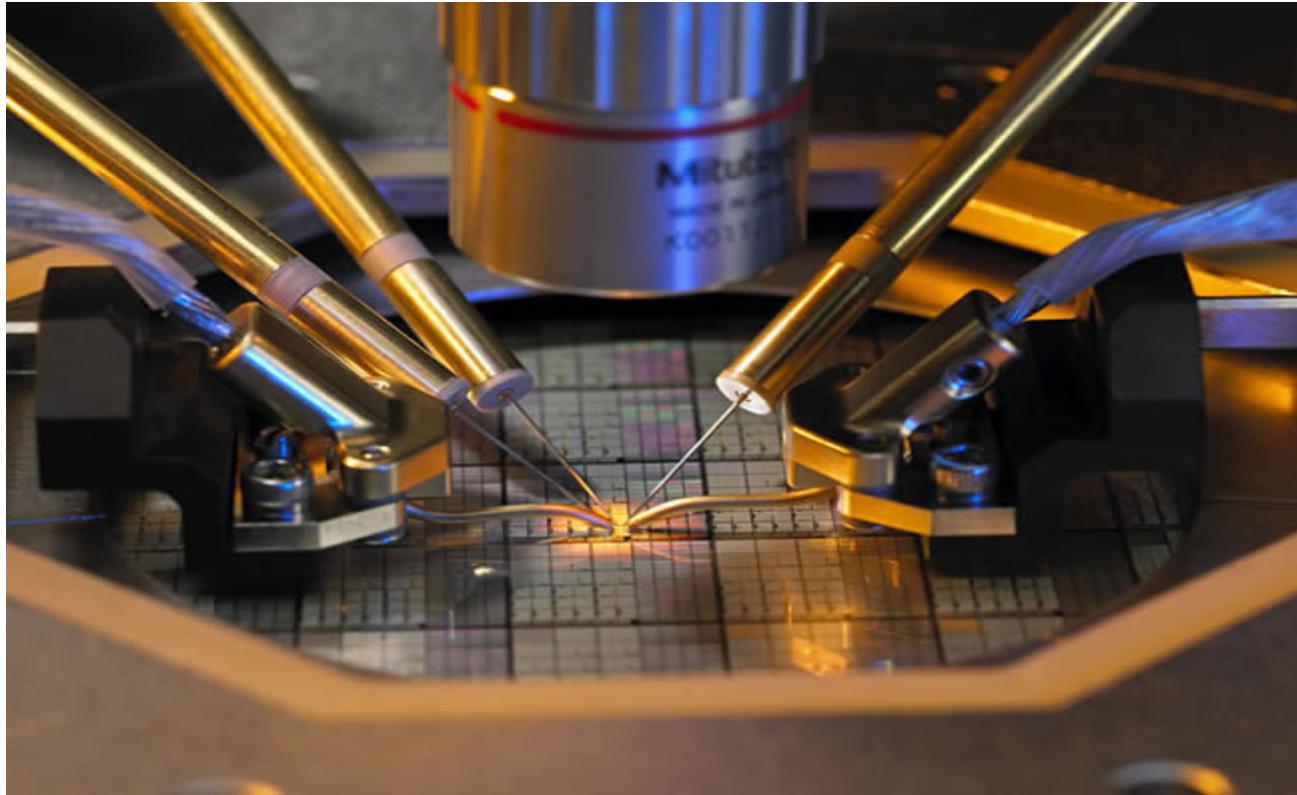


EE312 Test Structures & Testing



Cascade Microtech IC prober

Outline

1. Introduction

2. Process test structures

- Resistors
- Continuity test structures
- MOS capacitors
- Contact chains

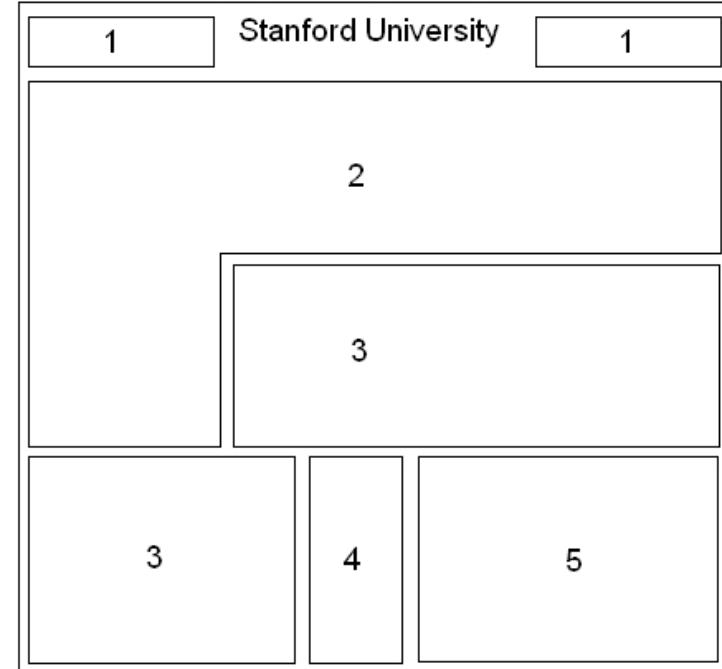
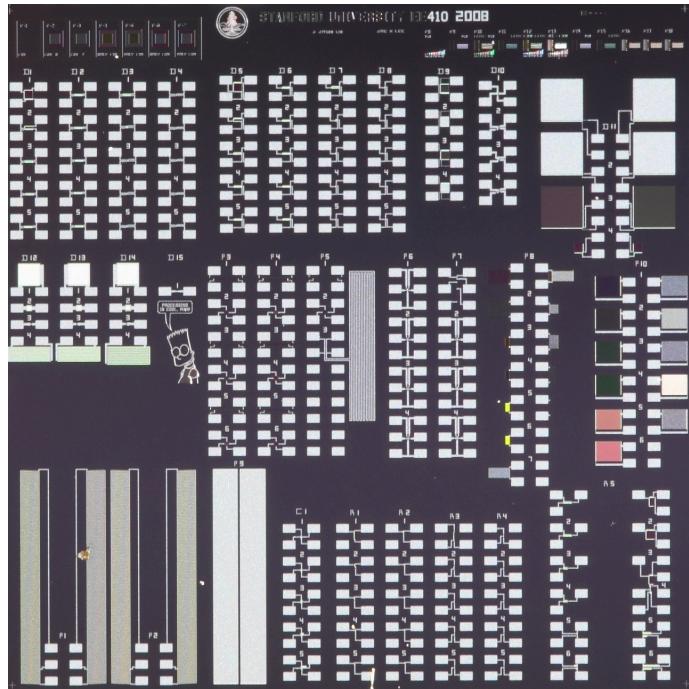
3. Device test structures

- Enhancement mode NMOS
- P-N diodes

4. Wafer probing 101

- How to do the measurements in Allen 155A

What's on the EE312 chip?



The MOS-LOCOS wafer contains 80 dice, each die measuring 8.3mm x 8.3mm.

1. Fabrication Test Structures — checked during processing
2. Device Test Structures — MOSFET's, parasitic MOS, capacitors, diodes
3. Process Test Structures — sheet resistance, contacts, continuity, isolation
4. Circuit Test Structures — CMOS inverters (Not used in EE312)
5. Research Test Structures (Not used in EE312)

PROCESS TEST STRUCTURES

Purpose

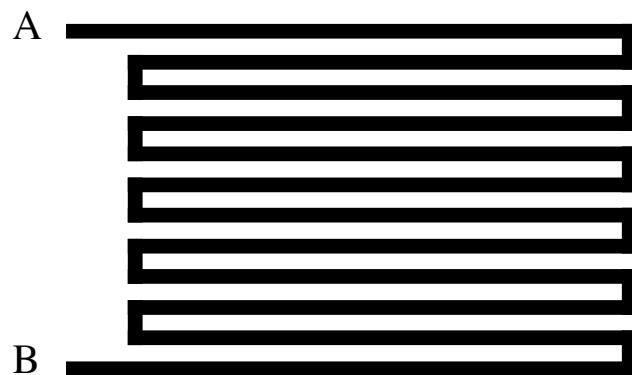
- Extract specific electrical information about the process.
- Identify process problems.
- Improve process.

Test structures

- Continuity and Isolation
- Contact Chains
- Sheet resistance
- Contact Resistance

Metal Continuity Test Structure

- These test structures have a thin, winding piece of metal connecting the two pads. If no current flows between the pads, there was a problem.
- Common sources of failure:
 - overetch
 - material failure (breakage) over aggressive topography (step)
- By measuring the current, the resistance of the metal wire can be calculated.
- **Directions:** Ground one metal pad, sweep other pad from 0V to +5V. There should be current flow through the pads.



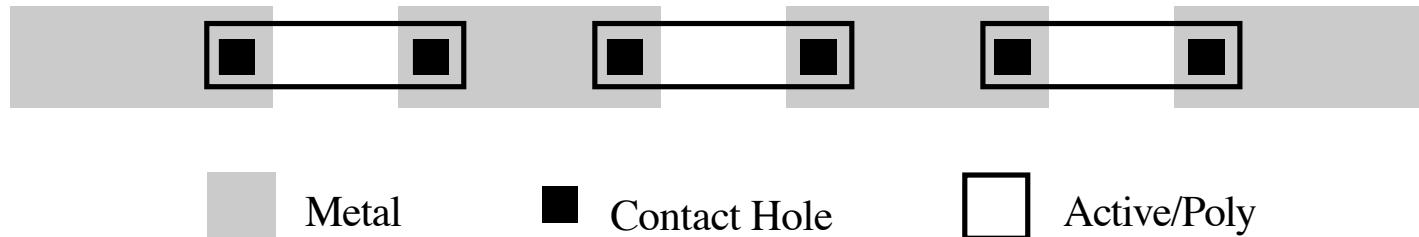
Continuity Structure
Small R_{AB} → PASS

Metal Isolation Test Structure

- These are test structures which have two inter-digitated set of fingers, which should not be connected. However, if there is a some process problem, then the two sets of fingers will be shorted together.
- Common sources of failure:
 - incomplete etch → stringers
 - Problem in lithography
- **Directions:** Ground one metal pad, sweep other pad from 0V to +5V. There should be zero current flow between the pads.



Contact Chain



Description:

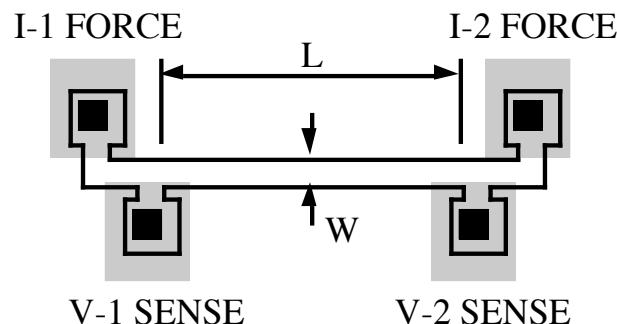
They are used to test contact integrity, i.e., to make sure the oxide etch to contact the source and drain and etched completely through. If it does not, no current will flow through the chain of contacts. This is also used to determine approximate value of the contact resistance between the metal and the semiconductor. It is not a good structure to measure contact resistance since it does not allow decoupling contact resistance from semiconductor resistance and metal resistance.

Directions:

Ground one pad, and sweep the other pad from -5V to +5V. Record the current. No current means the contact etch to the silicon didn't clear with sufficient yield.

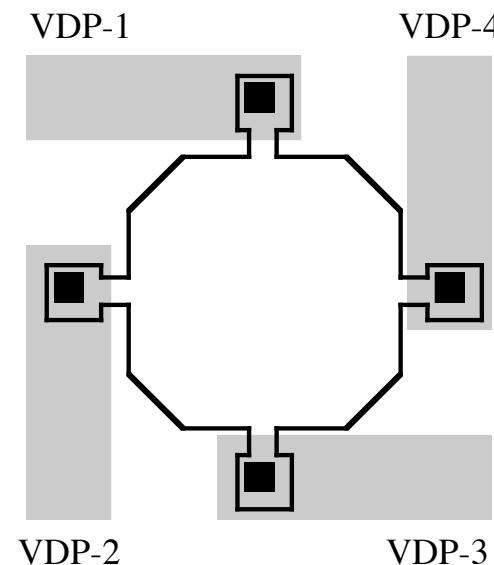
Sheet Resistance

4-Point Probe Structure



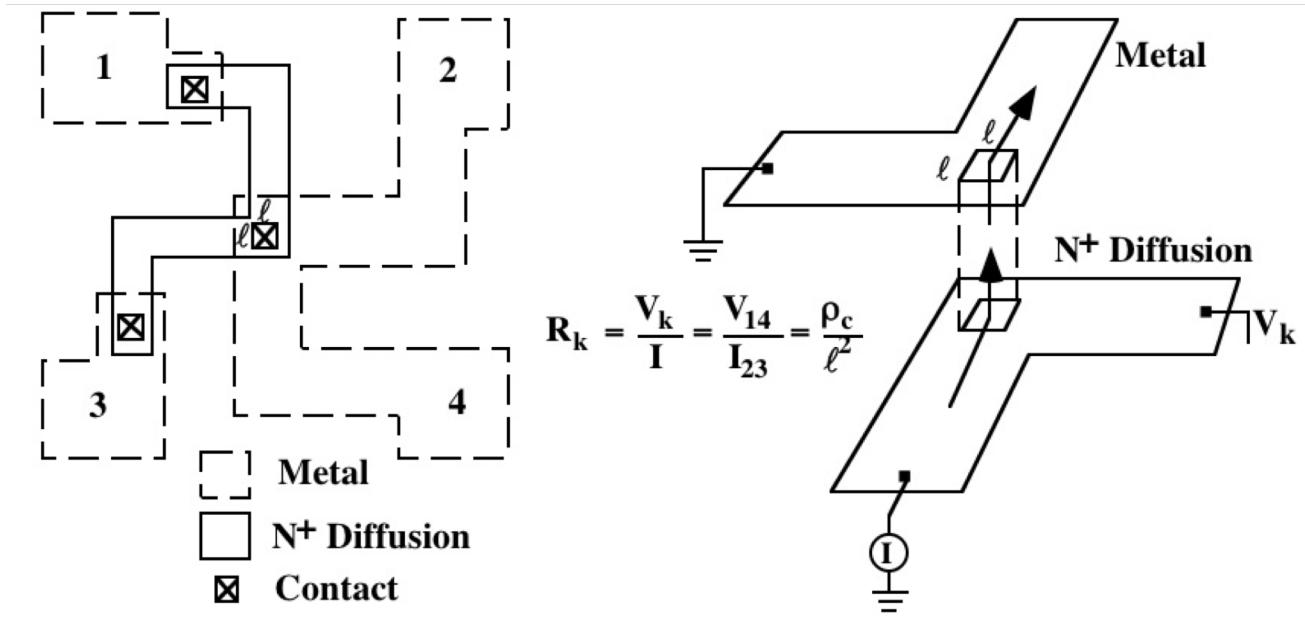
Metal Contact Hole
Specified Wafer Layer

Van der Pauw Structure



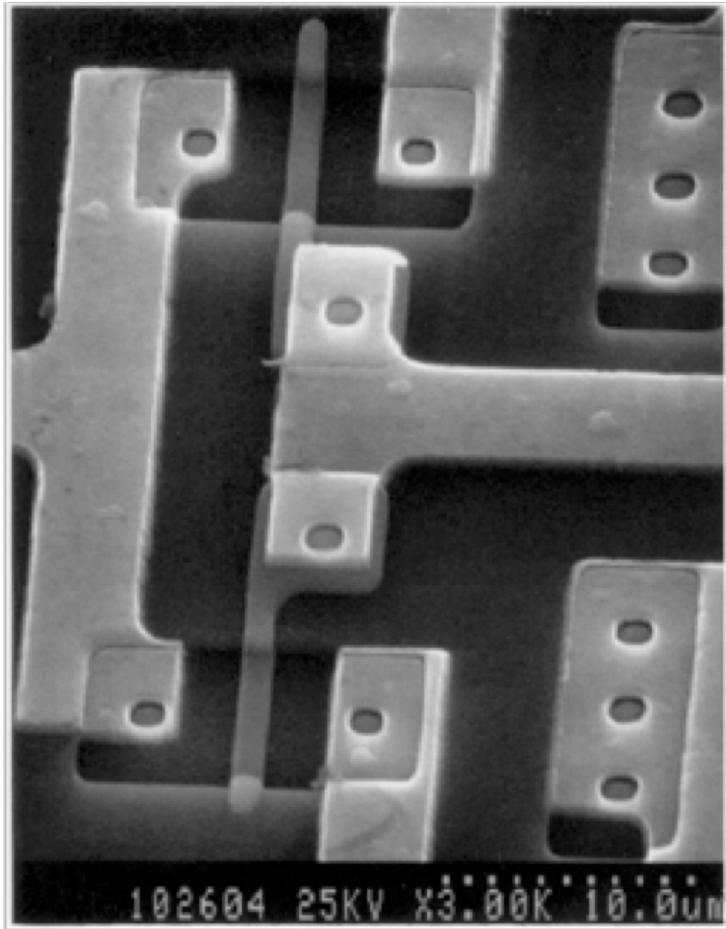
- Force a current and measure the resulting voltage.
- 4-point probe vs. van der Pauw
- Compare measured results with simulated and hand-calculated values.

Contact Resistance: Cross-bridge Kelvin Structure



- Measure resistance across contact interface — Ohmic or Schottky behavior?
- Force a vertical current through contact and measure voltage above and below.
- Examine dependences on material and contact size.

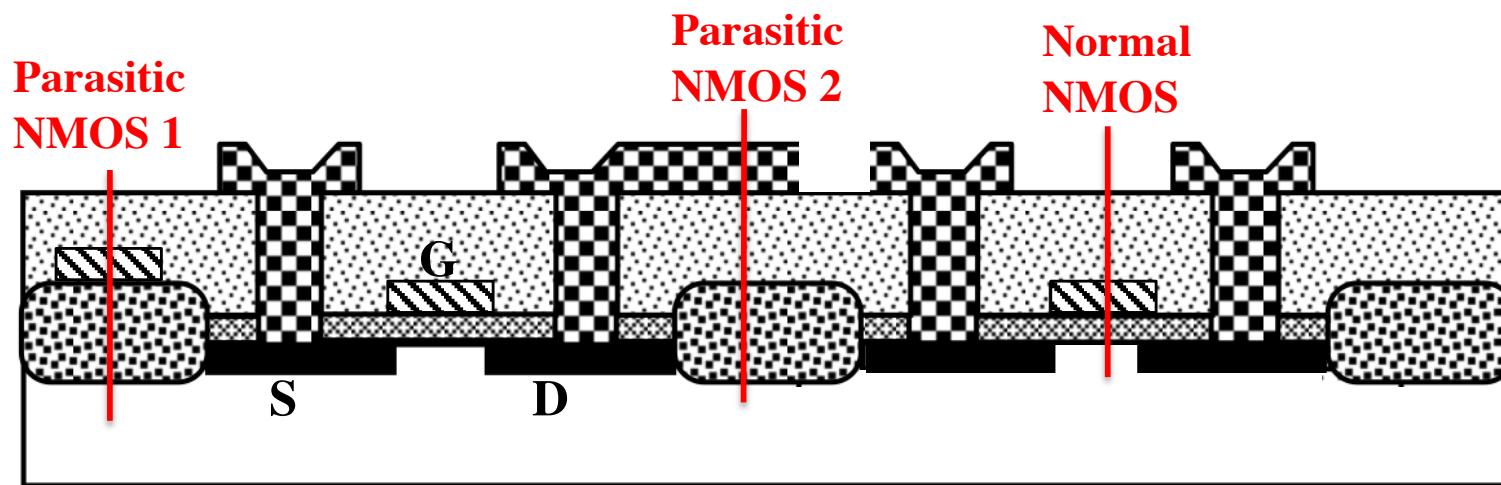
SEM TEST STRUCTURES



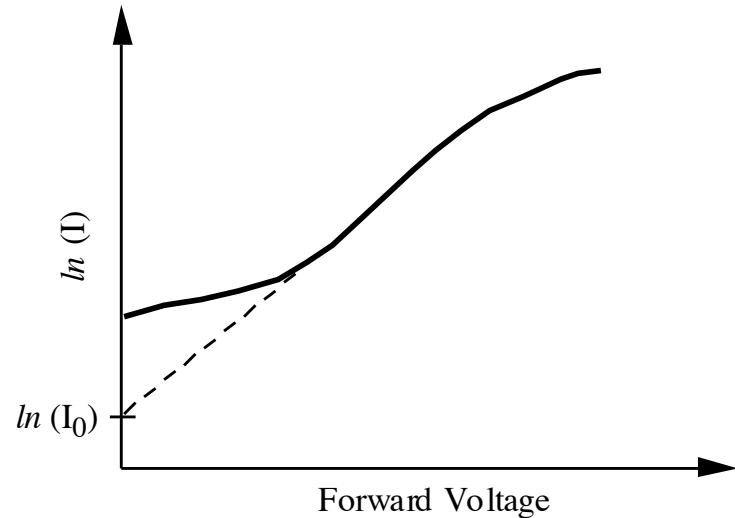
- These structures are specifically designed for cross-sectioning.
- You will need access *outside EE312* to use a Scanning Electron Microscope. The instructor and TA are not responsible for any SEM-related work.
- You will need to cleave your wafers for SEM viewing. Silicon cleaves very nicely along <110> directions. Ask your TA for details.
- You may need to do some etching to enhance the contrast of different regions.
- Not required this quarter unless you have access to SEM

Device test structures

- P-N diode
- MOS Capacitors
- Enhancement mode NMOS
- Parasitic MOSFETS



Diodes



$$I_{\text{Diode}} = I_0 \times \left(e^{qV/nkT} - 1 \right)$$

- Extract both area and edge components of diode current.
- Need to measure low current levels — watch out for noise sources.
- Can reduce surface leakage by applying nitrogen stream to remove surface moisture.
- Measure breakdown and CV characteristics.
- Are diode leakages acceptable?

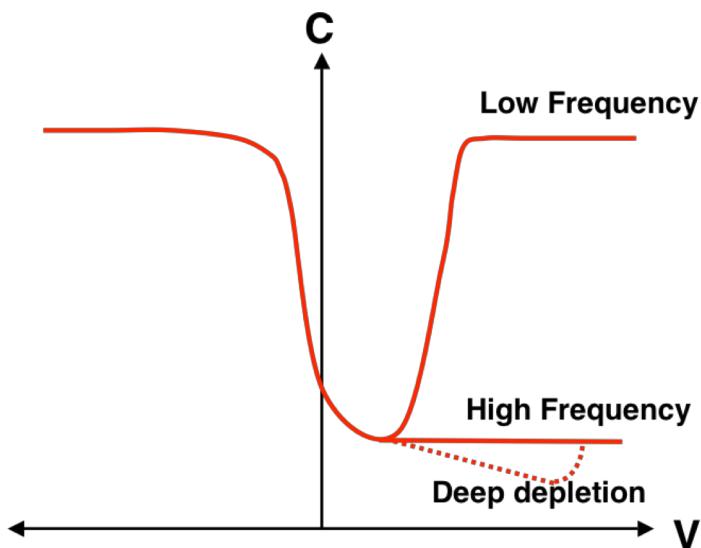
MOS Capacitors

Capacitance-Voltage Measurements:

These are moscap structures. By measuring the capacitance between the metal pad and the substrate, the thickness of the oxide, doping level (and profile) of the substrate and doped regions, and the interface quality between the oxide and silicon can be extracted.

Directions:

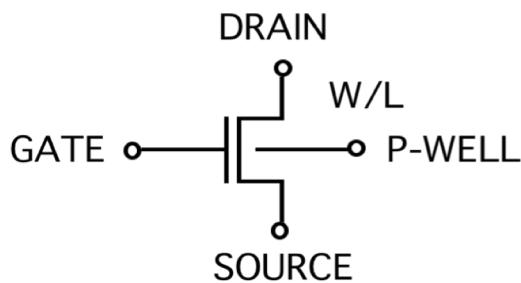
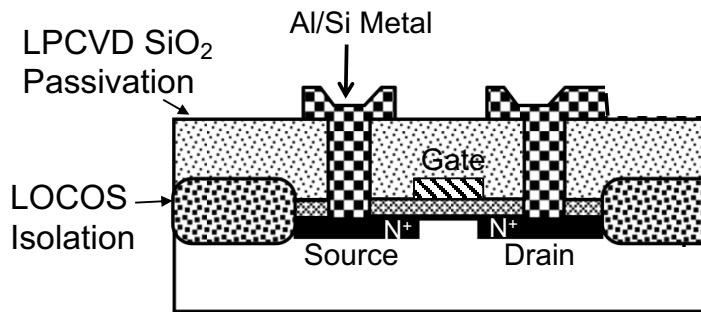
Ground the substrate, and sweep a bias from -3V to 3V to -3V in steps of 50mV, on the metal pad, while apply a 10mV AC signal on top of the DC bias sweep, and record capacitance. This is done with a standard MOSCAP measurement set-up, with the AC signal being low or high frequency. **Low-frequency (quasi-static) CV not to be done.**



Devices to be measured

- Poly-Si gate on thin gate oxide
- Poly-Si gate on field oxide
- Metal gate on field oxide + LTO

NMOS Transistors



Triode Region

$$I_D = \frac{\mu_N C_{OX}}{2} \frac{W_{eff}}{L_{eff}} [2(V_{GS} - V_T) - V_{DS}] V_{DS}$$

Saturation Region

$$I_{DSAT} = \frac{\mu_N C_{OX}}{2} \frac{W_{eff}}{L_{eff}} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

- Need a fairly thorough investigation of MOSFET behavior.
- I_D - V_{DS} curves (the most standard plot)
- I_D - V_{GS} behavior

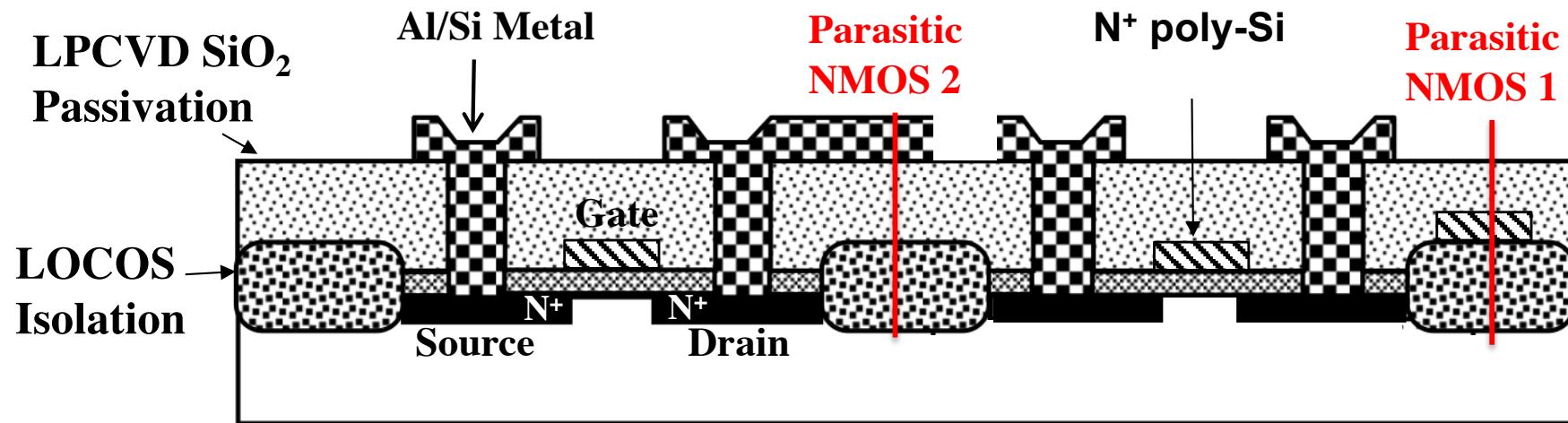
Things you should at least measure:

- Threshold voltages (V_T)
- Transconductance (g_m)
- Body effect (γ)
- Channel doping (N_A, N_D)
- Subthreshold behavior (ξ)
- Channel mobility (μ_N)
- Channel length modulation (λ)
- Breakdown (V_{BD})
- Size of smallest functioning device — if some fail, find out why.
- Short channel effect — V_T as a function of L
- Narrow channel effect — V_T as a function of W
- Effective L and W

$$I_D \propto \frac{W_{eff}}{L_{eff}} = \frac{W + \Delta W}{L + \Delta L}$$

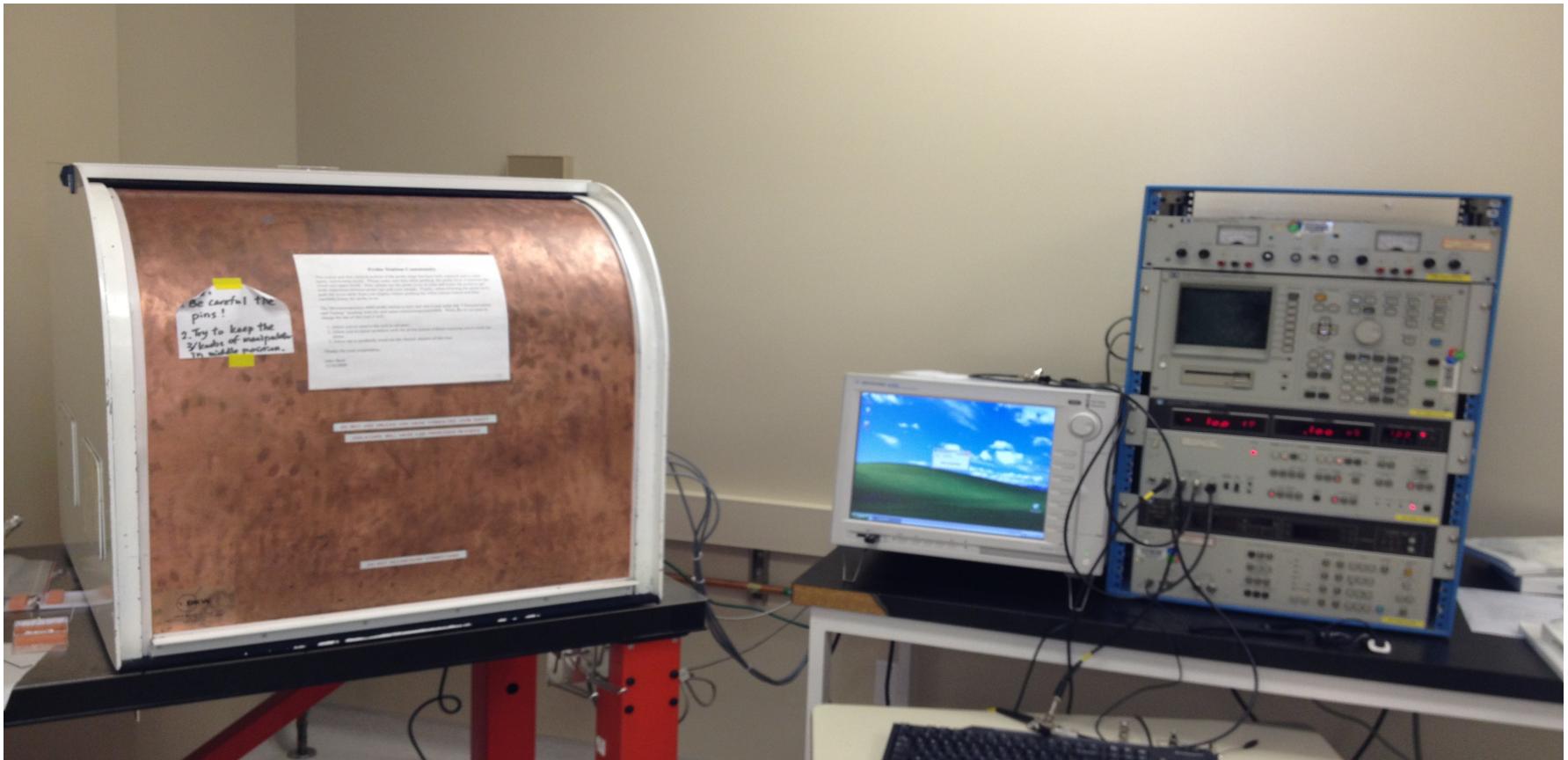
Think about whether you want the transistor to be in triode or saturation to measure the above items.

Parasitic MOSFETs

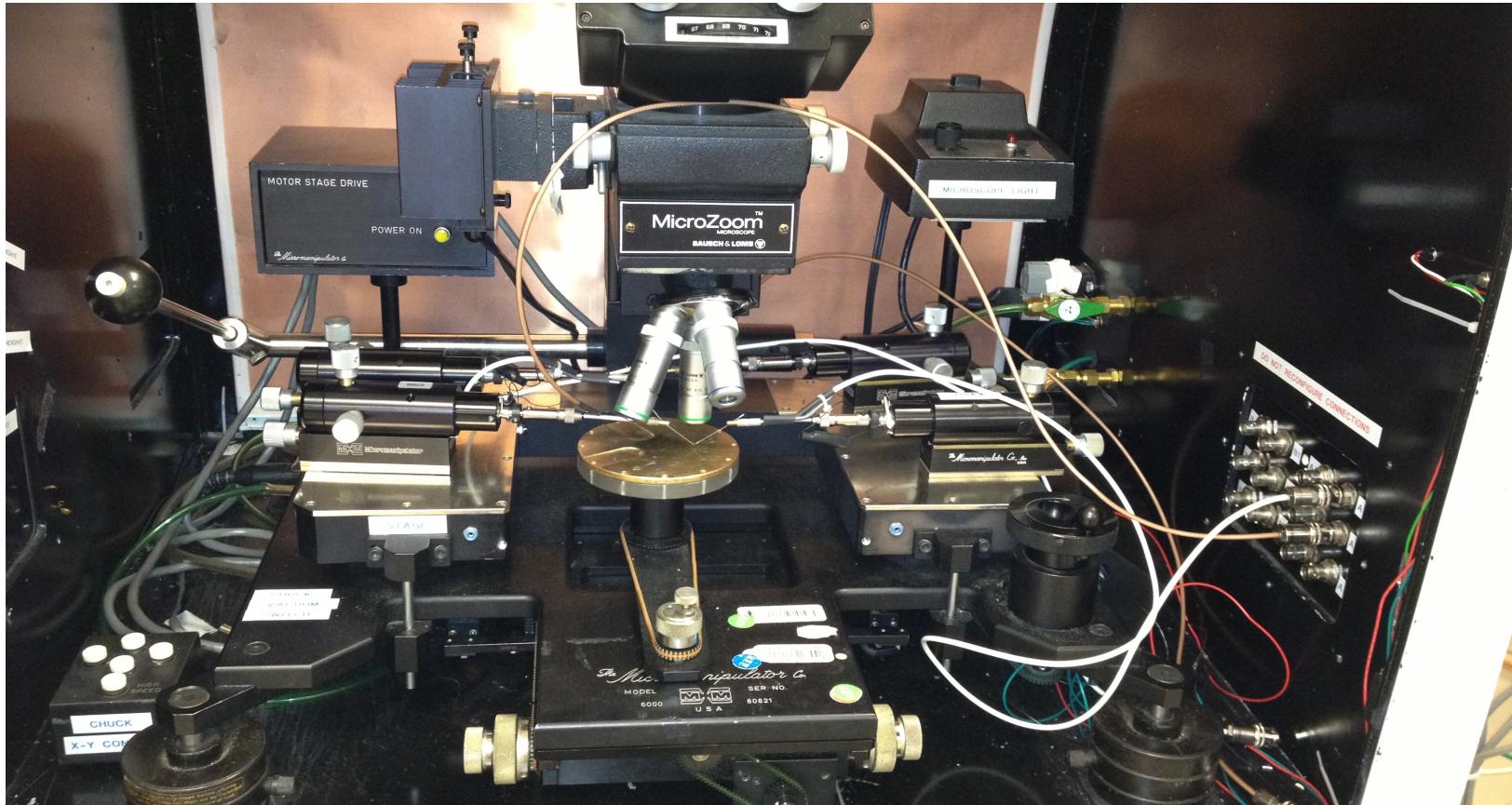


- **Isolation** — are parasitic channel thresholds sufficiently large (i.e., $|V_T| \gg V_{DD}$)?
- Two types: poly on field oxide, metal on LTO + field oxide
- Check agreement with SENTAURUS predictions?

Wafer Probe Station in Allen 155A



Wafer Prober



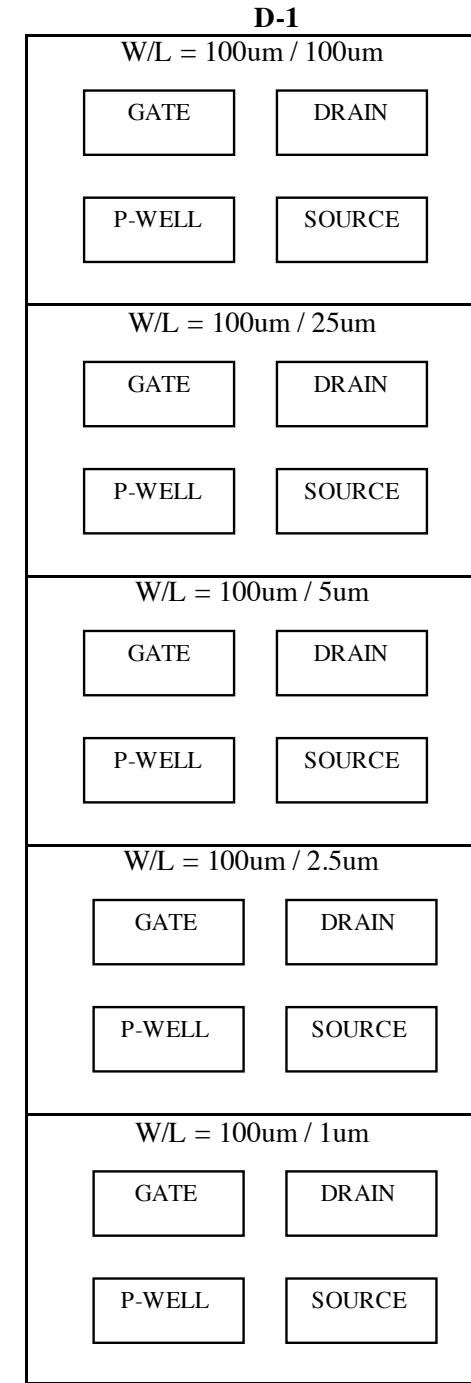
What you need to do for EE312?

- Confirm that process works. If it doesn't, find out why.
- Test every unique structure at least once, but don't waste time testing everything.
- Gather some statistics only on important parameters such as threshold voltages and diode leakage currents. Examine across-wafer and wafer-to-wafer variations. But once again, don't measure everything.
- Make comparisons with simulated and hand-calculated results wherever possible.
- Compare results obtained from different measurement techniques. e.g
 - oxide thickness — Nanospec vs. CV
 - threshold voltage — I_D - V_{GS} vs. CV

WAFER PROBING

- Access device terminals by probing $100\mu\text{m} \times 160\mu\text{m}$ metal pads situated on thick oxide (field region).
- Pads are arranged in 12×2 arrays to accommodate automated probe tester (not used in EE312).
- There are no shared connections between adjacent structures.
- Once all probe tips are positioned, only the probe station stage needs to be raised or lowered to move to the next device.
- The wafer backside is not used as a contact.
- Example D-1
- L (Length) SERIES ($W=100\mu\text{m}$)
- $L = 100, 50, 20, 10, 8, 6\mu\text{m}$
- This set of pads allows you to access 6 different NMOS transistors of fixed gate width and variable gate lengths.

Refer to EE312 Instruction Manual
Appendix A — List of Test Structures
Appendix B — Pad Assignments



Policies and procedures for EE312 testing

- After the fabrication is complete your TA will give you a demonstration on the testing set up. This will be done during your regular lab time slot. The responsibility of the TA is to get you started. Subsequently he/she won't be present when you are testing.
- Every user should read testing handouts before TA's demonstration and exercise caution when operating the testers. Generally, the probe tips and probe position adjustment screws are the most fragile parts.

PRACTICAL TESTING & TROUBLESHOOTING

Important tips...

- Understand why a test structure is on the chip.
 - This tells you what information you can get from the structure and what you need to measure.
- Be able to sketch a cross-section of the test structure to be tested.

Some general notes...

- Take good care of the testing setup — it's your only one and it cannot be replaced.
- Be very careful with the probe tips & manipulators — they are *very* expensive.
- **Avoid working alone** — it's safer and less frustrating.
- BE SAFE — watch out for high currents & voltages (set equipment compliances).
- BE PATIENT & DON'T RUSH — testing is very time-consuming.
- Make sure you distribute the chores *evenly* within your group.

Final Report

- ❑ Written by each group who tested together. It may be divided up into chapters and each chapter written by a member. Please indicate on the report specific contributions of each individual.
- ❑ Contents:
 1. A discussion of the process flow used, including the reasons for each step, any problems encountered and the solutions adopted
 2. Simulations by Sentaurus and calculations of the structures (e.g., oxide thickness, implant profiles) and electrical parameters (e.g., sheet resistance) that should result from the process flow. (from your simulation report)
 3. Methodology and results of measurements taken on test structures, devices and optionally, circuits
 4. Comparison of (2) and (3), where possible, with explanations of differences.
 5. Conclusions
 6. References
 7. Due Date: One soft copy of the final report will be due on March 20.

When things don't work...

- Remember: *Murphy is always watching you!*
 - It's almost always the simplest things that go wrong, so check them first!
- Check the same structure elsewhere first.
 - Never assume anything.
 - Your DUT (device under test) could be defective.
 - You have 6 wafers and 43 dice per wafer, so don't be afraid to look around.
- If you get the same result (no variation), verify your setup.
- Some common problems:
 - wrong connections (e.g., gate and source connections reversed)
 - bad connections (e.g., dirty contact surfaces)
 - faulty cables (a multimeter could be your best friend here)
 - bad probe tips (e.g., high leakage > 10 pA when disconnected)
 - noise — important for low noise, low current measurements
 - Noise sources are often very difficult to find. Sources may be as obvious (?) as transformer noise coming from the microscope light power supply or may come from fundamental grounding and shielding problems with your probe station.
- If your setup is fine, perform important sanity checks.
 - e.g., for MOSFET's, make sure $I_{GATE} = 0$ and $I_{SOURCE} = I_{DRAIN}$
 - These simple tests may sound silly and unnecessary, but they are the only systematic way to locate your problem.
- You have an exhaustive list of process test structures to your avail.
 - Exploit this luxury to deduce the culprit.

Policies and procedures for EE312 testing

A signing up sheet will be posted online. The rules for the testing phase are:

- The time slots for testing have been divided into 4 hours/slot and are classified as
 - Peak Time I (8am to 4 pm, Sunday to Saturday),
 - Peak time II (4 pm to 12am, Sunday to Saturday) and
 - Off Peak hours (12am to 8 am, Sunday to Saturday).
- Each group is limited to a maximum of 5 reserved slots during Prime Time I inclusive of their regular processing hours, 5 reserved slots during Prime Time II and 5 reserved slots during Off Peak Time.

Date/ Time	Monday	Tuesday	Wednesday	Thursday	Friday	Saturday	Sunday
12AM- 4AM							
4AM-8AM							
8AM- Noon							
Noon-4PM							
4PM-8PM							
8PM – 12AM							

Policies and procedures for EE312 testing

- The remaining slots are to be left unreserved for other lab users.
- A slot can be taken if no one shows up 15 minutes after the sign-up time.
- You are not allowed to sign-up for 2 consecutive sessions.
- No TA support will be provided during nights and weekends.
- A minimum of 2 students should always be present for safety reasons.
- Any damage to the test bench must be promptly reported to Prof. Saraswat or the TAs. Remember, we won't punish you for breaking the setup but will definitely mind if the incident is hidden from us. Please check the test setup before starting your measurements.
- Write any comment if you think it would benefit others or help avoid damage on the testers.

SOME FINAL REMARKS

- There should be no mystery about testing. If you are unsure, ASK!!!
- To make sure you understand the process well, you should be able to:
 - Correlate observed device anomalies with problems in the process test structures.
 - Explain differences between prediction and actual measurement.
 - Explain the consequences of any changes made to the wafers during processing.
- To make sure that you have grasped the *big picture*, you should:
 - Compare measured values with a comparable CMOS process.
 - Relate compromises in device performance with process simplicity.
 - Try to evaluate CIS/CMOS-II from a circuit standpoint.
Is it suitable for VLSI circuits, analog circuits, or neither?
 - Try to offer improvements to process flow without greatly increasing complexity.

☺ *Good luck and have fun!!* ☺