CGRA Configuration & Debug Support

1. 32 bit config address bus
2. 32 bit input data bus
3. 32 bit output data bus

|  |  |  |  |
| --- | --- | --- | --- |
| Control Bits | Address Bits | Data Bits | Action |
| 0 | X | X | NOP |
| 1 | A | D | Write config word D to tile address A |
| 2 | A | X | Read config word from tile address A |
| ~~3~~ | ~~A~~ | ~~D~~ | ~~Set base register to D for burst read/write~~ |
| ~~4~~ | ~~A~~ | ~~D~~ | ~~Set rw bit D[15] and count register to D[14:0] for burst~~ |
| ~~5~~ | ~~X~~ | ~~X~~ | ~~Burst start~~ |
| ~~5~~ | ~~A~~ | ~~D~~ | ~~Write data word D to tile address A~~ |
| ~~6~~ | ~~A~~ | ~~X~~ | ~~Read data word from tile address A~~ |
| 7 | 0 | X | Writes A050 to the JTAG data bus |
| 8 | X | D | Writes data word D to special register TST |
| 9 | X | X | Read special register TST (in GC) |
| 10 | X | D | Global reset (Active high) for D clk cycles |
| ~~11~~ | ~~X~~ | ~~D~~ | ~~Reset tile D[14:0] (Just pass in as is for 1 cycle)~~ |
| 11 | X | D | Write D to stall reg (4 stall signals) |
| 12 | X | X | Read stall reg |
| 13 | A | D | Advance clock by D pulses for stall networks A (one-hot encoding) |
| 14 | X | X | Read Clock Domain (0=tck, 1=sys\_clk) |
| 15 | X | D | Switch to clk D (D=0: tck, D=1: sys\_clk) |
| 16 | X | D | Write D to rd\_delay\_reg (How many cycles until data valid?) |
| 17 | X | X | Read rd\_delay\_reg |
| 18 | X | D | Write D[1:0] to delay select register (chicken bits) |
| 19 | X | X | Read delay select register (chicken bits) |
| 20 | A | D | Write to D to analog control register A |
| 21 | A | X | Read from analog control register A |

# Address Space

Config word represents the configuration state of a tile.

Config address fields are { Reg[31:24], Feature[23:16], TileID[15:0]} Reg being the MSB.

Data address space is different from config address space [details on addressing PE input/output regs and SB regs; memory words to be added]

# ~~Bursts~~

~~Burst read/write modes can be used for programming memory during boot up (LUTs), or during debug to read/write to a memory, or to a PE tile~~

~~Burst mode stalls the fabric clock i.e. CGRA application is stalled while data is read/written to the fabric elements.~~

~~To use burst mode, setup base and count registers as needed. Assert burst start after 10 cycles to start the operation.~~

~~Burst start will read/write “count” registers from base address depending on “rw” bit. rw bit is 0 for read burst, and 1 for write burst.~~

~~Global reset, or setting base/count register resets burst read/write count to 0~~

~~Latency between initiation of two bursts should be 10 cycles~~

# Clock Advance

There are 4 stall signals. For the advance clock operation, we must specify which signals we want to temporarily unstall. This is done using the following encoding. I.e. Each of the 4 least significant address bits corresponds to a stall signal.

Example:

If you send an advance clk operation with the address 1010 and data 6, stall signals 3 and 1 will be deasserted for 6 cycles and then reasserted, provided that they are both 1 at the time the op is sent.

# CGRA bring up

Read from special address {70} to get A050

Write data D to special address {71}

Read from special address 71 to check if D is returned

Program CGRA

Issue global reset

<CGRA should sync to incoming data and start operations, unless a trigger IO is needed in the application>

# CGRA debug

Application can trigger breakpoints causing a stall, or the host can issue a stall command (write to special address {75})

Global reset clears stalls

Once stalled, special address 76 can be used to issue a certain number of clock pulses. CGRA is stalled at the end of D pulses.

~~Burst mode reads/write can be used to read and change memory/PE data/config states when CGRA is stalled. Not all states can be modified.~~

~~To resume normal operation till the next breakpoint (if any), write to special address {77}~~