CGRA Configuration & Debug Support

1. 30 bit config address bus
   1. {29:27} Control bits
   2. {26:0} Tile address bits
2. 16 bit input data bus
3. 16 bit output data bus

|  |  |  |  |
| --- | --- | --- | --- |
| Control Bits | Address Bits | Data Bits | Action |
| 0 | X | X | NOP |
| 1 | A | D | Write config word D to tile address A |
| 2 | A | X | Read config word from tile address A |
| 3 | A | D | Set base register to D for burst read/write |
| 4 | A | D | Set rw bit D[15] and count register to D[14:0] for burst |
| 5 | X | X | Burst start |
| 6 | A | X | Read data word D from tile address |
| 7 | 0 | X | Writes A050 to the data bus |
| 7 | 1 | D | Writes data word D to special register TST |
| 7 | 2 | X | Read special register TST |
| 7 | 3 | X | Global reset |
| 7 | 4 | D | Reset tile D[14:0] |
| 7 | 5 | X | Stall |
| 7 | 6 | D | Advance clock by D pulses |
| 7 | 7 | X | Resume clock |

# Address Space

Config word represents the configuration state of a tile.

Config address fields are {TileID[26:12], Feature[11:8], Reg[7:0]}, TileID being the MSB.

Data address space is different from config address space [details on addressing PE input/output regs and SB regs; memory words to be added]

# Bursts

Burst read/write modes can be used for programming memory during boot up (LUTs), or during debug to read/write to a memory, or to a PE tile

Burst mode stalls the fabric clock i.e. CGRA application is stalled while data is read/written to the fabric elements.

To use burst mode, setup base and count registers as needed. Assert burst start after 10 cycles to start the operation.

Burst start will read/write “count” registers from base address depending on “rw” bit. rw bit is 0 for read burst, and 1 for write burst.

Global reset, or setting base/count register resets burst read/write count to 0

Latency between initiation of two bursts should be 10 cycles

# CGRA bring up

Read from special address {70} to get A050

Write data D to special address {71}

Read from special address 71 to check if D is returned

Program CGRA

Issue global reset

<CGRA should sync to incoming data and start operations, unless a trigger IO is needed in the application>

# CGRA debug

Application can trigger breakpoints causing a stall, or the host can issue a stall command (write to special address {75})

Global reset clears stalls

Once stalled, special address 76 can be used to issue a certain number of clock pulses. CGRA is stalled at the end of D pulses.

Burst mode reads/write can be used to read and change memory/PE data/config states when CGRA is stalled. Not all states can be modified.

To resume normal operation till the next breakpoint (if any), write to special address {77}