



Cortex-M3 DesignStart FPGA-Xilinx edition

(r0p1-00rel0)

Release Note

Cortex-M3 DesignStart FPGA-Xilinx edition Release Note

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Product Status

The information in this document is for a product at Full Release status.

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- The document title
- The document's number
- The page number(s) to which your comments refer
- A concise explanation of your comments

General suggestion for additions and improvements are also welcome.

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Arm Internal Document Reference

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Contents

1	PRODUCT DELIVERABLES	1
1.1	Product Release Status	1
1.2	About Cortex-M3 DesignStart FPGA-Xilinx edition	1
1.3	Arm Part Numbers for this product	1
2	INSTALLATION	2
2.1	Disk space required	2
2.2	Installation procedure for Unix	2
2.2.1	Unpacking the shipment	2
2.3	Installation procedure for Windows	2
2.3.1	Unpacking the shipment	2
2.4	Add the Arm IP library to your Vivado installation	2
2.5	Directory Structure	3
3	TOOLS	3
3.1	Tools	3
3.2	Operating Systems	3
3.3	Standards Compliance	3
4	USAGE NOTES	3
5	KNOWN ISSUES AND LIMITATIONS	4
6	DIFFERENCES FROM PREVIOUS RELEASE	4
7	SUPPORT	4

1 PRODUCT DELIVERABLES

1.1 Product Release Status

These deliverables are being released under the terms of the agreement between Arm and each licensee (the "Agreement"). Use by recipient of the deliverables is subject to the terms and conditions of the Agreement. The release is suitable for volume production under the terms of the Agreement.

1.2 About Cortex-M3 DesignStart FPGA-Xilinx edition

Cortex-M3 DesignStart FPGA-Xilinx edition includes:

- An Arm Cortex-M3 processor, packaged for use in the Xilinx Vivado tool
- Example design for Artix-A7
- Example software for the design examples.

The Cortex-M3 DesignStart FPGA-Xilinx edition package provides an easy way to use the Cortex-M3 processor in the Xilinx Vivado design environment. The Cortex-M3 processor is intended for deeply embedded applications that require a small processor to be integrated into an FPGA. The processor implements the Armv7-M architecture and is designed for ASIC implementation.

An example design flow is provided for use with the Digilent ARTY-A7 evaluation board. You can use this with the optional V2C-DAPLink board from Arm.

1.3 Arm Part Numbers for this product

The Cortex-M3 DesignStart FPGA-Xilinx edition product is delivered as a single zipped tar file through Arm's IP delivery server.

The following table lists the Arm part number for the Cortex-M3 DesignStart FPGA-Xilinx edition product.

Table 1.3-1: Arm part number for Cortex-M3 DesignStart FPGA-Xilinx edition

Product code	Description	Version
AT426-BU-98000	Cortex-M3 DesignStart FPGA-Xilinx edition	r0p1-00rel0

2 INSTALLATION

2.1 Disk space required

This installation will require about 22 Mbytes of free disk space.

2.2 Installation procedure for Unix

You will have a single tar file of the following format e.g.

```
AT426-BU-98000-r0p1-00rel0.tgz
```

The installation procedure is summarized below:

2.2.1 Unpacking the shipment

The following steps describe how to unpack the separate products delivered in this shipment.

1. Relocate the shipment file

Copy the tgz file to the directory where it is to be installed.

2. Extract tar files

Extract the tar file contents using the UNIX GNU tar utility:

```
gtar -zxvf AT426-BU-98000-r0p1-00rel0.tgz
```

NOTE: A version of GNU tar later than 1.13 should be used to untar the deliverables as some versions of tar have problems dealing with very long path names. To find the version of gtar being used type `gtar --version`.

This will extract the deliverables into a directory named the same as the bundle number `AT426-BU-98000-r0p1-00rel0`.

2.3 Installation procedure for Windows

You will have a single tar file of the following format e.g.

```
AT426-BU-98000-r0p1-00rel0.tgz
```

The installation procedure is summarized below:

2.3.1 Unpacking the shipment

Use a tool such as 7-Zip to unpack the tar file. You may need to do this in two stages:

1. Unzip the file to get the file:

```
AT426-BU-98000-r0p1-00rel0.tar
```

2. Extract the contents of this file to a working area.

2.4 Add the Arm IP library to your Vivado installation

After unpacking the deliverables, you must add the library of Arm IP to your Vivado installation. Follow the instructions in the user guide to do this.

The user guide can be found in the bundle, at the following location:

```
AT426-BU-98000-r0p0-00rel0/docs
```

2.5 Directory Structure

Figure 2-1 shows the principal directory structure of this release created after unpacking the bundle and merging the deliverables:

```
AT426-BU-98000-r0p1-00rel0/
├── Arm_Cortex-M3_DesignStart_FPGA-Xilinx_edition_r0p1-00rel0_Release_Note.pdf
├── docs/
├── hardware/
│   ├── M3_for_arty_a7/
│   └── software/
│       ├── flash_downloader
│       ├── M3_for_arty_a7/
│       └── vivado/
│           ├── Arm_ipi_repository/
│           └── Arm_sw_repository/
```

Figure 2-1: Principal directory structure after unpacking the bundle

3 TOOLS

3.1 Tools

This release has been developed with the following tools:

- Xilinx Vivado 2019.1
- Arm Keil Microcontroller Development Kit (MDK) version 5.28.

3.2 Operating Systems

This release has been developed with the following operating system:

- Microsoft Windows 10

3.3 Standards Compliance

This release has been tested with the following standards

- AMBA® 3 AXI Protocol Specification EAC 1 release – ARM IHI 0022F.b

4 USAGE NOTES

For initial product usage, refer to the Arm® Cortex®-M3 DesignStart™ FPGA-Xilinx edition User Guide, ARM 101483.

This can be found in the following directory if the Cortex-M3 DesignStart FPGA-Xilinx edition deliverables have been merged as described in section 0:

```
AT426-BU-98000-r0p1-00rel0/docs
```

Before loading the example design project files into Xilinx Vivado, you must install the packaged IP and the relevant board files, otherwise the example design will be automatically updated where components are not found in the Vivado component library.

5 KNOWN ISSUES AND LIMITATIONS

There are no known issues in this release.

6 DIFFERENCES FROM PREVIOUS RELEASE

The following updates are included from r0p0 to r0p1:

- 1) Example design updated to Vivado version 2019.1.
- 2) **SWV** output pin added to Cortex-M3 component. This provides Serial Wire Output (instrumentation trace) if debug is enabled in the configured core.
- 3) Instruction TCM regions are only written to when the alias region is enabled.
- 4) Exclusive access (LDREX/STREX) can be performed to TCM regions (both instruction and data), but will always return a FAIL response when performed to any address mapped to the AXI interfaces.

7 SUPPORT

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