Akash Poptani

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Publication

SANNA: Secure Acceleration of Neural Network Applications

Accepted at International Conference on VLSI Design (VLSID'23), Hyderabad, India, 2023.

LCM: LLM-focused Hybrid SPM-cache Architecture with Cache Management for Multi-Core AI Accelerators

Submitted at IEEE International Parallel & Distributed Processing Symposium (IPDPS), 2024.

Decoding Drought: Embracing Simplicity in Effective Predictive Models

Submitted at IEEE Asia-Pacific Conference on Geoscience, Electronics and Remote Sensing Technology (AGERS), 2023

Projects and Internship

Research Internships

Hong Kong University of Science and Technology (HKUST) Jun 2023 - Present
Developed a prefetcher architecture for multi-AI core systems using Verilog. Optimized performance by integrating a prefetcher and dead-block predictor using SMAUG and gem5-aladdin tools.
Mentor: Prof. Wei Zhang.

Arizona State University Jun-Aug 2023
Applied Machine Learning to predict static IR drop in Electronic Design Automation.
Mentor: Prof. Vidya A. Chhabria.

Tata Consultancy Services (TCS) Bangalore May-Jun 2023
Enhanced TensorFlow to TensorFlow Lite compatibility for TinyML applications. Gained expertise in TinyML.

IIT Dharwad Apr-Jul 2022
Designed and evaluated Task Scheduling Algorithms for Heterogeneous Secure Systems (HSS) with a focus on securing neural network applications against Hardware Trojans through assisted parallelism.
Mentor: Prof. Rajshekar K.

IIT Ropar Apr-Jul 2022
Explored Replacement Policies and Cache Partitioning techniques. Implemented UCP and Hawkeye Predictor on ChampSim simulator.
Mentor: Prof. Shirshendu Das.

Current Projects

CASH: Criticality-Aware Split Hybrid Cache Dec 2022
Assisted in implementing a Criticality Aware Tiered Cache Hierarchy, encorporating SRAM and STTRAM Technologies. Specialized in optimizing the placement of write-intensive lines to minimize write energy while enhancing performance. Conducted experiments on Branch predictors to fine-tune efficiency.

Design and Development of Runtime Monitor Processors July 2022
Implemented Temporal-Logic Based Runtime Observer Pairs for System Health Management. Developed FSM models using Haskell on the CLASH compiler.

Tejas Architectural Simulator Extension (McPat and Hotspot) Jan 2023
Enhanced Tejas with power and temperature modeling capabilities. Enabled accurate power and temperature tracking during program execution.

Other Projects

Breadboard Calculator Design Digital design implementation of a calculator on a breadboard using RTL model and CMOS logic gates.

Processor Simulators Study Comparative study of passive cooling techniques and familiarity with Sniper, HotSpot, and 3D-ICE simulators.

MIPS Implementation in Verilog Proficiency in digital circuit design, including combinational and sequential circuits using Xilinx tools and assembly code.

Treasure Hunt & Snakes and Ladders Developed Minesweeper and Snakes and Ladders games in C, utilizing binary files and library functions for interactive gaming.

Skills

Programming	VHDL, Verilog, Haskell, CLASH C,C++,Python, Java, MATLAB
Technical	Computer Architecture, Formal Verification, Hardware Security, Digital Design, Arduino, Linux Basics, Data Analysis, Version Controlling
Documentation	LaTeX
Management	Good communication and efficient planning
Tools	Tejas, McPat, Hotspot, SMAUG, gem5-aladdin, ChampSim

Teaching

Teaching Assistant (TA) - CS103 Evaluated student coding proficiency, facilitated group discussions, and conducted code reviews to enhance skills.

Freelance Tutor, Raipur Developed custom materials, assessed progress, and maintained communication with parents.

Subject Matter Expert at Embibe Contributed to content development, categorized questions, and ensured alignment with learning objectives.

Extracurriculars

AI-Based Mental Health Monitoring and Feedback System Sep 2022
Selected for **VLSID Design Contest** at International Conference on VLSI Design, 2024.

Contributed to **Inter IIT Tech Meet 2023 (Student's Academic Conclave)** with a presentation on Task Scheduling algorithms for secure neural network acceleration. Previously involved in **Inter IIT Tech Meet 2022 (Bosch Age and Gender Detection event)** focusing on ML models for Face recognition. Currently engaged in **Inter IIT Tech Meet 2024 (JLR Chiplet Design)** driving innovation in automotive chiplet technology, emphasizing electronic component design, throughput, interconnect technology, and thermal management for enhanced efficiency.

Proactively engaged in various extracurriculars, including facilitating company-institute outreach and coordinating HR conclave activities in Public Relations role. Influenced decisions and judged competitions as a Council Member in the Eunoia Literary Club, mentored peers in the Department Academic Mentorship Programme (DAMP), and coordinated soft skills development in the Rational Eloquence Unit (REU-CDC), provided one-on-one mentoring in the Student Mentorship Programme (SMP). Organized and anchored talks, webinars, and sessions within the Event Management Team (Career Development Cell) to ensure high-quality events. Actively participated in diverse clubs: Robotics, Hardly Human (AI), Code Geass (Coding), Fierce Gallants (Chess), Udghosh (Dramatics), and Sapphire (Dance).