AKASH RAVI BHAT

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EDUCATION

PES University, Bangalore — *Bachelor of Technology*
Branch: Electronics and Communication Engineering🔗

2021 - 2025 **Score: 7.63 CGPA** with recent **8.46 SGPA**

COURSEWORK:

• Analog Circuit Design • Digital VLSI Design • Machine Learning
• Functional and Formal Verification • Hardware Accelerators
• Communication Networks • Digital System Design
• Analog and Digital Testing • Computer Architecture

Branch: Minors in Data Structures And Applications 🔗

2022 - 2023 **Score: 9 CGPA**

COURSEWORK:

Queues, Stacks, Linked List, Trees, Graphs, Heaps, Hashmaps, Set

YTSS PU COLLEGE, YELLAPUR — *PUC* 🔗
STATE 10TH RANK **Score: 98.5%**

GOVERNMENT HIGH SCHOOL, Bisgod— *SSLC* 🔗
STATE 12TH RANK **Score: 98.24%**

SKILLS

Languages: **System Verilog, Verilog HDL, MATLAB, C, System C, C++, Python, RISC-V, SQL**

Tools: **VS CODE, NC VERILOG, XILINX-VIVADO, TANNER EDATOOL, MATLAB, WIRESHARK, LTSPICE SIMULATOR, RIPES RISC-V, INCISIVE, GENUS, INNOVUS, TEMPUS**

ACHIEVEMENTS

-DAC AND MRD SCHOLARSHIPS IN B.TECH

-SPECIALIZATION IN VLSI

-STATE LEVEL INTER UNIVERSITY DEBATE 1ST PRIZE

-KANNADA HACKATHON

-IDEAL STUDENT AWARD FROM PRIMARY TO PUC

-ACHIEVED 20+ MEDALS AND 100+ WINNING CERTIFICATES IN DISTRICT, STATE LEVEL SPORTS AND CULTURAL COMPETITIONS

-STATE LEVEL PICK AND SPEECH 1ST PRIZE ORGANIZED BY KARNATAKA GOVERNMENT

-LAPTOP FROM KARNATAKA GOVERNMENT FOR ACHIEVING 1ST RANK IN SSLC

-NMMS EXAM - DISTRICT 1ST AND STATE 9TH RANK CONDUCTED BY DIRECTORATE OF EDUCATION, DELHI

-COMPUTER EDUCATION CERTIFICATE WITH "A" GRADE CERTIFICATION.

PROJECTS

8 Input Bitonic Sorter Design using INCISIVE, GENUS, INNOVUS and TEMPUS 🔗 *DIGITAL SYSTEM DESIGN*

-Designed 8- and 4-input bitonic sorter using CAE blocks.
-Analyzed Timing, Area, and Power using various tools.
-Achieved code coverage of 99% in CAE blocks and 95% in the 8-input sorter with positive slack time

Design of two-stage operational amplifier using TANNER EDATOOL 🔗 *ANALOG CIRCUIT DESIGN*

-Used Tanner EDA's S-Edit to design the circuit and T-Spice to run simulations, verified parameters like gain of 70dB and ensured stable operation without oscillations.
-The first stage consists of a differential amplifier for high gain and input signal amplification, followed by a current mirror for biasing and a common-source amplifier in the second stage for additional gain.
-A compensation capacitor is connected between the output of the first stage and the input of the second stage to improve stability and bandwidth

Insertion Sort using HLS C++ with Xilinx Vivado🔗 *HARDWARE ACCELERATORS*

-Calculated the number of hardware resources used, such as:
LUTs: Used for combinational logic; **DSPs**: Specialized units for arithmetic operations;
BRAMs: Memory blocks for data storage; **FFs**: Used for storage elements.
- Achieved correct **CP (Critical Path) time** in the implementation report of exported RTL with all timing constraints met after place and route.

Binary converted decimal counter using XILINX-VIVADO 🔗 *DIGITAL VLSI*

-Designed a BCD counter, which counts from 0 to 9 in binary-coded decimal format. When it reaches 9 (1001 in binary), it resets to 0 (0000) and continues counting.
-We did our code in System Verilog . This includes both the main code and testbench code for the simulation.
-The BCD counter was implemented using D flip-flops and simulated using Vivado software

Simulation and FPGA Implementation of FSM of Tic-Tac-Toe game using Xilinx Vivado tool.🔗 *COMPUTER AIDED DIGITAL DESIGN*

-Designed a finite state machine (FSM) on inputs such as 'play', 'illegal_move', 'no_space', and 'win'. we designed a Tic-Tac-Toe game using Xilinx Vivado.
-Simulated the FSM to verify functionality and performance, ensuring accurate representation of game states and transitions.
-Implemented the design on an FPGA.The project targets a Xilinx Artix-7 FPGA, specifically the XC7A35T-1CPG236C.

Configuring email servers and showing end-to-end flow of email between hosts using WIRESHARK🔗 *COMMUNICATION NETWORKS*

- Set up SMTP and IMAP servers to facilitate the sending and receiving of emails between hosts, ensuring proper authentication and encryption.
- Monitored the end-to-end email transmission using Wireshark, capturing packets to analyze the SMTP handshake, message transfer, and retrieval processes.
- Documented the packet flow and headers to illustrate the email lifecycle, highlighting key communication protocols and their roles in successful email delivery.

Mental health detection using PYTHON 🔗 *MACHINE LEARNING*

-Achieved an accuracy of **85%**, indicating that 85 out of 100 predictions were correct when classifying mental health status.
-The precision score was **80%**, reflecting that when the model predicted a positive mental health condition, it was correct 80% of the time.
-These metrics highlight the model's effectiveness in identifying mental health issues while minimizing false positives, crucial for sensitive applications.

Weibull distribution using MATLAB🔗 *ELECTRONICS MATHEMATICS*

-Developed a MATLAB program to simulate and visualize the Weibull distribution, analyzing its shape and scale parameters to model reliability data.
-Conducted statistical analysis to estimate parameters using maximum likelihood estimation (MLE) and fitted the distribution to real-world failure data.
-Generated plots to demonstrate the impact of different parameters on the distribution's behavior, aiding in reliability engineering and life data analysis.

INTERESTS

CHESS, CRICKET, DEBATE, QUIZ, PICK AND SPEECH, BALL BADMINTON, POLITICS, GEOGRAPHY, HISTORY.

COMMUNICATION LANGUAGES

English, Kannada, Hindi.