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Generated by: Genus(TM) Synthesis Solution 17.22-s017\_1

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Module: ASTS

Technology library: tsmc18 1.0

Operating conditions: slow (balanced\_tree)

Wireload mode: enclosed

Area mode: timing library

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Instance Module Cell Count Cell Area Net Area Total Area Wireload

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ASTS 128 3412.886 0.000 3412.886 <none> (D)

(D) = wireload is default in technology library