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Generated by: Genus(TM) Synthesis Solution 17.22-s017\_1

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Module: ASTS

Operating conditions: slow (balanced\_tree)

Wireload mode: enclosed

Area mode: timing library

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Path 1: MET (0 ps) Setup Check with Pin RF\_current\_state\_reg[5]/CK->D

Group: clock

Startpoint: (F) dime\_in

Clock: (R) clock

Endpoint: (R) RF\_current\_state\_reg[5]/D

Clock: (R) clock

Capture Launch

Clock Edge:+ 2000 0

Src Latency:+ 0 0

Net Latency:+ 0 (I) 0 (I)

Arrival:= 2000 0

Setup:- 236

Uncertainty:- 10

Required Time:= 1754

Launch Clock:- 0

Input Delay:- 1000

Data Path:- 754

Slack:= 0

Exceptions/Constraints:

input\_delay 1000 asts.sdc\_4\_line\_5\_5\_1

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# Timing Point Flags Arc Edge Cell Fanout Load Trans Delay Arrival Instance

# (fF) (ps) (ps) (ps) Location

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dime\_in - - F (arrival) 2 16.4 0 0 1000 (-,-)

g4129\_\_1840/Y - B->Y R NOR2X2 8 35.5 384 248 1248 (-,-)

g4122/Y - A->Y F INVX2 12 47.6 212 184 1432 (-,-)

g4026\_\_8757/Y - B0->Y R OAI222XL 1 1.8 497 321 1754 (-,-)

RF\_current\_state\_reg[5]/D <<< - R DFFRHQX1 1 - - 0 1754 (-,-)

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