

# Layout of Low Dropout Regulators (LDO)

**PKP-09** 

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#### **Problem statement**

This project presents layout of LDO optimized for compact area, low parasitics, and DRC/LVS compliance, making well-suited for low-power embedded SoC applications.

## **Objectives**

- Design of high PSRR Low Dropout Regulator.
- Implement and verify both LVS and DRC of LDO.

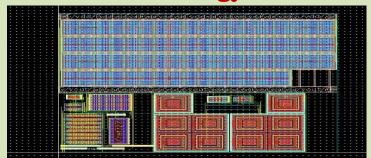
#### **Contributions**

- Full-custom layout of LDO
- Integration of error amplifier, pass transistor, and compensation network
- Post-layout simulation confirming stable output voltage.

### Literature survey

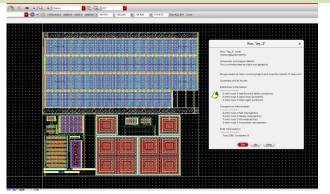
"Design of Low Dropout Voltage Regulator" for Battery Operated Devices" (2019) focuses on an LDO .

## **Methodology**



- 1. Modular Placement: Error amplifier, pass transistor, and compensation circuitry were placed in dedicated blocks to simplify signal routing, improve layout clarity, and enhance analog performance.
- 2. Symmetric Layout & MOS Matching: Critical analog devices, including differential pair MOSFETs in the error amplifier, were laid out using commoncentroid and techniques to minimize mismatch, offset, and systematic variations.
- **3. Power Routing:** VDD/VSS rails were employed to ensure robust power delivery, reduce IR drop.
- **4. Signal Isolation:** High-impedance analog paths and feedback lines were routed away from power and bias lines to prevent coupling and noise injection into sensitive nodes.
- **5. Verification:** Complete physical verification was performed, including DRC and LVS checks, ensuring the layout passed all design rules and achieved accurate netlist matching.

## **Results**



## Optimization details

- Matched MOSFET sizing for precise current control and improved load regulation.
- Layout symmetry applied to differential pairs ensure analog accuracy
- strategic routing to reduce parasitic capacitance and resistance, enhancing PSRR and transient response.

## **Conclusions**

A fully integrated analog Low Dropout (LDO) regulator was successfully designed and implemented. Post-layout simulation results confirm its effectiveness for low-power embedded applications, demonstrating stable voltage regulation, high PSRR, and reliable performance across varying load conditions.

Mini Project-2024-25