# Low Dropout Regulators (LDO) Design

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## Problem statement

Design and Implementation of Low Dropout Voltage Regulator

## Objectives

- Implement 300mV Dropout Voltage with 3.3 V power supply and Load current is 50mA.
- Optimized Load and Line Regulation to maintain a consistent output voltage.
- Improve Power Supply Rejection Ratio (PSRR) to ensure stable operation in noisy environments.

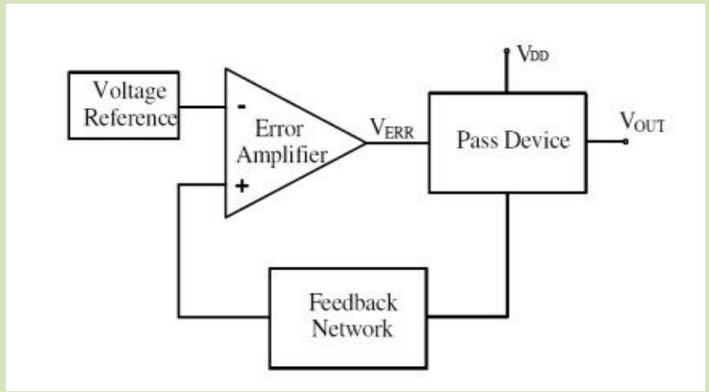
## Contributions

- Designed the Powerfet by setting the Width and Length.
- Optimization of Error Amplifier and Pass Transistor to achieve low dropout and high PSRR

## Literature survey

- "Design of a Low-Dropout Linear Regulator" (2020) discusses an efficient and stable LDO regulator.
- "Design of Low Dropout Voltage Regulator for Battery Operated Devices" (2019) focuses on an LDO optimized for battery-powered applications

## Methodology




**1. Design of Error Amplifier :**

Designed the Two Stage Amplifier (7-Pack) for 330nm technology and 3.3V Powersupply.

**2. Design of Pass transistor :**

Pass transistor is also designed for 330nm technology ,3.3V Powersupply and it supplies 50mA load current to the output with 300mV dropout Voltage.

**3. Design Bandgap Reference :**

BGR will supply the 1.2V to the Inverting terminal of Error Amp.

**4. Compensation :**

Miller Compensation.

Dominant pole Compensation.

## Results

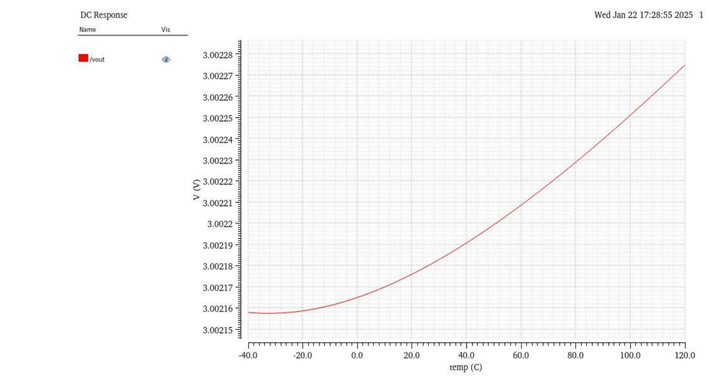



Fig 1 : Vout v/s Temp

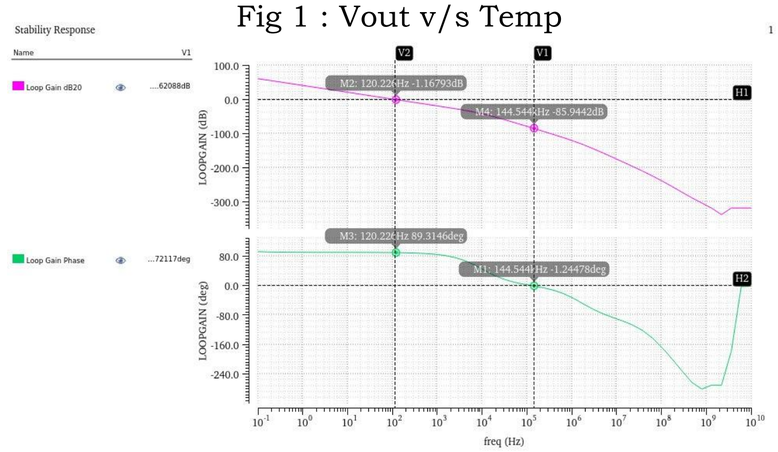



Fig 2 : Stability Analysis

## Conclusions

The designed LDO has a DC gain of 85dB with a phase margin of 89° for the load current of 50mA. The results are verified for the temp. variations from -40 to 125 degree Celsius. The fast transient compensation is demonstrated with a current mirroring technique using a capacitor of 80nF.