Design and Layout of High PSRR LDO Regulator in 0.33µm Technology

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***Abstract*—This paper introduces the circuit design and layout of high PSRR low dropout (LDO) voltage regulator specifically designed for memory systems and high-load current applications. Designed in UMC 330nm CMOS technology and simulated by Cadence Virtuoso, the LDO provides a stable output voltage of 3V from an input voltage of 3.3V with a dropout voltage of 300mV and up to 50mA load current support. The design emphasizes fast transient response, low output noise, and short-circuit protection, making it extremely well-suited for power-aware memory applications. Helpful with the support of a 3µF load capacitance, the regulator provides stable performance with varying loads while maintaining high power efficiency. The total layout is 53,648.37 units square in size and has already undergone both DRC and LVS verification checks successfully, determining the manufacturability and functional accuracy of the design.**

***Index Terms*—Low Dropout Voltage Regulator (LDO), High PSRR, CMOS 0.33µm Technology, Bandgap Reference(BGR),Error Amplifier(EA), DRC/LVS Verification.**

I. Introduction

Low Dropout (LDO) voltage regulators play a critical role in today's low-power and battery-powered electronic systems with a high-quality output voltage having low dropout. Dropout voltage, which is the smallest voltage across the pass element at which regulation can be maintained, is important for effective operation in circuits where the voltages are constrained. With integrated circuits shrinking and being operated at reduced voltages, LDOs have emerged as a solution of choice for on-chip power management.

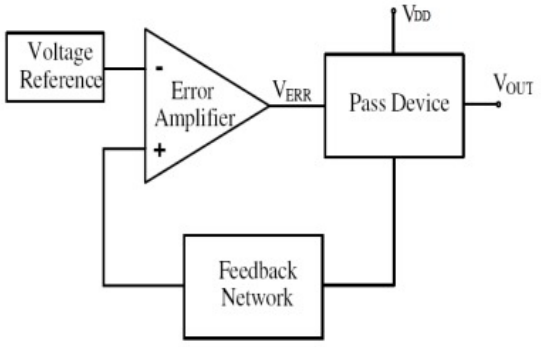

Fig. 1. Basic block diagram of a Low Dropout (LDO) voltage regulator

The minimum configuration of an LDO, depicted in Fig.1, consists of a voltage reference, an error amplifier, a pass device (a PMOS transistor in most cases), and a feedback network. The voltage reference gives a stable input at the inverting input of the error amplifier. The non-inverting input is fed a portion of the output voltage by the feedback network. The error amplifier compares the two voltages and gives a control signal (V_{ERR}) that drives the gate of the pass device. This control loop keeps the output voltage stable and equal to the reference voltage for changing load conditions. In steady-state operation, the pass transistor is controlled by the error amplifier for output regulation. In full load, current is established through the load and the feedback network. Instantaneous switching of the load demands the pass device to respond rapidly, and this forms the transient response of the LDO. A 1µF to 100µF external capacitor is commonly connected at the output for a rapid response and stability. This topology utilizes a two-stage

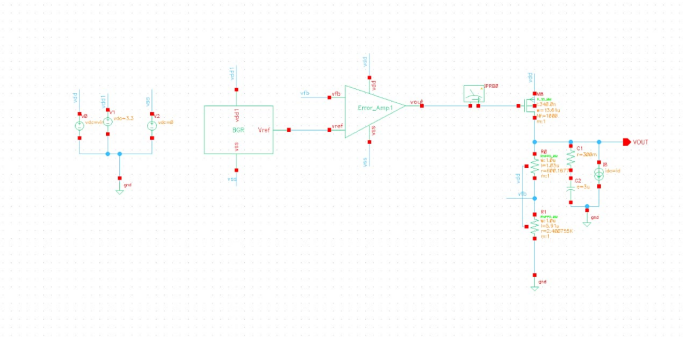

Fig. 2. Complete Symbol of LDO

differential amplifier as an error amplifier for gain boosting, improved PSRR, and fast transient response. The circuit was designed and verified in UMC 330nm CMOS technology and validated by Cadence Virtuoso simulations.The implemented LDO provides a 3V stable output from an input voltage of 3.3V, a maximum load current of 50mA with a 3µF output capacitor, and stable operation in dynamic loads.

II. Voltage Reference Circuit - BGR

A Bandgap Reference (BGR) circuit is a fundamental building block of Low Dropout (LDO) voltage regulators as it generates a stable reference voltage that is highly insensitive to supply and temperature changes. The reference voltage must

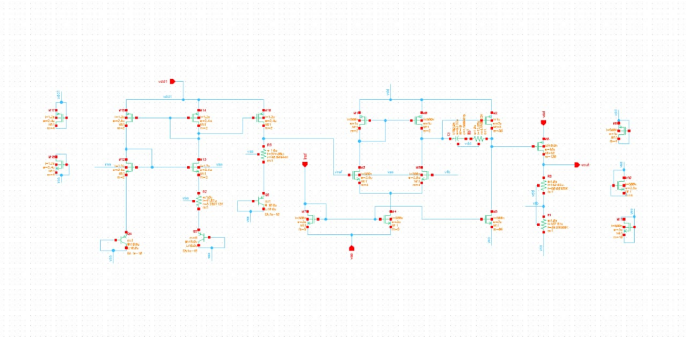

Fig. 3. Schematic diagram of LDO

keep the LDO output steady under varying input and load conditions. The reference voltage stability will have a direct impact on the accuracy, reliability, and overall performance of the regulator.

The BGR circuit takes advantage of semiconductor junction's absolute-temperature-dependent characteristic, that is, the voltage difference between two bipolar junction transistors (BJTs) at two different current densities. This is utilized to produce a voltage component proportional to absolute temperature (PTAT), which is added to a complementary-to-absolute-temperature (CTAT) voltage—typically the base-emitter voltage of a forward-biased BJT—to produce a temperature-compensated reference voltage. The output voltage is close to the silicon bandgap (1.12V) and is very stable over a very large temperature range.

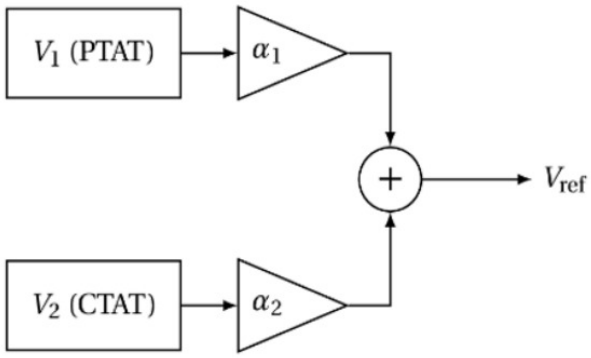

Fig. 4. Building blocks of BGR

As indicated by Fig.2, the Bandgap Reference (BGR) circuit reference voltage is achieved by combining PTAT and CTAT components, either as series voltages or parallel currents, to render the circuit temperature-independent. The most apparent performance parameter is the temperature coefficient (TC), while other noteworthy parameters are PSRR, process variation tolerance, and low power.

III. Proposed Design of BGR

A. CTAT Characteristics

The diode current equation is written as:

$$I_0 = I_S \cdot e^{V_D/V_T} \tag{1}$$

where I_S is the saturation current, V_0 is the applied voltage and V_T is the thermal voltage.

By re-arranging, diode voltage can be expressed as:

$$V_D = V_T \ln\left(\frac{I_0}{I_S}\right) \tag{2}$$

The Reverse saturation current is temperature dependent as indicated below:

$$I_S \propto \mu \cdot k \cdot T \cdot n_i^2$$

Its diode voltage temperature coefficient is its CTAT (Complementary To Absolute Temperature) characteristic:

$$\frac{\partial V_D}{\partial T} = \frac{V_D - (4+m)V_T - \frac{E_g}{q}}{T} \tag{3}$$

where E_g is the bandgap energy of silicon, and m is the temperature coefficient of mobility. By utilizing this temperature dependence, a PTAT current or voltage can be generated by combining diodes operated at varying current densities.

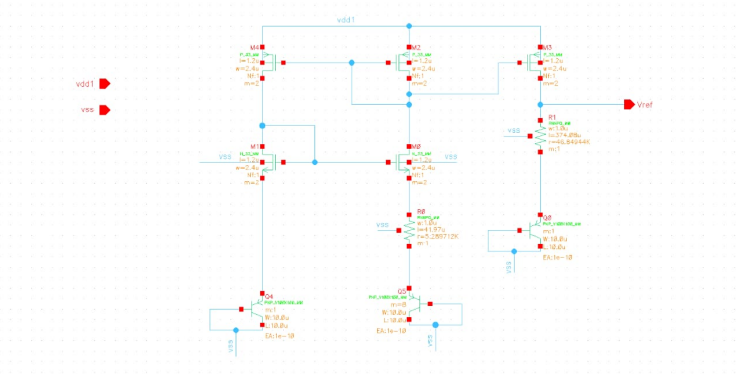

Fig. 5. Schematic diagram of BGR

B. PTAT Characteristics

Following a bipolar junction transistor (BJT), the voltage and current relationship is expressed as:

$$I_0 R = V_0 - V_{D1} = V_T ln(n) \tag{4}$$

the thermal voltage is represented by:

$$V_T = \frac{kT}{q}$$

The PTAT voltage generated across resistors is:

$$V_{R2} = \frac{R_2}{R_1} \cdot \ln(n) \cdot V_T \tag{5}$$

C. Vref Characteristics

The term PTAT and the term CTAT together form the bandgap reference voltage.

$$V_{ref} = \alpha_1(PTAT) + \alpha_2(CTAT) \tag{6}$$

Otherwise,

$$V_{ref} = \alpha_1 V_T + \alpha_2 V_b$$

For a typical bandgap reference, this means:

$$V_{\text{ref}} = 1.189 \text{ V} \approx 1.2 \text{ V}.$$

Since:

$$R_1 I_0 = V_T ln(N) for N = 8$$

with resistor values:

$$R_1 = 5.2 \ k\Omega, \qquad R_2 = 46.8 \ k\Omega.$$

IV. Error amplifier

The error amplifier in a Low Dropout (LDO) regulator is an essential analog block whose function is to provide for the stability of the output voltage Vout at some desired level. It does this by comparing a scaled output voltage (through a resistive feedback divider) with a well-defined reference voltage Vref, normally supplied through a bandgap reference.

The error amplifier produces an error voltage proportional to the difference between Vfb and Vref as follows:

Error Amplifier Output Voltage

$$V_{\text{ERR}} = A_{\text{EA}}(V_{\text{REF}} - V_{\text{FB}}) \tag{7}$$

Where:

- V_{ERR}: Error signal generated by the amplifier
- A_{EA}: Gain of the error amplifier
- V_{REF}: Reference voltage (usually from bandgap)
- V_{FB}: Feedback voltage

Feedback Voltage via Resistor Divider

$$V_{\text{FB}} = \frac{R_2}{R_1 + R_2} V_{\text{OUT}} \tag{8}$$

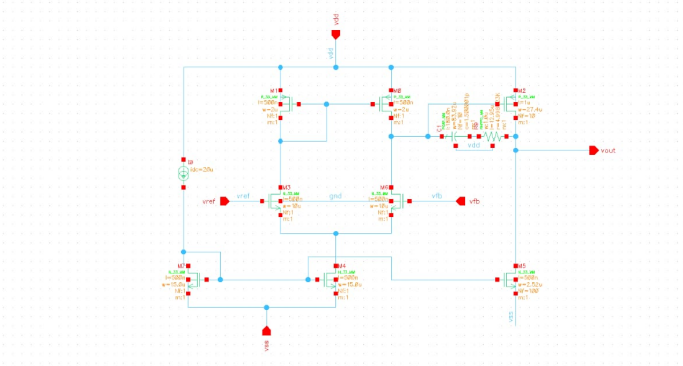

Fig. 6. Schematic diagram of Error Amplifier

This error voltage Verr controls the gate of the pass transistor, typically a PMOS device, varying its conductance to control the Vout . In most LDO circuits, a PMOS is utilized as the pass device because of its low dropout behavior when the source is connected to Vin. The drain is at Vout, and the gate is supplied by the error amplifier.

The drain current Id through the PMOS in saturation (which is generally true during regulation) is provided by:

PMOS Drain Current (Expanded Form)

$$I_D = \frac{1}{2}\mu_p C_{\text{ox}} \frac{W}{L}(V_{\text{IN}} - V_G - |V_{THP}|)^2 \tag{9}$$

In order to stabilize the output, the LDO is a negative feedback system:

Output Voltage in Terms of Feedback Divider

$$V_{\text{OUT}} = V_{\text{REF}} \left(1 + \frac{R_1}{R_2}\right) \tag{10}$$

Such a condition is sustained by dynamically regulating the pass transistor's resistance by the error amplifier. Any variation in Vout because of load or line changes makes Vfb vary, which the error amplifier detects and offsets by changing VG, thereby controlling current through the PMOS and restoring Vout to the desired level.

V. PASSFET

The pass element, or passFET, is in an LDO regulator an extremely important part that is tasked with controlling current flow from input to output at a low dropout voltage. It is normally constructed with a PMOS or NMOS transistor, although the PMOS is more prevalent in conventional LDO design because of its simplicity in referencing the gate drive to ground. In a PMOS-based LDO, the source of the PMOS is connected to the input voltage (VDD), and the drain is connected to the output (VOUT). The gate of the passFET is controlled by the error amplifier, which compares the feedback voltage (VFB) with a reference voltage (VREF), and adjusts the gate voltage (VG) accordingly to maintain regulation. The PMOS usually runs in the saturation region, and its drain current (ID) is described by the typical MOSFET saturation current equation:

ID = (1/2) × upCox(W/L)(VSG - (VTHP))^2

where VSG is the source-to-gate voltage (VDD VG), and VTHP is the PMOS transistor threshold voltage. The error amplifier makes the gate voltage adjustable so that VOUT is maintained in a stable condition, even with variations in input voltage or load conditions. The secret to low dropout operation is to keep the voltage difference VDO = VIN VOUT as low as possible, which is most directly related to the overdrive voltage (VSG —VTHP—). The passFET needs to be sized correctly in order to supply the intended output load current (ILOAD). With the above equation, the W/L ratio required can be found such that the PMOS will be able to supply at least the maximum anticipated ILOAD. For instance, by substituting

known values of up, Cox, VIN, VOUT, and VTHP, one can solve for VSG and calculate the W/L required to achieve the desired drain current. Therefore, the passFET acts as the primary control valve of the LDO, dynamically varying current conduction to control output voltage, and its efficiency plays a crucial role in setting the dropout voltage, transient response, and current-handling capability of the regulator.

VI. LAYOUT IMPLEMENTATION

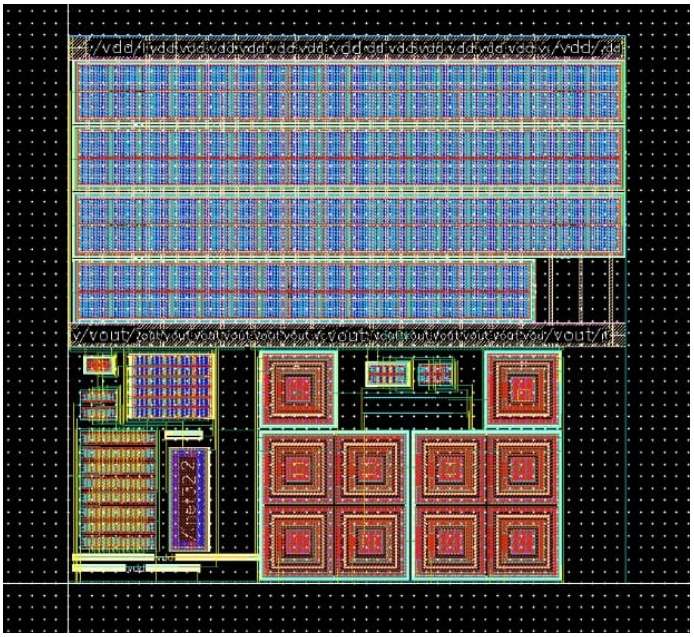

Fig. 7. Complete Layout of LDO

Above figure shows the post-layout implementation of the developed Low Dropout (LDO) Voltage Regulator on the Cadence Virtuoso Layout Suite. The layout follows conventional analog layout methods, ensuring proper matching, symmetry, and negligible parasitic interference. The design is overall oriented to performance optimization, layout minimization, and process reliability.

The top part of the layout has the PMOS pass transistor array, which is responsible for controlling the output voltage. The transistors are routed using uniform geometry and with low routing resistance to achieve good current drive and low dropout voltage.

The lower-left area contains the error amplifier and the bias generation circuits, implemented with common-centroid and interdigitated topologies to enhance device matching and minimize offset. A reference voltage generator positioned at the center area offers a stable bias input to the amplifier and guarantees accurate performance over different process-voltage-temperature (PVT) conditions.

Metal routing is carefully done with several metal layers to efficiently route VDD, VOUT, VREF, and ground signals with minimal parasitic capacitance and resistance. Pad structures and ESD protection are incorporated on the periphery.

The design has properly undergone Design Rule Check (DRC) and Layout Versus Schematic (LVS) checks with no violations, indicating its adherence to the design rules and functional similarity to the schematic. This leaves the physical design ready for parasitic extraction and post-layout simulation.

VII. RESULTS

A. Performance Summary

TABLE I
PERFORMANCE SUMMARY OF THE LDO

Properties	Results
Output Voltage	3V
Input Voltage	3.3V
Reference Voltage	1.2V
Dropout Voltage	300mV
Load Current	50mA
Loop Gain	65.58dB
Gain Margin	28.08dB
Phase Margin	53.78deg
Unity Gain Bandwidth (UGB)	2.78 MHz
Slew Rate	21.78 µs

B. LOOPGAIN

Loop gain and phase margin are critical parameters in analyzing the stability and performance of a Low Dropout (LDO) regulator. Loop gain refers to the product of the open-loop gain and feedback factor, which determines how effectively the regulator maintains a steady output voltage. Higher loop gain improves regulation accuracy but may impact stability if not properly compensated. Above graph shows that gain of 65.58 dB and phase margin of 53.78 degree with the unity band width of 2.78 Mhz.

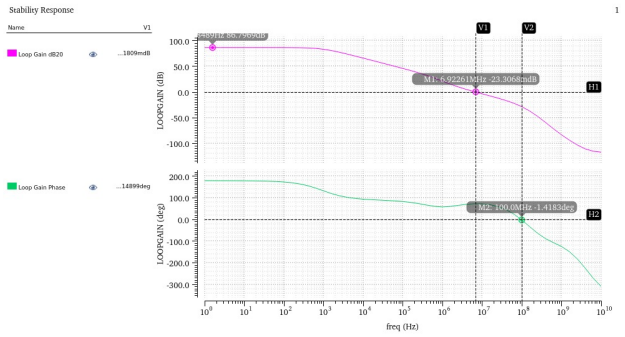

Fig. 8. Loopgain

C. PSRR

PSSR tells about ability of the device to maintain stable output voltage or signal amplitude in the power supply. Above figure shows PSSR of ldo. PSRR stands for Power Supply Rejection Ratio. It is an essential parameter for LDO regulators; that is, it indicates one's ability to suppress variations in the input supply voltage and ensure that the output voltage is less affected by them. PSRR is usually measured in decibels, with

a frequency dependency. Therefore, for a high PSRR, it can be said that an LDO effectively filters noise and ripples in the power supply.

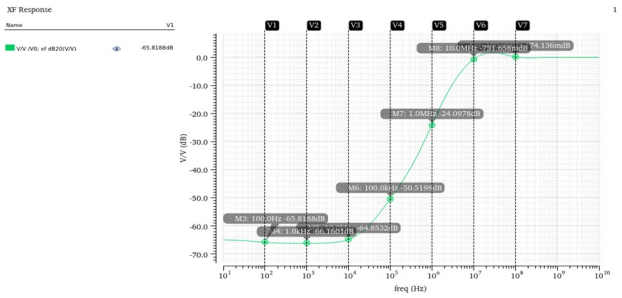

Fig. 9. PSRR

D. LINE REGULATION and LOAD REGULATION

A primary performance parameter of an LDO regulator is the line regulation and load regulation to maintain the output voltage in the event of fluctuating input voltages and changing loads. Line regulation describes how much an LDO changes the output voltage as a function of input supply. It can be described by the change in output voltage per unit change in input voltage.

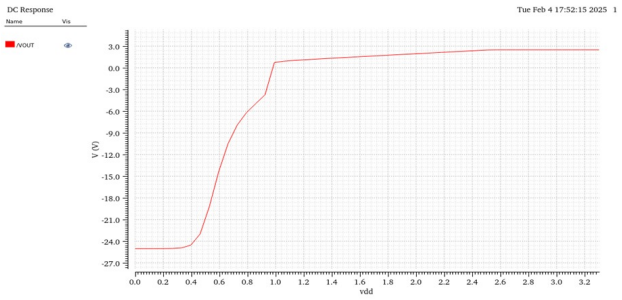

Fig. 10. Line Regulation

Load regulation is an LDO's ability to ensure a constant output voltage despite changes in the value of the current drawn by the load. It refers to the derivative of output with respect to its load current.

VIII. CONCLUSION

The topology of a Low Dropout (LDO) voltage regulator exhibits its ability to deliver stable and efficient output voltage with low dropout, which is appropriate for low-voltage and noise-critical applications. Main components like error amplifier, pass element (in most cases a PMOS transistor), and a precision bandgap reference all collaborate to provide tight voltage regulation for changing input and load conditions. The strong loop gain and adequate error amplifier compensation provide good phase and gain margins, which enable fast transient response and system stability.

Utilization of an optimized feedback loop and optimally selected output capacitor improves the LDO's performance when it comes to load regulation and power supply rejection ratio (PSRR). Simulation results validate that the design complies with requirements for output accuracy, dropout voltage, bandwidth, and dynamic performance. Due to such features, the LDO is ideal for applications such as battery-powered systems and analog circuits where low noise and consistent voltage regulation are paramount.

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