PROJECT REPORT

Course Name: Active Filters
Course Code: EC447

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Submitted to
Professor Laxminidhi T

Problem Statement:

Design a Transconductance-C (Gm-C) low pass filter in 0.35 µm CMOS Technoogy node from TSMC using LTSpice Circuit Simulator (or any other suitable circuit simulator) for the given specifications.

Broad Expectations:

1. Realizing ideal Gm-C filter
   a) Ideal filter using RLC circuits which meets the given specifications
   b) Ideal Gm-C filter for the specifications using the macromodel for Gm
2. Designing the transconductor in 0.35 µm CMOS technology node from TSMC and validating its use as a Gm-C integrator. The capacitor calculated to be used in the first node of the filter may be used as the integrating capacitor for testing the Gm-C integrator.
3. Realize the transistor level Gm-C filter for the given specification.

General Specifications:

1. Fourth order Maximally flat response
2. Power supply 3.3 V
3. Use length of 0.5 µm for all transistors
4. Use even number of fingers for the transistors.

Transconductor Specifications:

1. Gm = 1 mS
2. Gate overdrive for input transistors = 200 mV
3. Input/output common-mode voltage = 1.65 V

Filter Specifications:

1. Attenuation at pass band edge = 0.5 dB
2. Band-edge= 70 Mhz

Theory: A maximally flat filter as the name suggests offers a flat magnitude response in the passband as compared to any other filter realized using the same order. The general expression for the magnitude response of an all pole low pass filter is given by:

$$|T_n(j\omega)|^2 = \frac{1}{1+|K_n(j\omega)|^2}$$

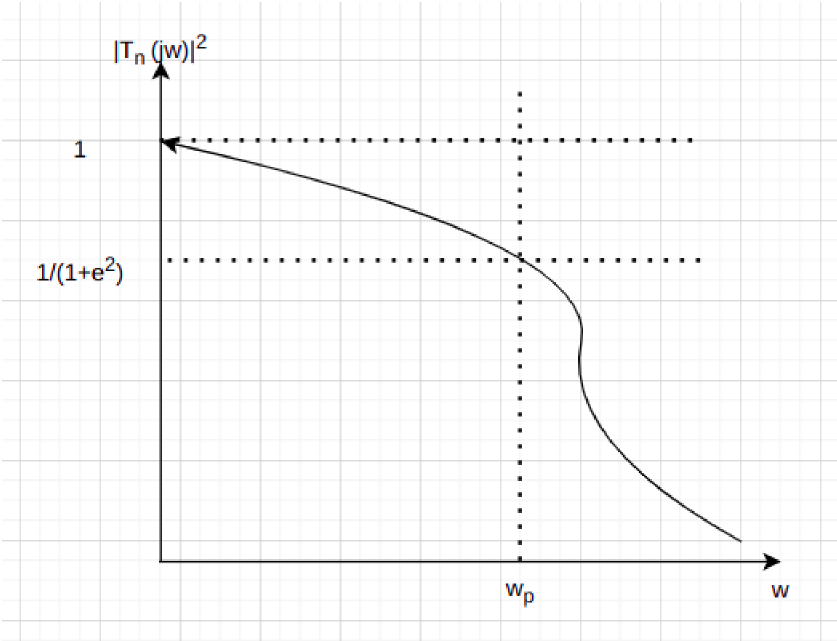
where,

$$|K_n(j\omega)|^2 = B_1\omega^2 + B_2\omega^4 + \ldots + B_n\omega^{2n}$$

for a prototype filter. n here represents the order of the filter. Mathematically, flatness of a function at a point is defined as the first and higher order derivatives of the function being equal to zero at that point. The greater the number of derivatives equal to zero, the more is the flatness of the function. We wish to make the polynomial $K_n^2(\omega)$ maximally flat at $\omega=0$ which would give maximal flatness for $|T_n(j\omega)|^2$ also at $\omega=0$. Since all the derivatives if equated to zero gives a zero polynomial, we make the first (n-1) derivatives of $K_n^2(\omega)$ with respect to ω^2 equal to zero. This gives us the result:

$$|K_n(j\omega)|^2 \;=\; B_n \omega^{2n}$$

The magnitude response curve of a general low pass filter is shown below:



Thus, it can be observed that at the passband edge (ω_p = 1 rad/sec),

$$|T_n(j\omega)|^2 \;=\; \frac{1}{1+\epsilon^2}$$

from which it can be shown that $K_n^2(\omega) = \epsilon^2$. This in turn implies that $B_n = \epsilon^2$..

$$\Rightarrow |K_n(j\omega)|^2 \;=\; \epsilon^2 \omega^{2n}$$

$$\Rightarrow |T_n(j\omega)|^2 \;=\; \frac{1}{1 \;+\; \epsilon^2 \omega^{2n}}$$

The special case of $\epsilon = 1$ is known as a Butterworth filter. Attenuation can be written as the inverse of gain and in dB scale we can write the attenuation as shown below:

$$\alpha_{dB} \;=\; 10 \log\left(1 \;+\; \epsilon^2 \omega^{2n}\right)$$

From the above formulas, it is implicitt that a Butterworth filter offers a gain of -3 dB at its passband edge. A maximally flat filter can be viewed as a Butterworth filter at some other passband frequency. The expression for this passband edge can be found by equating the magnitude responses of a maximally flat and Butterworth filter and is given below:

$$\omega_{p,B} \;= \omega_{p,MF}\, \epsilon^{\frac{-1}{n}}$$

Thus, once we find the values of ϵ and n, we transform the maximally flat filter to a Butterworth filter and then design the Butterworth filter. This is done since the design procedure for a Butterworth filter is standardized and tables are available with numerical values that can be used to quickly design the filter.

Once we have the magnitude response, we must find the pole locations of the filter. This can be done using the relation:

$$|T_n(j\omega)|^2 = T_n(j\omega)T_n(-j\omega) = T_n(s)T_n(-s) \, at \, s = j\omega$$

$$\Rightarrow T_n(s)T_n(-s) = |T_n(j\omega)|^2 \, at \, \omega = \frac{s}{j}$$

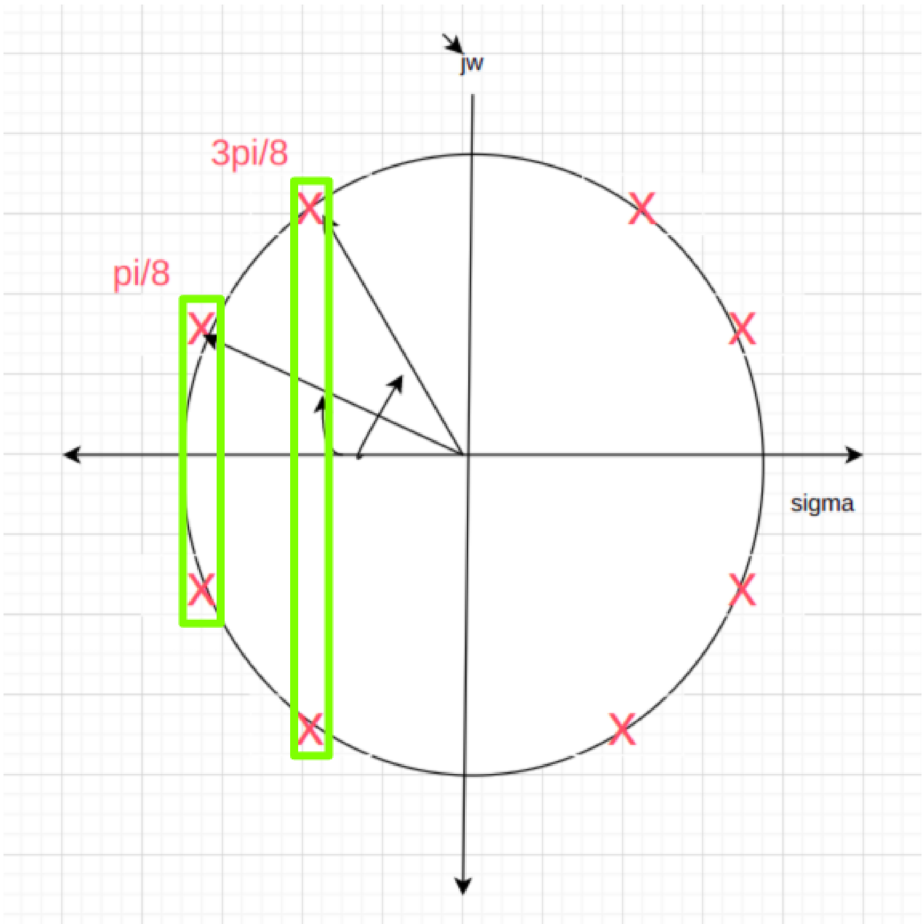
Thus, for a fourth order Butterworth filter that we are required to design,

$$T_4(s)T_4(-s) = \frac{1}{1+s^8}$$

The pole locations of the above transfer function are given by:

$$s = e^{j(2k+1)\frac{\pi}{8}} \qquad for \, k=0,1,2,\ldots,7$$

The poles of the fourth order Butterworth filter thus lie on a unit circle and have been plotted as shown below:



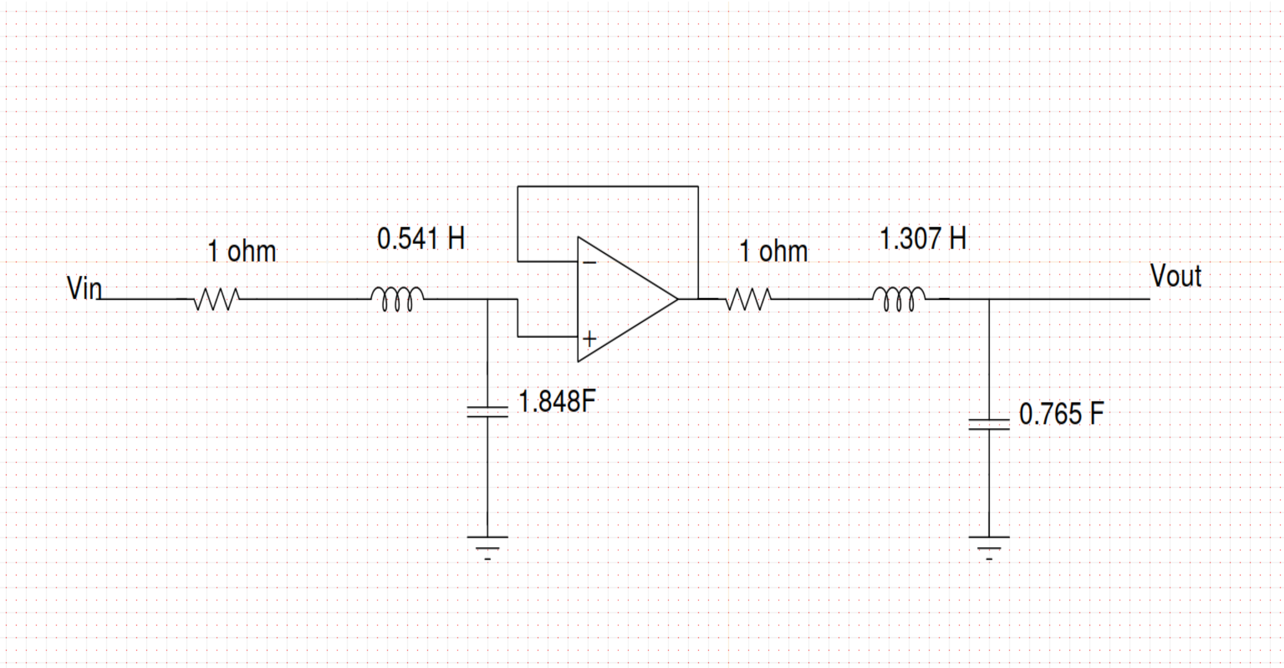
To ensire stability, we take the oles on the left half of the s plane to be the poles of $T_4(s)$. As shown in the above figure, the fourth order Butterworth filter can be realized using two second order sections each with passband edge of 1 rad/sec. The quality factor of a second order circuit from its pole locations on the unit circle are given by:

$$Q = \frac{1}{2\cos\psi}$$

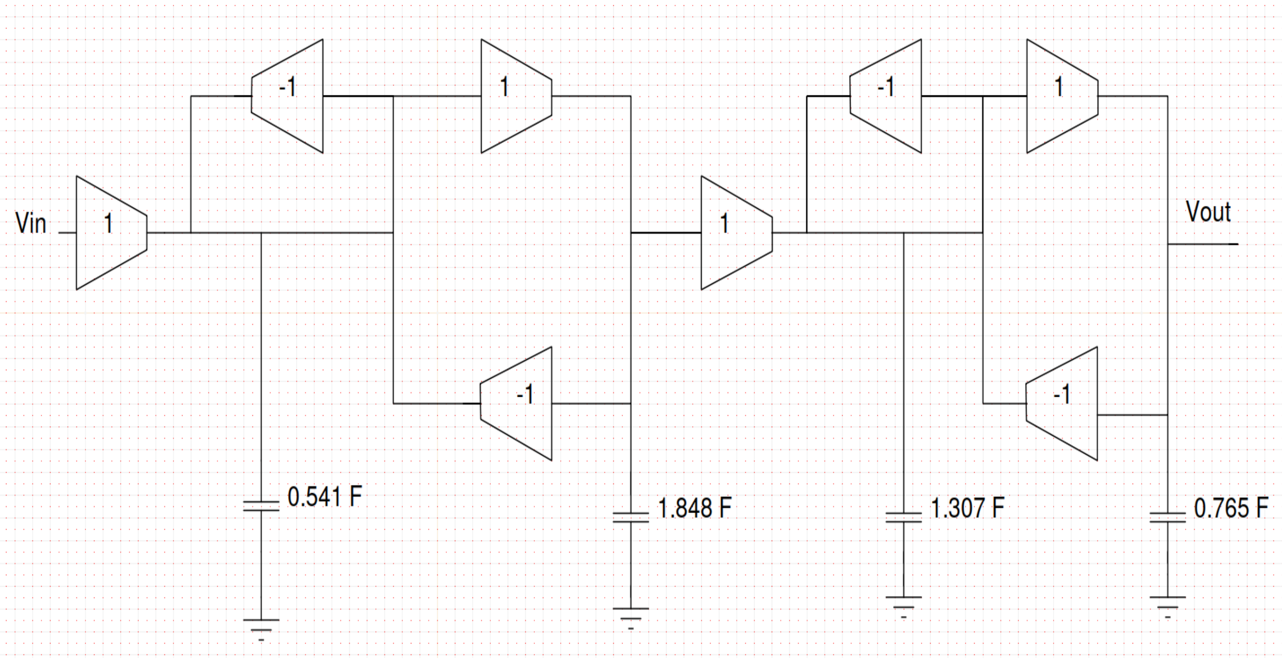
where ψ is the angle made with the negative real axis by the two complex conjugate poles. From the above relation, the quality factors of the two second order filters can be shown to be $Q_1 = 0.541$ and $Q_2 = 1.307$. The transfer function of the fourth order filter is thus given by:

$$T_4(s) = \frac{1}{(s^2+1.848\,s+1)(s^2+0.765\,s+1)}$$

A second low pass filter can be realized using a series RLC circuit where output is taken across the capacitor. For a prototype filter, we normally choose R = 1 Ω, L = Q H and C = 1/Q F. By cascading two low pass filters with a buffer realizing using opamp to avoid the loading effect, the fourth order Butterworth filter shown above can be realized. The RLC circuit for the same is as shown below:



In order to arrive at the Gm – C equivalent, we normally start off with a band pass filter and realize the inductor and resistor using transconductors. This is done since converting the above circuit directly to its Gm – C equivalent produces a non-integrating node at the terminal between the resistor and the floating inductor and the parasitic capacitances cannot be absorbed. The bandpass equivalent has no non-integrating node and thus, the parasitic capacitances can be absorbed into the integrating caacitors. Thus, the order of the circuit remains the same and we also obtain a more exact version of the desired response. The output of the gyrator used to realize the inductor is then a low pass node. The Gm – C equivalent of the above circuit is shown below. We also note that the section with a lower quality factors have been placed and then followed by sections with high quality factors. This is done since higher quality factors have gains greater than one in their magnitude response and if placed early on in the cicuit, they will amplify the non-linear distortions to a higher extent.



Design:

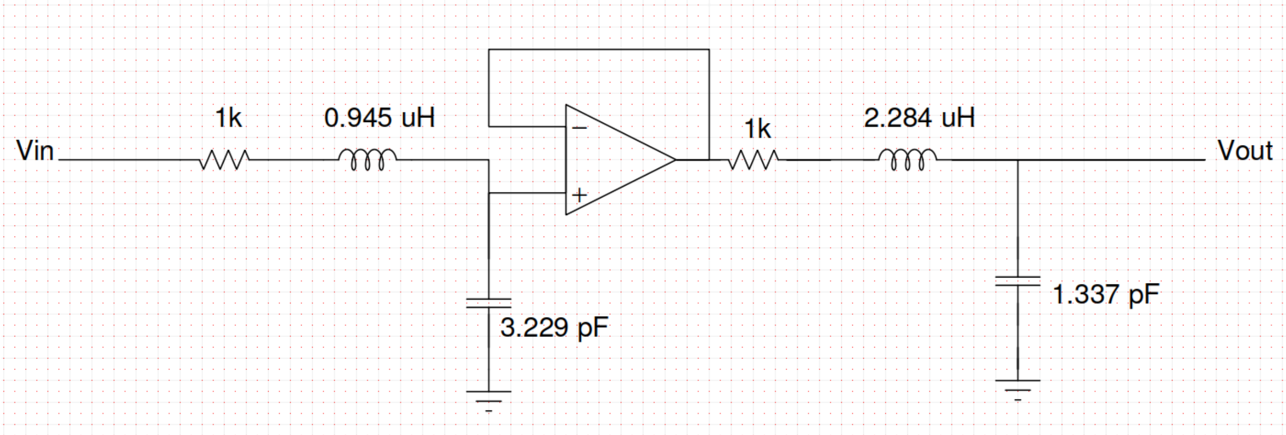
We are told that the attenuation at the passband edge must be -0.5 dB. Applying the formula for attenuation for a prototype (ω_p = 1 rad/sec),

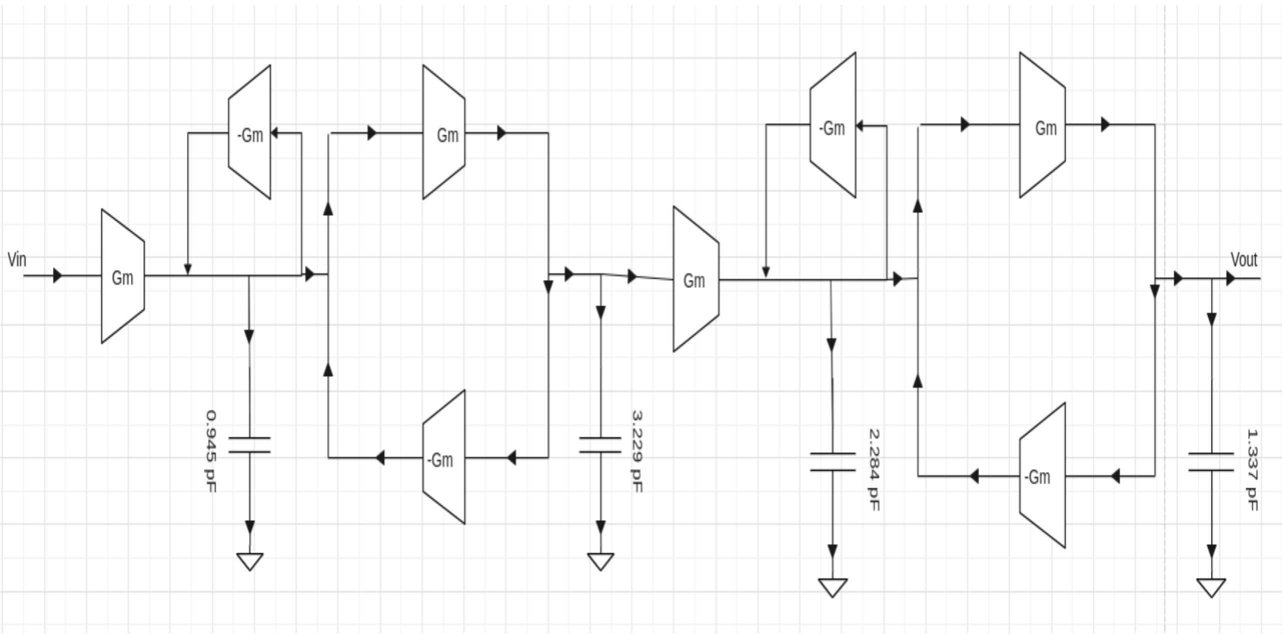
$$0.5 \;=\; 10\log(1+\epsilon^2) \;\Rightarrow\; \epsilon \;=\; 0.349$$

The passband edge for the maximally flat filter is given to be 70 Mhz. Since we are realizing a fourth order filter, n = 4. Thus, to convert the maximally flat filter to a Butterworth filter, we find the passband edge for the Butterworth filter using the formula told earlier.

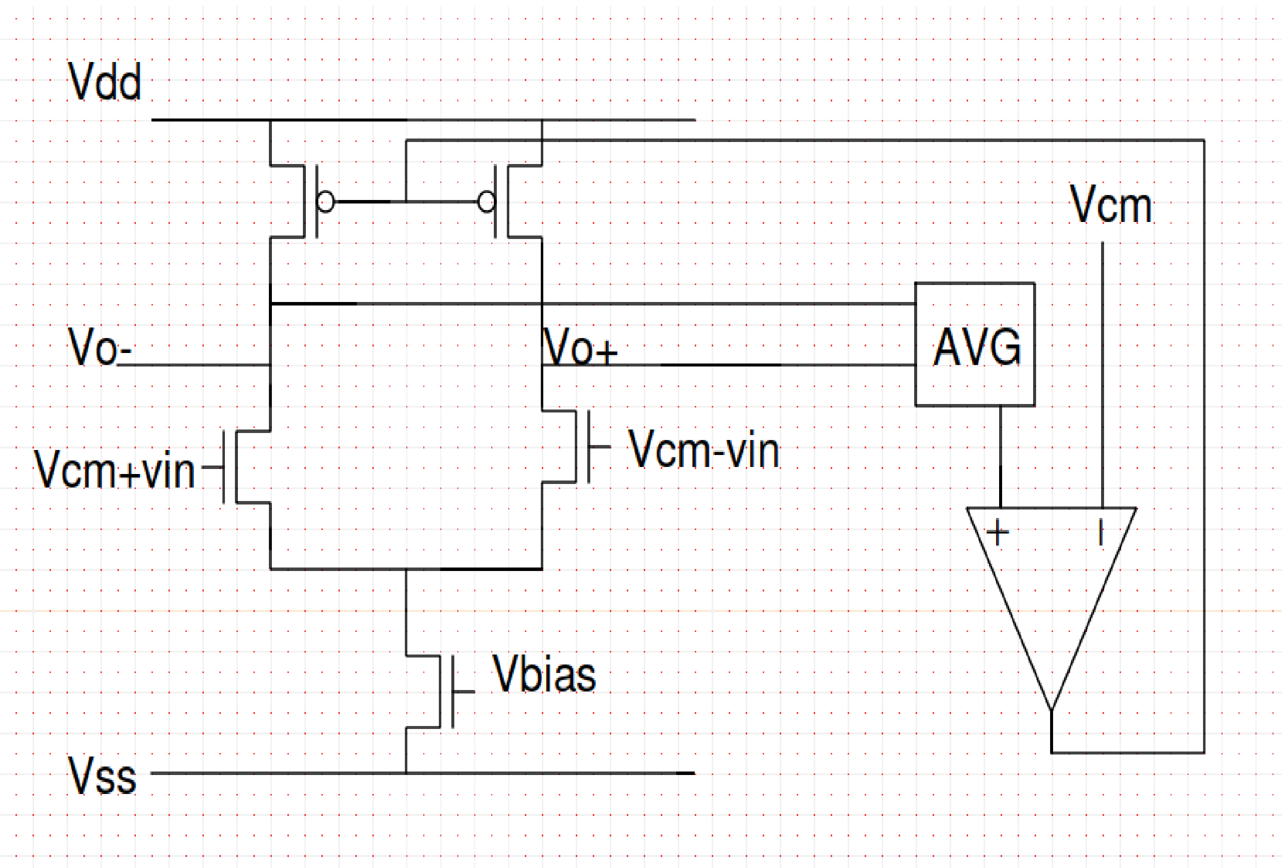
$$\omega_{p,BF} \;=\; (2\pi*70)*(0.349)^{\left(\frac{-1}{4}\right)} \;\Rightarrow\; \omega_{p,BF} \;=\; 572.231\,Mrad/sec \;=\; 91.07\,MHz$$

Thus, we need to design a fourth order Butterworth filter with a passband edge of 572.231 Mrad/sec. Earlier, we have designed a prototype Butterworth fourth order filter with a passband edge of 1 rad/sec. Thus, we just need to frequency scale the circuit. Further the impedance level of the prototype is 1Ω. Since the Gm value that we need to realize is 1mS, we also need to impedance scale the circuit to a resistance value of 1kΩ. The final RLC and Gm-C circuits after performing frequency and impedance scaling is as shown below:





To design the transconductor, a common source differential pair was used with NMOS transistors as input transistors and PMOS transistors as the load transistors. Common mode feedback was implemented to ensure that the output common mode voltage is same as the input common mode voltage. This is essential for proper operation of the circuit since the output of one transconductor is given as input to the next transconductor. The basic configuration of the transconductors is as shown below:



We need to set the width of the transistors and the drain current so that the correct transconductance (gm) is achieved. Simultaneously, specification is also given for the gate overdrive voltage Vdsat. The following expressions are used to achieve the required gm and Vdsat:

$$gm = \sqrt{2KI_D}$$

$$I_D = \frac{K}{2}(Vdsat)^2$$

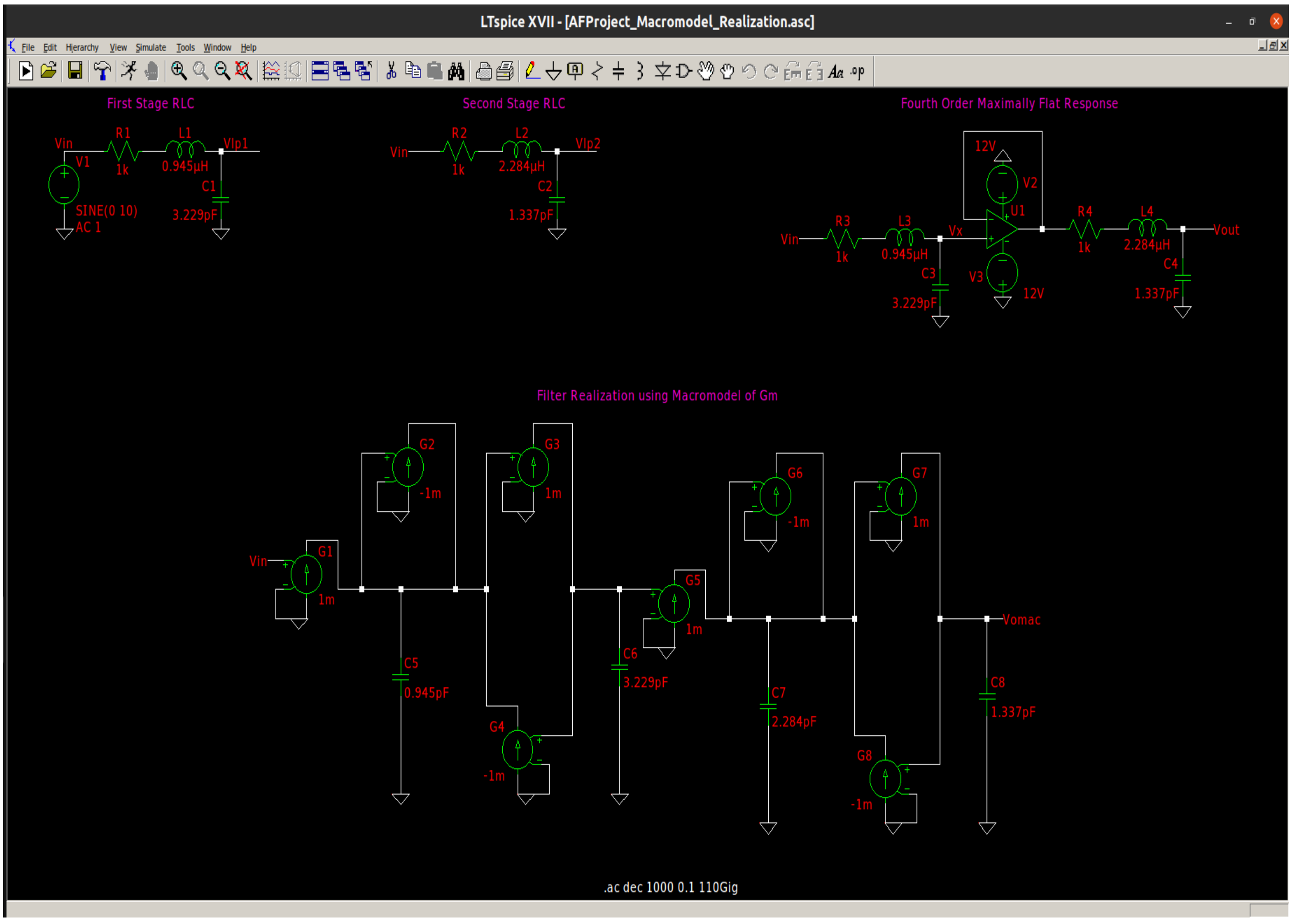
$$K = \mu_n C_{ox}(\frac{W}{L})$$

Initially, we begin by setting arbitrary widths for the NMOS transistors and observing the values of Vdsat. If Vdsat is say less than required, we can either increase the drain current (by increasing the bias voltage to the tail NMOS) or by reducing the width of the transistors. Once, we achieve the required Vdsat, we now need to achieve the desired gm without changing the value of Vdsat. From the above expressions, to increase the gm without changing Idsat, both K and the drain current must be increased by the same factor. The reverse holds true for decreasing gm. Once we achieve the required gm and Vdsat, the transconductor is ready for use in the final circuit. We can then replace the Gm's by the transistor level implementation and make the circuit fully differential.

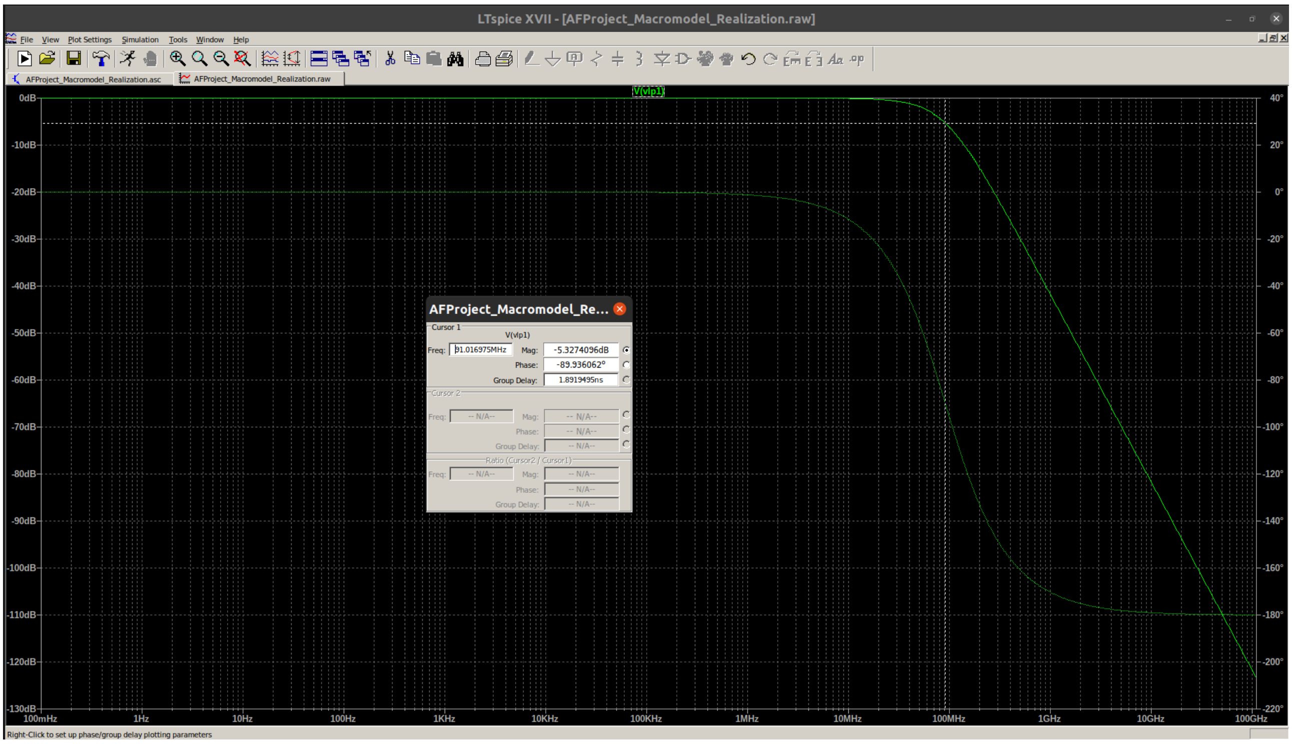
SIMULATIONS AND OBSERVATIONS

1. RLC and Gm-C Macromodel Realization:

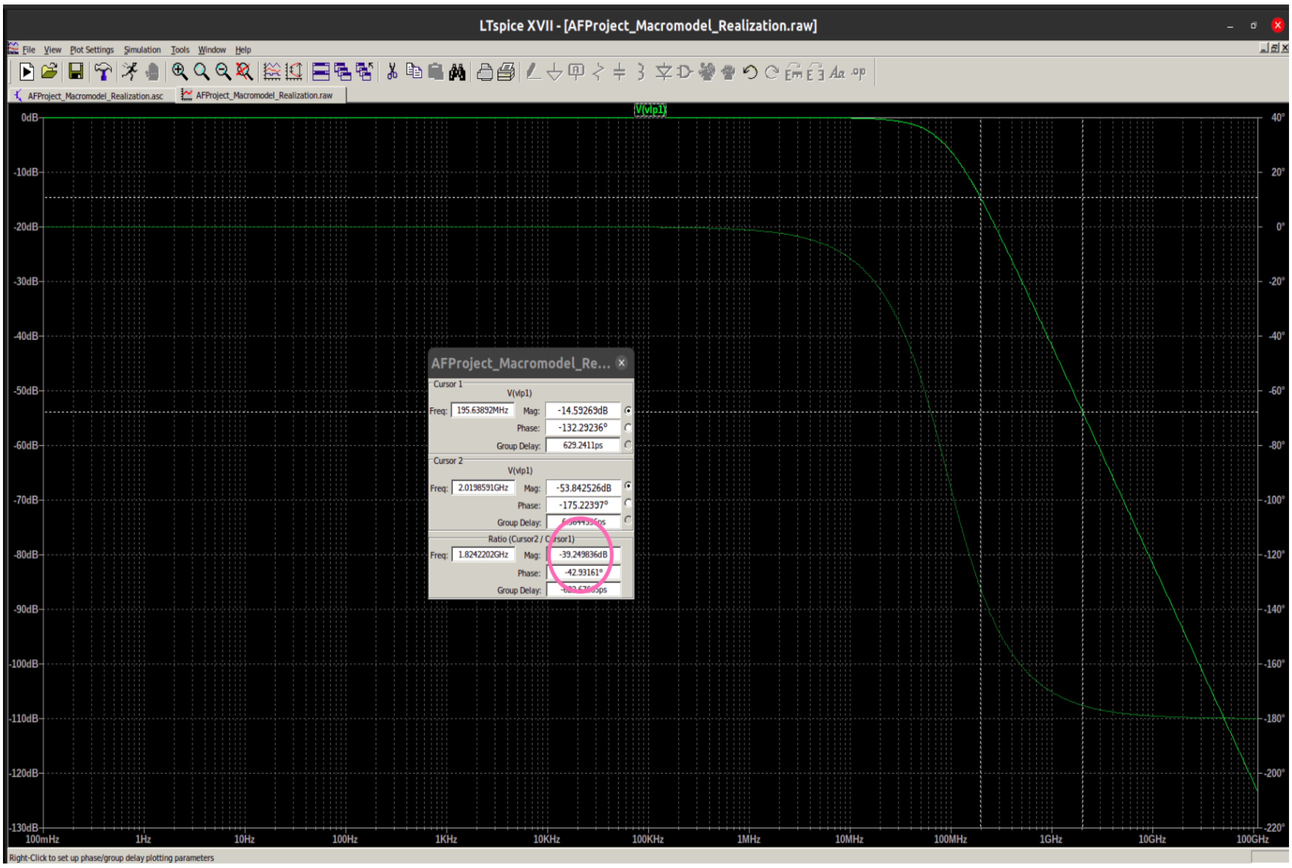
Circuit Schematic



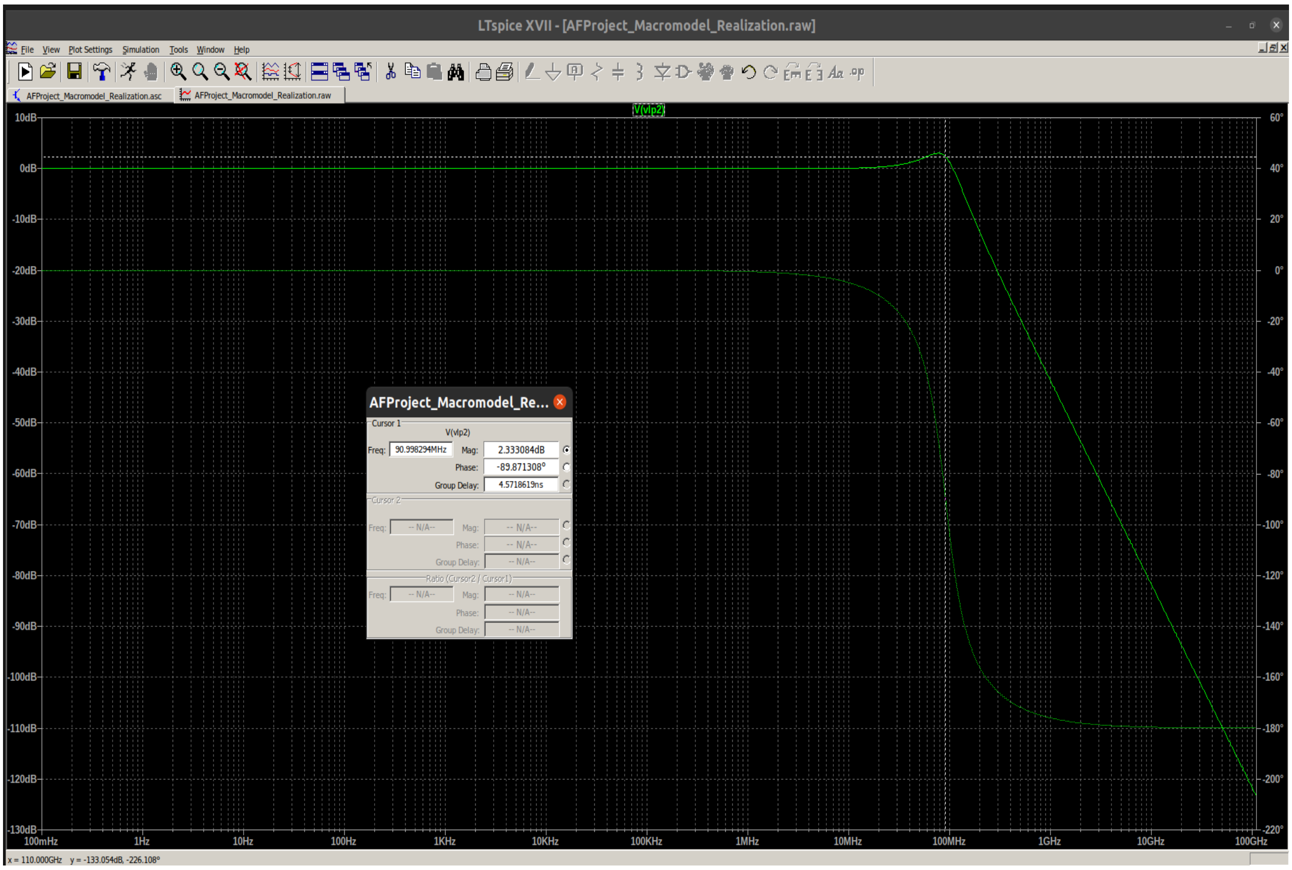
RLC First Stage Waveform



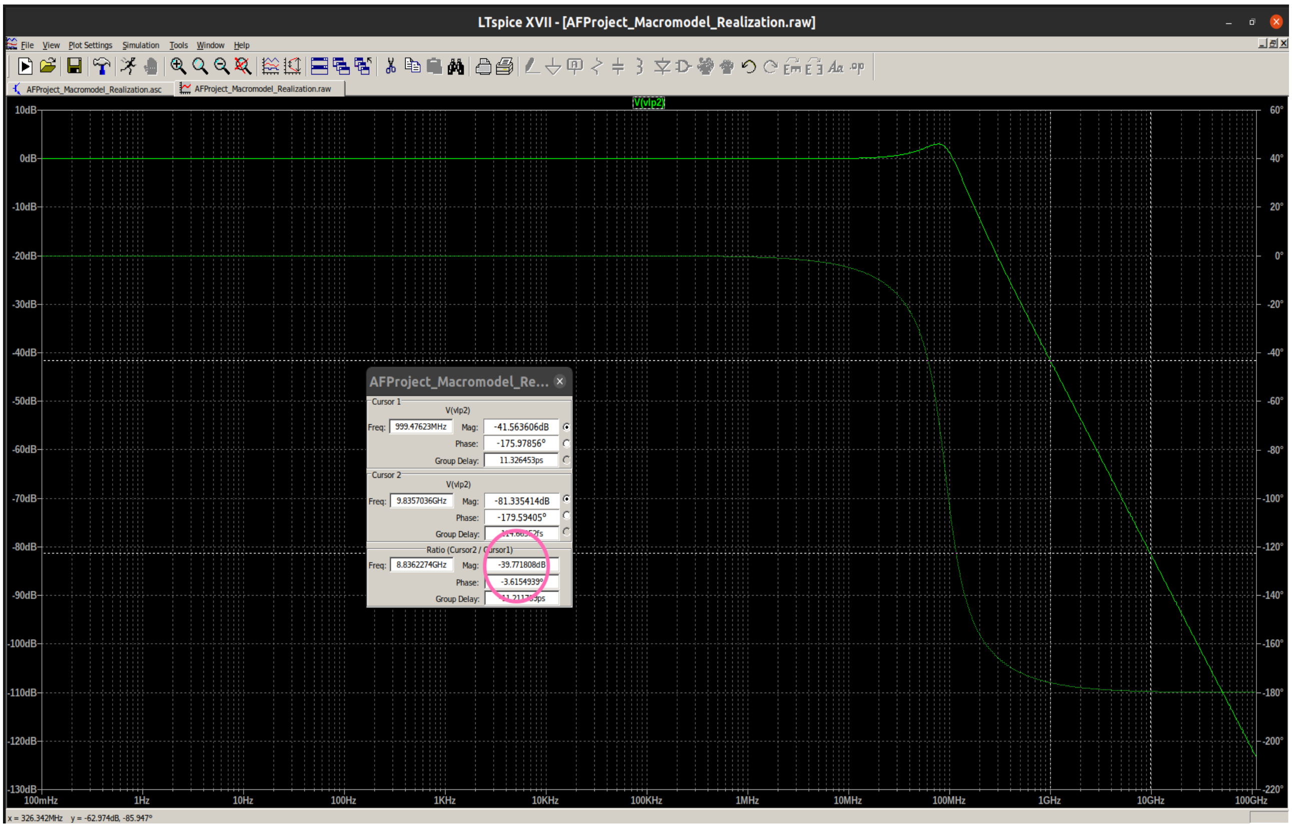
RLC First Stage Rolloff



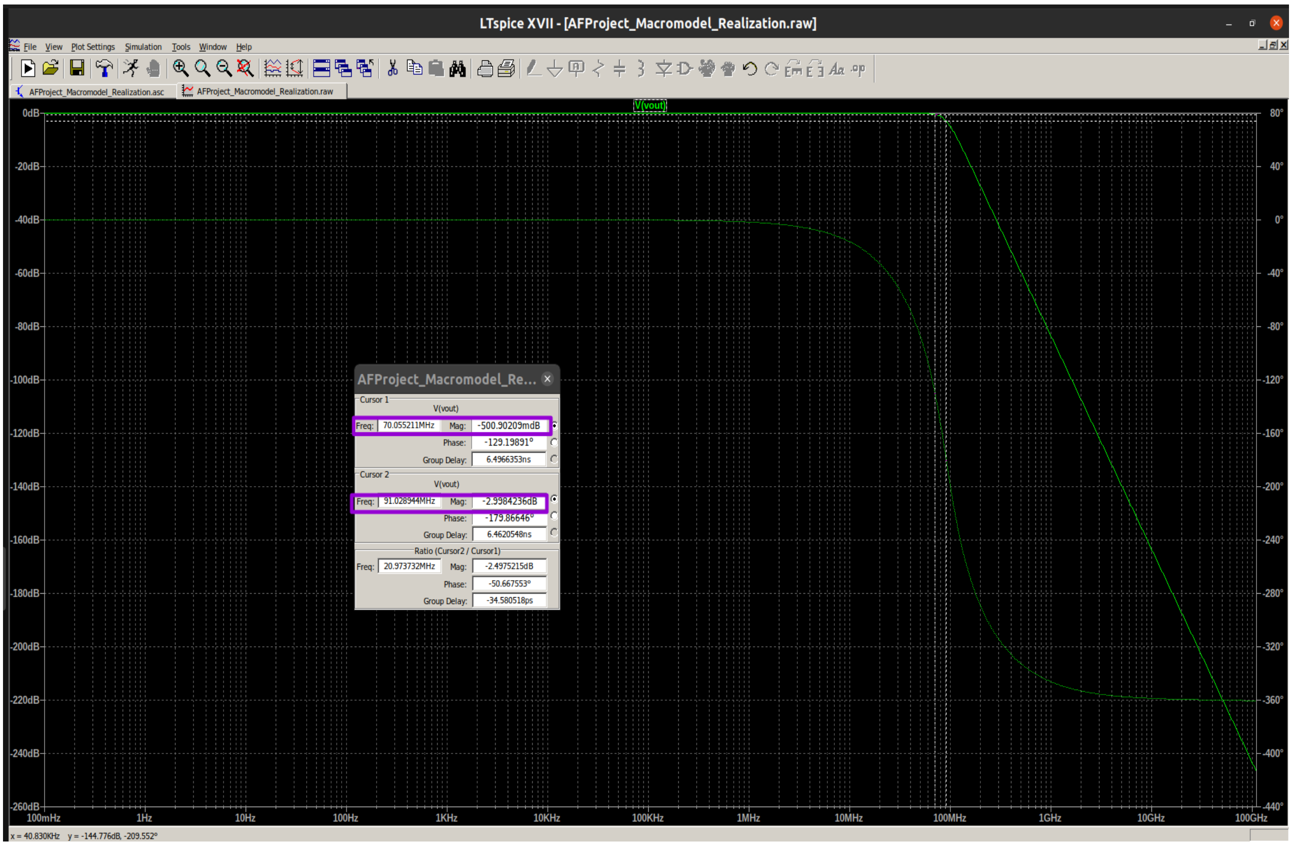
Second Stage RLC Waveform



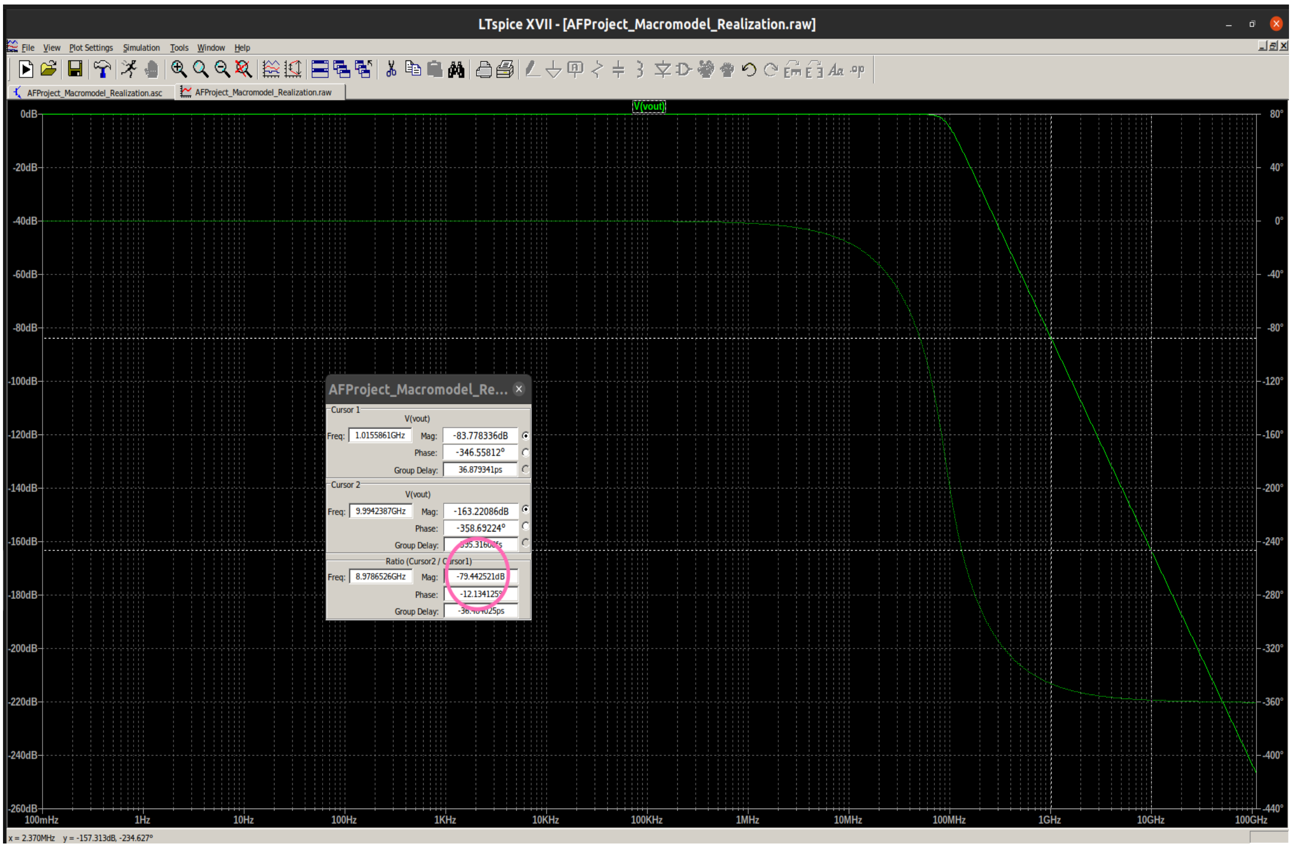
Second Stage RLC Rolloff



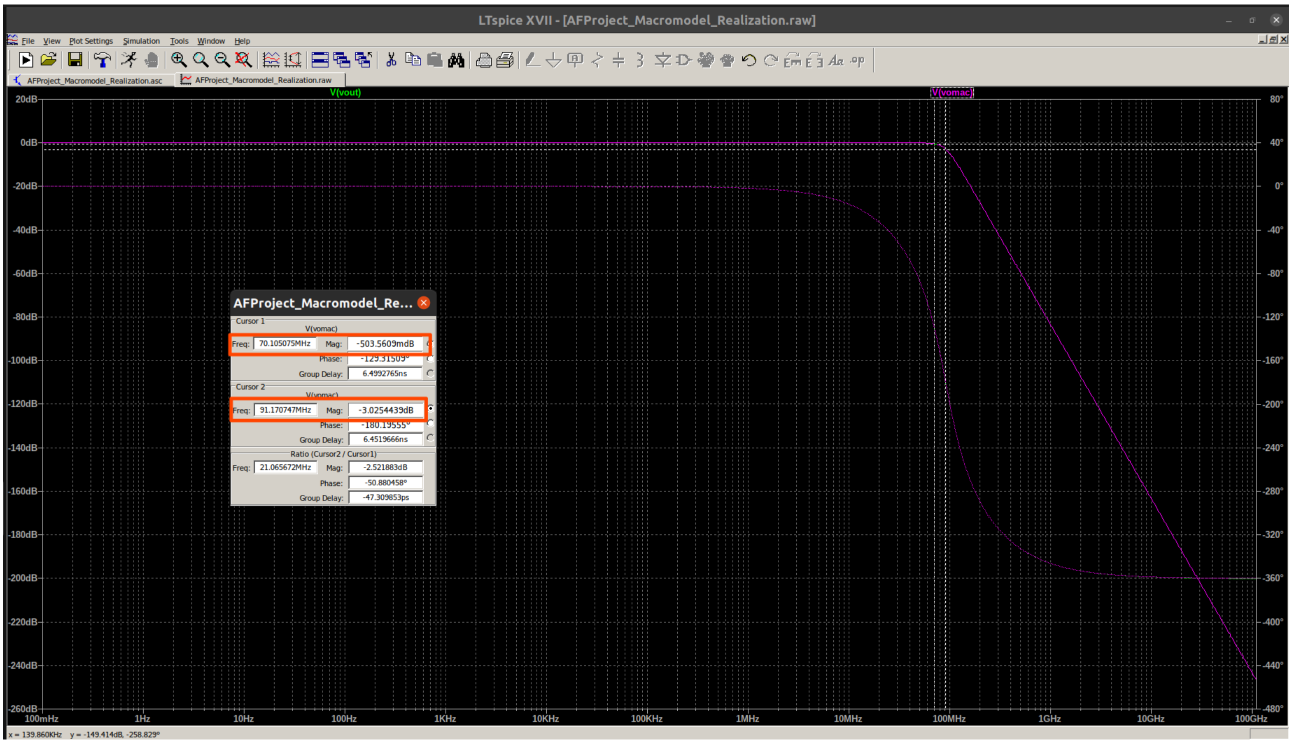
Complete RLC Realization Waveform



Complete RLC Realization Rolloff



Gm – C Realization Waveform:



Observations:

- The first and second stage RLC circuits offer a DC gain of 0 dB. At the Butterworth passband edge of approximately 91 Mhz, each offers a gain equal to the quality factor in decibel. The rolloff for each of the second order filters is observed to be -40 dB/decade.

- The final fourth order RLC realization offers a gain of approximately -500 millidecibels at the passband edge of 70 Mhz and a gain of -3 dB at the Butterworth passband edge of 91 Mhz. The rolloff of the fourth order filter is observed to be -80 dB/decade. The phase plot varies from 0 degress to -360 degrees.

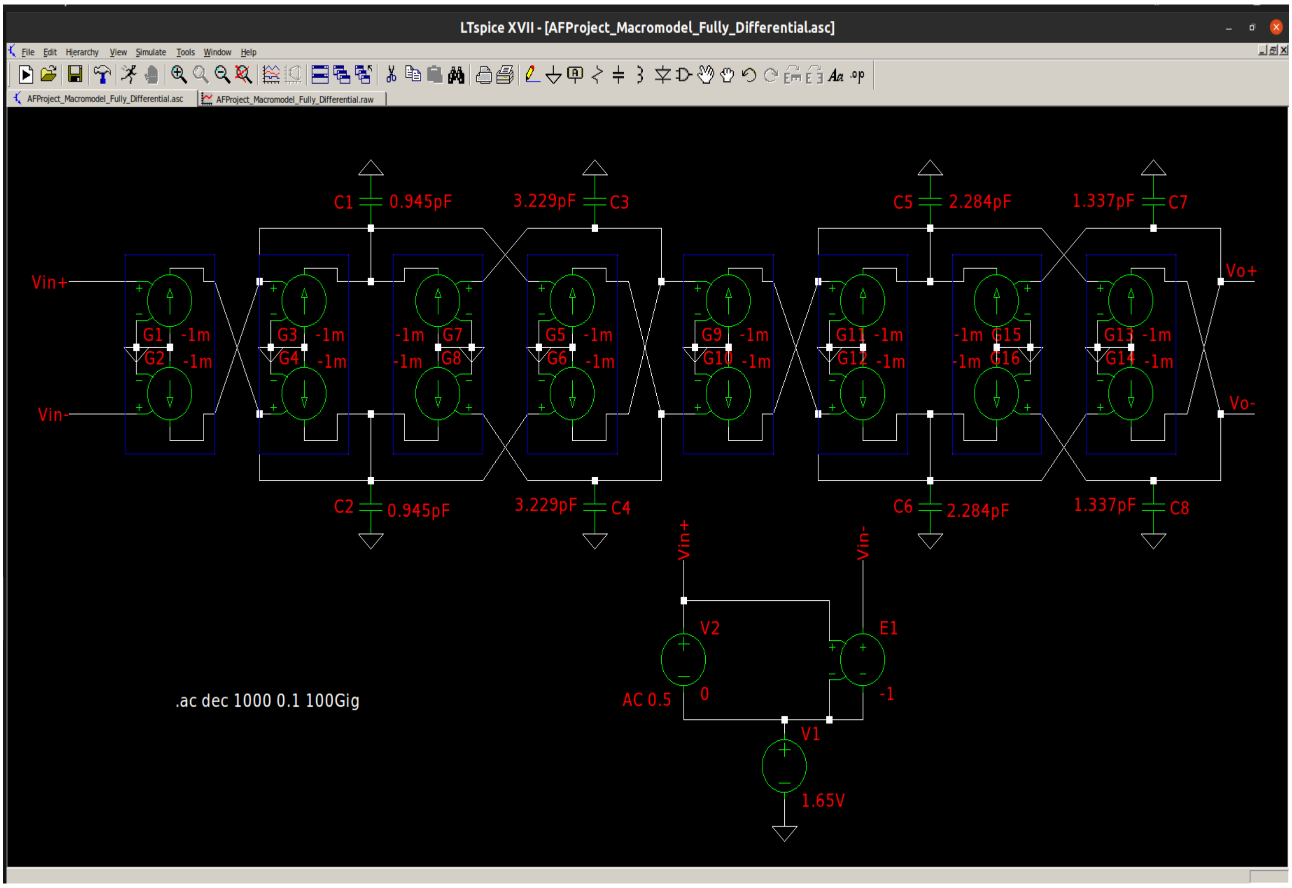
- The Gm – C realization exactly coincides with the RLC realization and offers the same gain and rolloff.

- Thus, the circuit realized using ideal transconductors provides the desired response which verifies the fact that our design is correct.

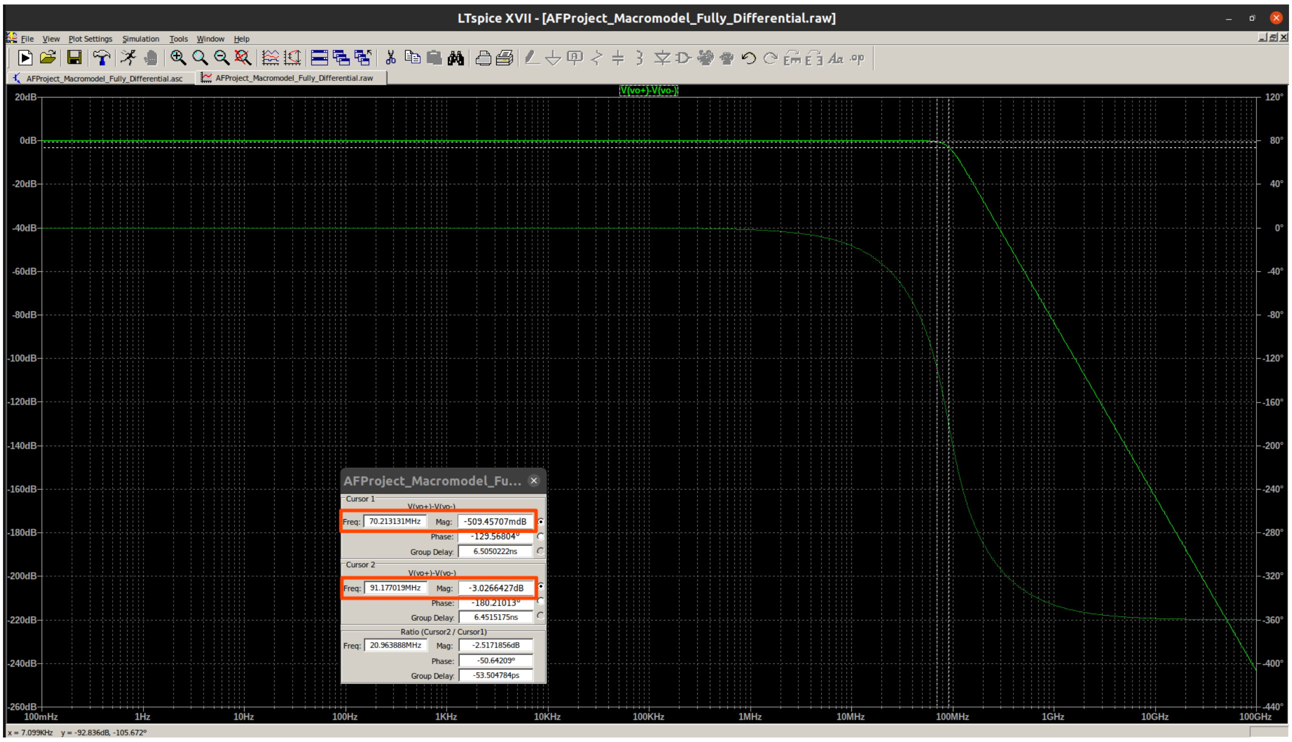
Now that we have realized the RLC and Gm – C macromodel circuits, the next step is to convert our singled ended circuit to a fullydifferential circuit which takes in positive and negative voltages and gives out both positive and negative voltages. This is done since differential circuits are known to offer better linearity as compared to single ended circuits. In the next step, we build a fully differential circuit using Gm macromodels. A fully differential macromodel was created in LtSpice using two voltage controlled current sources.

2. Fully Differential Macromodel Realization

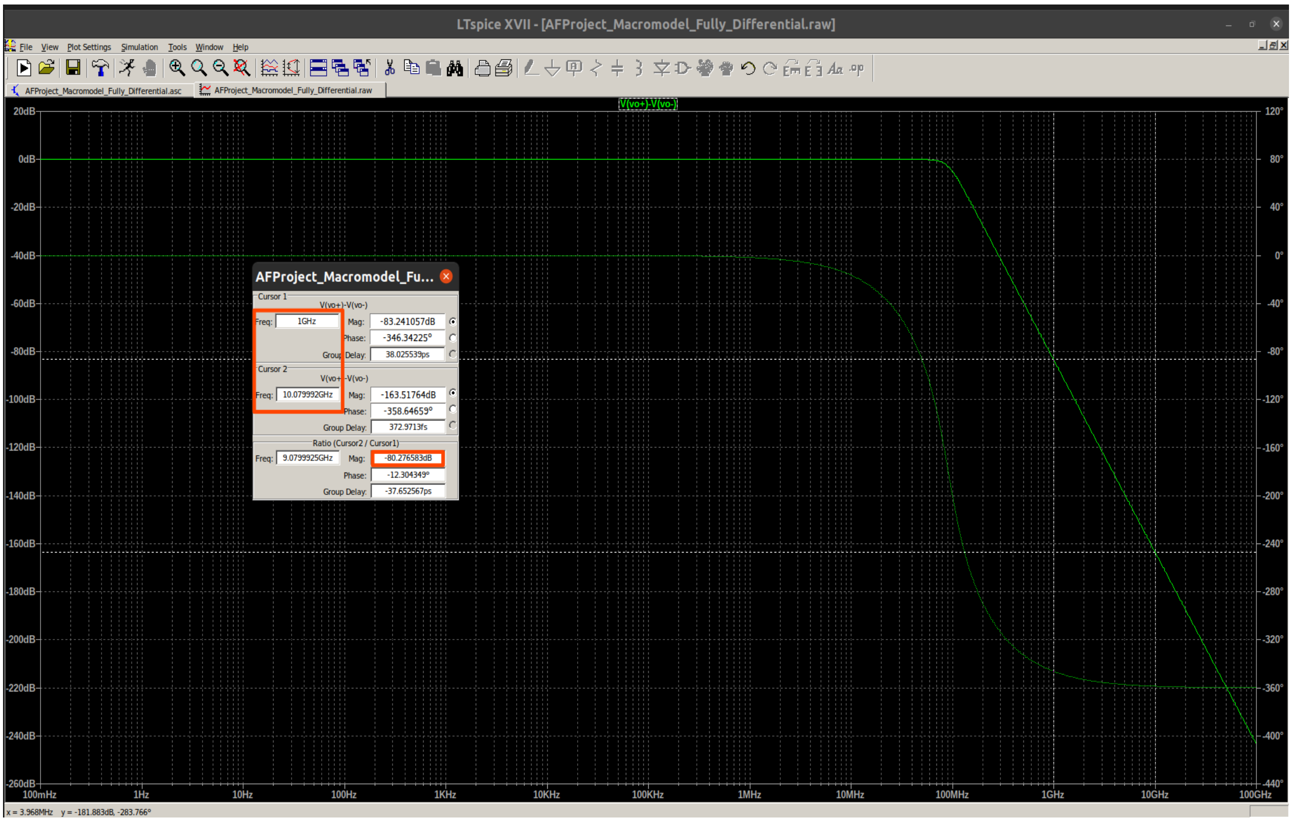
Circuit Schematic



Waveform:



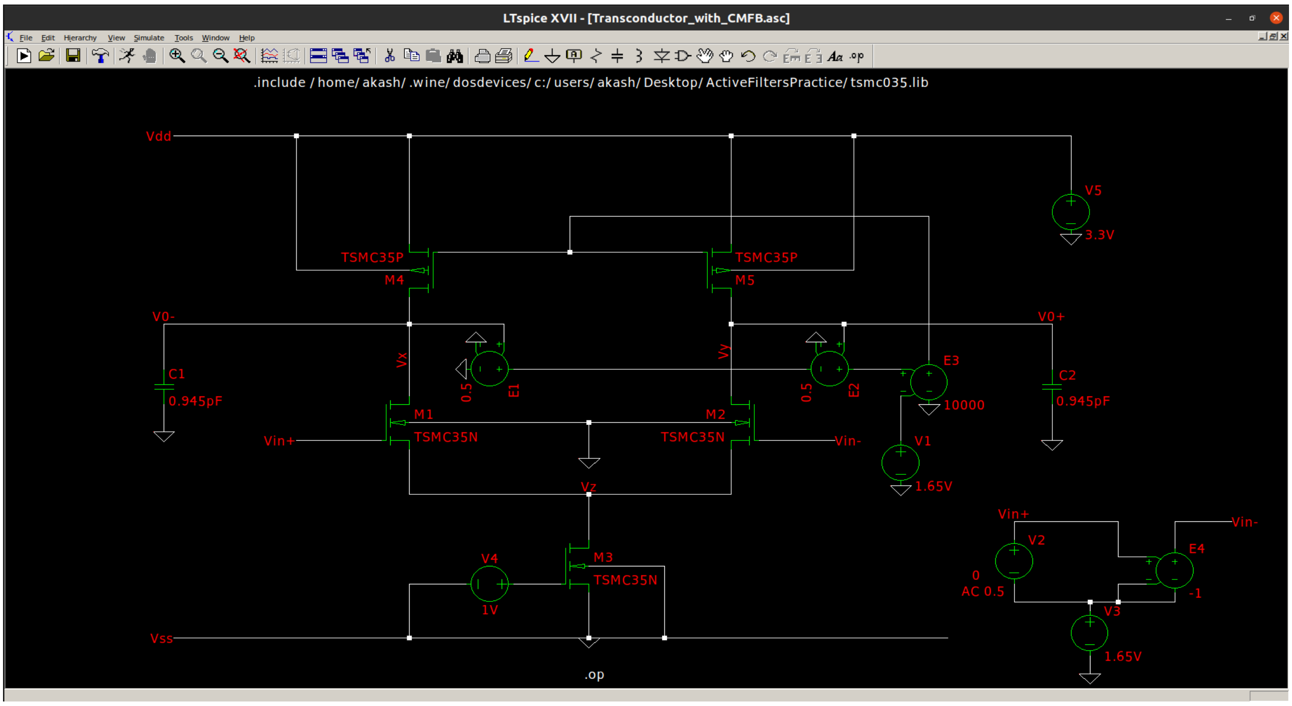
Rolloff:



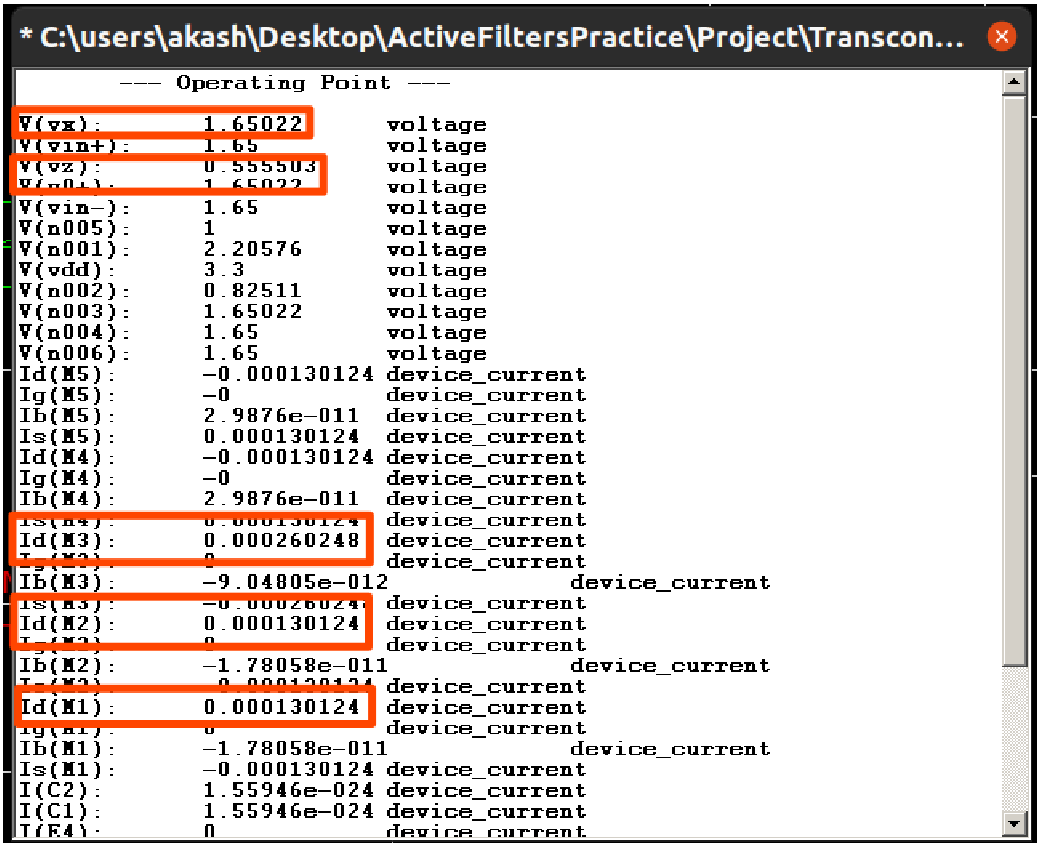
Thus, the fully differential circuit offers the exact same response as the single ended circuit which verifies its correctness

3. Transconductor Design:

Circuit Schematic



DC Operating Point



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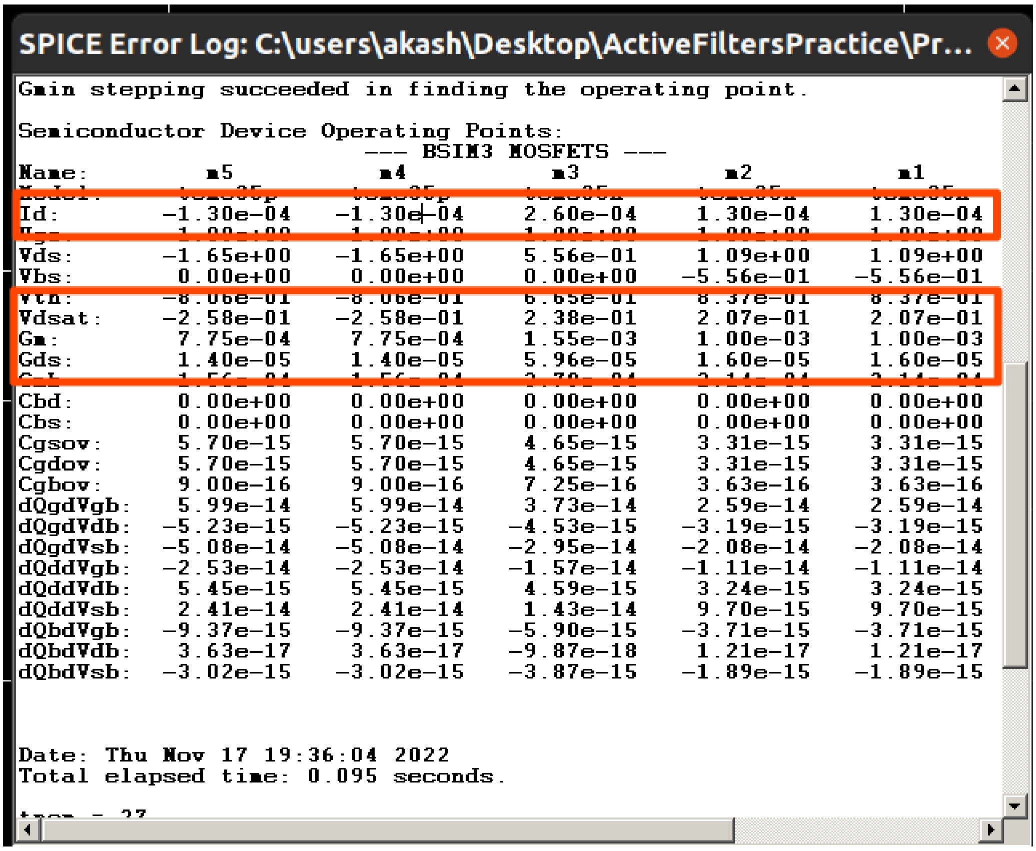
* C:\users\akash\Desktop\ActiveFiltersPractice\Project\Transcon...
       --- Operating Point ---

V(vx):          1.65022      voltage
V(vin+):        1.65         voltage
V(vz):          0.555503     voltage
V(n0+):         1.65022      voltage
V(vin-):        1.65         voltage
V(n005):        1            voltage
V(n001):        2.20576      voltage
V(vdd):         3.3          voltage
V(n002):        0.82511      voltage
V(n003):        1.65022      voltage
V(n004):        1.65         voltage
V(n006):        1.65         voltage
Id(M5):         -0.000130124 device_current
Ig(M5):         -0           device_current
Ib(M5):         2.9876e-011  device_current
Is(M5):         0.000130124  device_current
Id(M4):         -0.000130124 device_current
Ig(M4):         -0           device_current
Ib(M4):         2.9876e-011  device_current
Is(M4):         0.000130124  device_current
Id(M3):         0.000260248  device_current
Ig(M3):         0            device_current
Ib(M3):         -9.04805e-012             device_current
Is(M3):         -0.000260248 device_current
Id(M2):         0.000130124  device_current
Ig(M2):         0            device_current
Ib(M2):         -1.78058e-011             device_current
Is(M2):         -0.000130124 device_current
Id(M1):         0.000130124  device_current
Ig(M1):         0            device_current
Ib(M1):         -1.78058e-011             device_current
Is(M1):         -0.000130124 device_current
I(C2):          1.55946e-024 device_current
I(C1):          1.55946e-024 device_current
I(E4):          0            device_current
```

Spice Log:



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SPICE Error Log: C:\users\akash\Desktop\ActiveFiltersPractice\Pr...
Gmin stepping succeeded in finding the operating point.

Semiconductor Device Operating Points:
                    --- BSIM3 MOSFETS ---
Name:          m5          m4          m3          m2          m1
Id:       -1.30e-04   -1.30e-04    2.60e-04    1.30e-04    1.30e-04
Vds:      -1.65e+00   -1.65e+00    5.56e-01    1.09e+00    1.09e+00
Vbs:       0.00e+00    0.00e+00    0.00e+00   -5.56e-01   -5.56e-01
Vth:      -8.06e-01   -8.06e-01    6.65e-01    8.37e-01    8.37e-01
Vdsat:    -2.58e-01   -2.58e-01    2.38e-01    2.07e-01    2.07e-01
Gm:        7.75e-04    7.75e-04    1.55e-03    1.00e-03    1.00e-03
Gds:       1.40e-05    1.40e-05    5.96e-05    1.60e-05    1.60e-05
Cbd:       0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
Cbs:       0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
Cgsov:     5.70e-15    5.70e-15    4.65e-15    3.31e-15    3.31e-15
Cgdov:     5.70e-15    5.70e-15    4.65e-15    3.31e-15    3.31e-15
Cgbov:     9.00e-16    9.00e-16    7.25e-16    3.63e-16    3.63e-16
dQgdVgb:   5.99e-14    5.99e-14    3.73e-14    2.59e-14    2.59e-14
dQgdVdb:  -5.23e-15   -5.23e-15   -4.53e-15   -3.19e-15   -3.19e-15
dQgdVsb:  -5.08e-14   -5.08e-14   -2.95e-14   -2.08e-14   -2.08e-14
dQddVgb:  -2.53e-14   -2.53e-14   -1.57e-14   -1.11e-14   -1.11e-14
dQddVdb:   5.45e-15    5.45e-15    4.59e-15    3.24e-15    3.24e-15
dQddVsb:   2.41e-14    2.41e-14    1.43e-14    9.70e-15    9.70e-15
dQbdVgb:  -9.37e-15   -9.37e-15   -5.90e-15   -3.71e-15   -3.71e-15
dQbdVdb:   3.63e-17    3.63e-17   -9.87e-18    1.21e-17    1.21e-17
dQbdVsb:  -3.02e-15   -3.02e-15   -3.87e-15   -1.89e-15   -1.89e-15


Date: Thu Nov 17 19:36:04 2022
Total elapsed time: 0.095 seconds.
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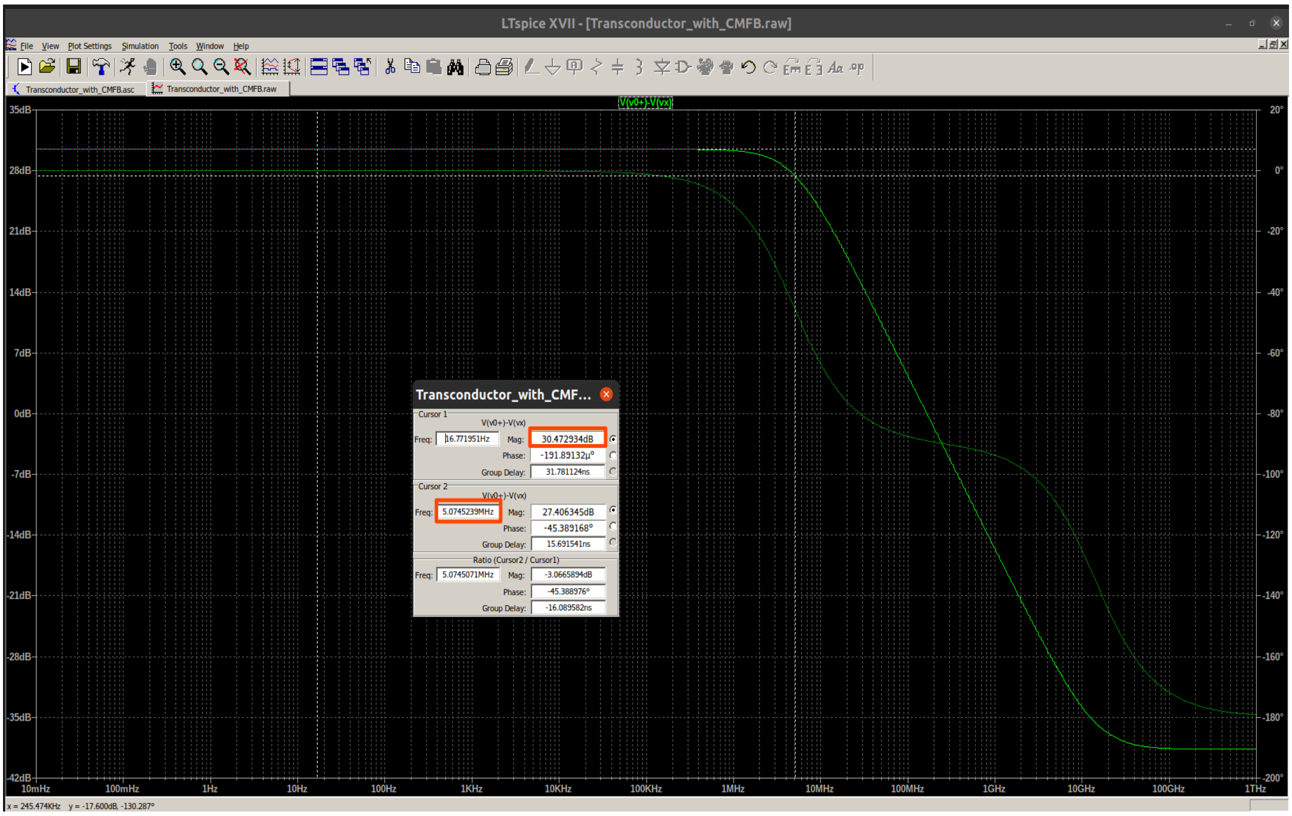
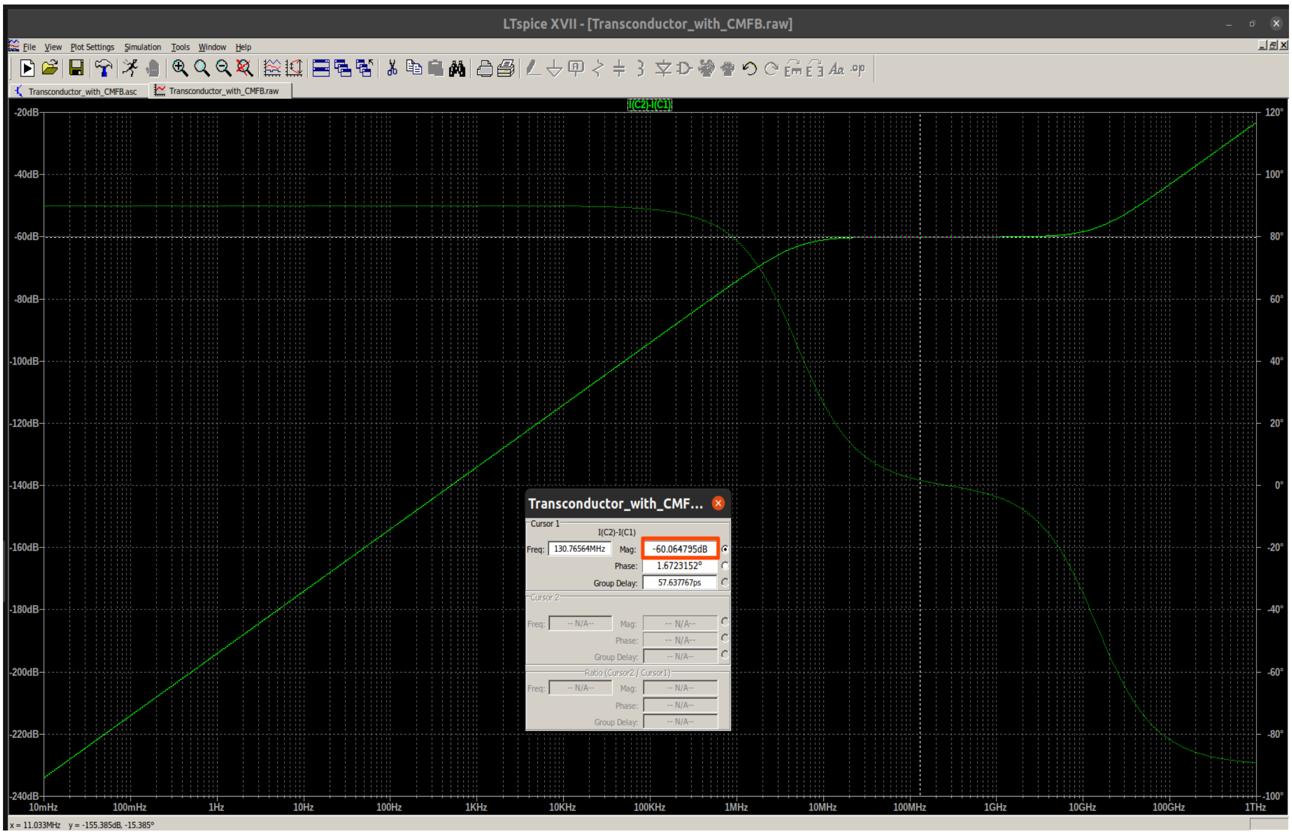
Output Voltage Waveform of Gm – C integrator



Output Current Waveform of Gm – C integrator

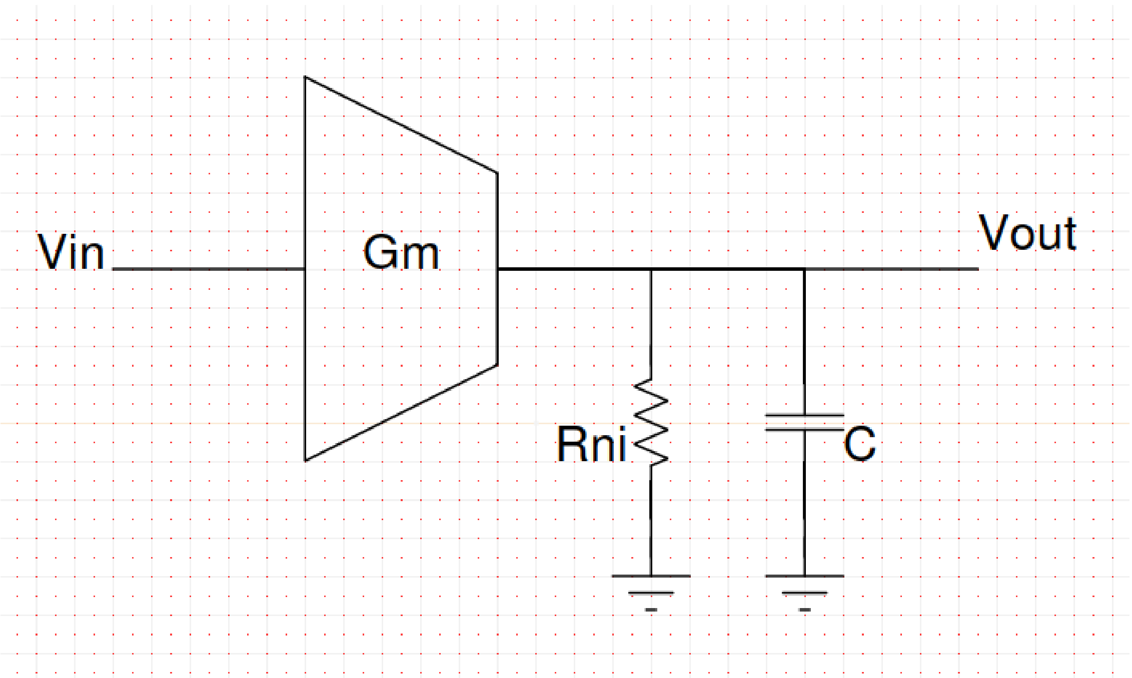


Observations:

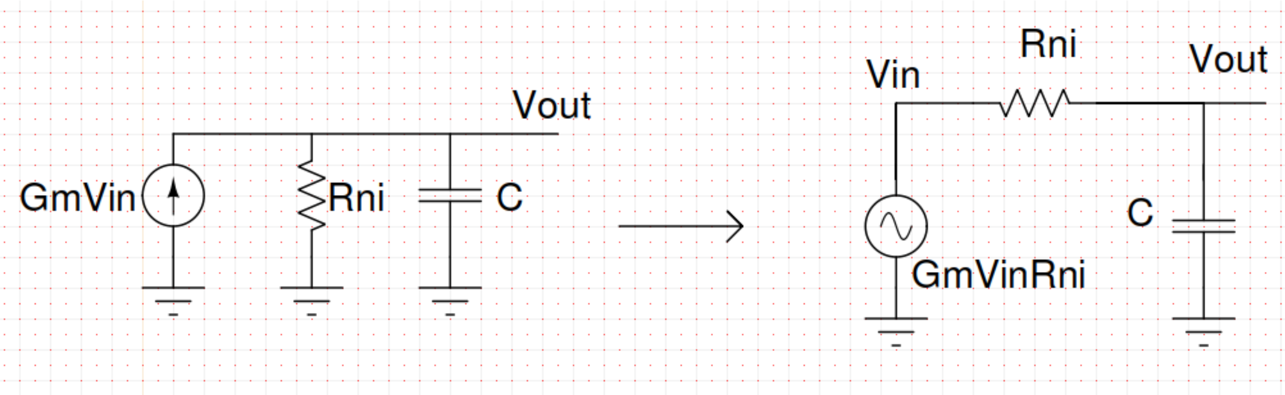
- From the operating point characteristics, we observe that the input operatingvoltage has been set to 1.65 V (common mode input) and the output operating voltage is 1.65022 V. We wanted the exact operating voltage at output to be 1.65 V so that input could be given to the next transconductor. The error arises from the fact that in the common mode feedback, we have used an error amplifier with a gain of 10,000 whereas the theoretical gain should be infinite. Thus, we have gotten the steady state error in the fourth decimal place. However, this error is negligible and it was observed that it did not affect the circuit operation greatly.
- From the Spice Error Log, the values of Gm for transistors M1 and M2 is observed to be 1mS as expected. This is also by definition the transconductance of the overall circuit. Further, it can be observed that the Vdsat (gate overdrive) of the transistor M1 and M2 is 207 mV. For the specifications, we need to get 200 mV. Thus, we have almost exactly realized the specifications on the transconductor. We also need to note the values of Gds for the NMOS and PMOS transistors. These are contributed by channel length modulation effect and cause non-idealities in the Gm – C integrator by appearing as a parasitic grounded resistor. Since both these resistors from M1 and M4 (or M2 and M5) appear in parallel, we can add the Gds values to get the overall non-ideal resistance at the output nodes. The channel length modulation effect of M3 can be ignored since node Vz acts as a small signal ground and thus, no current can flow through this resistor as boh the terminals have been grounded. The total non-ideal admittance at each of the output nodes is calculated as follows:

$$G_{ni} = 1.6*10^{-5} + 1.4*10^{-5} = 3*10^{-5} S \Rightarrow R_{ni} = \frac{1}{G_{ni}} = 33.33 k\Omega$$

- The output of the Gm – C integrator is ideally expected to be a straight line with slope of ~~20~~ dB/decade where it across the 0dB line at ω = Gm/C. However, our actual output appears to have a low pass response with some dc gain. This can be shown to be correct if the nonideal resistor is taken into account. The circuit of anon-ideal Gm – C integrator that we have realized is as shown below:



The RLC equivalent of the above circuit is as shown below:



Thus, the non-ideal Gm-C integrator is nothing but a first order low pass filter. The cutoff frequency of this low pass filter is given by:

$$\omega_o = \frac{1}{R_{ni} * C} = \frac{1}{33.33*10^3*0.945*10^{-12}} \Rightarrow \omega_o = 31.749\, Mrad/sec = 5.05\, MHz$$

Similarly, the dc gain of the low pass filter is given by:

$$A_o = 20\log(G_m * R_{ni}) = 20\log(1*10^{-3}*33.33*10^3) = 30.457\, dB$$

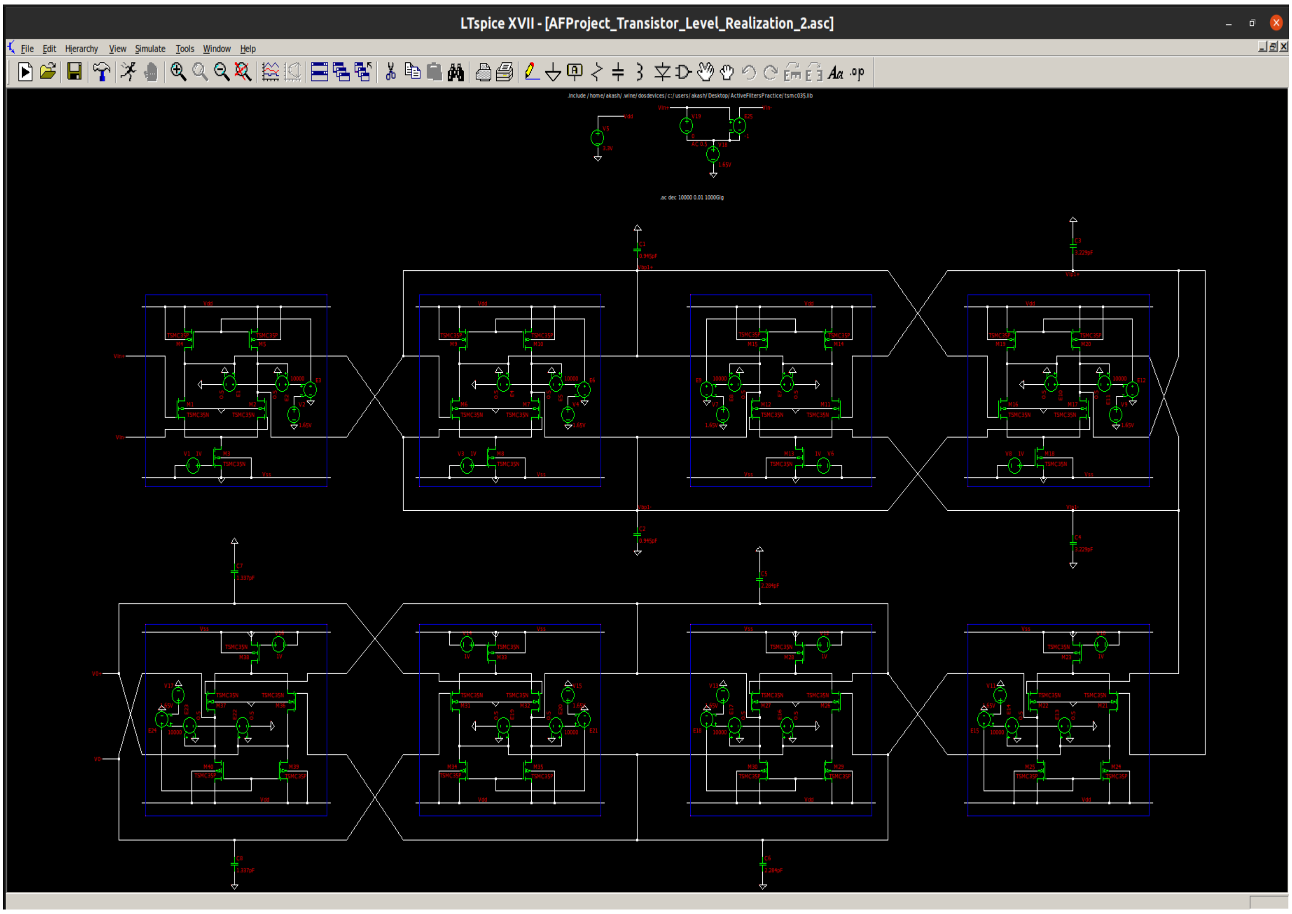
These values can be verified to be very close to those obtained from the simulation waveform of the output voltage (Enclose in colored rectangles in the cursor window). The slight differences are due to the fact that there are also parasitic capacitances which will decrease the bandwidth but which we have ignored in out analysis for simplicity.

- The output current waveform is expected to be a straight line of -60 dB (1mS) throughout the range of frequencies. However, due to the introduction of the resistor, the current throught the capacitor now has a high pass response since at low frequencies, the resistor impedance dominates the capacitor impedance in parallel combination and all the current flows through the resistor giving a low value for current through the capacitor. In the range of 100 Mhz to 1 Ghz, the response is exactly correct and gives a value of -60 dBm as can be observed from the cursor values.

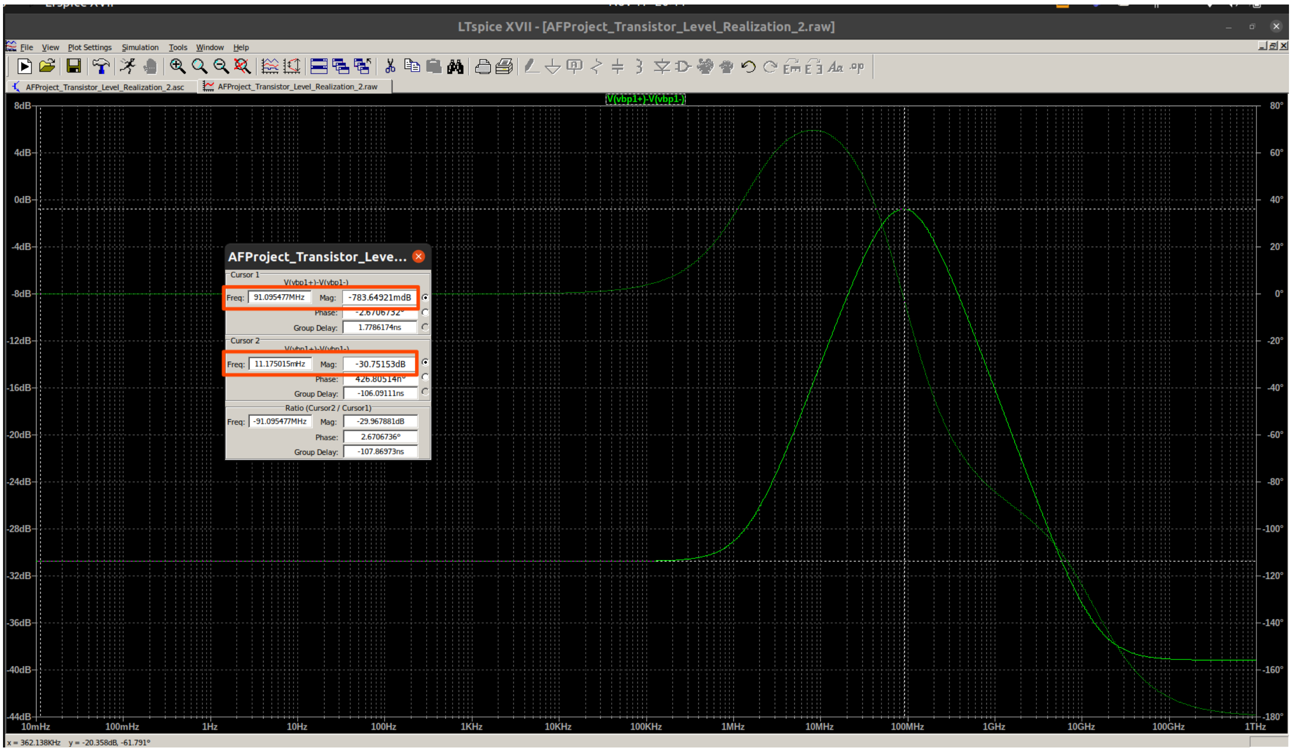
Now that we have built the transconductor using common mode feedback, the final step is to realize the fully differential circuit by replacing the voltage controlled current sources in our earlier design with actual transistor implementations that we have used. We also note the sizes of the transistors that have been used to realize the transconductor. The NMOS input transistors have a length of 0.5 micron and a width of 1.77 micron with 8 parallel fingers. The PMOS load transistors use the same length and width but double the number of parallel fingers. This is done since the mobility of holes is approximately half the mobility of the electrons and we want to sustain the same current through both the NMOS and PMOS transistors.

4. Transistor Level Implementation:

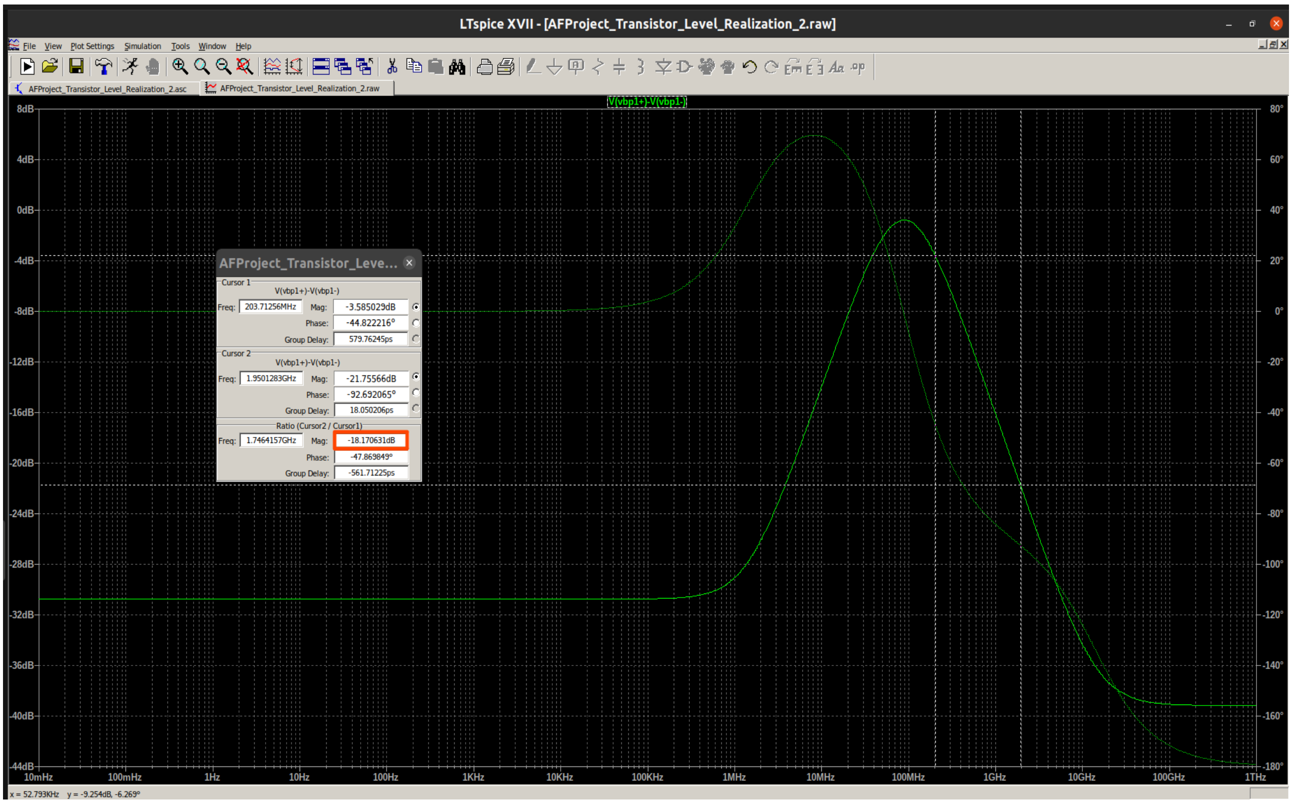
Circuit Schematic



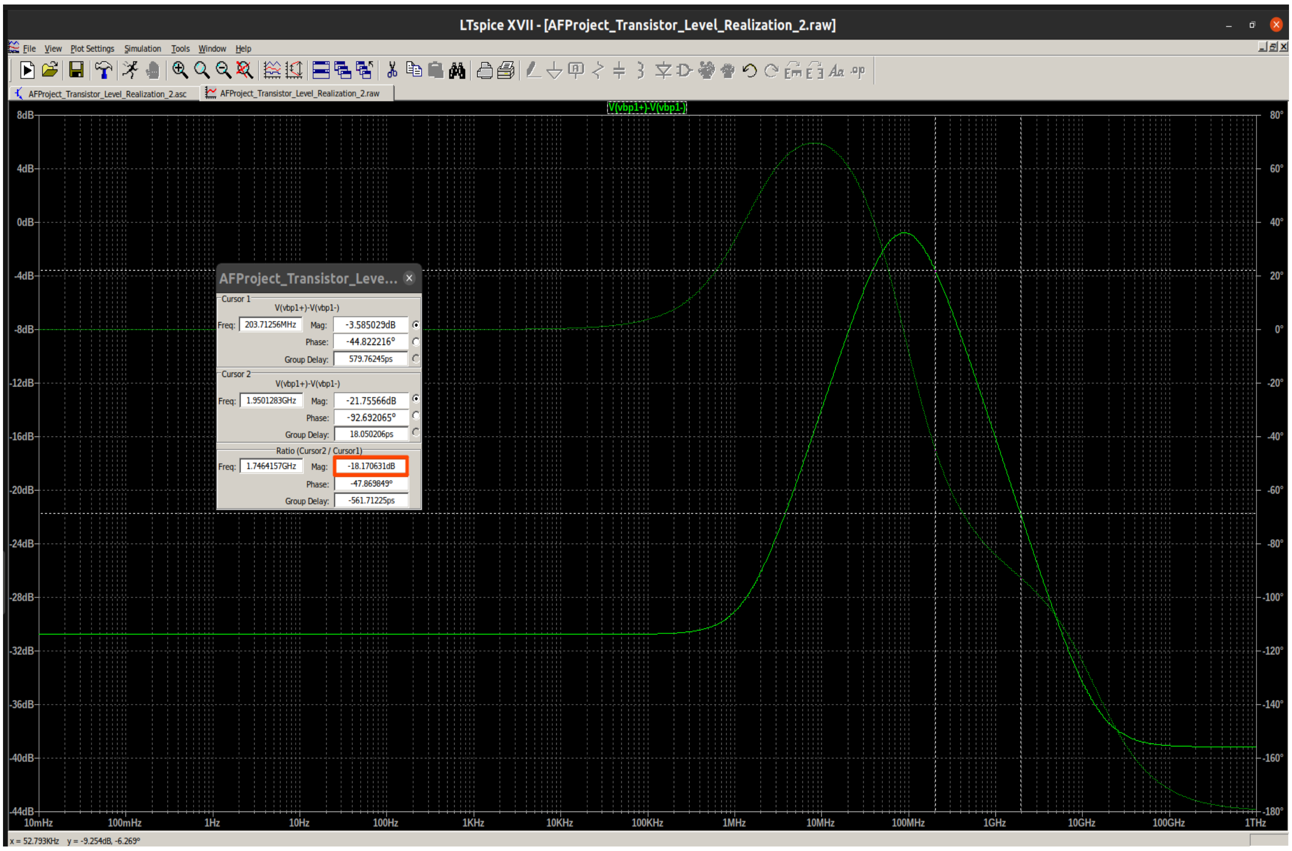
Output Waveform at first Band Pass Node:



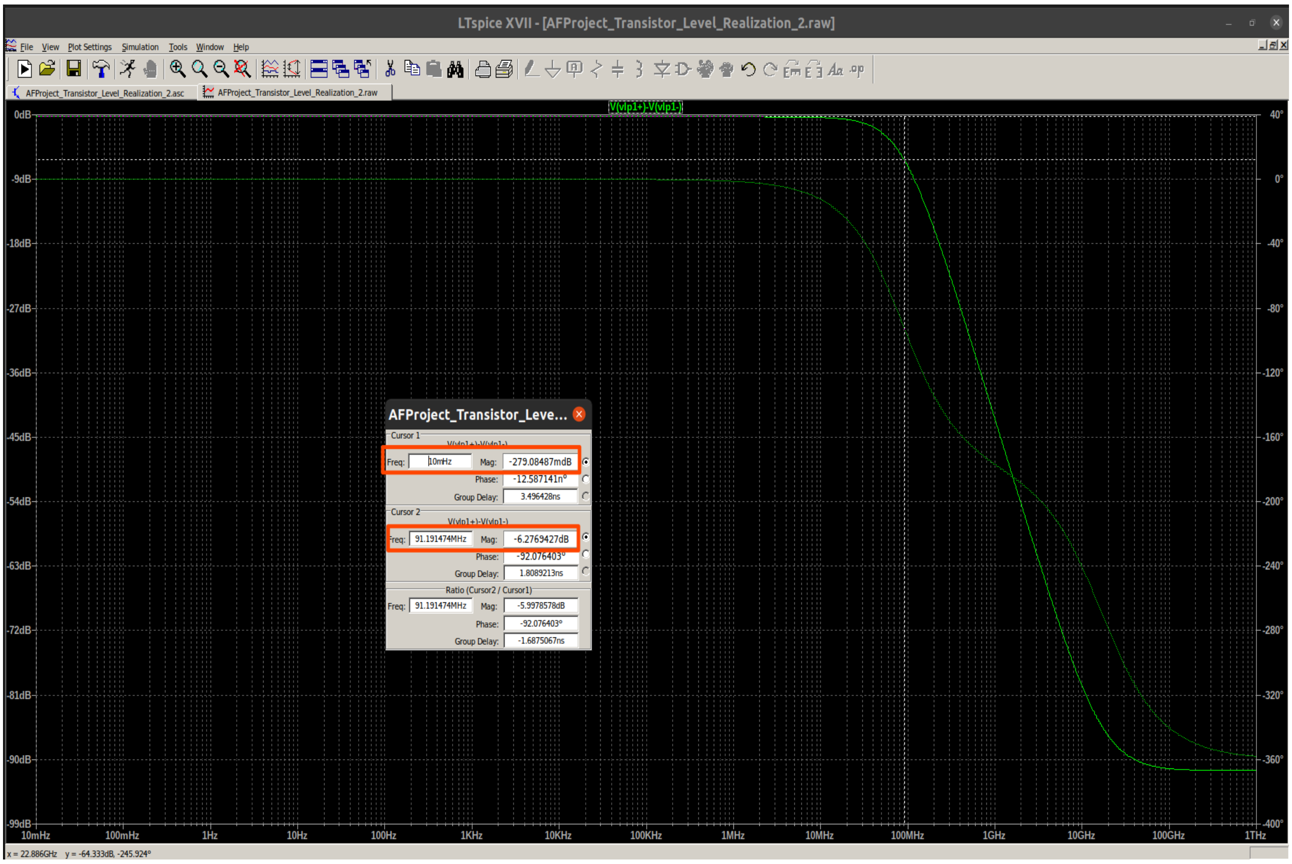
Rolloff at raising edge of first Band Pass Node:



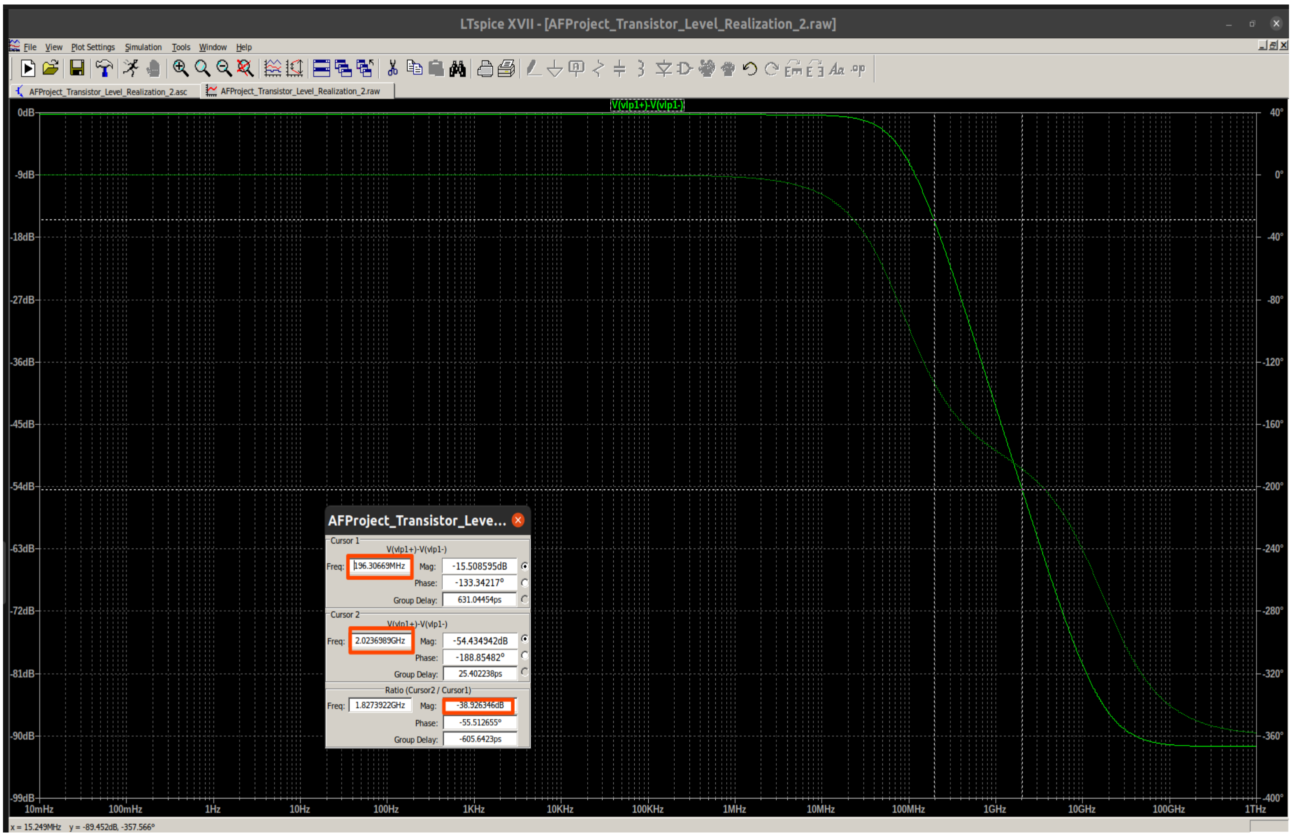
Rolloff at Falling Edge of first Bandpass Node:



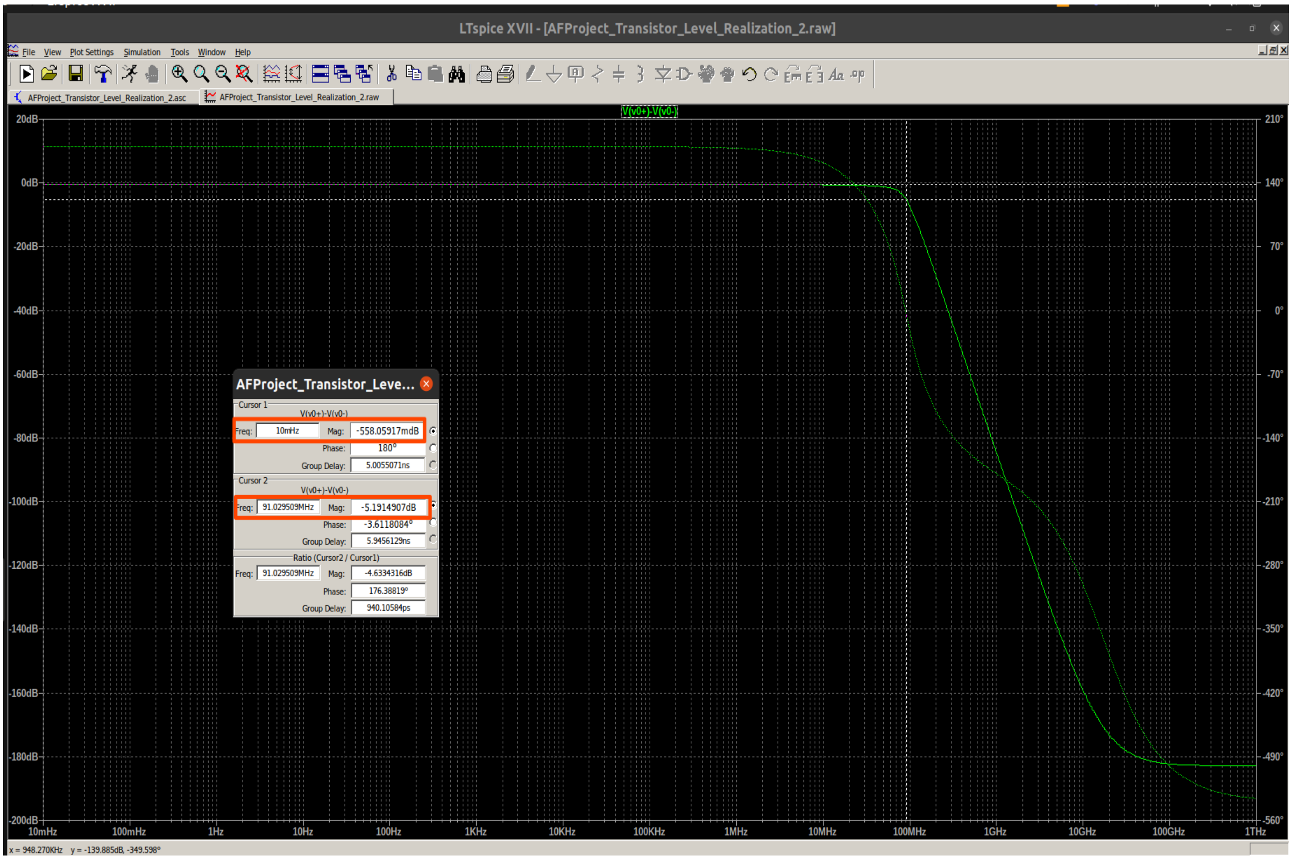
Output Waveform at First Low Pass Node:



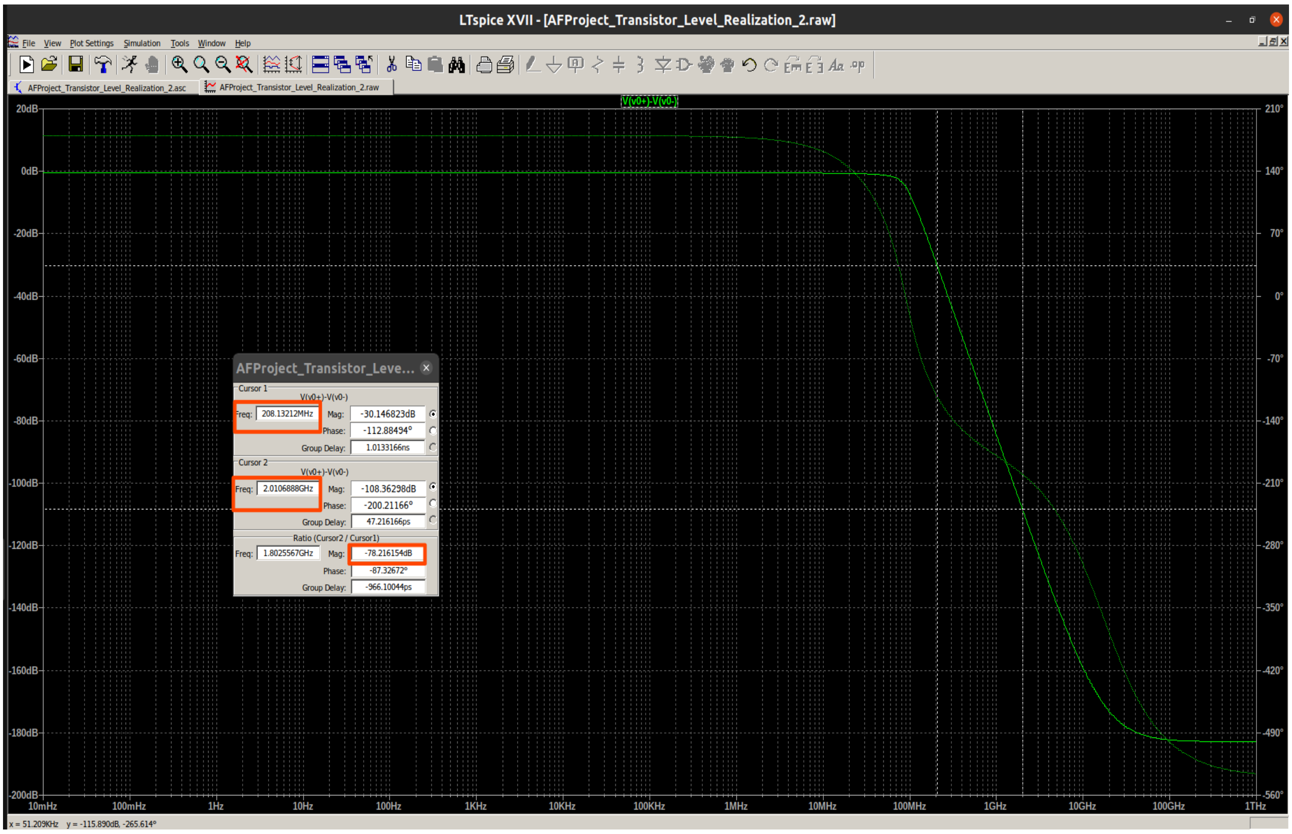
Rolloff at First Low Pass Node:



Waveform at Output Node:

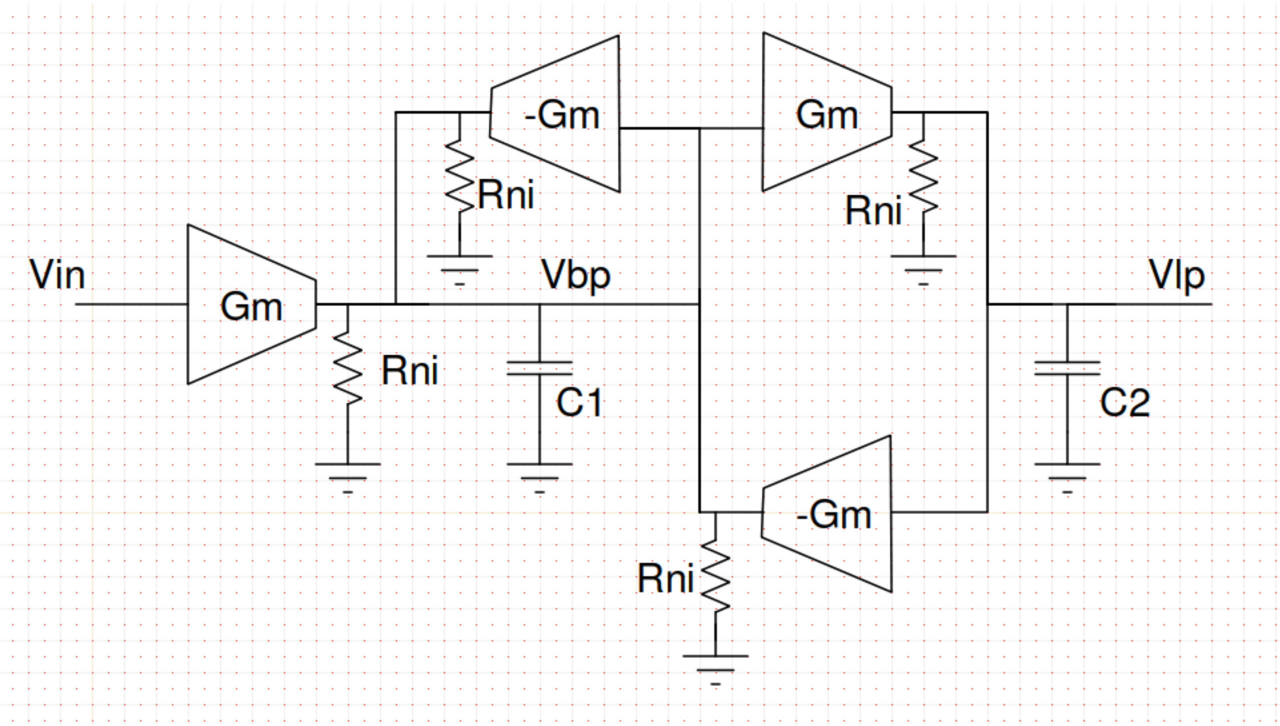


Rolloff at Output Node:



Observations:

- At the first band pass node, we observe that the peak in the waveform occurs at around 91 Mhz. This, if we recall is the passband edge of the Butterworth filter that we had designed which means that the passband edge has been accurately obtained. The rolloff at the raising and falling edge is also about 20 dB/decade which is also as per our expectations. However, the gain at the passband edge is not 0dB but a passband gain of around -785 millidecibels is observed. Further, at low frequencies, the gain in dB should ideally go to negative infinity but it is observed to stabilize at around -30.7 dB. We now try to see if the lossy transconductor has contributed to these changes. Shown below is the Gm – C realization of the band pass filter with lossy transconductances.



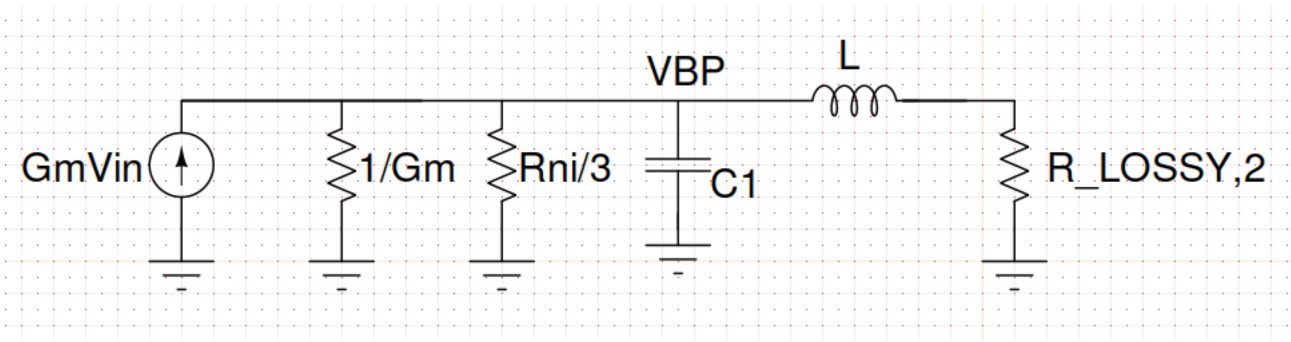
We are now required to analyze the above circuit for the Vbp node. At node Vbp, three resistors are in parallel which can be combined together. Similarly, the load of the gyrator is a resistor in parallel with a capacitor. This gives an effective impedance of an inductor in series with a resistor at the input of the gyrator. The values of the resistor and inductor can easily br derived from the relation for the input impedance of a gyrator:

$$Z_{in} = \frac{Y_L}{G_m^2}$$

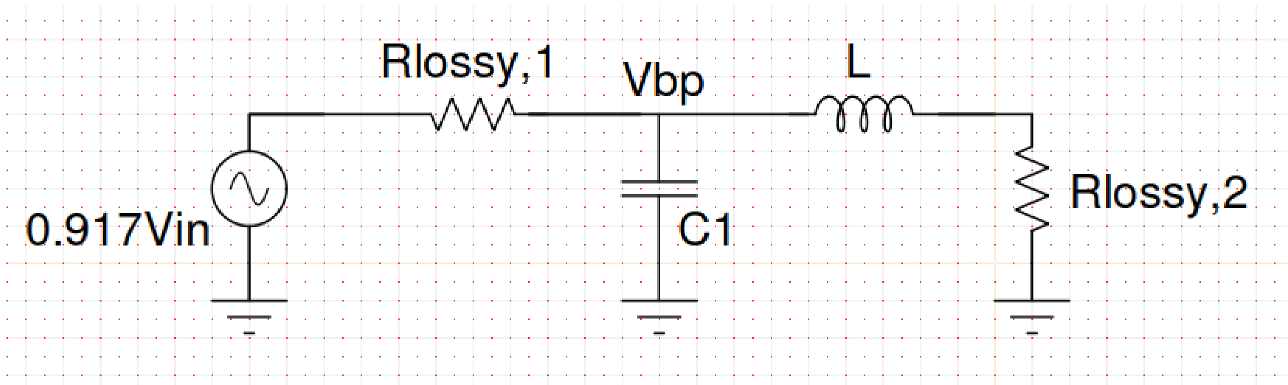
where Y_L is the load admittance. In our case,

$$Z_{in} = \frac{1}{G_m^2} * \left(\frac{1}{R_{ni}} + C_2 s\right) = R_{LOSSY,2} + Ls \quad where \quad R_{LOSSY,2} = \frac{1}{G_m^2 R_{ni}} \wedge L = \frac{C_2}{G_m^2}$$

The RLC equivalent of the above circuit is as shown below. Note that we have also converted the initial voltage source along with Gm into a current source to completely eliminate transconductors from the circuit.



The above circuit is now relatively simpler to analyze. In order to further simplify our analysis, we replace the the circuit on the left hand side of node Vbp by its Thevinin's equivalent. The resultant circuit is as shown below:



The values of the components are as shown below:

$$R_{LOSSY,1} = 0.917\,k\Omega,\ R_{LOSSY,2} = 30\Omega,\ C_1 = 0.945\,pF,\ L = 3.229\,\mu H$$

The expression for the transfer function at the passband node is as shown below:

$$\frac{V_{BP}(s)}{V_{in}(s)} = \frac{\dfrac{R_{LOSSY,2}}{R_{LOSSY,1}+R_{LOSSY,2}}+\dfrac{L}{R_{LOSSY,1}+R_{LOSSY,2}}s}{\dfrac{R_{LOSSY,1}LCs^2}{R_{LOSSY,1}+R_{LOSSY,2}}+\dfrac{(R_{LOSSY,1}R_{LOSSY,2}C+L)s}{R_{LOSSY,1}+R_{LOSSY,2}}+1}$$

The above expression is approximately of the form:

$$\frac{V_{BP}(s)}{V_{in}(s)} = \frac{A_0+\dfrac{1}{Q}\left(\dfrac{s}{\omega_0}\right)}{\left(\dfrac{s}{\omega_0}\right)^2+\dfrac{1}{Q}\left(\dfrac{s}{\omega_0}\right)+1}$$

This is similar to the standard bandpass transfer function except for the A_0 term. The A_0 term contributes to the constant gain at very low frequencies that we observed in the waveform. Thus, the dc gain of the circuit can be expressed as:

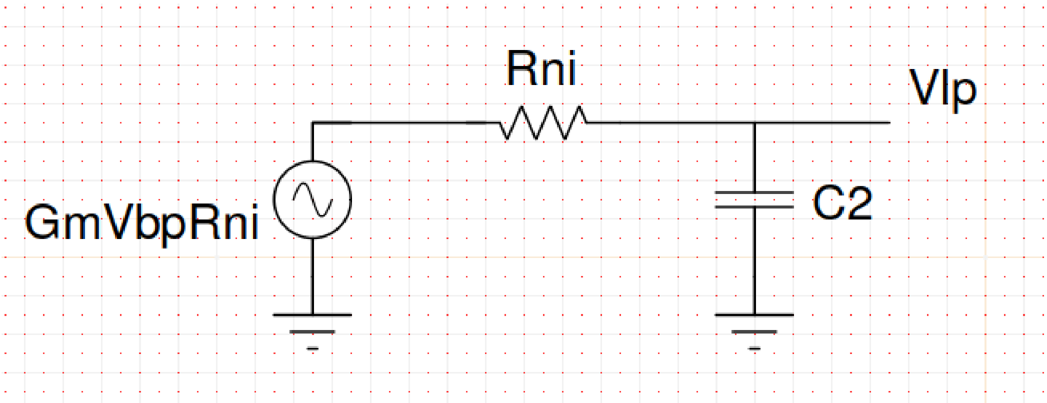
$$DC\ \ gain = 20\log(A_0) = 20\log\left(\frac{R_{LOSSY,2}}{R_{LOSSY,1}+R_{LOSSY,2}}\right) = -30\,dB$$

For passband gain, we can ignore the A_0 term. Hence the passband gain only comes from the fact that we are applying not the entire input but 0.917 times the input due to the Thevinin's equivalent. The passband gain is thus given by the relation:

$$Passband\,Gain \;=\; 20\log(0.917) \;=\; -752\,millidecibels$$

This is consistent with the output that we had observed at the bandpass node.

- At the first low pass node, we observe that there is a gain of about -279 millidecibels. Further, at the Butterworth passband edge, the gain is about -6.296dB. Similar to the badpass node, we try to prove by mathematical analysis that the above results have occured due to the lossy transconductor. The effective circuit for the low pass node from the bandpass node output can be shown to be as below:



The transfer function for the low pass node can then be written to be of the form:

$$\frac{V_{LP}(s)}{V_{in}(s)} \;=\; \frac{\dfrac{R_{LOSSY,2}}{R_{LOSSY,1}+R_{LOSSY,2}}+\dfrac{L}{R_{LOSSY,1}+R_{LOSSY,2}}s}{\dfrac{R_{LOSSY,1}LCs^2}{R_{LOSSY,1}+R_{LOSSY,2}}+\dfrac{(R_{LOSSY,1}R_{LOSSY,2}C+L)s}{R_{LOSSY,1}+R_{LOSSY,2}}+1} \;*\; \left(\frac{G_m R_{ni}}{1+R_{ni}C_2 s}\right)$$

In order to find the dc gain, we set s = 0. This gives us:

$$DC\,Gain \;=\; G_m\frac{R_{ni}*R_{LOSSY,2}}{R_{LOSSY,1}+R_{LOSSY,2}} \;=\; -282\,millidecibels$$

At the passband edge, we can make the approximation:

$$1+R_{ni}C_2 s \approx R_{ni}C_2 s$$

This in turn gives us the simpler transfer function:

$$\frac{V_{LP}(s)}{V_{in}(s)} \;=\; \frac{\dfrac{G_m L}{C_2 R_{LOSSY,1}}}{LC_1 s^2+\dfrac{L}{R_{LOSSY,1}}s+1}$$

From the above result, we observe that the passband edge is almost the same but there is a change in the quality factor since we now have a resistor of 917 ohm instead of a 1k resistor that was ideally needed. The new quality factor which is also the gain at the Butterworth passband edge is given by:

$$Q_1 = \frac{R_{LOSSY,1}}{\sqrt{(\frac{L}{C_1})}} = 0.496$$

The theoretical value of the quality factor that we had to realize was 0.541. Thus the gain at the passband edge now works out to be anout -6.09 dB while the theoretical value is -5.336 dB. To this, we also need to add the dc gain of -0.28 dB which -6.37 dB which is quite close to the experimental value.

- Finally for the observations at the output node, we obtain that it is almost close to a low pass response but the gain at the Butterworth passband edge is about -5.19 dB (expected -3 dB) and there is also a dc gain of -558 millidecibels. The reason for this can be attributed to the fact that each of the Gm – C biquads offers a dc gain of approximately -280 millidecibels (since the dc gain expression for low pass node derived earlier is independent of the L and C values, it will be same for both the biquads). Further, we can prove using similar analysis as above that the quality factor of the second biquad will also change since we are having a resistance of 917 ohm instead of ideal 1k resistor that we needed in the RLC realization. The new quality factor for the second biquad works out to be 1.1985 instead of 1.307 that is theoretically needed. The gain at the Butterworth passband edge is then given to be:

$$Passband\,Gain = 20\log(Q_1 * Q_2) + DC\,Gain = -5.081\,dB$$

This is almost in line with the simulation value. Thus, we can say that the circuit that we have designed is correct.

Conclusion:

A fourth order maximally flat low pass filter has been successfully designed and tested for the given specifications. The final results are in close proximity to the ideal values and the reasons for the minor deviations have been explained.