MAJOR PROJECT – EC498

IMPLEMENTATION OF MAJORITY LOGIC DECODING OF BLOCK CODES

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Problem Statement:

Implement a well-known algorithm that can perform multiple error detection and correction of block cyclic codes using majority logic. Study about the functioning and construction of this class of error control codes and understand the underlying mathematics and working principles of the algorithm.

Implement the algorithm first at a high level using C programming language and then realize it at a lower level using Hardware Description Languages like Verilog or VHDL. Once the simulation works correctly, synthesize the created hardware using a Field Programmable Gate Array (FPGA). Demonstrate that the algorithm works correctly by generating all possible input test combinations and verifying that the practical results match the theoretical expectations.

The encoder and decoder must be separately implemented. A physical channel must also be modelled in both simulation and hardware to create the errors.

Project Objectives:

- Knowledge on basics Error Control Coding (ECC) will be gained such as the importance of parity bits, generator and parity check matrices and parity and generating polynomials. The principles of Majority Logic Decoding (MLD) will be studied in detail and its advantages over other error controlling codes will be identified.

- Implementation of algorithms at a higher level using C programming will be done to gain practical exposure. The algorithm will then be mapped to hardware using popular HDLs and FPGA. Practical considerations like delays, complexities and timing errors will be observed and understood.

- Basics of abstract algebra will be studied including topics of Galois fields and finite geometries. The application of these concepts in error controlling codes will be studied at great length. Theorems regarding construction of majority logic decodable codes will be understood.

Workplan:

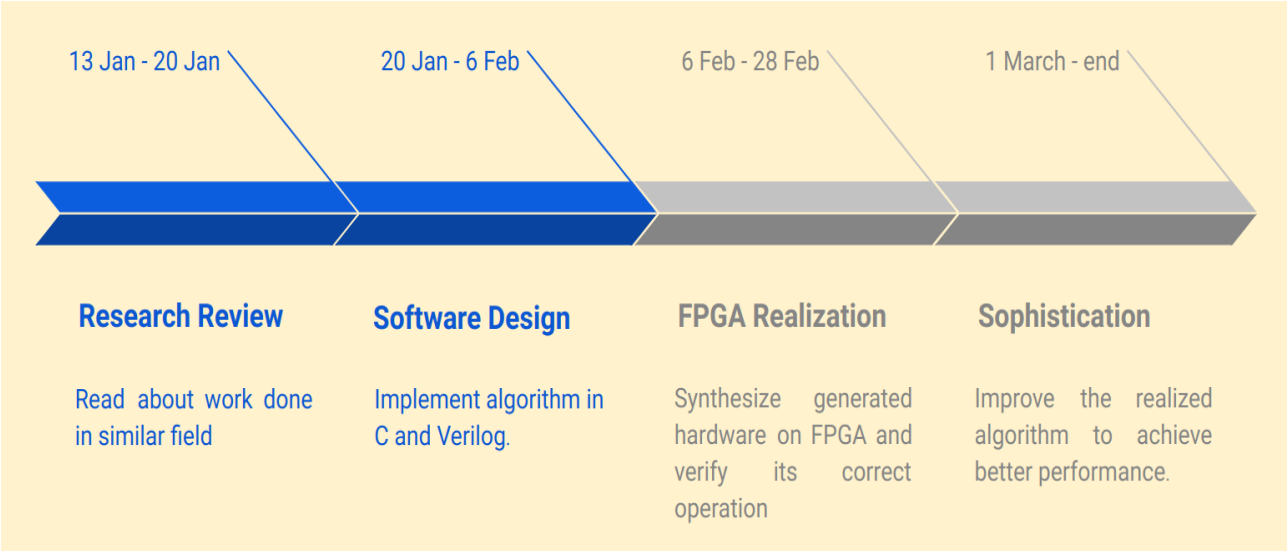
1. Go through literature to understand the theory and underlying mathematics required to design the Majority Logic Decoder. Study about the construction od error control codes that are majority logic decodable such as maximum length and difference set codes.

2. Start with implementation of one-step majority logic decodable codes in C language and FPGA. Verify its correct working by generating all possible combinations of information and error vectors. Also observe what happens when the number of errors exceeds the maximum limit. Implement both type – 1 and type – 2 MLDs.

3. Understand the need for multi-step majority logic decoders. Implement a multi-step MLD on block codes in both C and FPGA and verify its correct operation. Demonstrate the advantage of multi-step MLDs over single-step MLDs.

4. Make attempts to improve on existing architectures to achieve better performance in terms of speed and memory size occupied. Also strive to find out new classes of codes that are majority logic decodable as the available codes are very few in number.

Timeline:



References:

1. S. Lin and D.J. Costello "*Error Control Coding; Fundamentals and Applications*", Pearson 2005

2. Meera.R and Shajimon K John, "*Majority Logic Fault Detection with Difference-Set Codes for Memory Applications*", International Journal of Emerging Technologies in Computational and Applied Sciences, 5(3), June-August, 2013, pp. 227-232