Akash Sridhar

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Education

Ph.D, Computer Engineering — **Oct 2014 - Dec 2020**
University of California, Santa Cruz
GPA: 3.89
Advisor: Jose Renau
Focus: Computer Architecture

Bachelor of Engineering, Computer Science and Engineering — **June 2010 - May 2014**
Anna University, Chennai
GPA: 7.82

Awards and Honors

- **UC Regents Fellowship** (Winter 2015)
- **Graduate Student Researcher** (Fall 2014 - Dec 2020)
- **Teaching Assistant** - Computer Architecture (CSE 120 and CSE 220) (Fall 2014 - Dec 2020)
- Selected in **"TOP 50"** out of 2000 participants in the **National Level Programming Contest** conducted by ACM in 2012.

Work Experience

- **Qualcomm Inc.** - Senior Engineer, CPU Performance and Architecture **(Mar 2021 - Present)**
  - Design and devolopment of front-end microarchitecture (leading the conditional branch predictor block) of next-gen Nuvia CPUs
  - Developing performance model for image compression engine for Snapdragon SoCs
  - Working on performance projections methodologies for future generation Qualcomm processors (includes microarchitecture simulations, workload analysis)
  - Developed microbenchmarks to analyze microarchitecture of competitor devices.
- **Intel Labs** - Microarchitecture Intern (Quantum Computing Research Group) **(Summer 2020)**
  - Worked with the Quantum Computer group to restructure the simulation model to study the quantum full-stack layer and study the potential to develop a data-streaming interface for a quantum computer.
  - Created a python interface to enable the quantum functional simulation model and quantum RTL model to communicate with each other.
- **Esperanto Technologies** - Architecture Intern **(Summer 2018)**
  - Worked in developing the cycle-accurate performance simulator to research on Esperanto's throughput cores to accelerate ML/AI applications.
  - Worked on implementing the ISA and optimizing cache replacement heuristics.
- **Xilinx Inc** - FPGA Architecture Intern **(Summer 2015)**
  Developed an automated framework to study delay patterns for Ultrascale Benchmark Suite. The model was used to study the potential to break the critical delay threshold.
- **Waran Research Foundation (WARFT)** - Research intern, September 2011 to June 2014.

Skills

- **Programming:** C/C++, Python, Shell Scripting
- **Web:** JavaScript, Node.JS, PEGjs, HTML5
- **Architecture Simulator:** ESESC, WIMAC Simulator
- **Others:** GDB, perf, Valgrind, Linux/Unix, Mac OS X, Windows, Gnuplot, LaTeX

Publications

- **Load Driven Branch Predictor (LDBP)**, 2020, arXiv:2009.09064
- **LNAST: A Language Neutral Intermediate Representation for Hardware Description Languages**, WOSET 2019 (Co-located with ICCAD 2019)
- **Performance and Energy Efficient Cache System Design: Simultaneous Execution of Multiple Applications on Heterogeneous Cores**, IEEE ISVLSI 2013

Professional Activities and Memberships

- **Fellow of the Institution of Engineering and Technology (IET)**
  1) Second youngest person in the world (and the youngest Indian) to be elected as IET Fellow
- **IET Fellowship Assessor**
  1) Serves on the panel that assesses/reviews new IET Fellow nominations
- **Artifact Evaluation Committee:**
  1) IEEE/ACM International Symposium on Microarchitecture (MICRO 2022)
  2) ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS 2023)
- **Program Committee:**
  1) International Conference on High Performance Computing, Data, & Analytics (HiPC 2022)
  2) International Conference on Embedded Computer Systems: Architectures, MOdeling, and Simulation (SAMOS 2022)

Press Coverage

- Computer Architecture Prodigy: Young Computer Scientist Awarded Esteemed Engineering Honor - **entrepreneur.com, 2023**
- Computer Architect Creates History: One Of The Youngest Ever To Receive Elite Engineering Accolade - **hackernoon.com, 2023**

Academic Projects

- **LDBP: Load Driven Branch Predictor(Ph.D Thesis)** **Jan 2018 - Dec 2020**
  LDBP targets hard-to-predict branches whose outcome depends on load instructions with highly random data. These branches have a poor prediction accuracy even with current state-of-the-art TAGE-based predictors(ineffective global history).
- **Enhanced SESC (ESESC)** **Dec 2014 - Mar 2021**
  ESESC is an open-source, fast multiprocessor simulator with detailed power, thermal, and performance models for modern out-of-order multicores. ESESC is an evolution of the popular SESC simulator (Enhanced SESC) that provides many new features.
- **WiCore: A scalable, energy efficient, wide-issue core** **Jan 2016 - Dec 2017**
  Proposed WiCore, an energy-efficient wide-issue core with focus on the execution engine. WiCore breaks Pollack's rule by maintaining a sub-linear relationship between area and performance. WiCore advocates a paradigm shift from multi-cores to wide-issue single core, stressing the importance of improving single-thread performance.
- **Pyrope: A modern HDL with a live flow** **Sept 2015 - Dec 2020**
  Developed the parser and Control Flow Graph generation framework for Pyrope, a new HDL developed at MASC lab, UCSC. Pyrope is designed to leverage fluid pipelines(a variant of latency-insensitive systems developed at MASC). Pyrope is going to be open-sourced by the second half of 2020.

*** References available up on request**