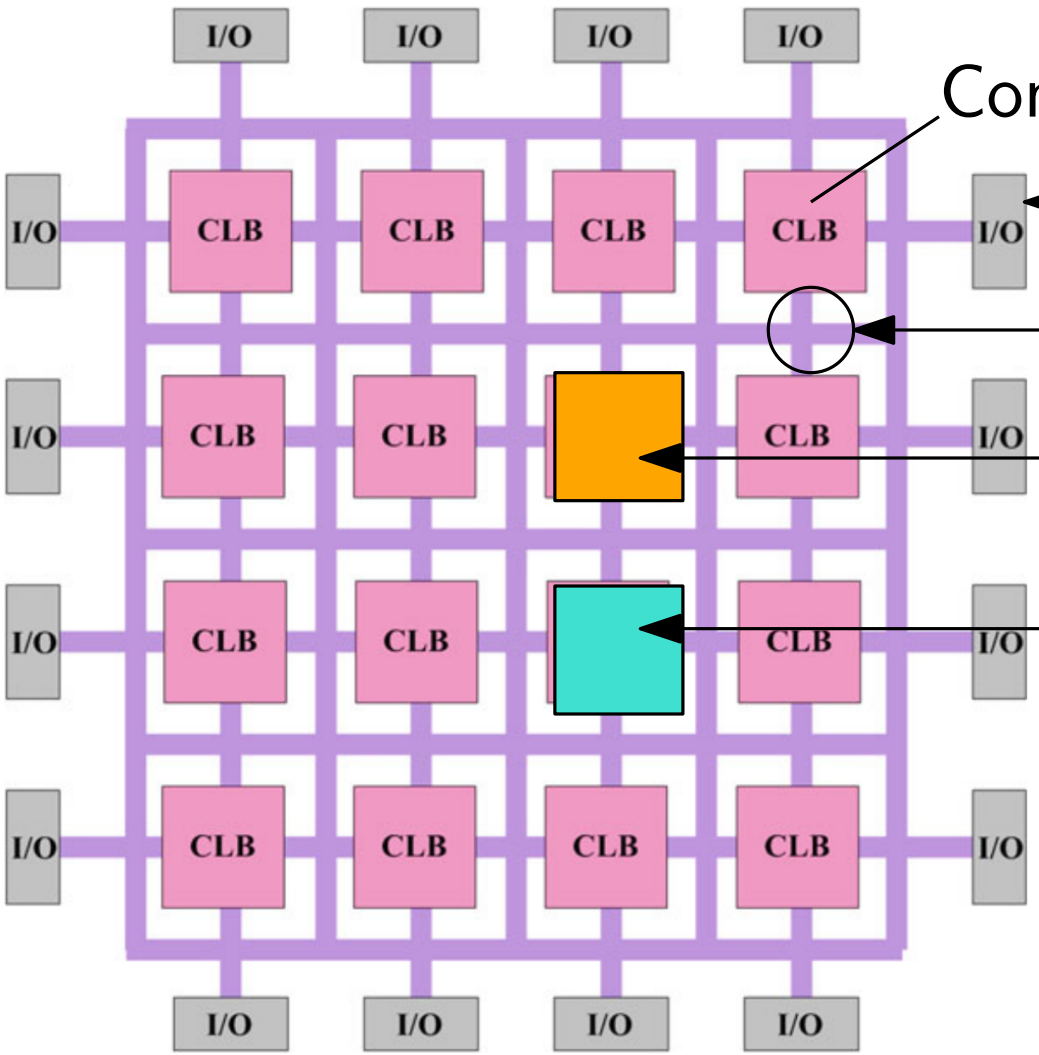
FPGAs: generic layout



Configurable Logic Blocks

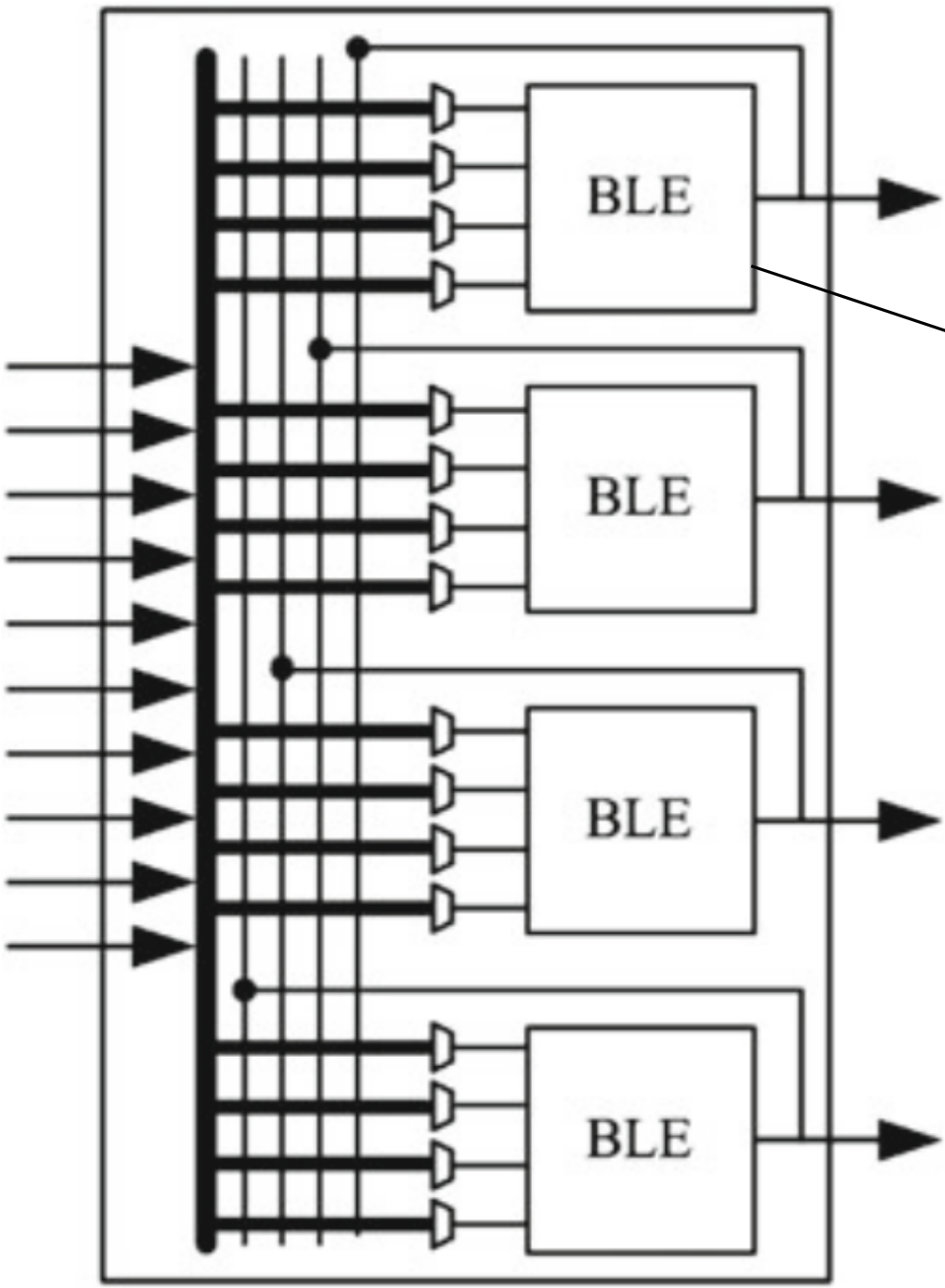
I/O Blocks

Switches / Connection Box

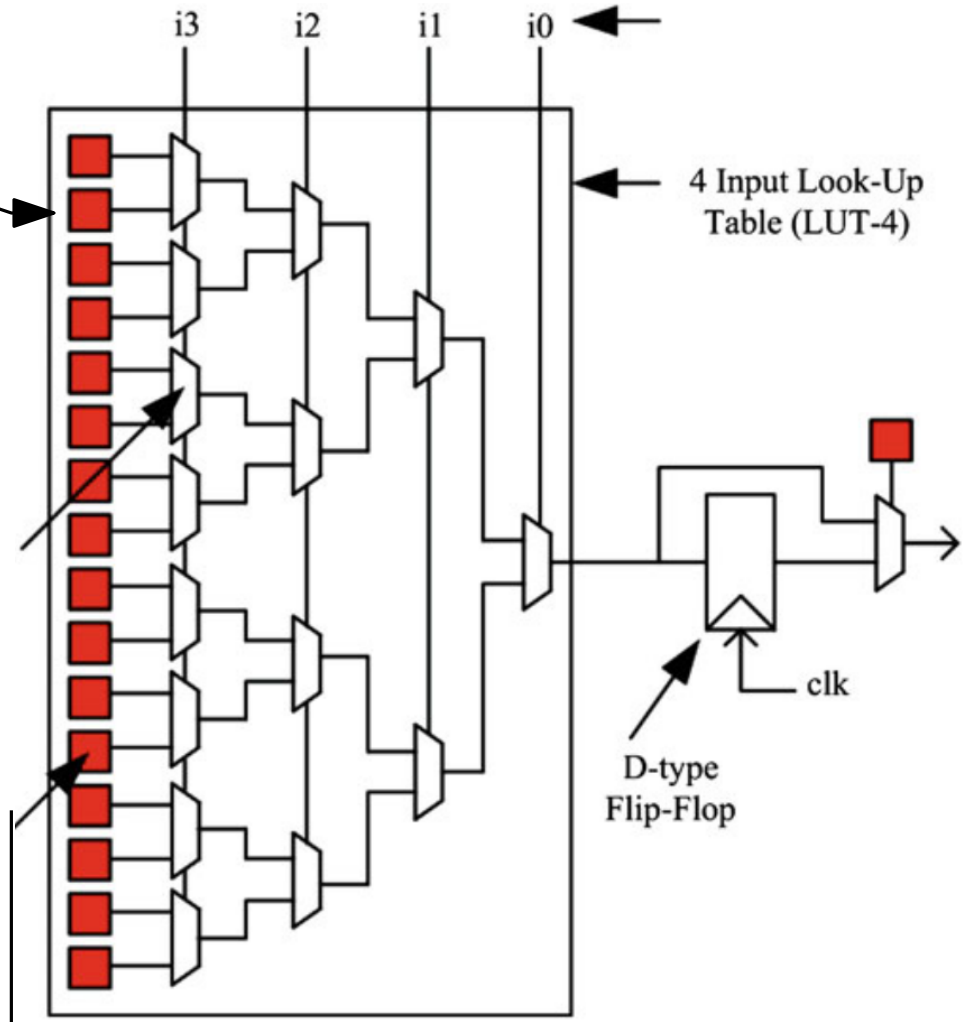
Memories (Block RAM)

DSP / Compute blocks

Configurable Logic Block (CLB)



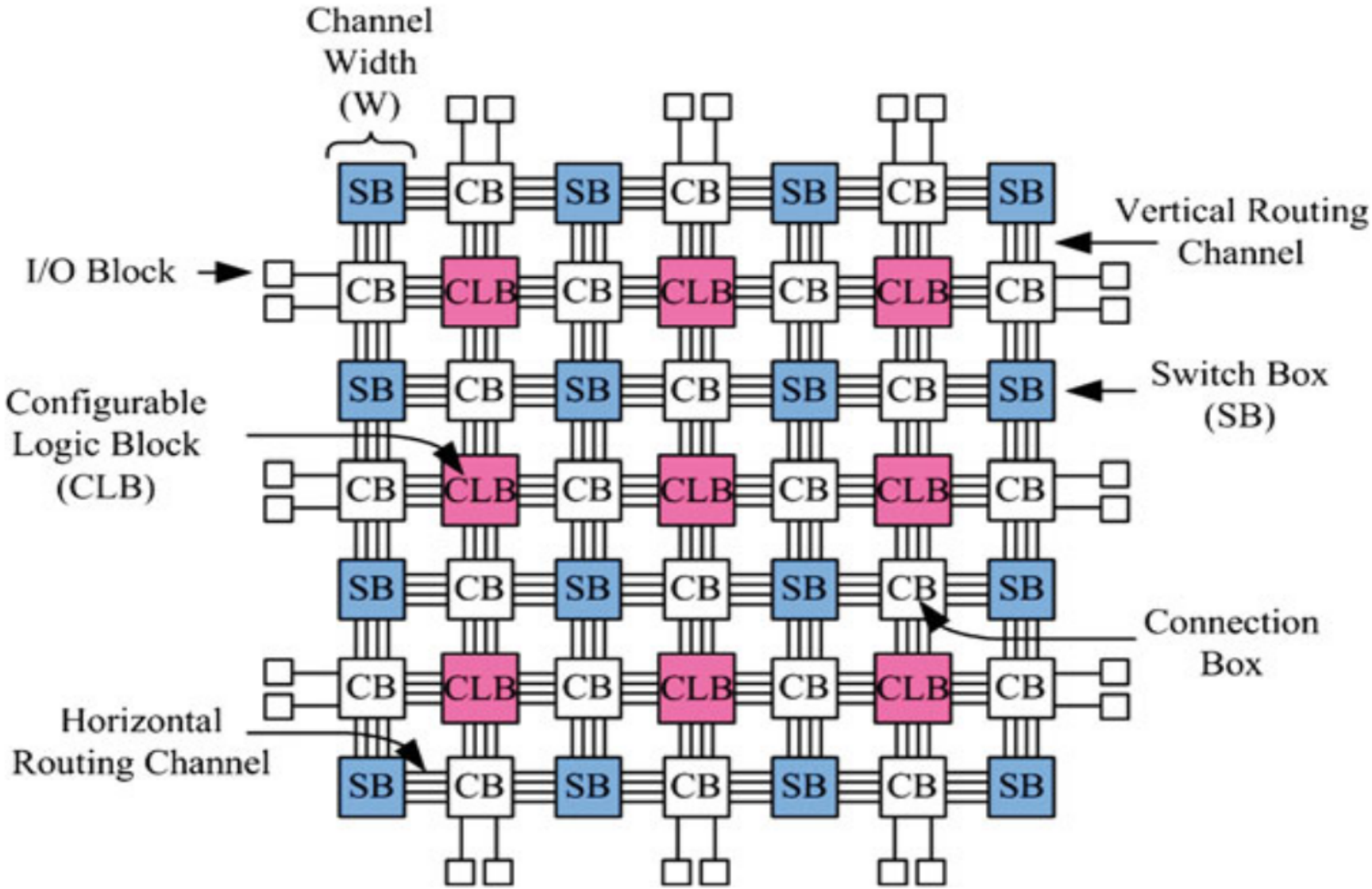
Basic Logic Element



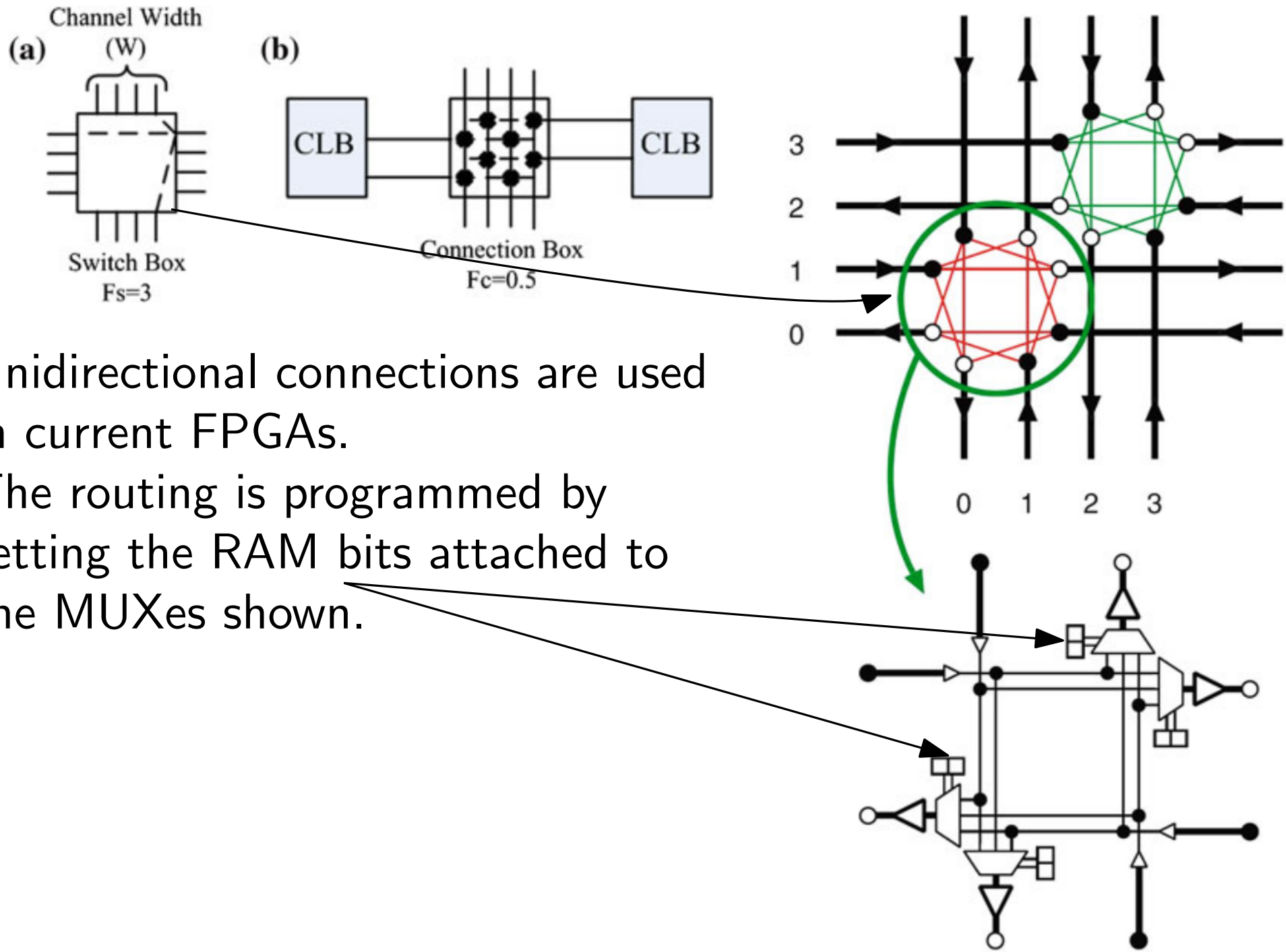
SRAM Memory Cell

Routing in FPGA

Routing takes 80%-90% of area on FPGAs!



Details of connections

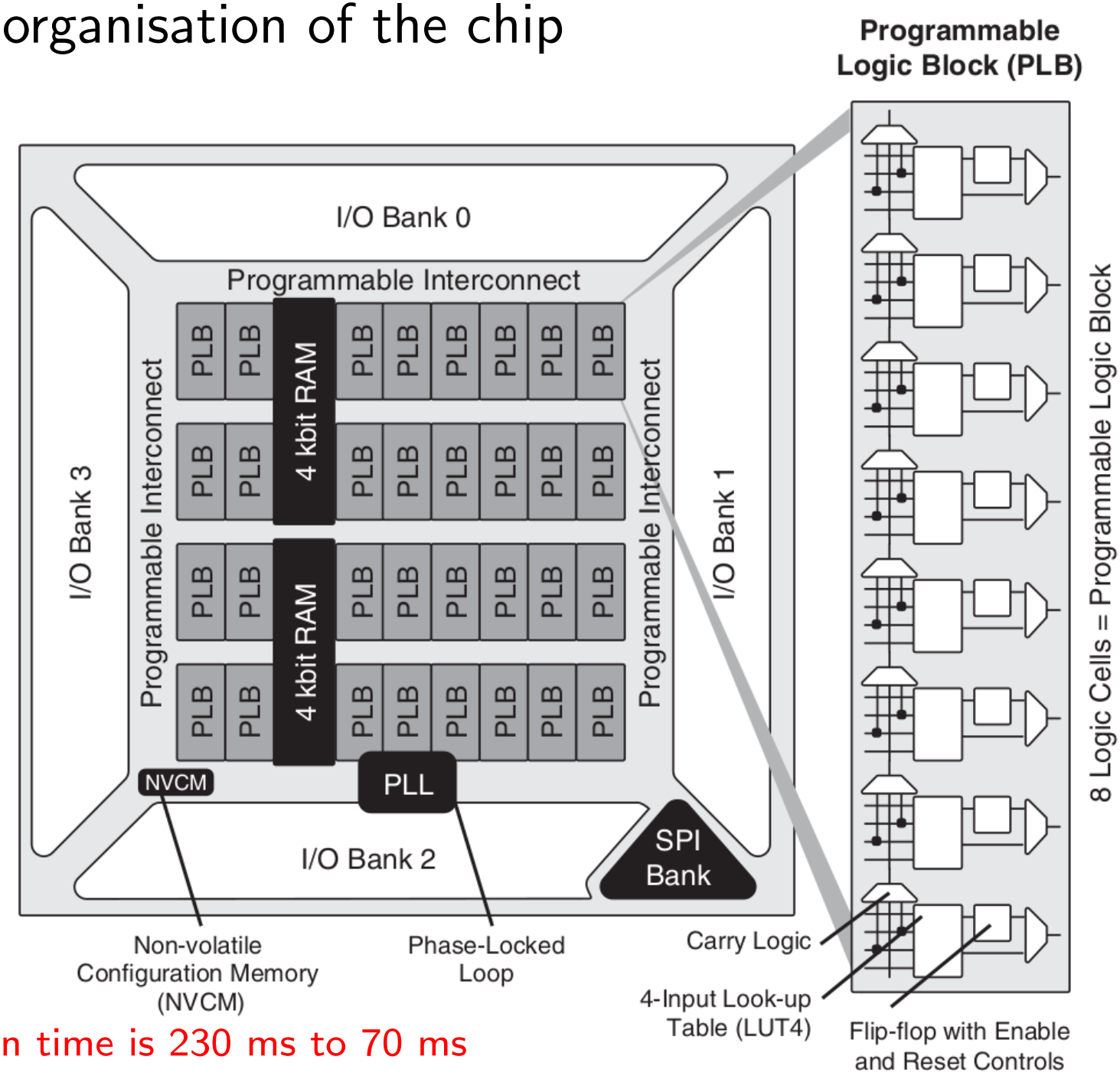


Unidirectional connections are used in current FPGAs.

The routing is programmed by setting the RAM bits attached to the MUXes shown.

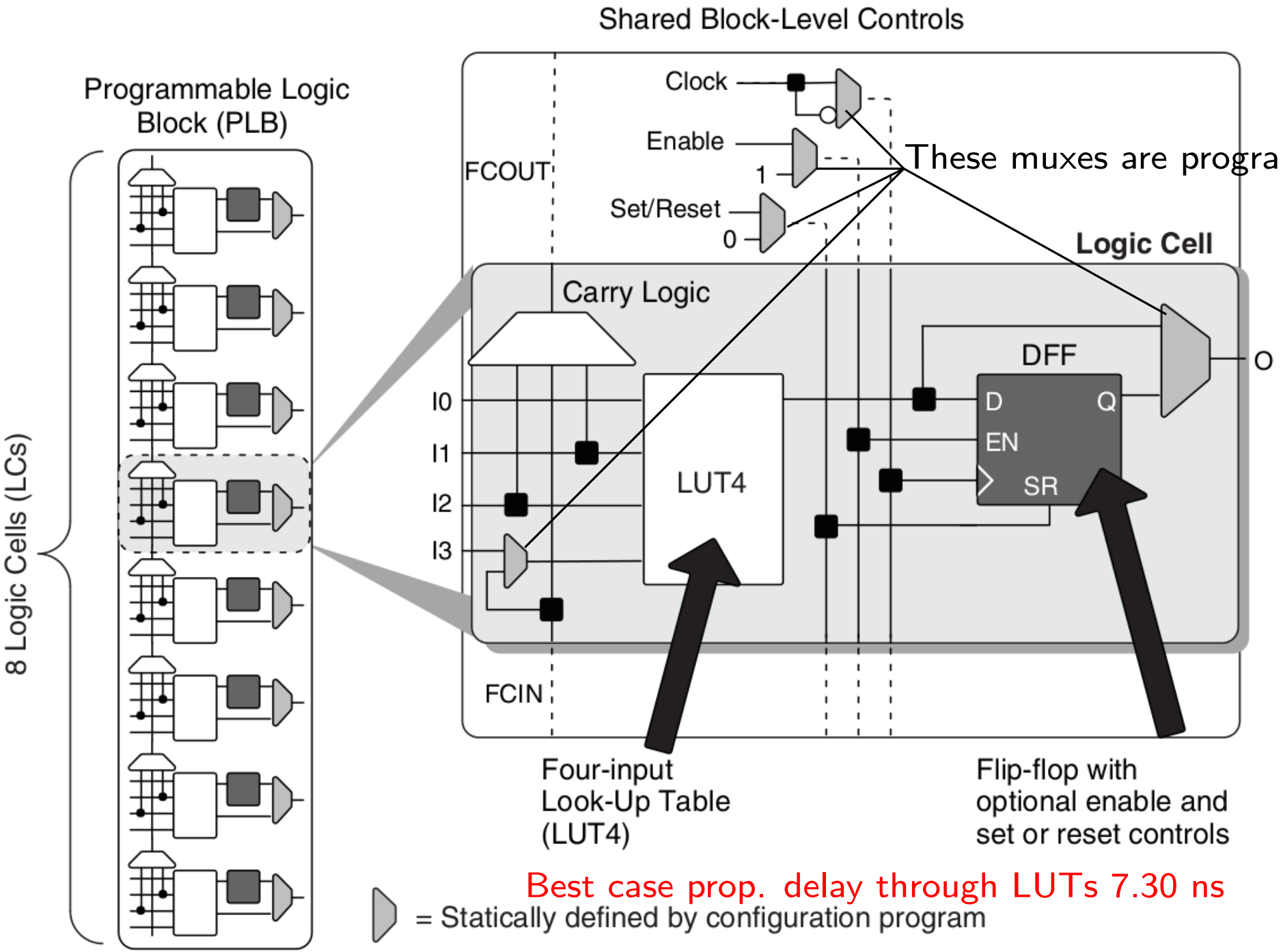
iCE40 HX8K FPGA

Overall organisation of the chip



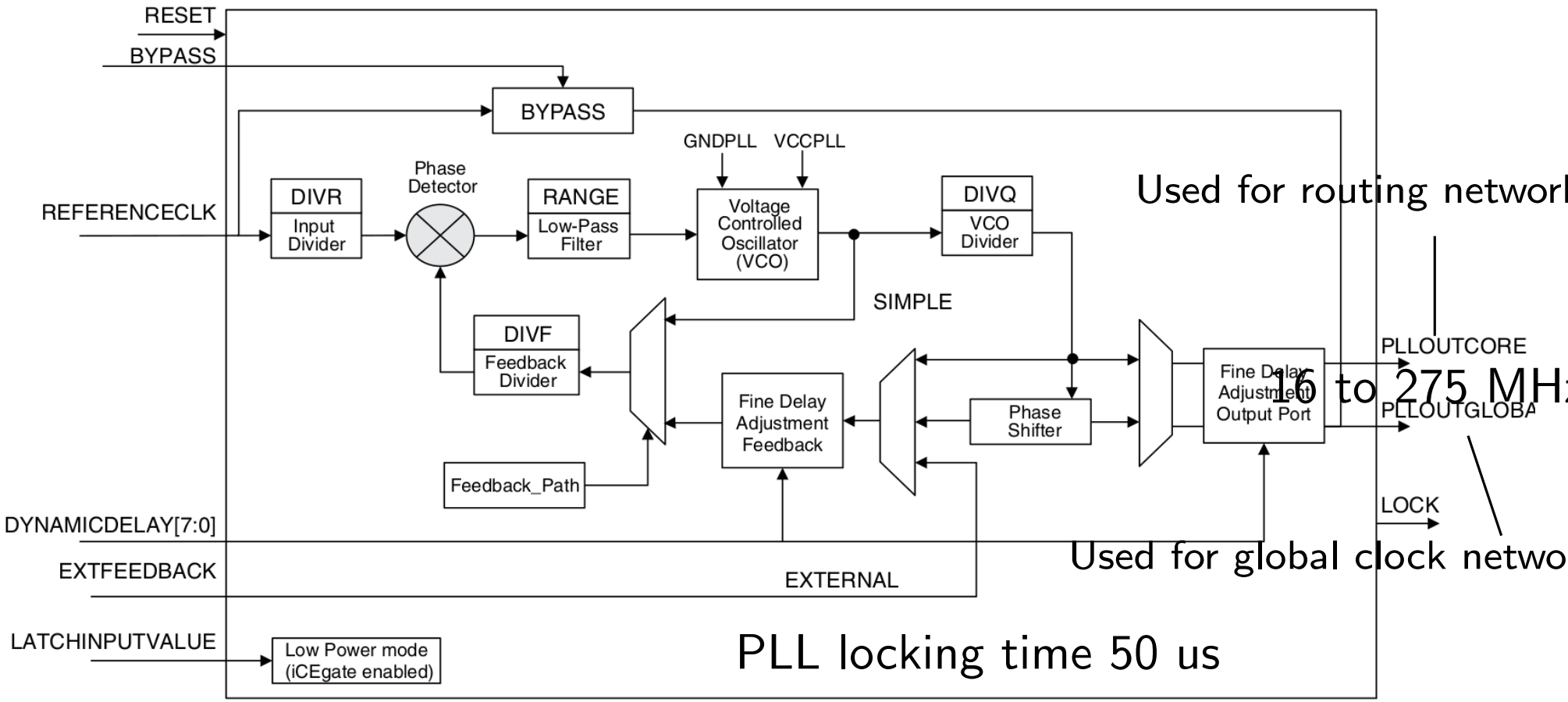
Configuration time is 230 ms to 70 ms

iCE40 HX8K - PLBs



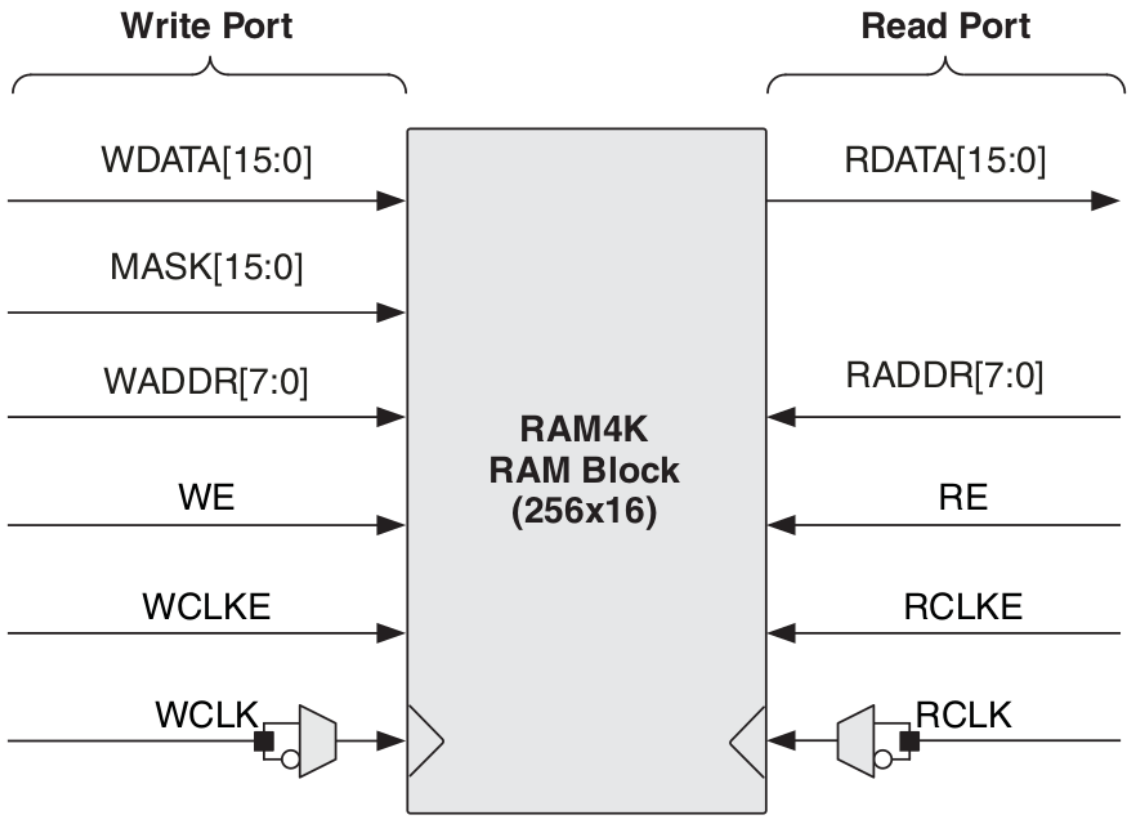
iCE40 HX8K - PLLs

- 8 global inputs and 8 global buffers
- They drive clk, reset, enable, logic values to all PLBs
- External clock can be fed to PLLs

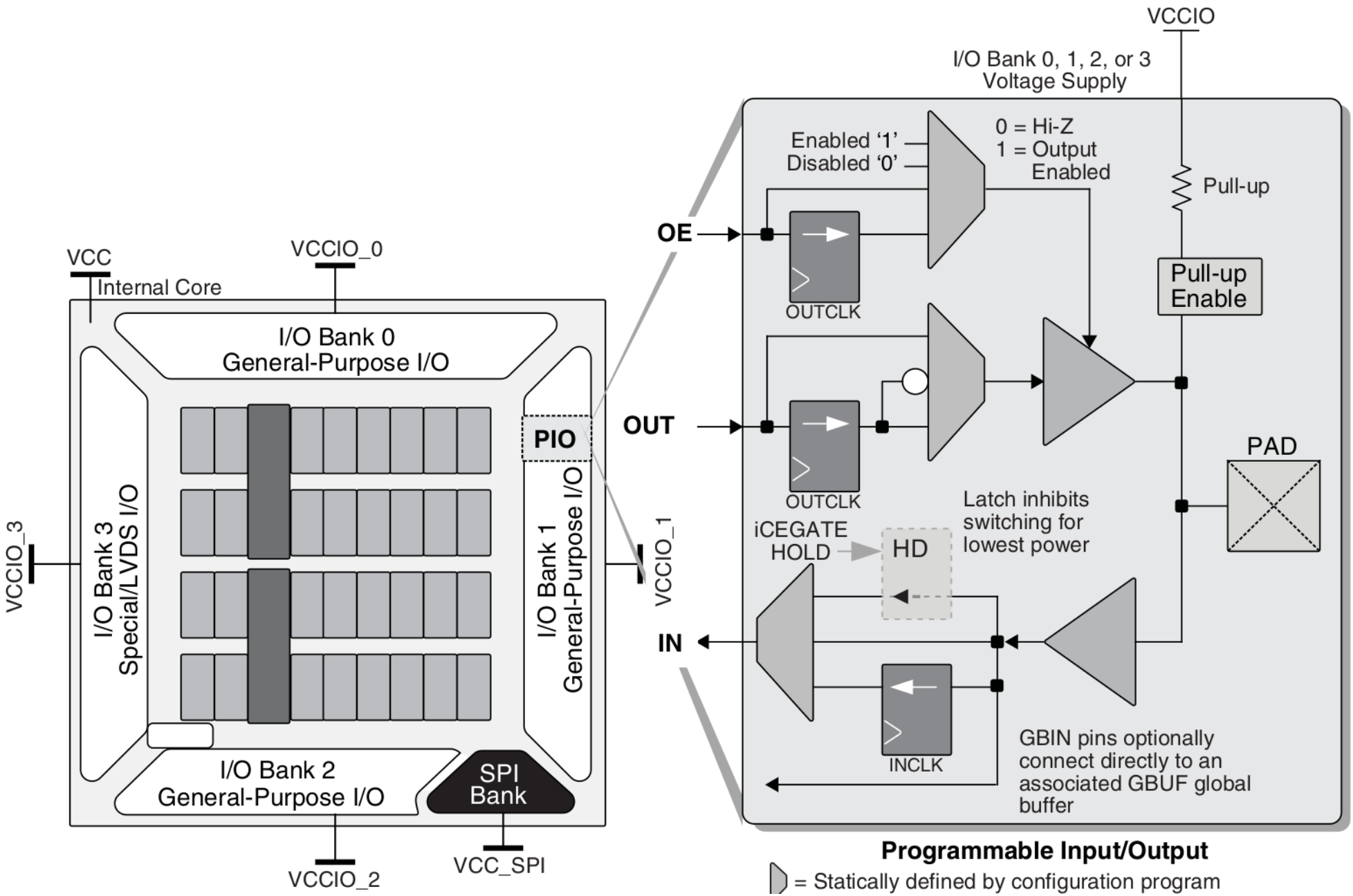


iCE40 HX8K - Block RAMs

- Embedded Block RAMs (EBR) are 4K bits in size, max freq is 400 MHz
- Can be organised in various configs (e.g. 256 locations of 16 bits each)
- These blocks can read and write at same time (pseudo dual port)

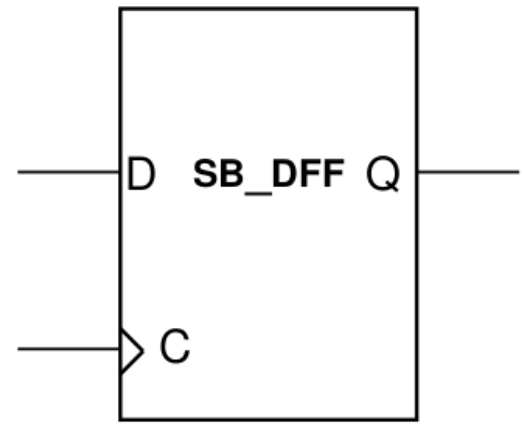


iCE40 HX8K - IO Blocks



iCE40 Library Cells: DFF

```
SB_DFF SB_DFF_inst (
       .Q(Q),                  // Registered Output
       .C(C),                  // Clock
       .D(D),                  // Data
       );
```

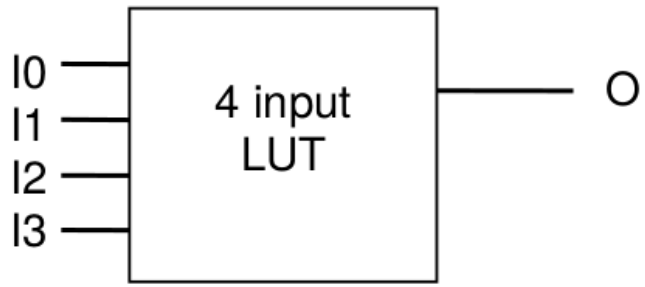


Inputs			Output
	D	**C**	**Q**
	0	↗	0
	1	↗	1
Power on State	X	X	0

Key

↗ Rising Edge
1 High logic level
0 Low logic level
X Don't care
? Unknown

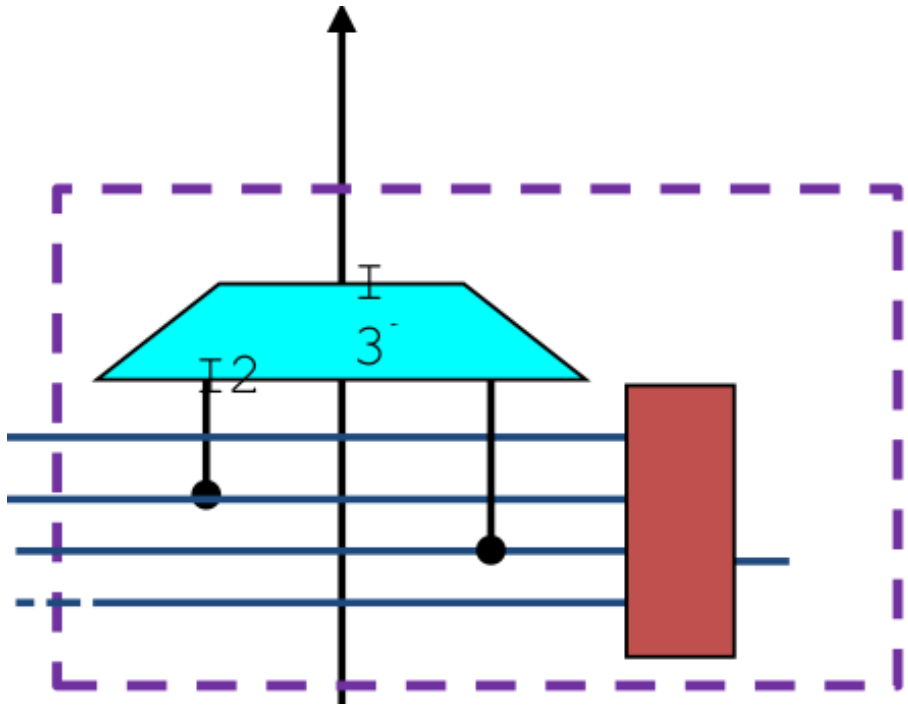
iCE40 Library Cells - SB_LUT4

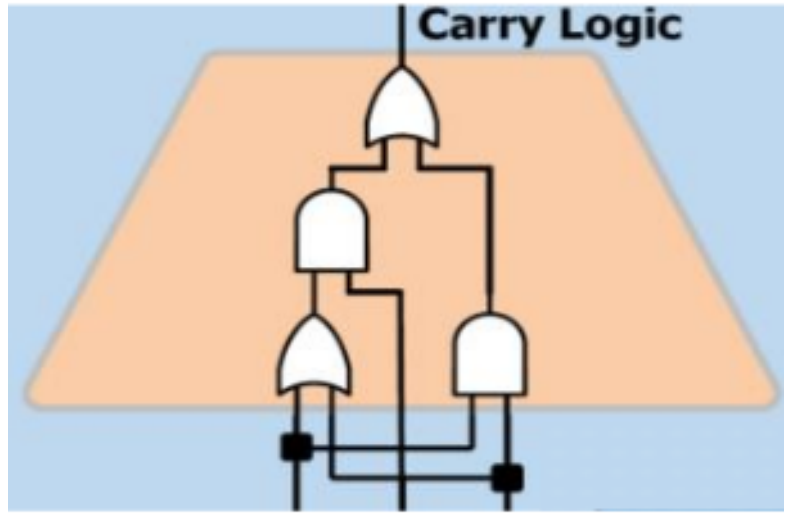


Inputs				Output
I3	I2	I1	I0	O
0	0	0	0	LUT_INIT[0]
0	0	0	1	LUT_INIT[1]
0	0	1	0	LUT_INIT[2]
0	0	1	1	LUT_INIT[3]
0	1	0	0	LUT_INIT[4]
0	1	0	1	LUT_INIT[5]
0	1	1	0	LUT_INIT[6]
0	1	1	1	LUT_INIT[7]
1	0	0	0	LUT_INIT[8]
1	0	0	1	LUT_INIT[9]
1	0	1	0	LUT_INIT[10]
1	0	1	1	LUT_INIT[11]
1	1	0	0	LUT_INIT[12]
1	1	0	1	LUT_INIT[13]
1	1	1	0	LUT_INIT[14]
1	1	1	1	LUT_INIT[15]

```
SB_LUT4      SB_LUT4_inst (
       .O (O),              // output
       .I0 (I0),            // data input 0
       .I1 (I1),            // data input 1
       .I2 (I2),            // data input 2
       .I3 (I3)             // data input 3
       );
defparam SB_LUT4_inst.LUT_INIT=16'hxxxx;
                  //LUT state initialization parameter, 16 bits.
```

iCE40 Library Cells - SB_Carry





Inputs			Output
I0	**I1**	**CI**	**CO**
0	0	X	0
0	X	0	0
X	1	1	1
X	0	0	0
1	X	1	1
1	1	X	1