Lab assignment 3 / Week 3

To be done during week 25/02/19-03/03/19.

Preparation for the lab

Please update your code with the repository. In your "intro_hdl" folder do:

```
git pull
```

Task 1. Simulation

A. Simulate example 1 (ex1.v) for event simulation and track the waveform generated. Is it correct according to the model discussed in class?
B. Provide an example of to show how monitor and display commands.

Task 2. Muxes

A. Run the testbench for mux21_1 and justify the waveform generated.
B. Synthesize the 2:1, two 2:1, 4:1 and 8:1 muxes to iCE40 FPGA (produce both .blif anf .asc files). Comment on the LUT4 used for these tasks.
C: For "case … endcase" based implementation, what is the use of "default" clause? Can you generate a test case where its utility can be seen?

Task 3. Encoder / Decoders

A. What is the use of default assignment in 8:3 encoder? Report the resource usage for when you include default statement and when you do not.
B. Write a "for" loop based priority encoder.
C. Write a 3:8 decoder using case and for statements.
D. Write a 3:6 decoder with enable signal, i.e. the output changes only when enable is high. The two unused input combinations are mapped to all zeros at the output. Compare the synthesized circuit with the one produced in part C.

Task 4. ALU

A. Write a test bench to test the ALU design provided.

Task 5. Memory

A. Write a verilog module that instantiate an array of 2-byte numbers. The length of array is 32. Fill this array with the any constant value. Synthesize the circuit and confirm the memory initialisation with ice40 layout viewer.