Chapter #1,2
Introduction

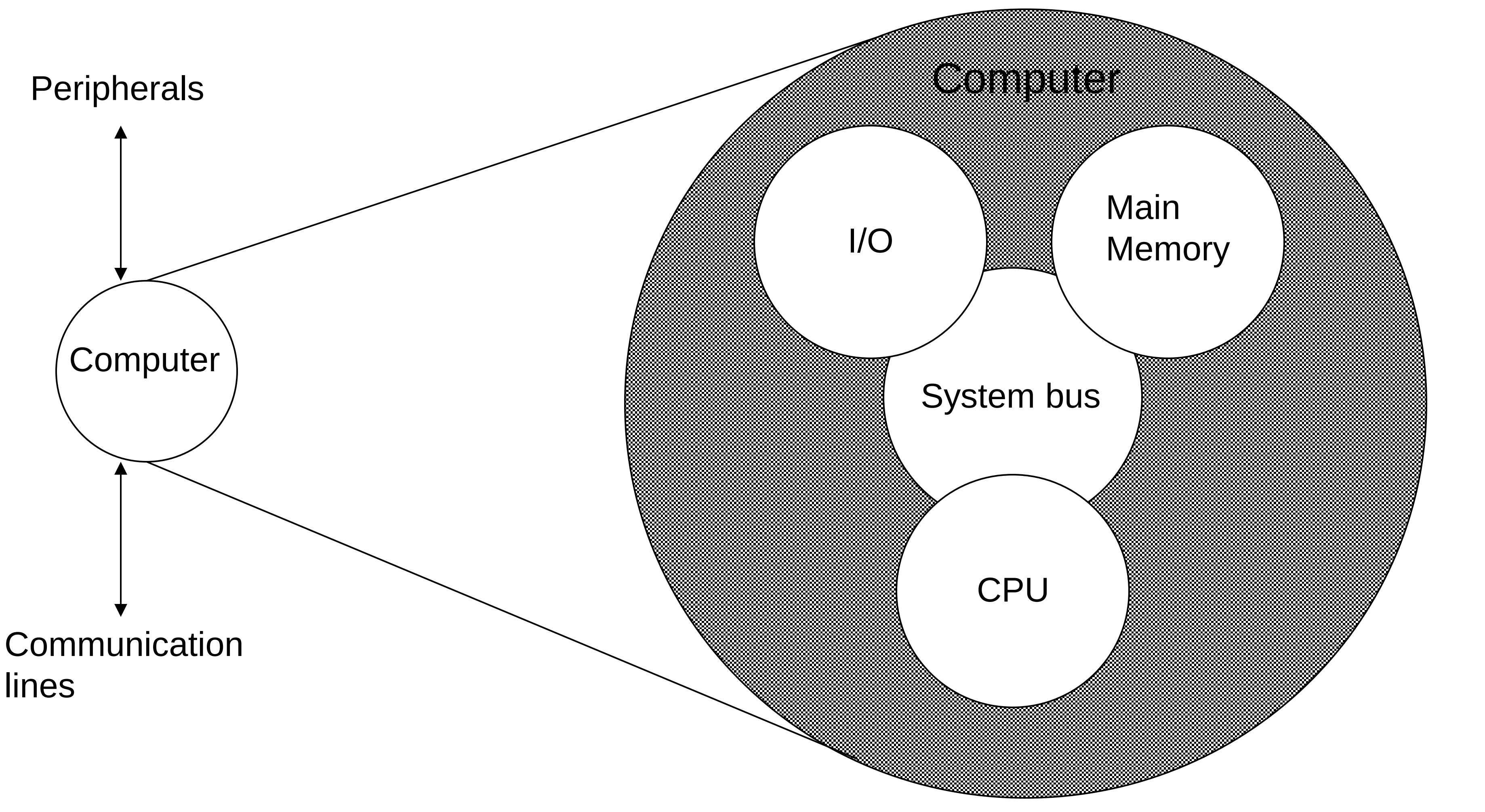
Architecture & Organization

- Architecture:
  - —Attributes visible to the programmer
  - —Instruction set, number of bits used for data representation, I/O mechanisms, addressing techniques, etc.
- Organization:
  - —How features are implemented
  - —Control signals, interfaces, memory technology
- Example:
  - —All Intel x86 CPUs share the same basic architecture
  - —Organization differs between different versions

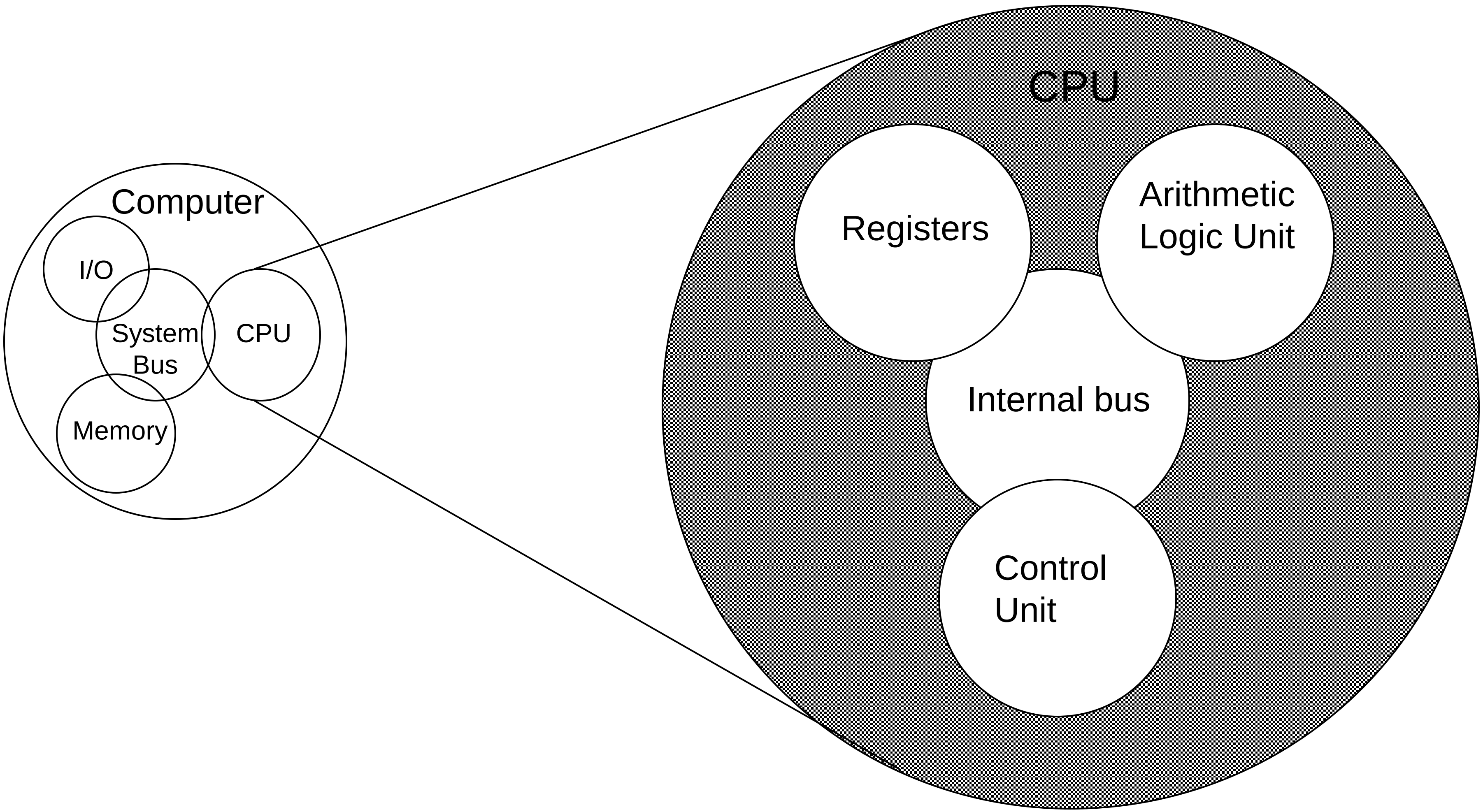
Structure & Function

- Structure:
  - Way in which components relate to each other
- Function:
  - Operation of individual components as part of the structure
  - e.g. Data processing, data storage, data movement, control

Structure - Top Level



Structure - The CPU



ENIAC – background

- What:
  - —Electronic Numerical Integrator And Computer
- Who & Where:
  - —Eckert and Mauchly, University of Pennsylvania
- Why:
  - —Trajectory tables for weapons in WW II
- When:
  - —Started in 1943
  - —Finished in 1946
    - – (WWII ended 1945)
  - —Used until 1955 to determine feasibility of hydrogen bomb

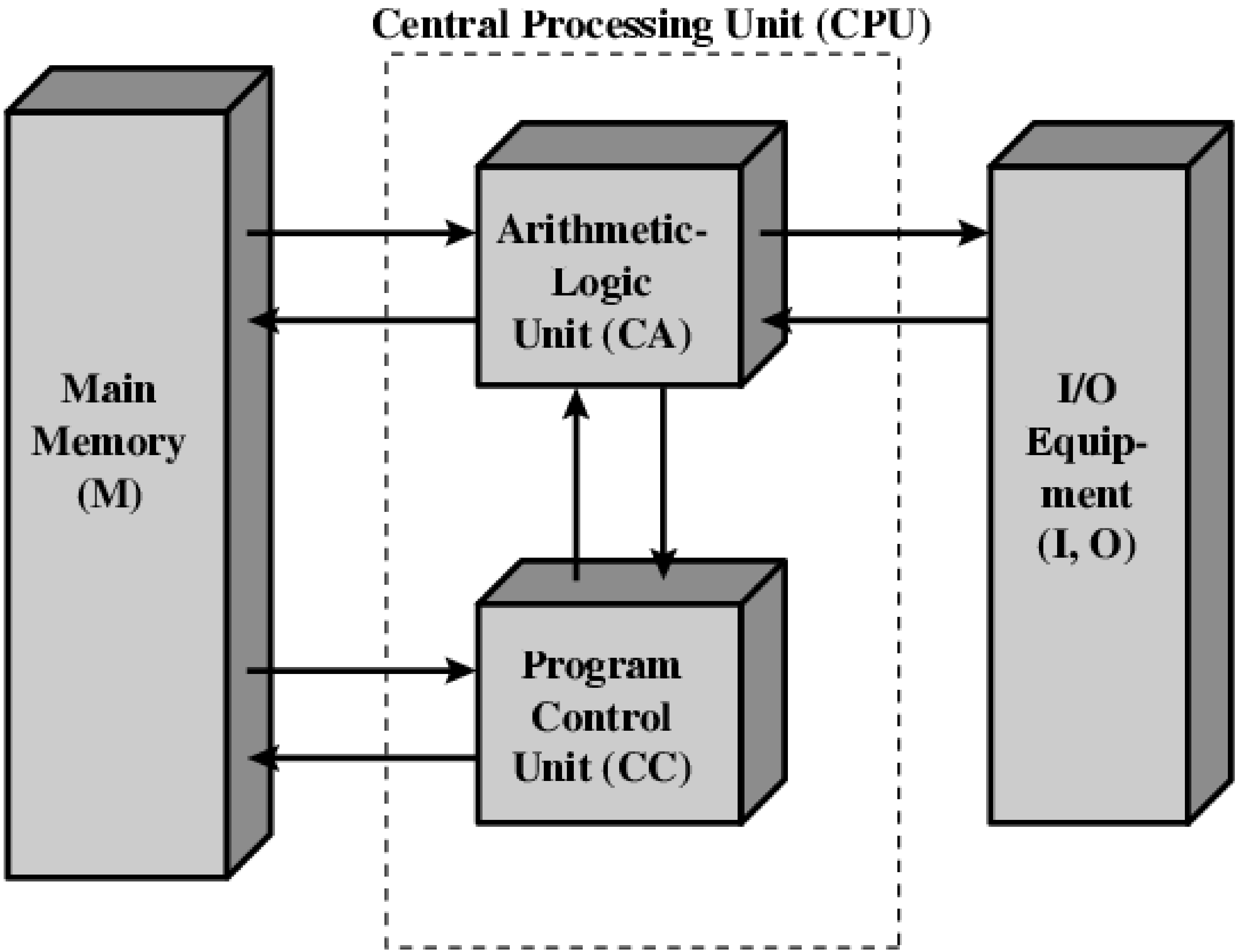
ENIAC – details

- Decimal (not binary)
- 20 accumulators of 10 digits
- Programmed manually by switches
- 18,000 vacuum tubes
- 30 tons
- 15,000 square feet
- 140 kW power consumption
- 5,000 additions per second

IAS computer/ von Neumann machine

- What:
  - —Started concept of storing a program
  - —Main memory storing programs and data
  - —ALU operating on binary data
  - —Control unit interpreting instructions from memory and executing
  - —Input and output equipment operated by control unit
- Who and Where:
  - —Von Neumann & colleagues at Princeton
- When:
  - —Started in 1946
  - —Completed in 1952

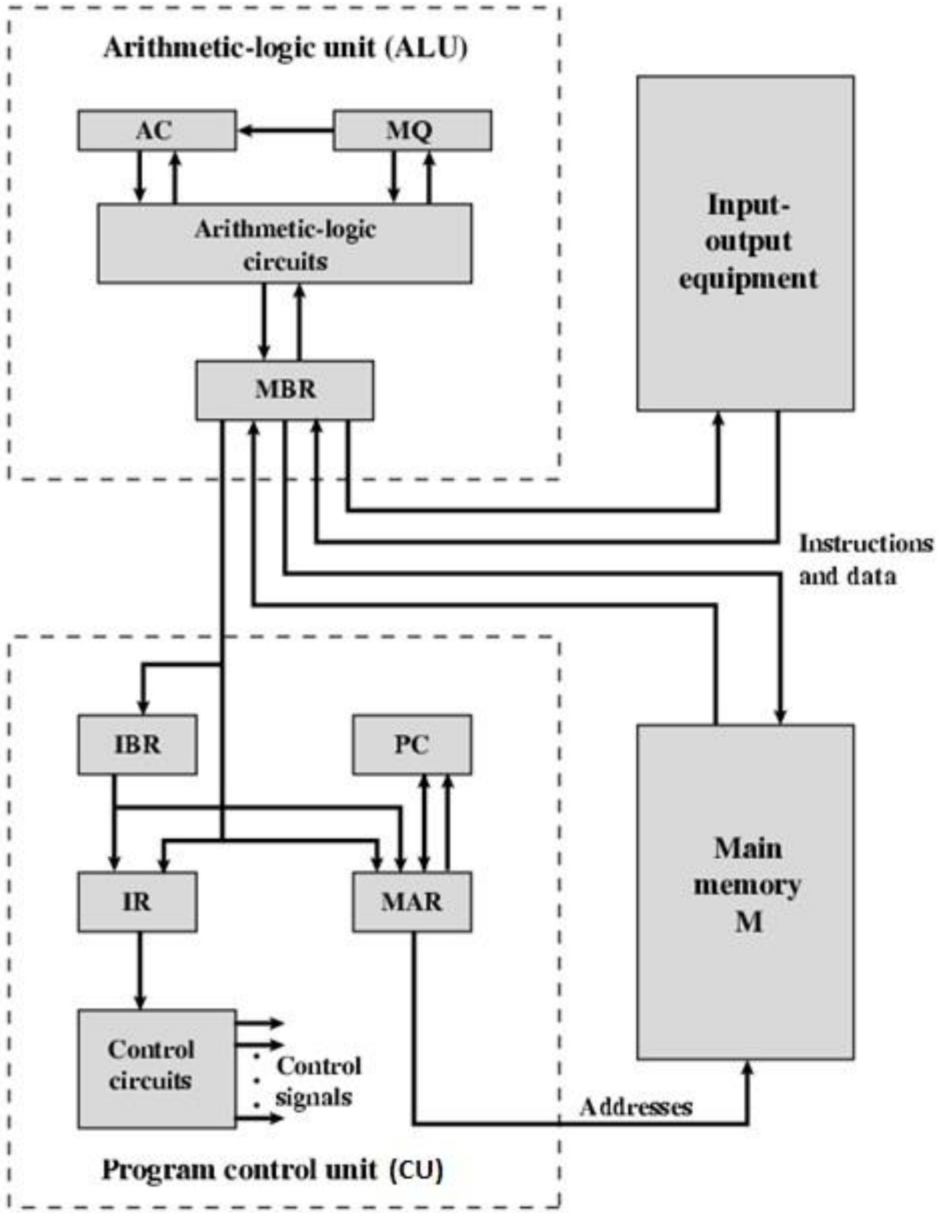
Structure of von Neumann machine



IAS - details

- 1000 x 40 bit words
  - Binary number
  - 2 x 20 bit instructions
- Set of registers (storage in CPU)
  - Memory Buffer Register
  - Memory Address Register
  - Instruction Register
  - Instruction Buffer Register
  - Program Counter
  - Accumulator
  - etc.

Structure of IAS – detail



Generations of Computers

- Vacuum tube (1946-1957)
  —40K ops/sec.
- Transistor (1958-1964)
  —200K ops/sec
- Small- /Medium-scale integration (1965-1971)
  —1M ops/sec
- Large scale integration (1972-1977)
  —10M ops/sec
- Very large scale integration (1978-1991)
  —100M ops/sec
- Ultra large scale integration (1991-?)
  —>1B ops/sec

Intel CPU's (the 4004, 80xx's)

Name	4004	8008	8080	8086	8088
Year	1971	1972	1974	1978	1979
Clock speed	108 KHz	108 KHz	2 MHz	5-10 MHz	5-8 MHz
Bus width	4 bits	8 bits	8 bits	16 bits	8 bits
# trans. (microns)	2300 (10)	3500	6000 (6)	29,000 (3)	29,000 (6)
Physical memory	640 B	16 KB	64 KB	1 MB	1 MB

Intel CPU's (the 80x86's)

Name	80286	80386TM DX	80386TM SX	80486TM DX	80486TM SX
Year	1982	1985	1988	1989	1991
Clock speed	6-12.5 MHz	16-33 MHz	16-33 MHz	25-50 MHz	16-133 MHz
Bus width	16 bits	32 bits	16 bits	32 bits	32 bits
# trans. (microns)	134,000 (1.5)	275,000 (1)	275,000 (1)	1.2M (1)	1.185M (1)
Physical memory	16 MB	4 GB	4 GB	4 GB	4 GB
Virtual memory	1 GB	64 TB	64 TB	64 TB	64 TB

Intel CPU's (the Pentium's)

Name	Pentium	Pentium Pro	Pentium II	Pentium III	Pentium IV
Year	1993	1995	1997	1999	2000
Clock speed	60-166 MHz	150-200 MHz	200-300 MHz	450-660 MHz	1.3-1.8 GHz
Bus width	32 bits	64 bits	64 bits	64 bits	64 bits
# trans. (microns)	3.1M (0.8)	5.5M (0.6)	7.5M (0.35)	9.5M (0.25)	42M (0.18)
Physical memory	4 GB	64 GB	64 GB	64 GB	64 GB
Virtual memory	64 TB	64 TB	64 TB	64 TB	64 TB

Intel CPU’s (the CORE’s)

Name	Core 2 Duo	Core 2 Quad	Core I7
Year	2006	2008	2011
Clock speed	1.2 GHz	3.0 GHz	3.5 GHz
Bus width	64 bits	64 bits	64 bits
# trans. (microns)	167M (0.065)	820M (0.045)	1170M (0.032)
Physical memory	64 GB	64 GB	64 GB
Virtual memory	64 TB	64 TB	64 TB

Performance Assessment

- Instruction execution rate
- Processor time
- MIPS (million instructions-per-second)
- MFLOPS (million floating-point instructions-per-second)
- Arithmetic mean
- Geometric mean
- Speedup

Instruction Execution Rate

- Parameters:
  - —CPI for each instruction type: CPI_i
  - —# times each instruction type I is executed: I_i
  - —Total # instructions: I

- Formula:

$$CPI = \frac{\sum_{i=1}^{n} CPI_i \times I_i}{I}$$

Measuring Processing time

- Parameters:
  - —Total # instructions: I
  - —Average cycles per instruction: CPI
  - —Cycle time: t
  - —Frequency: $f=1/t$
- Formula:

$$T=I * CPI * t = I * (CPI / f)$$

Other Performance Measures

- Total execution time: T
- Execution time for *i*th program: T_i

$$MIPS = \frac{\text{Instruction count}}{T \times 10^6} = \frac{\text{Clock rate}}{CPI \times 10^6}$$

$$MFLOPS = \frac{\text{Number of floating-point operations in a program}}{T \times 10^6}$$

$$Arithmetic\ mean = \frac{1}{n}\sum_{i=1}^{n} T_i$$

$$Geometric\ mean = \sqrt[n]{\prod_{i=1}^{n} T_i}$$

Speedup (Amdahl's Law)

$$\text{Speedup} = \frac{Execution\ time\ before\ enhancement}{Execution\ time\ after\ enhancement}$$

Speedup for fraction of time f with speedup factor SU_f :

$$S = \frac{1}{(1-f) + \frac{f}{SU_f}}$$

Speedup with multiple fractional enhancements f_1 , f_2 , ... , f_n and individual speedups $SU_1, SU_2, \ldots, SU_n$:

$$S = \frac{1}{[1-(f_1+f_2+\cdots+f_n)] + \frac{f_1}{SU_1} + \frac{f_2}{SU_2} + \cdots + \frac{f_n}{SU_n}}$$