DIGITAL SYSTEM DESIGN

QUESTION BANK WITH ANSWER & EXPLANATION

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Counter

1. In digital logic, a counter is a device which _____
a) Counts the number of outputs
b) Stores the number of times a particular event or process has occurred
c) Stores the number of times a clock pulse rises and falls
d) Counts the number of inputs

Answer: b
Explanation: In digital logic and computing, a counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal.

2. A counter circuit is usually constructed of _____
a) A number of latches connected in cascade form
b) A number of NAND gates connected in cascade form
c) A number of flip-flops connected in cascade
d) A number of NOR gates connected in cascade form

Answer: c
Explanation: A counter circuit is usually constructed of a number of flip-flops connected in cascade. Preferably, JK Flip-flops are used to construct counters and registers.

3. What is the maximum possible range of bit-count specifically in n-bit binary counter consisting of 'n' number of flip-flops?
a) 0 to 2^n
b) 0 to $2^n + 1$
c) 0 to $2^n - 1$
d) 0 to $2^{n+1/2}$

Answer: c
Explanation: The maximum possible range of bit-count specifically in n-bit binary counter consisting of 'n' number of flip-flops is 0 to 2^n-1. For say, there is a 2-bit counter, then it will count till 2^2-1 = 3. Thus, it will count from 0 to 3.

4. How many types of the counter are there?
a) 2
b) 3
c) 4
d) 5

Answer: b
Explanation: Counters are of 3 types, namely, (i)asynchronous/synchronous, (ii)single and multi-mode & (iii)modulus counter. These further can be subdivided into Ring Counter, Johnson Counter, Cascade Counter, Up/Down Counter and such like.

5. A decimal counter has _____ states.
a) 5
b) 10
c) 15
d) 20

Answer: b
Explanation: Decimal counter is also known as 10 stage counter. So, it has 10 states. It is also known as Decade Counter counting from 0 to 9.

6. Ripple counters are also called _____
a) SSI counters
b) Asynchronous counters
c) Synchronous counters
d) VLSI counters

Answer: b
Explanation: Ripple counters are also called asynchronous counter. In Asynchronous counters, only the first flip-flop is connected to an external clock while the rest of the flip-flops have their preceding flip-flop output as clock to them.

7. Synchronous counter is a type of _____
a) SSI counters
b) LSI counters
c) MSI counters
d) VLSI counters

Answer: c
Explanation: Synchronous Counter is a Medium Scale Integrated (MSI). In Synchronous Counters, the clock pulse is supplied to all the flip-flops simultaneously.

8. Three decade counter would have _____
a) 2 BCD counters
b) 3 BCD counters
c) 4 BCD counters
d) 5 BCD counters

Answer: b
Explanation: Three decade counter has 30 states and a BCD counter has 10 states. So, it would require 3 BCD counters. Thus, a three decade counter will count from 0 to 29.

9. BCD counter is also known as _____
a) Parallel counter
b) Decade counter
c) Synchronous counter
d) VLSI counter

Answer: b
Explanation: BCD counter is also known as decade counter because both have the same number of stages and both count from 0 to 9.

10. The parallel outputs of a counter circuit represent the _____
a) Parallel data word
b) Clock frequency
c) Counter modulus
d) Clock count

Answer: d
Explanation: The parallel outputs of a counter circuit represent the clock count. A counter counts the number of times an event takes place in accordance to the clock pulse.

Asynchronous Counter

1. How many natural states will there be in a 4-bit ripple counter?
a) 4
b) 8
c) 16
d) 32

Answer: c
Explanation: In an n-bit counter, the total number of states = 2^n.
Therefore, in a 4-bit counter, the total number of states = 2^4 = 16 states.

2. A ripple counter's speed is limited by the propagation delay of _____
a) Each flip-flop
b) All flip-flops and gates
c) The flip-flops only with gates
d) Only circuit gates

Answer: a
Explanation: A ripple counter is something that is derived by other flip-flops. It's like a series of Flip Flops. Output of one FF becomes the input of the next. Because ripple counter is composed of FF only and no gates are there other than FF, so only propagation delay of FF will be taken into account. Propagation delay refers to the amount of time taken in producing an output when the input is altered.

3. One of the major drawbacks to the use of asynchronous counters is that _____
a) Low-frequency applications are limited because of internal propagation delays
b) High-frequency applications are limited because of internal propagation delays
c) Asynchronous counters do not have major drawbacks and are suitable for use in high- and low-frequency counting applications
d) Asynchronous counters do not have propagation delays, which limits their use in high-frequency applications

Answer: b
Explanation: One of the major drawbacks to the use of asynchronous counters is that High-frequency applications are limited because of internal propagation delays. Propagation delay refers to the amount of time taken in producing an output when the input is altered.

4. Internal propagation delay of asynchronous counter is removed by _____
a) Ripple counter
b) Ring counter
c) Modulus counter
d) Synchronous counter

Answer: d
Explanation: Propagation delay refers to the amount of time taken in producing an output when the input is altered. Internal propagation delay of asynchronous counter is removed by

synchronous counter because clock input is given to each flip-flop individually in synchronous counter.

5. What happens to the parallel output word in an asynchronous binary down counter whenever a clock pulse occurs?
a) The output increases by 1
b) The output decreases by 1
c) The output word increases by 2
d) The output word decreases by 2

Answer: b
Explanation: In an asynchronous counter, there isn't any clock input. The output of 1^{st} flip-flop is given to second flip-flop as clock input. So, in case of binary down counter the output word decreases by 1.

6. How many flip-flops are required to construct a decade counter?
a) 4
b) 8
c) 5
d) 10

Answer: a
Explanation: Number of flip-flop required is calculated by this formula: $2^{(n-1)} <= N< = 2^n$.
$2^4=16 and 2^3=8$, therefore, 4 flip flops needed.

7. The terminal count of a typical modulus-10 binary counter is _____
a) 0000
b) 1010
c) 1001
d) 1111

Answer: c
Explanation: A binary counter counts or produces the equivalent binary number depending on the cycles of the clock input. Modulus-10 means count from 0 to 9. So, the terminal count is 9 (1001).

8. How many different states does a 3-bit asynchronous counter have?
a) 2
b) 4
c) 8
d) 16

Answer: c
Explanation: In a n-bit counter, the total number of states = 2^n.
Therefore, in a 3-bit counter, the total number of states = 2^3 = 8 states.

9. A 5-bit asynchronous binary counter is made up of five flip-flops, each with a 12 ns propagation delay. The total propagation delay (tp(total)) is _____

a) 12 ms
b) 24 ns
c) 48 ns
d) 60 ns

Answer: d
Explanation: Since a counter is constructed using flip-flops, therefore, the propagation delay in the counter occurs only due to the flip-flops. Each bit has propagation delay = 12ns. So, 5 bits = 12ns * 5 = 60ns.

10. An asynchronous 4-bit binary down counter changes from count 2 to count 3. How many transitional states are required?
a) 1
b) 2
c) 8
d) 15

Answer: d
Explanation: Transitional state is given by $(2^n - 1)$. Since, it's a 4-bit counter, therefore, transition states = $2^4 - 1 = 15$. So, total transitional states are 15.

11. A 4-bit ripple counter consists of flip-flops, which each have a propagation delay from clock to Q output of 15 ns. For the counter to recycle from 1111 to 0000, it takes a total of _____
a) 15 ns
b) 30 ns
c) 45 ns
d) 60 ns

Answer: d
Explanation: Since a counter is constructed using flip-flops, therefore, the propagation delay in the counter occurs only due to the flip-flops. One bit change is 15 ns, so 4-bit change = 15 * 4 = 60.

12. Three cascaded decade counters will divide the input frequency by _____
a) 10
b) 20
c) 100
d) 1000

Answer: d
Explanation: Decade counter has 10 states. So, three decade counters are cascaded i.e. 10*10*10=1000 states.

13. A ripple counter's speed is limited by the propagation delay of _____
a) Each flip-flop
b) All flip-flops and gates

c) The flip-flops only with gates
d) Only circuit gates

Answer: a
Explanation: A ripple counter is something that is derived by other flip-flops. Its like a series of Flip Flops. Output of one FF becomes the input of the next. Because ripple counter is composed of FF only and no gates are there other than FF, so only propagation delay of FF will be taken into account. Propagation delay refers to the amount of time taken in producing an output when the input is altered.

14. A 4-bit counter has a maximum modulus of _____
a) 3
b) 6
c) 8
d) 16

Answer: d
Explanation: In a n-bit counter, the total number of states = 2^n.
Therefore, in a 4-bit counter, the total number of states = 2^4 = 16 states.

15. A principle regarding most display decoders is that when the correct input is present, the related output will switch _____
a) HIGH
b) To high impedance
c) To an open
d) LOW

Answer: d
Explanation: A principle regarding most display decoders is that when the correct input is present, the related output will switch LOW. Since it's an active-low device.

Asynchronous down counter

1. Which of the following statements are true?
a) Asynchronous events does not occur at the same time
b) Asynchronous events are controlled by a clock
c) Synchronous events does not need a clock to control them
d) Only asynchronous events need a control clock

Answer: a
Explanation: Asynchronous events does not occur at the same time because of propagation delay and they do need a clock pulse to trigger them. Whereas, synchronous events occur in presence of clock pulse.

2. A down counter using n-flip-flops count _____
a) Downward from a maximum count
b) Upward from a minimum count
c) Downward from a minimum to maximum count
d) Toggles between Up and Down count

Answer: a
Explanation: As the name suggests down counter means counting occurs from a higher value to lower value (i.e. (2^n – 1) to 0).

3. UP Counter is _____
a) It counts in upward manner
b) It count in down ward manner
c) It counts in both the direction
d) Toggles between Up and Down count

Answer: a
Explanation: UP counter counts in an upward manner from 0 to $(2^n – 1)$.

4. DOWN counter is _____
a) It counts in upward manner
b) It count in downward manner
c) It counts in both the direction
d) Toggles between Up and Down count

Answer: b
Explanation: DOWN counter counts in a downward manner from $(2^n – 1)$ to 0.

5. How many different states does a 3-bit asynchronous down counter have?
a) 2
b) 4
c) 6
d) 8

Answer: d
Explanation: In a n-bit counter, the total number of states = 2^n.
Therefore, in a 3-bit counter, the total number of states = 2^3 = 8 states.

6. In a down counter, which flip-flop doesn't toggle when the inverted output of the preceeding flip-flop goes from HIGH to LOW.
a) MSB flip-flop
b) LSB flip-flop
c) Master slave flip-flop
d) Latch

Answer: b
Explanation: Since the LSB flip-flop changes its state at each negative transition of clock. That is why LSB flip-flop doesn't have toggle.

7. In a 3-bit asynchronous down counter, the initial content is _____
a) 000
b) 111
c) 010
d) 101

Answer: a
Explanation: Initially, all the flip-flops are RESET. So, the initial content is 000. At the first negative transition of the clock, the counter content becomes 101.

8. In a 3-bit asynchronous down counter, at the first negative transition of the clock, the counter content becomes _____
a) 000
b) 111
c) 101
d) 010

Answer: b
Explanation: Since, in the down counter, the counter content is decremented by 1 for every negative transition. Hence, in a 3-bit asynchronous down counter, at the first negative transition of the clock, the counter content becomes 111.

9. In a 3-bit asynchronous down counter, at the first negative transition of the clock, the counter content becomes _____
a) 000
b) 111
c) 101
d) 010

Answer: c
Explanation: Since, in the down counter, the counter content is decremented by 1 for every

negative transition. Hence, in a 3-bit asynchronous down counter, at the first negative transition of the clock, the counter content becomes 101.

10. The hexadecimal equivalent of 15,536 is _____
a) 3CB0
b) 3C66
c) 63C0
d) 6300

Answer: a
Explanation: You just divide the number by 16 at the end and store the remainder from bottom to top.

11. In order to check the CLR function of a counter _____
a) Apply the active level to the CLR input and check all of the Q outputs to see if they are all in their reset state
b) Ground the CLR input and check to be sure that all of the Q outputs are LOW
c) Connect the CLR input to Vcc and check to see if all of the Q outputs are HIGH
d) Connect the CLR to its correct active level while clocking the counter; check to make sure that all of the Q outputs are toggling

Answer: a
Explanation: CLR stands for clearing or resetting all states of flip-flop. In order to check the CLR function of a counter, apply the active level to the CLR input and check all of the Q outputs to see if they are all in their reset state.

Ripple Counter

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on "Propagation Delay in Ripple Counter".

1. Modulus refers to _____
a) A method used to fabricate decade counter units
b) The modulus of elasticity, or the ability of a circuit to be stretched from one mode to another
c) An input on a counter that is used to set the counter state, such as UP/DOWN
d) The maximum number of states in a counter sequence

Answer: d
Explanation: Modulus is defined as the maximum number of stages/states a counter has. It is independent of the number of states the counter will actually traverse.

2. A sequential circuit design is used to _____
a) Count up
b) Count down
c) Decode an end count
d) Count in a random order

Answer: d
Explanation: A sequential circuit design is used to count in a random manner which is faster than the combinational circuit. It is used for storing data.

3. In general, when using a scope to troubleshoot digital systems, the instrument should be triggered by _____
a) The A channel or channel 1
b) The vertical input mode, when using more than one channel
c) The system clock
d) Line sync, in order to observe troublesome power line glitches

Answer: c
Explanation: All the information is sent from one end to another end through the clock pulse which behaves like a carrier. So, for troubleshooting it should be triggered by the same. Since the system clock is internally produced.

4. Which counters are often used whenever pulses are to be counted and the results displayed in decimal?
a) Synchronous
b) Bean
c) Decade
d) BCD

Answer: d
Explanation: BCD means Binary Coded Decimal, which means that decimal numbers coded of binary numbers. It displays the decimal equivalent of corresponding binary numbers.

5. The _____ counter in the Altera library has controls that allow it to count up or down, and perform synchronous parallel load and asynchronous cascading.
a) 74134
b) LPM
c) Synchronous
d) AHDL

Answer: b
Explanation: The library of parameterized modules (LPM) counter in the Altera library has controls that allow it to count up or down, and perform synchronous parallel load and asynchronous cascading.

6. The minimum number of flip-flops that can be used to construct a modulus-5 counter is ___
a) 3
b) 8
c) 5
d) 10

Answer: a
Explanation: The minimum number of flip-flops used in a counter is given by: $2^{(n-1)}<=N<=2^n$. Thus, for modulus-5 counter: $2^2 <= N <= 2^3$, where N = 5 and n = 3.

7. The duty cycle of the most significant bit from a 4-bit (0–9) BCD counter is _____
a) 20%
b) 50%
c) 10%
d) 80%

Answer: a
Explanation: There are 10 states, out of which MSB is high only for (1000, 1001) 2 times. Hence duty cycle is 2/10*100 = 20%. Since the duty cycle is the ratio of on-time to the total time.

8. Normally, the synchronous counter is designed using _____
a) S-R flip-flops
b) J-K flip-flops
c) D flip-flops
d) T flip-flops

Answer: b
Explanation: Since J-K flip-flops have options of recovery from toggle condition and by using less number of J-K flip-flops a synchronous counter can be designed. So, it is more preferred. Also, because JK-flip-flops resolves the problem of Forbidden States.

9. MOD-16 counter requires _____ no. of states.
a) 8
b) 4
c) 16
d) 32

Answer: c
Explanation: $2^n >= N >= 2^{(n-1)}$, by using this formula we get the value of N=16 for n=4.

10. What is a state diagram?
a) It provides the graphical representation of states
b) It provides exactly the same information as the state table
c) It is same as the truth table
d) It is similar to the characteristic equation

Answer: b
Explanation: The state diagram provides exactly the same information as the state table and is obtained directly from the state table.

11. High speed counter is _____
a) Ring counter
b) Ripple counter
c) Synchronous counter
d) Asynchronous counter

Answer: c
Explanation: Synchronous counter doesn't have propagation delay. Propagation delay refers to the amount of time taken in producing the output when the input is altered.

12. Program counter in a digital computer _____
a) Counts the number of programs run in the machine
b) Counts the number of times a subroutine
c) Counts the number of time the loops are executed
d) Points the memory address of the current or the next instruction

Answer: d
Explanation: Program counter in a digital computer points the memory address of the current or the next instruction which is to be executed.

13. Fundamental mode is another name for _____
a) Level operation
b) Pulse operation
c) Clock operation
d) Edge operation

Answer: b
Explanation: Whatever the input given to the devices are in the form of pulses always. That is why it is known as a fundamental mode.

Up Down Counter

1. UP-DOWN counter is a combination of _____
a) Latches
b) Flip-flops
c) UP counter
d) Up counter & down counter

Answer: d
Explanation: As the name suggests UP-DOWN, it means that it has up-counter and down-counter as well. It alternatively counts up and down.

2. UP-DOWN counter is also known as _____
a) Dual counter
b) Multi counter
c) Multimode counter
d) Two Counter

Answer: c
Explanation: UP-DOWN counter is also known as multimode counter because it has capability of counting upward as well as downwards.

3. In an UP-counter, each flip-flop is triggered by _____
a) The output of the next flip-flop
b) The normal output of the preceding flip-flop
c) The clock pulse of the previous flip-flop
d) The inverted output of the preceding flip-flop

Answer: b
Explanation: In an UP-counter, each flip-flop is triggered by the normal output of the preceding flip-flop. UP-counter counts from 0 to a maximum value.

4. In DOWN-counter, each flip-flop is triggered by _____
a) The output of the next flip-flop
b) The normal output of the preceding flip-flop
c) The clock pulse of the previous flip-flop
d) The inverted output of the preceding flip-flop

Answer: d
Explanation: In DOWN-counter, each flip-flop is triggered by the inverted output of the preceding flip-flop. DOWN-counter counts from a maximum value to 0.

5. Binary counter that count incrementally and decrement is called _____
a) Up-down counter
b) LSI counters
c) Down counter
d) Up counter

Answer: a
Explanation: Binary counter that counts incrementally and decrement is called UP-DOWN counter/multimode counter. It alternately counts up and down.

6. Once an up-/down-counter begins its count sequence, it _____
a) Starts counting
b) Can be reversed
c) Can't be reversed
d) Can be altered

Answer: d
Explanation: In up/down ripple counter once the counting begins, we can simply change the pulse M (mode control) M = 0 or 1 respectively for UP counter or Down counter.

7. In 4-bit up-down counter, how many flip-flops are required?
a) 2
b) 3
c) 4
d) 5

Answer: c
Explanation: An n-bit bit counter requires n number of FFs. In a 4-bit up-down counter, there are 4 J-K flip-flops required.

8. A modulus-10 counter must have _____
a) 10 flip-flops
b) 4 Flip-flops
c) 2 flip-flops
d) Synchronous clocking

Answer: b
Explanation: $2^{n-1} <= N <= 2^n$
For modulus-10 counter, N = 10. Therefore, $2^3 <= 10 <= 2^4$. Thus, n = 4, and therefore, we require 4 FFs.

9. Which is not an example of a truncated modulus?
a) 8
b) 9
c) 11
d) 15

Answer: a
Explanation: An n-bit counter whose modulus is less than the maximum possible is called a truncated counter. Here, 9, 11 and 15 modulus counters are truncated counters. Whereas, modulus-8 is not a truncated counter.

10. The designation means that the _____
a) Up count is active-HIGH, the down count is active-LOW

b) Up count is active-LOW, the down count is active-HIGH
c) Up and down counts are both active-LOW
d) Up and down counts are both active-HIGH

Answer: a
Explanation: The designation means that the up count is active-HIGH, the down count is active-LOW. Active-High means that up-count would be triggered when clock is 1 else when clock is 0, down-count would be triggered, which is referred to as Active-low.

11. An asynchronous binary up counter, made from a series of leading edge-triggered flip-flops, can be changed to a down counter by _____
a) Taking the output on the other side of the flip-flops (instead of Q)
b) Clocking of each succeeding flip-flop from the other side (instead of Q)
c) Changing the flip-flops to trailing edge triggering
d) All of the Mentioned

Answer: d
Explanation: By all of the mentioned ideas, an asynchronous binary up counter, made from a series of leading edge-triggered flip-flops, can be changed to a down counter. Edge-triggered FFs refer to FFs being triggered during a clock transition from LOW to HIGH or HIGH to LOW.

12. A 4-bit binary up counter has an input clock frequency of 20 kHz. The frequency of the most significant bit is _____
a) 1.25 kHz
b) 2.50 kHz
c) 160 kHz
d) 320 kHz

Answer: a
Explanation: Input clock is given by 20/2 kHz. So, count on the basis of 10 kHz clock. And MSB changes on 8th stage; Hence, f = 10/8 = 1.25 kHz.

FLIP FLOP

D Flip Flop

1. In D flip-flop, D stands for _____
a) Distant
b) Data
c) Desired
d) Delay

Answer: b
Explanation: The D of D-flip-flop stands for “data”. It stores the value on the data line.

2. The D flip-flop has _____ input.
a) 1
b) 2
c) 3
d) 4

Answer: a
Explanation: The D flip-flop has one input. The D of D-flip-flop stands for “data”. It stores the value on the data line.

3. The D flip-flop has _____ output/outputs.
a) 2
b) 3
c) 4
d) 1

Answer: a
Explanation: The D flip-flop has two outputs: Q and Q complement. The D flip-flop has one input. The D of D-flip-flop stands for “data”. It stores the value on the data line.

4. A D flip-flop can be constructed from an _____ flip-flop.
a) S-R
b) J-K
c) T
d) S-K

Answer: a
Explanation: A D flip-flop can be constructed from an S-R flip-flop by inserting an inverter between S and R and assigning the symbol D to the S input.

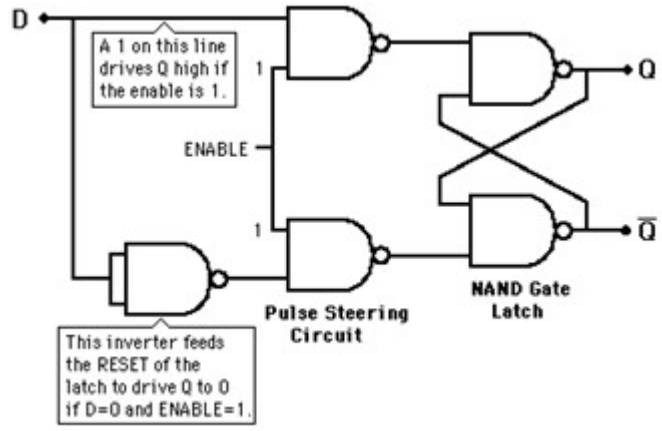
5. In D flip-flop, if clock input is LOW, the D input _____
a) Has no effect
b) Goes high

c) Goes low
d) Has effect

Answer: a
Explanation: In D flip-flop, if clock input is LOW, the D input has no effect, since the set and reset inputs of the NAND flip-flop are kept HIGH.

6. In D flip-flop, if clock input is HIGH & D=1, then output is _____
a) 0
b) 1
c) Forbidden
d) Toggle

Answer: a
Explanation: If clock input is HIGH & D=1, then output is 0. It can be observed from this diagram:



7. Which statement describes the BEST operation of a negative-edge-triggered D flip-flop?
a) The logic level at the D input is transferred to Q on NGT of CLK
b) The Q output is ALWAYS identical to the CLK input if the D input is HIGH
c) The Q output is ALWAYS identical to the D input when CLK = PGT
d) The Q output is ALWAYS identical to the D input

Answer: a
Explanation: By the truth table of D flip flop, we can observe that Q always depends on D.

Hence, for every negative trigger pulse, the logic at input D is shifted to Output Q.

D Flip-flop

Symbol

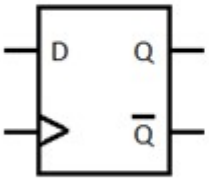


Table of truth:

clk	D	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	Q	$\overline{Q}$
1	0	0	1
1	1	1	0

8. Which of the following is correct for a gated D flip-flop?
a) The output toggles if one of the inputs is held HIGH
b) Only one of the inputs can be HIGH at a time
c) The output complement follows the input when enabled
d) Q output follows the input D when the enable is HIGH

Answer: d
Explanation: If clock is high then the D flip-flop operate and we know that input is equals to output in case of D flip-flop. It stores the value on the data line.

9. With regard to a D latch _____
a) The Q output follows the D input when EN is LOW
b) The Q output is opposite the D input when EN is LOW
c) The Q output follows the D input when EN is HIGH
d) The Q output is HIGH regardless of EN's input state

Answer: c
Explanation: Latch is nothing but flip flop which holds the o/p or i/p state. And in D flip-flop output follows the input. It stores the value on the data line.

10. Which of the following is correct for a D latch?
a) The output toggles if one of the inputs is held HIGH
b) Q output follows the input D when the enable is HIGH
c) Only one of the inputs can be HIGH at a time
d) The output complement follows the input when enabled

Answer: b
Explanation: If the clock is HIGH then the D flip-flop operates and we know that input equals to output in case of D flip flop. It stores the value on the data line.

11. Which of the following describes the operation of a positive edge-triggered D flip-flop?
a) If both inputs are HIGH, the output will toggle
b) The output will follow the input on the leading edge of the clock

c) When both inputs are LOW, an invalid state exists
d) The input is toggled into the flip-flop on the leading edge of the clock and is passed to the output on the trailing edge of the clock

Answer: b
Explanation: Edge-triggered flip-flop means the device will change state during the rising or falling edge of the clock pulse. The main phenomenon of the D flip-flop is that the o/p will follow the i/p when the enable pin is HIGH.

12. A D flip-flop utilizing a PGT clock is in the CLEAR state. Which of the following input actions will cause it to change states?
a) CLK = NGT, D = 0
b) CLK = PGT, D = 0
c) CLOCK NGT, D = 1
d) CLOCK PGT, D = 1

Answer: d
Explanation: PGT refers to Positive Going Transition and NGT refers to negative Going Transition. Earlier, the DFF is in a clear state (output is 0). So, if D = 1 then in the next stage output will be 1 and hence the stage will be changed.

13. A positive edge-triggered D flip-flop will store a 1 when _____
a) The D input is HIGH and the clock transitions from HIGH to LOW
b) The D input is HIGH and the clock transitions from LOW to HIGH
c) The D input is HIGH and the clock is LOW
d) The D input is HIGH and the clock is HIGH

Answer: b
Explanation: A positive edge-triggered D flip-flop will store a 1 when the D input is HIGH and the clock transitions from LOW to HIGH. While a negative edge-triggered D flip-flop will store a 0 when the D input is HIGH and the clock transitions from HIGH to LOW.

14. Why do the D flip-flops receive its designation or nomenclature as ‘Data Flip-flops’?
a) Due to its capability to receive data from flip-flop
b) Due to its capability to store data in flip-flop
c) Due to its capability to transfer the data into flip-flop
d) Due to erasing the data from the flip-flop

Answer: c
Explanation: Due to its capability to transfer the data into flip-flop. D-flip-flops stores the value on the data line.

15. The characteristic equation of D-flip-flop implies that _____
a) The next state is dependent on previous state
b) The next state is dependent on present state
c) The next state is independent of previous state
d) The next state is independent of present state

Answer: d
Explanation: A characteristic equation is needed when a specific gate requires a specific output in order to satisfy the truth table. The characteristic equation of D flip-flop is given by Q(n+1) = D; which indicates that the next state is independent of the present state.

Flip Flops – 1

1. Latches constructed with NOR and NAND gates tend to remain in the latched condition due to which configuration feature?
a) Low input voltages
b) Synchronous operation
c) Gate impedance
d) Cross coupling

Answer: d
Explanation: Latch is a type of bistable multivibrator having two stable states. Both inputs of a latch are directly connected to the other's output. Such types of structure is called cross coupling and due to which latches remain in the latched condition.

2. One example of the use of an S-R flip-flop is as _____
a) Transition pulse generator
b) Racer
c) Switch debouncer
d) Astable oscillator

Answer: c
Explanation: The SR flip-flop is very effective in removing the effects of switch bounce, which is the unwanted noise caused during the switching of electronic devices.

3. The truth table for an S-R flip-flop has how many VALID entries?
a) 1
b) 2
c) 3
d) 4

Answer: c
Explanation: The SR flip-flop actually has three inputs, Set, Reset and its current state. The Invalid or Undefined State occurs at both S and R being at 1.

4. When both inputs of a J-K flip-flop cycle, the output will _____
a) Be invalid
b) Change
c) Not change
d) Toggle

Answer: c
Explanation: After one cycle the value of each input comes to the same value. Eg: Assume J=0 and K=1. After 1 cycle, it becomes as J=0->1->0(1 cycle complete) and K=1->0->1(1 cycle complete). The J & K flip-flop has 4 stable states: Latch, Reset, Set and Toggle.

5. Which of the following is correct for a gated D-type flip-flop?
a) The Q output is either SET or RESET as soon as the D input goes HIGH or LOW

b) The output complement follows the input when enabled
c) Only one of the inputs can be HIGH at a time
d) The output toggles if one of the inputs is held HIGH

Answer: a
Explanation: In D flip flop, when the clock is high then the output depends on the input otherwise reminds previous output. In a state of clock high, when D is high the output Q also high, if D is '0' then output is also zero. Like SR flip-flop, the D-flip-flop also have an invalid state at both inputs being 1.

6. A basic S-R flip-flop can be constructed by cross-coupling of which basic logic gates?
a) AND or OR gates
b) XOR or XNOR gates
c) NOR or NAND gates
d) AND or NOR gates

Answer: c
Explanation: The basic S-R flip-flop can be constructed by cross coupling of NOR or NAND gates. Cross coupling means the output of second gate is fed to the input of first gate and vice-versa.

7. The logic circuits whose outputs at any instant of time depends only on the present input but also on the past outputs are called
a) Combinational circuits
b) Sequential circuits
c) Latches
d) Flip-flops

Answer: b
Explanation: In sequential circuits, the output signals are fed back to the input side. So, The circuits whose outputs at any instant of time depends only on the present input but also on the past outputs are called sequential circuits. Unlike sequential circuits, if output depends only on the present state, then it's known as combinational circuits.

8. Whose operations are more faster among the following?
a) Combinational circuits
b) Sequential circuits
c) Latches
d) Flip-flops

Answer: a
Explanation: Combinational circuits are often faster than sequential circuits. Since, the combinational circuits do not require memory elements whereas the sequential circuits need memory devices to perform their operations in sequence. Latches and Flip-flops come under sequential circuits.

9. How many types of sequential circuits are?
a) 2

b) 3
c) 4
d) 5

Answer: a
Explanation: There are two type of sequential circuits viz., (i) synchronous or clocked and (ii) asynchronous or unclocked. Synchronous Sequential Circuits are triggered in the presence of a clock signal, whereas, Asynchronous Sequential Circuits function in the absence of a clock signal.

10. The sequential circuit is also called _____
a) Flip-flop
b) Latch
c) Strobe
d) AddeR

Answer: b
Explanation: The sequential circuit is also called a latch because both are a memory cell, which are capable of storing one bit of information.

11. The basic latch consists of _____
a) Two inverters
b) Two comparators
c) Two amplifiers
d) Two adders

Answer: a
Explanation: The basic latch consists of two inverters. It is in the sense that if the output Q = 0 then the second output Q' = 1 and vice versa.

12. In S-R flip-flop, if Q = 0 the output is said to be _____
a) Set
b) Reset
c) Previous state
d) Current state

Answer: b
Explanation: In S-R flip-flop, if Q = 0 the output is said to be reset and set for Q = 1.

13. The output of latches will remain in set/reset untill _____
a) The trigger pulse is given to change the state
b) Any pulse given to go into previous state
c) They don't get any pulse more
d) The pulse is edge-triggered

Answer: a
Explanation: The output of latches will remain in set/reset untill the trigger pulse is given to change the state.

14. What is a trigger pulse?
a) A pulse that starts a cycle of operation
b) A pulse that reverses the cycle of operation
c) A pulse that prevents a cycle of operation
d) A pulse that enhances a cycle of operation

Answer: a
Explanation: Trigger pulse is defined as a pulse that starts a cycle of operation.

15. The circuits of NOR based S-R latch classified as asynchronous sequential circuits, why?
a) Because of inverted outputs
b) Because of triggering functionality
c) Because of cross-coupled connection
d) Because of inverted outputs & triggering functionality

Answer: c
Explanation: The cross-coupled connections from the output of one gate to the input of the other gate constitute a feedback path. For this reason, the circuits of NOR based S-R latch classified as asynchronous sequential circuits. Moreover, they are referred to as asynchronous because they function in the absence of a clock pulse.

Flip Flops – 2

1. What is an ambiguous condition in a NAND based S'-R' latch?
a) S'=0, R'=1
b) S'=1, R'=0
c) S'=1, R'=1
d) S'=0, R'=0

Answer: d
Explanation: In a NAND based S-R latch, If S'=0 & R'=0 then both the outputs (i.e. Q & Q') goes HIGH and this condition is called an ambiguous/forbidden state. This state is also known as an Invalid state as the system goes into an unexpected situation.

2. In a NAND based S'-R' latch, if S'=1 & R'=1 then the state of the latch is _____
a) No change
b) Set
c) Reset
d) Forbidden

Answer: a
Explanation: In a NAND based S'-R, latch if S'=1 & R'=1 then there is no any change in the state. It remains in its prior state. This state is used for the storage of data.

3. A NAND based S'-R' latch can be converted into S-R latch by placing _____
a) A D latch at each of its input
b) An inverter at each of its input
c) It can never be converted
d) Both a D latch and an inverter at its input

Answer: d
Explanation: A NAND based S'-R' latch can be converted into S-R latch by placing either a D latch or an inverter at its input as it's operations will be complementary.

4. One major difference between a NAND based S'-R' latch & a NOR based S-R latch is _____
a) The inputs of NOR latch are 0 but 1 for NAND latch
b) The inputs of NOR latch are 1 but 0 for NAND latch
c) The output of NAND latch becomes set if S'=0 & R'=1 and vice versa for NOR latch
d) The output of NOR latch is 1 but 0 for NAND latch

Answer: a
Explanation: Due to inverted input of NAND based S'-R' latch, the inputs of NOR latch are 0 but 1 for NAND latch.

5. The characteristic equation of S-R latch is _____
a) Q(n+1) = (S + Q(n))R'

b) Q(n+1) = SR + Q(n)R
c) Q(n+1) = S'R + Q(n)R
d) Q(n+1) = S'R + Q'(n)R

Answer: a
Explanation: A characteristic equation is needed when a specific gate requires a specific output in order to satisfy the truth table. The characteristic equation of S-R latch is Q(n+1) = (S + Q(n))R'.

6. The difference between a flip-flop & latch is _____
a) Both are same
b) Flip-flop consist of an extra output
c) Latches has one input but flip-flop has two
d) Latch has two inputs but flip-flop has one

Answer: c
Explanation: Flip-flop is a modified version of latch. To determine the changes in states, an additional control input is provided to the latch.

7. How many types of flip-flops are?
a) 2
b) 3
c) 4
d) 5

Answer: c
Explanation: There are 4 types of flip-flops, viz., S-R, J-K, D, and T. D flip-flop is an advanced version of S-R flip-flop, while T flip-flop is an advanced version of J-K flip-flop.

8. The S-R flip flop consist of _____
a) 4 AND gates
b) Two additional AND gates
c) An additional clock input
d) 3 AND gates

Answer: b
Explanation: The S-R flip flop consists of two additional AND gates at the S and R inputs of S-R latch.

9. What is one disadvantage of an S-R flip-flop?
a) It has no Enable input
b) It has a RACE condition
c) It has no clock input
d) Invalid State

Answer: d
Explanation: The main drawback of s-r flip flop is invalid output when both the inputs are high, which is referred to as Invalid State.

10. One example of the use of an S-R flip-flop is as _____
a) Racer
b) Stable oscillator
c) Binary storage register
d) Transition pulse generator

Answer: c
Explanation: S-R refers to set-reset. So, it is used to store two values 0 and 1. Hence, it is referred to as binary storage element. It functions as memory storage during the No Change State.

11. When is a flip-flop said to be transparent?
a) When the Q output is opposite the input
b) When the Q output follows the input
c) When you can see through the IC packaging
d) When the Q output is complementary of the input

Answer: b
Explanation: Flip-flop have the property of responding immediately to the changes in its inputs. This property is called transparency.

12. On a positive edge-triggered S-R flip-flop, the outputs reflect the input condition when _____
a) The clock pulse is LOW
b) The clock pulse is HIGH
c) The clock pulse transitions from LOW to HIGH
d) The clock pulse transitions from HIGH to LOW

Answer: c
Explanation: Edge triggered device will follow when there is transition. It is a positive edge triggered when transition takes place from low to high, while, it is negative edge triggered when the transition takes place from high to low.

13. What is the hold condition of a flip-flop?
a) Both S and R inputs activated
b) No active S or R input
c) Only S is active
d) Only R is active

Answer: b
Explanation: The hold condition in a flip-flop is obtained when both of the inputs are LOW. It is the No Change State or Memory Storage state if a flip-flop.

14. If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____
a) SET
b) RESET

c) Clear
d) Invalid

Answer: b
Explanation: If S=0, R=1, the flip flop is at reset condition. Then at S=0, R=0, there is no change. So, it remains in reset. If S=1, R=0, the flip flop is at the set condition.

15. The circuit that is primarily responsible for certain flip-flops to be designated as edge-triggered is the _____
a) Edge-detection circuit
b) NOR latch
c) NAND latch
d) Pulse-steering circuit

Answer: a
Explanation: The circuit that is primarily responsible for certain flip-flops to be designated as edge-triggered is the edge-detection circuit.

Flip Flops – 3

1. Which circuit is generated from D flip-flop due to addition of an inverter by causing reduction in the number of inputs?
a) Gated JK-latch
b) Gated SR-latch
c) Gated T-latch
d) Gated D-latch

Answer: d
Explanation: Since, both inputs of the D flip-flop are connected through an inverter. And this causes reduction in the number of inputs.

2. The characteristic of J-K flip-flop is similar to _____
a) S-R flip-flop
b) D flip-flop
c) T flip-flop
d) Gated T flip-flop

Answer: a
Explanation: In an S-R flip-flop, S refers to “SET” whereas R refers to “RESET”. The same behaviour is shown by J-K flip-flop.

3. A J-K flip-flop can be obtained from the clocked S-R flip-flop by augmenting _____
a) Two AND gates
b) Two NAND gates
c) Two NOT gates
d) Two OR gates

Answer: a
Explanation: A J-K flip-flop can be obtained from the clocked S-R flip-flop by augmenting two AND gates.

4. How is a J-K flip-flop made to toggle?
a) J = 0, K = 0
b) J = 1, K = 0
c) J = 0, K = 1
d) J = 1, K = 1

Answer: d
Explanation: When j=k=1 then the race condition is occurs that means both output wants to be HIGH. Hence, there is toggle condition is occurs, where 0 becomes 1 and 1 becomes 0. That is device is either set or reset.

5. The phenomenon of interpreting unwanted signals on J and K while Cp (clock pulse) is HIGH is called _____
a) Parity error checking

b) Ones catching
c) Digital discrimination
d) Digital filtering

Answer: b
Explanation: Ones catching means that the input transitioned to a 1 and back very briefly (unintentionally due to a glitch), but the flip-flop responded and latched it in anyway, i.e., it caught the 1. Similarly for 0's catching.

6. In J-K flip-flop, "no change" condition appears when _____
a) J = 1, K = 1
b) J = 1, K = 0
c) J = 0, K = 1
d) J = 0, K = 0

Answer: d
Explanation: If J = 0, K = 0, the output remains unchanged. This is the memory storing state.

7. A J-K flip-flop with J = 1 and K = 1 has a 20 kHz clock input. The Q output is _____
a) Constantly LOW
b) Constantly HIGH
c) A 20 kHz square wave
d) A 10 kHz square wave

Answer: d
Explanation: The flip flop is sensitive only to the positive or negative edge of the clock pulse. So, the flip-flop toggles whenever the clock is falling/rising at edge. This triggering of flip-flop during the transition state, is known as Edge-triggered flip-flop. Thus, the output curve has a time period twice that of the clock. Frequency is inversely related to time period and hence frequency gets halved.

8. What is the significance of the J and K terminals on the J-K flip-flop?
a) There is no known significance in their designations
b) The J represents "jump," which is how the Q output reacts whenever the clock goes high and the J input is also HIGH
c) The letters were chosen in honour of Jack Kilby, the inventory of the integrated circuit
d) All of the other letters of the alphabet are already in use

Answer: c
Explanation: The letters J & K were chosen in honour of Jack Kilby, the inventory of the integrated circuit.

9. On a J-K flip-flop, when is the flip-flop in a hold condition?
a) J = 0, K = 0
b) J = 1, K = 0
c) J = 0, K = 1
d) J = 1, K = 1

Answer: a
Explanation: At J=0 k=0 output continues to be in the same state. This is the memory storing state.

10. Two J-K flip-flops with their J-K inputs tied HIGH are cascaded to be used as counters. After four input clock pulses, the binary count is _____
a) 00
b) 11
c) 01
d) 10

Answer: a
Explanation: Every O/P repeats after its mod. Here mod is 4 (because 2 flip-flops are used. So mod = $2^2 = 4$). So after 4 clock pulses the O/P repeats i.e. 00.

11. Four J-K flip-flops are cascaded with their J-K inputs tied HIGH. If the input frequency (fin) to the first flip-flop is 32 kHz, the output frequency (fout) is _____
a) 1 kHz
b) 2 kHz
c) 4 kHz
d) 16 kHz

Answer: b
Explanation: 32/2=16:-first flip-flop, 16/2=8:- second flip-flop, 8/2=4:- third flip-flop, 4/2=2:- fourth flip-flop. Since the output frequency is determined on basis of the 4^{th} flip-flop.

12. Determine the output frequency for a frequency division circuit that contains 12 flip-flops with an input clock frequency of 20.48 MHz.
a) 10.24 kHz
b) 5 kHz
c) 30.24 kHz
d) 15 kHz

Answer: b
Explanation: 12 flip flops = $2^{12} = 4096$
Input Clock frequency = $20.48*10^6 = 20480000$
Output Clock frequency = 20480000/4096 = 5000 i.e., 5 kHz.

13. How many flip-flops are in the 7475 IC?
a) 2
b) 1
c) 4
d) 8 Answer: c
Explanation: There are 4 flip-flops used in 7475 IC and those are D flip-flops only.

REGISTER

1. A register is defined as _____
a) The group of latches for storing one bit of information
b) The group of latches for storing n-bit of information
c) The group of flip-flops suitable for storing one bit of information
d) The group of flip-flops suitable for storing binary information

Answer: d
Explanation: A register is defined as the group of flip-flops suitable for storing binary information. Each flip-flop is a binary cell capable of storing one bit of information. The data in a register can be transferred from one flip-flop to another.

2. The register is a type of _____
a) Sequential circuit
b) Combinational circuit
c) CPU
d) Latches

Answer: a
Explanation: Register's output depends on the past and present states of the inputs. The device which follows these properties is termed as a sequential circuit. Whereas, combinational circuits only depend on the present values of inputs.

3. How many types of registers are?
a) 2
b) 3
c) 4
d) 5

Answer: c
Explanation: There are 4 types of shift registers, viz., Serial-In/Serial-Out, Serial-In/Parallel-Out, Parallel-In/Serial-Out and Parallel-In/Parallel-Out.

4. The main difference between a register and a counter is _____
a) A register has no specific sequence of states
b) A counter has no specific sequence of states
c) A register has capability to store one bit of information but counter has n-bit
d) A register counts data

Answer: a
Explanation: The main difference between a register and a counter is that a register has no specific sequence of states except in certain specialised applications.

5. In D register, ‘D’ stands for _____
a) Delay
b) Decrement
c) Data
d) Decay

Answer: c
Explanation: D stands for “data” in case of flip-flops and not delay. Registers are made of a group of flip-flops.

6. Registers capable of shifting in one direction is _____
a) Universal shift register
b) Unidirectional shift register
c) Unipolar shift register
d) Unique shift register

Answer: b
Explanation: The register capable of shifting in one direction is unidirectional shift register. The register capable of shifting in both directions is known as a bidirectional shift register.

7. A register that is used to store binary information is called _____
a) Data register
b) Binary register
c) Shift register
d) D – Register

Answer: b
Explanation: A register that is used to store binary information is called a binary register. A register in which data can be shifted is called shift register.

8. A shift register is defined as _____
a) The register capable of shifting information to another register
b) The register capable of shifting information either to the right or to the left
c) The register capable of shifting information to the right only
d) The register capable of shifting information to the left only

Answer: b
Explanation: The register capable of shifting information either to the right or to the left is termed as shift register. A register in which data can be shifted only in one direction is called unidirectional shift register, while if data can shifted in both directions, it is known as a bidirectional shift register.

9. How many methods of shifting of data are available?
a) 2

b) 3
c) 4
d) 5

Answer: a
Explanation: There are two types of shifting of data are available and these are serial shifting & parallel shifting.

10. In serial shifting method, data shifting occurs _____
a) One bit at a time
b) simultaneously
c) Two bit at a time
d) Four bit at a time

Answer: a
Explanation: As the name suggests serial shifting, it means that data shifting will take place one bit at a time for each clock pulse in a serial fashion. While in parallel shifting, shifting will take place with all bits simultaneously for each clock pulse in a parallel fashion.

Shift Registers

1. Based on how binary information is entered or shifted out, shift registers are classified into _____ categories.
a) 2
b) 3
c) 4
d) 5

Answer: c
Explanation: The registers in which data can be shifted serially or parallelly are known as shift registers. Based on how binary information is entered or shifted out, shift registers are classified into 4 categories, viz., Serial-In/Serial-Out(SISO), Serial-In/Parallel-Out (SIPO), Parallel-In/Serial-Out (PISO), Parallel-In/Parallel-Out (PIPO).

2. The full form of SIPO is _____
a) Serial-in Parallel-out
b) Parallel-in Serial-out
c) Serial-in Serial-out
d) Serial-In Peripheral-Out

Answer: a
Explanation: SIPO is always known as Serial-in Parallel-out.

3. A shift register that will accept a parallel input or a bidirectional serial load and internal shift features is called as?
a) Tristate
b) End around
c) Universal
d) Conversion

Answer: c
Explanation: A shift register can shift it's data either left or right. The universal shift register is capable of shifting data left, right and parallel load capabilities.

4. How can parallel data be taken out of a shift register simultaneously?
a) Use the Q output of the first FF
b) Use the Q output of the last FF
c) Tie all of the Q outputs together
d) Use the Q output of each FF

Answer: d
Explanation: Because no other flip-flops are connected with the output Q, therefore one can use the Q out of each FF to take out parallel data.

5. What is meant by parallel load of a shift register?
a) All FFs are preset with data

b) Each FF is loaded with data, one at a time
c) Parallel shifting of data
d) All FFs are set with data

Answer: a
Explanation: At Preset condition, outputs of flip-flops will be 1. Preset = 1 means Q = 1, thus input is definitely 1.

6. The group of bits 11001 is serially shifted (right-most bit first) into a 5-bit parallel output shift register with an initial state 01110. After three clock pulses, the register contains _____
a) 01110
b) 00001
c) 00101
d) 00110

Answer: c
Explanation: LSB bit is inverted and feed back to MSB:
01110->initial
10111->first clock pulse
01011->second
00101->third.

7. Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first)
a) 1100
b) 0011
c) 0000
d) 1111

Answer: c
Explanation: In Serial-In/Serial-Out shift register, data will be shifted one at a time with every clock pulse. Therefore,
Wait | Store
1100 | 0000
110 | 0000 1st clock
11 | 0000 2nd clock.

8. A serial in/parallel out, 4-bit shift register initially contains all 1s. The data nibble 0111 is waiting to enter. After four clock pulses, the register contains _____
a) 0000
b) 1111
c) 0111
d) 1000

Answer: c
Explanation: In Serial-In/Parallel-Out shift register, data will be shifted all at a time with every clock pulse. Therefore,

Wait | Store
0111 | 0000
011 | 1000 1st clk
01 | 1100 2nd clk
0 | 1110 3rd clk
X | 1111 4th clk.

9. With a 200 kHz clock frequency, eight bits can be serially entered into a shift register in ____
a) 4 µs
b) 40 µs
c) 400 µs
d) 40 ms

Answer: b
Explanation: f = 200 KHZ; T = (1/200) m sec = (1/0.2) micro-sec = 5 micro-sec;
In serial transmission, data enters one bit at a time. After 8 clock cycles only 8 bit will be loaded = 8 * 5 = 40 micro-sec.

10. An 8-bit serial in/serial out shift register is used with a clock frequency of 2 MHz to achieve a time delay (td) of _____
a) 16 us
b) 8 us
c) 4 us
d) 2 us

Answer: c
Explanation: One clock period is = (½) micro-s = 0.5 microseconds. In serial transmission, data enters one bit at a time. So, the total delay = 0.5*8 = 4 micro seconds time is required to transmit information of 8 bits.

Universal Shift Registers

1. A sequence of equally spaced timing pulses may be easily generated by which type of counter circuit?
a) Ring shift
b) Clock
c) Johnson
d) Binary

Answer: a
Explanation: In Ring counter, the feedback of the output of the FF is fed to the same FF's input. Thus, it generates equally spaced timing pulses.

2. A bidirectional 4-bit shift register is storing the nibble 1101. Its input is HIGH. The nibble 1011 is waiting to be entered on the serial data-input line. After three clock pulses, the shift register is storing _____
a) 1101
b) 0111
c) 0001
d) 1110

Answer: b
Explanation: Mode is high means it's a right shift register. Then after 3 clock pulses enter bits are 011 and remained bit in register is 1. Therefore, 0111 is the required solution.
1011 | 1101
101 | 1110 -> 1st clock pulse
10 | 1111 -> 2nd clock pulse
1 | 0111 -> 3rd clock pulse.

3. To operate correctly, starting a ring shift counter requires _____
a) Clearing all the flip-flops
b) Presetting one flip-flop and clearing all others
c) Clearing one flip-flop and presetting all others
d) Presetting all the flip-flops

Answer: b
Explanation: In Ring counter, the feedback of the output of the FF is fed to the same FF's input. To operate correctly, starting a ring shift counter requires presetting one flip-flop and clearing all others so that it can shift to the next bit.

4. A 4-bit shift register that receives 4 bits of parallel data will shift to the _____ by _____ position for each clock pulse.
a) Right, one
b) Right, two
c) Left, one
d) Left, three

Answer: a
Explanation: If register shifts towards left then it shift by a bit to the left and if register shifts right then it shift to the right by one bit. Since, it receives parallel data, then by default, it will shift to right by one position.

5. How many clock pulses will be required to completely load serially a 5-bit shift register?
a) 2
b) 3
c) 4
d) 5

Answer: d
Explanation: A register is a collection of FFS. To load a bit, we require 1 clock pulse for 1 shift register. So, for 5-bit shift register we would require of 5 clock pulses.

6. How is a strobe signal used when serially loading a shift register?
a) To turn the register on and off
b) To control the number of clocks
c) To determine which output Qs are used
d) To determine the FFs that will be used

Answer: b
Explanation: A strobe is used to validate the availability of data on the data line. It (an auxiliary signal used to help synchronize the real data in an electrical bus when the bus components have no common clock) signal is used to control the number of clocks during serially loading a shift register.

7. An 8-bit serial in/serial out shift register is used with a clock frequency of 150 kHz. What is the time delay between the serial input and the Q3 output?
a) 1.67 s
b) 26.67 s
c) 26.7 ms
d) 267 ms

Answer: b
Explanation: In serial-sifting, one bit of data is shifted one at a time. From Q0 to Q3 total of 4 bit shifting takes place. Therefore, 4/150kHz = 26.67 microseconds.

8. What are the three output conditions of a three-state buffer?
a) HIGH, LOW, float
b) High-Z, 0, float
c) Negative, positive, 0
d) 1, Low-Z, float

Answer: a
Explanation: Three conditions of a three-state buffer are HIGH, LOW & float.

9. The primary purpose of a three-state buffer is usually _____
a) To provide isolation between the input device and the data bus
b) To provide the sink or source current required by any device connected to its output without loading down the output device
c) Temporary data storage
d) To control data flow

Answer: a
Explanation: The primary purpose of a three-state buffer is usually to provide isolation between the input device or peripheral devices and the data bus. Three conditions of a three-state buffer are HIGH, LOW & float.

10. What is the difference between a ring shift counter and a Johnson shift counter?
a) There is no difference
b) A ring is faster
c) The feedback is reversed
d) The Johnson is faster

Answer: c
Explanation: A ring counter is a shift register (a cascade connection of flip-flops) with the output of the last one connected to the input of the first, that is, in a ring. Whereas, a Johnson counter (or switchtail ring counter, twisted-ring counter, walking-ring counter, or Moebius counter) is a modified ring counter, where the output from the last stage is inverted and fed back as input to the first stage.

Shift Register Counters

1. What is a recirculating register?
a) Serial out connected to serial in
b) All Q outputs connected together
c) A register that can be used over again
d) Parallel out connected to Parallel in

Answer: a
Explanation: A recirculating register is a register whose serial output is connected to the serial input in a circulated manner.

2. When is it important to use a three-state buffer?
a) When two or more outputs are connected to the same input
b) When all outputs are normally HIGH
c) When all outputs are normally LOW
d) When two or more outputs are connected to two or more inputs

Answer: a
Explanation: When two or more outputs are connected to the same input, in such situation we use of tristate buffer always because it has the capability to take upto three inputs. A buffer is a circuit where the output follows the input.

3. A bidirectional 4-bit shift register is storing the nibble 1110. Its input is LOW. The nibble 0111 is waiting to be entered on the serial data-input line. After two clock pulses, the shift register is storing _____
a) 1110
b) 0111
c) 1000
d) 1001

Answer: d
Explanation: Given,

Stored nibble | waiting nibble

0111 | 1110, Initially

111 | 1100, 1st pulse

11 | 1001, 2nd pulse.

4. In a parallel in/parallel out shift register, D0 = 1, D1 = 1, D2 = 1, and D3 = 0. After three clock pulses, the data outputs are _____
a) 1110
b) 0001
c) 1100
d) 1000

Answer: b
Explanation: Parallel in parallel out gives the same output as input. Thus, after three clock pulses, the data outputs are 0001.

5. The group of bits 10110111 is serially shifted (right-most bit first) into an 8-bit parallel output shift register with an initial state 11110000. After two clock pulses, the register contains _____
a) 10111000
b) 10110111
c) 11110000
d) 11111100

Answer: d
Explanation: After first clock pulse, the register contains 11111000. After second clock pulse, the register would contain 11111100. Since the bits are shifted to the right at every clock pulse.

6. By adding recirculating lines to a 4-bit parallel-in serial-out shift register, it becomes a _____ _____ and _____ out register.
a) Parallel-in, serial, parallel
b) Serial-in, parallel, serial
c) Series-parallel-in, series, parallel
d) Bidirectional in, parallel, series

Answer: a
Explanation: One bit shifting takes place just after the output obtained on every register. Hence, by adding recirculating lines to a 4-bit parallel-in serial-out shift register, it becomes a Parallel-in, Serial, and Parallel-out register. Since, the bots can be inputted all at the same time, while the data can be outputted either one at a time or simultaneously.

7. What type of register would have a complete binary number shifted in one bit at a time and have all the stored bits shifted out one at a time?
a) Parallel-in Parallel-out
b) Parallel-in Serial-out
c) Serial-in Serial-out
d) Serial-in Parallel-out

Answer: c
Explanation: Serial-in Serial-out register would have a complete binary number shifted in one bit at a time and have all the stored bits shifted out one at a time. Since in serial transmission, bits are transmitted or received one at a time and not simultaneously.

8. In a 4-bit Johnson counter sequence, there are a total of how many states or bit patterns?
a) 1
b) 3
c) 4
d) 8

Answer: d
Explanation: In johnson counter, total number of states are determined by $2^N = 2*4 = 16$
Total Number of Used states = 2N = 2*4 = 8
Total Number of Unused states = 16 – 8 = 8.

9. If a 10-bit ring counter has an initial state 1101000000, what is the state after the second clock pulse?
a) 1101000000
b) 0011010000
c) 1100000000
d) 0000000000

Answer: b
Explanation: After shifting 2-bit we get the output as 0011010000 (Since two zeros are at 1^{st} position and 2^{nd} position which came from the last two bits). As in a ring counter, the bits rotate in clockwise direction.

10. How much storage capacity does each stage in a shift register represent?
a) One bit
b) Two bits
c) Four bits
d) Eight bits

Answer: a
Explanation: A register is made of flip-flops. And each flip-flop stores 1 bit of data. Thus, a shift register has the capability to store one bit and if another bit is to store, in such a situation it deletes the previous data and stores them.

MEMORY DEVICE

Memory Devices – 1

1. Memory is a/an _____
a) Device to collect data from other computer
b) Block of data to keep data separately
c) Indispensable part of computer
d) Device to connect through all over the world

Answer: c
Explanation: Memory is an indispensable unit of a computer and microprocessor based systems which stores permanent or temporary data.

2. The instruction used in a program for executing them is stored in the _____
a) CPU
b) Control Unit
c) Memory
d) Microprocessor

Answer: c
Explanation: All of the program and the instructions are stored in the memory. The processor fetches it as and when required.

3. A flip flop stores _____
a) 10 bit of information
b) 1 bit of information
c) 2 bit of information
d) 3-bit information

Answer: b
Explanation: A flip-flop has capability to store 1 bit of information. It can be used further after erasing previous information.

4. A register is able to hold _____
a) Data
b) Word
c) Nibble
d) Both data and word

Answer: b
Explanation: Register is also a part of memory inside a computer. It stands there to hold a word. A word is a group of 16-bits or 2-bytes.

5. A register file holds _____
a) A large number of word of information
b) A small number of word of information

c) A large number of programs
d) A modest number of words of information

Answer: d
Explanation: A register file is different from a simple register because of capability to hold a modest number of words of information. A word is a group of 16-bits or 2-bytes.

6. The very first computer memory consisted of _____
a) A small display
b) A large memory storage equipment
c) An automatic keyboard input
d) An automatic mouse input

Answer: b
Explanation: The very first computer memory consisted of a minute magnetic toroid, which required large, bulky circuit boards stored in large cabinates.

7. A minute magnetic toroid is also called as _____
a) Large memory
b) Small memory
c) Core memory
d) Both small and large memory

Answer: c
Explanation: A minute magnetic toroid is also called as core memory which is made up of a semiconductor. A semiconductor is a device whose electrical conductivity lies between that of conductor and insulator.

8. Which one of the following has capability to store data in extremely high densities?
a) Register
b) Capacitor
c) Semiconductor
d) Flip-Flop

Answer: c
Explanation: Semiconductor has capability to store data in extremely high densities.

9. A large memory is compressed into a small one by using _____
a) LSI semiconductor
b) VLSI semiconductor
c) CDR semiconductor
d) SSI semiconductor

Answer: b
Explanation: VLSI (Very Large Scale Integration) semiconductor is used in modern computers to short the size of memory.

10. VLSI chip utilizes _____
a) NMOS
b) CMOS
c) BJT
d) All of the Mentioned

Answer: d
Explanation: VLSI (Very Large Scale Integration) is a memory chip which is made up of NMOS, CMOS, BJT, and BiCMOS. It can include 10,000 to 100,000 gates per IC.

11. CD-ROM refers to _____
a) Floppy disk
b) Compact Disk-Read Only Memory
c) Compressed Disk-Read Only Memory
d) Compressed Disk- Random Access Memory

Answer: b
Explanation: CD-ROM refers to Compact Disk-Read Only Memory.

12. Data stored in an electronic memory cell can be accessed at random and on demand using _____
a) Memory addressing
b) Direct addressing
c) Indirect addressing
d) Control Unit

Answer: b
Explanation: Direct addressing eliminates the need to process a large stream of irrelevant data in order to the desired data word.

13. The full form of PLD is _____
a) Programmable Large Device
b) Programmable Long Device
c) Programmable Logic Device
d) Programmable Lengthy Device

Answer: c
Explanation: The full form of PLD is Programmable Logic Device.

14. The evolution of PLD began with _____
a) EROM
b) RAM
c) PROM
d) EEPROM

Answer: a
Explanation: The evolution of PLD (Programmable Logic Device) began with Programmable Read Only Memory (i.e. PROM). Here, the ROM can be externally programmed as per the user.

15. A ROM is defined as _____
a) Read Out Memory
b) Read Once Memory
c) Read Only Memory
d) Read One Memory

Answer: c
Explanation: A ROM is defined as Read Only Memory which can read the instruction stored in a computer.

Memory Devices – 2

1. The full form of ROM is _____
a) Read Outside Memory
b) Read Out Memory
c) Read Only Memory
d) Read One Memory

Answer: c
Explanation: The full form of ROM is Read Only Memory.

2. ROM consist of _____
a) NOR and OR arrays
b) NAND and NOR arrays
c) NAND and OR arrays
d) NOR and AND arrays

Answer: c
Explanation: ROM consists of NAND and OR arrays which can be programmed by the user to implement combinational & sequential functions. Combinational Operations like that of adders and subtractors and Sequential Functions like that of storing in the memory.

3. For re-programmability, PLDs use _____
a) PROM
b) EPROM
c) CDROM
d) PLA

Answer: b
Explanation: For re-programmability, PLDs use EPROM (i.e. Erasable PROM). It erases the previous program and starts uploading a new one. However, data is erased by exposing it to UV-light, which is a tedious and time-consuming process.

4. The full form of PROM is _____
a) Previous Read Only Memory
b) Programmable Read Out Memory
c) Programmable Read Only Memory
d) Previous Read Out Memory

Answer: c
Explanation: The full form of PROM is Programmable Read Only Memory, where the ROM can be programmed by the user.

5. The full form of EPROM is _____
a) Easy Programmable Read Only Memory
b) Erasable Programmable Read Only Memory

c) Eradicate Programmable Read Only Memory
d) Easy Programmable Read Out Memory

Answer: b
Explanation: The full form of EPROM is Erasable Programmable Read Only Memory, where the ROM can be erased and re-used by the user.

6. PLDs with programmable AND and fixed OR arrays are called _____
a) PAL
b) PLA
c) APL
d) PPL

Answer: a
Explanation: PLDs with programmable AND and fixed OR arrays are called PAL (i.e. Programmable Array Logic). However, PAL is less flexible but has higher speed.

7. When both the AND and OR are programmable, such PLDs are known as _____
a) PAL
b) PPL
c) PLA
d) APL

Answer: c
Explanation: When both the AND and OR are programmable, such PLDs are known as PLA (i.e. Programmable Logic Array). However, PLA is more flexible but has less speed.

8. ASIC stands for _____
a) Application Special Integrated Circuits
b) Applied Special Integrated Circuits
c) Application Specific Integrated Circuits
d) Applied Specific Integrated Circuits

Answer: c
Explanation: In digital electronics, ASIC stands for Application Specific Integrated Circuits. It is a customized integrated circuit which is produced for a specific use and not for a common-purpose.

9. The programmability and high density of PLDs make them useful in the design of _____
a) ISAC
b) ASIC
c) SACC
d) CISF

Answer: b
Explanation: The programmability and high density of PLDs make them useful in the design of ASIC (i.e. Application Specific Integrated Circuits) where design changes can be more rapidly and inexpensively.

10. FPGA stands for _____
a) Full Programmable Gate Array
b) Full Programmable Genuine Array
c) First Programmable Gate Array
d) Field Programmable Gate Array

Answer: d
Explanation: In digital electronics, FPGA stands for Field Programmable Gate Array. This type of integrated circuit is for general-purpose which is configured by the user as per their requirement.

11. Which of the following is a reprogrammable gate array?
a) EPROM
b) FPGA
c) Both EPROM and FPGA
d) ROM

Answer: c
Explanation: Both FPGA and EPROM are reprogrammable gate array.

12. The difference between FPGA and PLD is that _____
a) FPGA is slower than PLD
b) FPGA has high power dissipation
c) FPGA incorporates logic blocks
d) All of the Mentioned

Answer: c
Explanation: The difference between FPGA and PLD is that FPGA incorporates logic blocks instead of fixed AND-OR gates and is faster with low power dissipation. FPGAs are designed for having higher gate count whereas, PLDs are used for lesser gate counts.

Memory Devices – 3

1. Memories are classified into _____ categories.
a) 3
b) 4
c) 5
d) 6

Answer: c
Explanation: Memory is typically classified of 2 types: Primary and Secondary. These are further classified into 5 types of memories and these are Secondary, RAM, Dynamic/Static, Volatile/Non-volatile, Magnetic/Semiconductor Memory.

2. Secondary memory is also known as _____
a) Registers
b) Main Memory
c) RAM
d) Both registers and main memory

Answer: d
Explanation: Secondary memory is also known as Registers/Main Memory. In secondary memory, data is usually stored for a long-term.

3. In a computer, registers are present _____
a) Within control unit
b) Within RAM
c) Within ROM
d) Within CPU

Answer: d
Explanation: In a computer, registers are present within the CPU to store data temporarily during arithmetic and logical operations and during the functioning of the ALU.

4. Which of the following has the lowest access time?
a) RAM
b) ROM
c) Registers
d) Flag

Answer: c
Explanation: Registers has the lowest access time, as they are available inside the CPU. Registers are present within the CPU to store data temporarily during arithmetic and logical operations and during the functioning of the ALU.

5. Main memories of a computer, usually made up of _____
a) Registers
b) Semiconductors

c) Counters
d) PLDs

Answer: b
Explanation: Main memories of a computer, usually made up of semiconductors which are available external to the CPU to store program and data during execution of a program. Registers are present within the CPU to store data temporarily during arithmetic and logical operations and during the functioning of the ALU.

6. As the storage capacity of the main memory is inadequate, which memory is used to enhance it?
a) Secondary Memory
b) Auxiliary Memory
c) Static Memory
d) Both Secondary Memory and Auxiliary Memory

Answer: d
Explanation: As the storage capacity of the main memory is inadequate, Secondary memory is used to enhance it and it is also known as auxiliary memory. Secondary memory is also known as Registers/Main Memory. In secondary memory, data is usually stored for a long-term.

7. Which memories are if magnetic memory type?
a) Main Memory
b) Secondary Memory
c) Static Memory
d) Volatile Memory

Answer: b
Explanation: Usually, secondary memories are of magnetic memory type that are used to store large type quantities of data. In secondary memory, data is usually stored for a long-term.

8. Which of the following comes under secondary memory/ies?
a) Floppy disk
b) Magnetic drum
c) Hard disk
d) All of the Mentioned

Answer: d
Explanation: All of the mentioned equipment's are of external storage which is known as secondary memories. In secondary memory, data is usually stored for a long-term.

9. Based on method of access, memory devices are classified into _____ categories.
a) 2
b) 3
c) 4
d) 5

Answer: a
Explanation: Based on the method of access, memory devices are classified into two categories and these are sequential access memory and RAM. A sequential access memory is one in which a particular memory location is accessed sequentially.

10. A sequential access memory is one in which _____
a) A particular memory location is accessed rapidly
b) A particular memory location is accessed sequentially
c) A particular memory location is accessed serially
d) A particular memory location is accessed parallely

Answer: b
Explanation: A sequential access memory is one in which A particular memory location is accessed sequentially (i.e. the ith memory location is accessed only after sequencing through previous (i-1) memory locations).

11. An example of sequential access memory is _____
a) Floppy disk
b) Hard disk
c) Magnetic tape memory
d) RAM

Answer: c
Explanation: A sequential access memory is one in which a particular memory location is accessed sequentially. In magnetic tape memory, data is accessed sequentially.

12. A Random Access Memory is one in which _____
a) Any location can be accessed sequentially
b) Any location can be accessed randomly
c) Any location can be accessed serially
d) Any location can be accessed parallely

Answer: b
Explanation: A Random Access Memory is one in which any location can be accessed randomly.

13. An example of RAM is _____
a) Floppy disk
b) Hard disk
c) Magnetic tape memory
d) Semiconductor RAM

Answer: d
Explanation: A Random Access Memory is one in which any location can be accessed randomly. A semiconductor RAM is too much fast and can occupy any space in the memory location.

14. A static memory is one in which _____
a) Content changes with time
b) Content doesn’t changes with time

c) Memory is static always
d) Memory is dynamic always

Answer: d
Explanation: A static memory is one in which content doesn't changes with time (i.e. stable). Dynamic memory is one in which content changes with time (i.e. unstable).

15. A dynamic memory is one in which _____
a) Content changes with time
b) Content doesn't changes with time
c) Memory is static always
d) Memory is dynamic always

Answer: d
Explanation: A static memory is one in which content doesn't change with time (i.e. stable). Dynamic memory is one in which content changes with time (i.e. unstable).

Memory Devices – 4

1. Dynamic memory cells use _____ as the storage device.
a) The reactance of a transistor
b) The impedance of a transistor
c) The capacitance of a transistor
d) The inductance of a transistor

Answer: c
Explanation: Capacitance of a transistor prevents from loss of information in a dynamic memory cell.

2. To store 1-bit of information, how many transistor is/are used _____
a) 1
b) 2
c) 3
d) 4

Answer: a
Explanation: Only one bit transistor is needed to store 1-bit of information.

3. Static memory holds data as long as _____
a) AC power is applied
b) DC power is applied
c) Capacitor is fully charged
d) High Conductivity

Answer: b
Explanation: In any semiconductor equipment, AC power can't be supplied directly. So, static memory holds the data as long as DC power is applied.

4. The example of dynamic memory is _____
a) CCD
b) Semiconductor dynamic RAM
c) Both CCD and semiconductor dynamic RAM
d) Floppy-Disk

Answer: c
Explanation: The examples of dynamic memories are CCD and semiconductor dynamic RAM because of the contents of both the memories changes with time.

5. In dynamic memory, CCD stands for _____
a) Charged Count Devices
b) Change Coupled Devices
c) Charge Coupled Devices
d) Charged Compact Disk

Answer: b
Explanation: In dynamic memory, CCD stands for Charge Coupled Devices.

6. Volatile memory refers to _____
a) The memory whose loosed data is achieved again when power to the memory circuit is removed
b) The memory which looses data when power to the memory circuit is removed
c) The memory which looses data when power to the memory circuit is applied
d) The memory whose loosed data is achieved again when power to the memory circuit is applied

Answer: b
Explanation: Volatile means 'liable to change rapidly' and volatile memory refers to the memory which looses data rapidly when power to the memory circuit is removed. Thus, it looks after it's data as long as it is powered. Non-volatile means 'not volatile' and non-volatile memory refers to the memory which retains the data even if there is a break in the power supply.

7. Non-volatile memory refers to _____
a) The memory whose loosed data is retained again when power to the memory circuit is removed/applied
b) The memory which looses data when power to the memory circuit is removed
c) The memory which looses data when power to the memory circuit is applied
d) The memory whose loosed data is achieved again when power to the memory circuit is applied

Answer: a
Explanation: Volatile means 'liable to change rapidly' and volatile memory refers to the memory which looses data rapidly when power to the memory circuit is removed. Thus, it looks after it's data as long as it is powered. Non-volatile means 'not volatile' and non-volatile memory refers to the memory which retains the data even if there is a break in the power supply.

8. The example of non-volatile memory device is _____
a) Magnetic Core Memory
b) Read Only Memory
c) Random Access Memory
d) Both Magnetic Core Memory and Read Only Memory

Answer: d
Explanation: Non-volatile means 'not volatile' and non-volatile memory refers to the memory which retains the data even if there is a break in the power supply. The examples of non-volatile memory devices are Magnetic Core Memory & ROM because both have capability to retain the data.

9. Based on material used for construction, memory devices are classifieds into _____ categories.
a) 2
b) 3

c) 4
d) 5

Answer: a
Explanation: Based on material used for construction, memory devices are classifieds into two categories, viz., Magnetic and Semiconductor memory. Magnetic recording is the process of storing data magnetically. Hard disk, floppy disk, magnetic tape are examples of magnetic recording process.

10. Magnetic recording is the process of _____
a) Storing data symmetrically
b) Storing data sequentially
c) Storing data magnetically
d) Both storing data symmetrically and

Answer: c
Explanation: Based on material used for construction, memory devices are classifieds into two categories, viz., Magnetic and Semiconductor memory. Magnetic recording is the process of storing data magnetically. Hard disk, floppy disk, magnetic tape are examples of the magnetic recording process.

11. Magnetic drum is a storage medium using _____
a) The surface of a jumping magnetic drum
b) The surface of a rotating magnetic drum
c) The surface of a stopped magnetic drum
d) The surface of a moving magnetic drum

Answer: b
Explanation: Magnetic drum is a storage medium using the surface of a rotating magnetic drum which have tendency to hold the data.

12. Magnetic core is the digital memory in which data is stored magnetically in individual cores operated by _____
a) Up and down select wires
b) Row and column select wires
c) Serial and parallel select wires
d) Up and Serial select wires

Answer: b
Explanation: Magnetic core is the digital memory in which data is stored magnetically in individual cores operated by row and column select wires, with data obtained from sense wire.

13. By which technology, semiconductor memories are constructed?
a) PLD
b) LSI
c) VLSI
d) Both LSI and VLSI

Answer: d
Explanation: Generally, semiconductor memories are constructed using Large Scale Integration (LSI) or Very Large Scale Integration (VLSI) because these are made up of NMOS, CMOS, BJT, etc.

Memory Devices – 5

1. When two or more devices try to write data in a bus simultaneously, is known as _____
a) Bus collisions
b) Address multiplexing
c) Address decoding
d) Bus contention

Answer: d
Explanation: Bus contention is an undesirable state of the bus of a computer, in which more than one memory mapped device or the CPU is attempting to place output values onto the bus at once.

2. A memory is a collection of _____
a) Unit cells
b) Storage cells
c) Data cells
d) Binary cells

Answer: b
Explanation: A memory is a collection of storage cells with associated circuits needed to transfer information.

3. To transfer the information from input to output and vice versa, the cells used are _____
a) Storage cells
b) Data cells
c) Unit cells
d) Both data and unit cells

Answer: a
Explanation: To transfer the information from input to output and vice versa, the cells used are called storage cells. The storage cells stores data in the form of binary information.

4. The data stored in a group of bits is called _____
a) Nibble
b) Word
c) Byte
d) Address

Answer: b
Explanation: The data stored in a group of bits is called word. Usually, a word is a group of 16-bits or 2-bytes.

5. Each word consist of a sequence of _____
a) Letters
b) Binary numbers

c) Hexadecimal numbers
d) Gray codes

Answer: b
Explanation: Each word consists of a sequence of 0s and 1s (i.e. binary numbers). Usually, a word is a group of 16-bits or 2-bytes.

6. Each word stored in a memory location is represented by _____
a) RAM
b) ROM
c) Storage class
d) Address

Answer: d
Explanation: Each word stored in a memory location is represented by address. Usually, a word is a group of 16-bits or 2-bytes.

7. The group of each 8-bit is called _____
a) Nibble
b) Flag
c) Byte
d) Word

Answer: c
Explanation: 1 byte = 8-bit, 4-bits = 1 nibble and 16-bits = 1 word.

8. The capacity of a memory unit is _____
a) The number of binary input stored
b) The number of words stored
c) The number of bytes stored
d) All of the Mentioned

Answer: c
Explanation: The total number of bytes that can be stored, is the maximum capacity of a memory unit. However, memory unit is the smallest unit of a processor.

9. The communication between memory and its environment is achieved through _____
a) Control lines
b) Data input/output lines
c) Address selection lines
d) All of the Mentioned

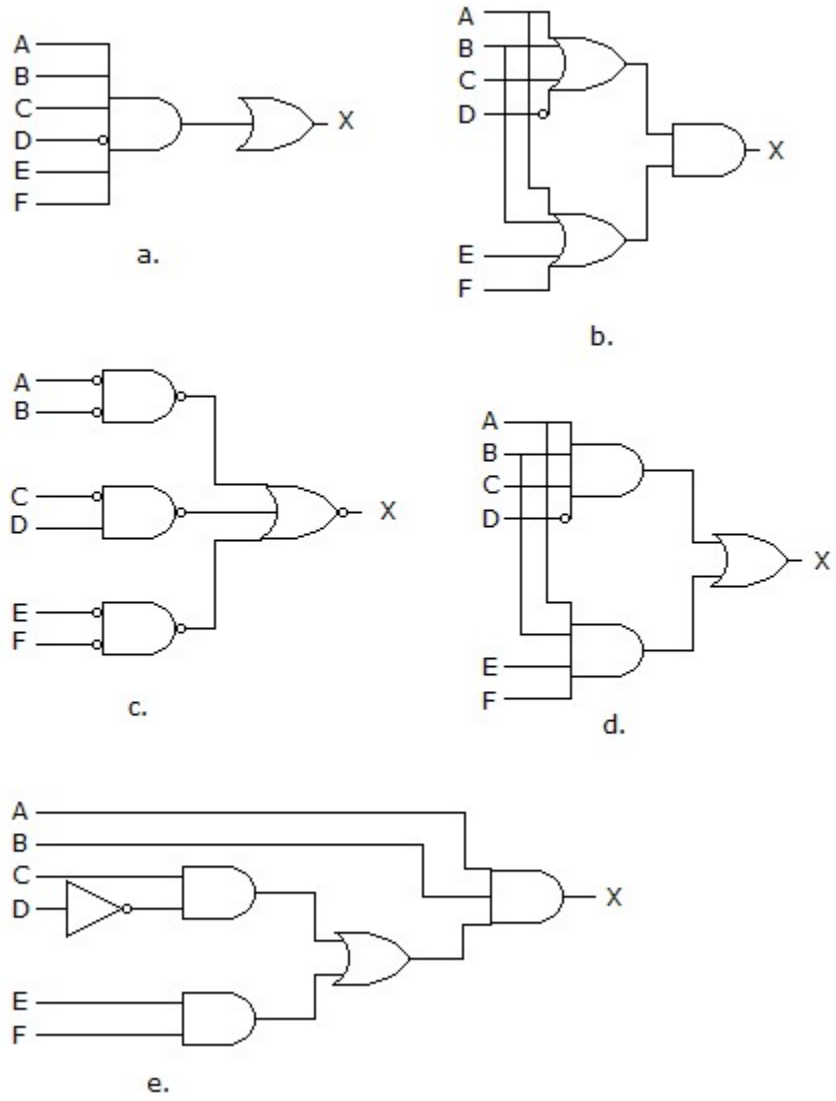
Answer: d
Explanation: Firstly, the data input is needed to transfer the information and it is passed through the address lines and then controlled by control lines. The control lines are responsible for the timing and control of the signals sent and received.

10. One of the most important specifications on magnetic media is the _____
a) Polarity reversal rate
b) Tracks per inch
c) Data transfer rate
d) Rotation speed

Answer: c
Explanation: The rate of data transfer depends on the properties of magnetic media.

COMBINATIONAL CIRCUIT

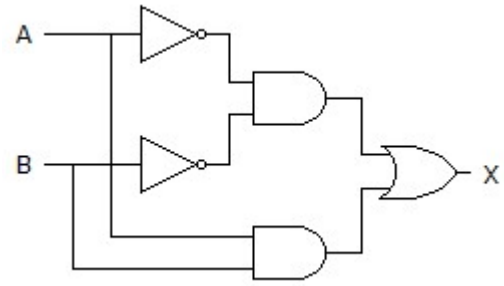
1. Which of the circuits in figure (a to d) is the sum-of-products implementation of figure (e)?



a) a
b) b
c) c
d) d

Answer: d
Explanation: SOP means Sum Of Products form which represents the sum of product terms having variables in complemented as well as in uncomplemented form. Here, the diagram of d contains the OR gate followed by the AND gates, so it is in SOP form.

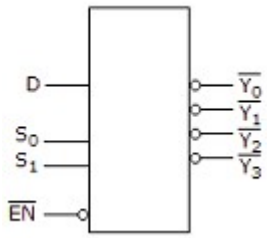
ons represents the logic diagram shown?



a) X=AB'+A'B
b) X=(AB)'+AB
c) X=(AB)'+A'B'
d) X=A'B'+AB

Answer: d
Explanation: 1st output of AND gate is = A'B'
2nd AND gate's output is = AB and,
OR gate's output is = (A'B')+(AB) = AB + A'B'.

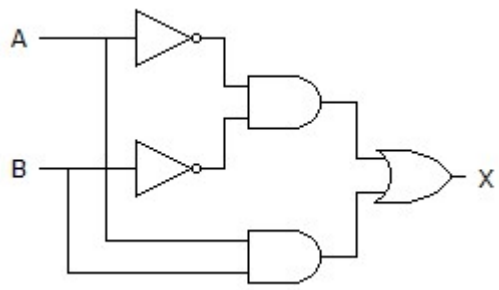
3. The device shown here is most likely a _____



a) Comparator
b) Multiplexer
c) Inverter
d) Demultiplexer

Answer: d
Explanation: The given diagram is demultiplexer, because it takes single input & gives many outputs. A demultiplexer is a combinational circuit that takes a single output and latches it to multiple outputs depending on the select lines.

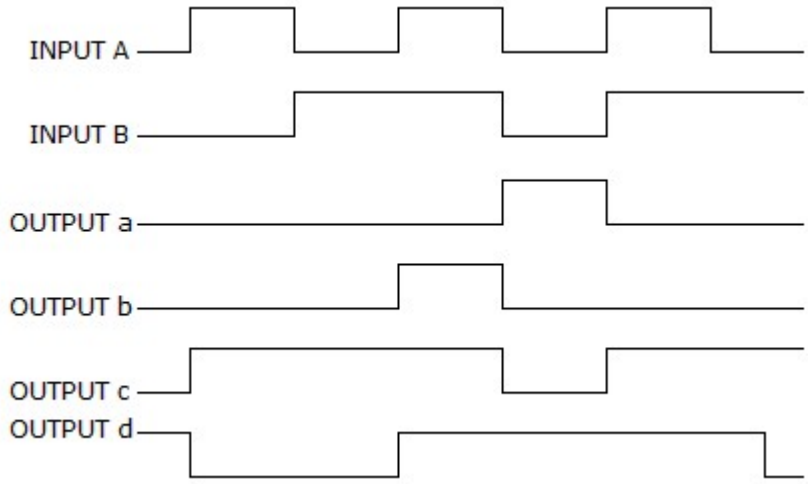
ed by the figure shown below?



a) XOR
b) XNOR
c) AND
d) XAND

Answer: b
Explanation: After solving the circuit we get (A'B')+AB as output, which is XNOR operation. Thus, it will produce 1 when inputs are even number of 1s or all 0s, and produce 0 when input is odd number of 1s.

5. For a two-input XNOR gate, with the input waveforms as shown below, which output waveform is correct?



a) d
b) a
c) c
d) b

Answer: a
Explanation: When both inputs are same then the o/p is high for a XNOR gate.
i.e., A B O/P
0 0 1
0 1 0

1 0 0
1 1 1.
Thus, it will produce 1 when inputs are even number of 1s or all 0s, and produce 0 when input is odd number of 1s.

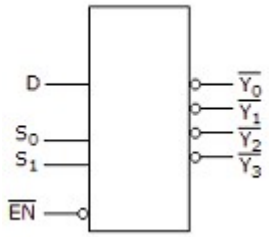
6. Which of the following combinations of logic gates can decode binary 1101?
a) One 4-input AND gate
b) One 4-input AND gate, one inverter
c) One 4-input AND gate, one OR gate
d) One 4-input NAND gate, one inverter

Answer: b
Explanation: For decoding any number output must be high for that code and this is possible in One 4-input NAND gate, one inverter option only. A decoder is a combinational circuit that converts binary data to n-coded data upto 2^n outputs.

7. What is the indication of a short to ground in the output of a driving gate?
a) Only the output of the defective gate is affected
b) There is a signal loss to all load gates
c) The node may be stuck in either the HIGH or the LOW state
d) The affected node will be stuck in the HIGH state

Answer: b
Explanation: Short to ground in the output of a driving gate indicates of a signal loss to all load gates. This results in information being disrupted and loss of data.

8. For the device shown here, assume the D input is LOW, both S inputs are LOW and the input is LOW. What is the status of the Y' outputs?



a) All are HIGH
b) All are LOW
c) All but Y0 are LOW
d) All but Y0 are HIGH

Answer: d
Explanation: In the given diagram, S0 and S1 are selection bits. So,
I/P S0 S1 O/P
D = 0 0 0 Y0

D = 0 0 1 Y1
D = 0 1 0 Y2
D = 0 1 1 Y3
Hence, inputs are S0 and S1 are Low means 0, so output is Y0 and rest all are HIGH.

9. The carry propagation can be expressed as _____
a) Cp = AB
b) Cp = A + B
c) All but Y0 are LOW
d) All but Y0 are HIGH

Answer: b
Explanation: This happens in parallel adders (where we try to add numbers in parallel via more than one adders). A carry propagation occurs when carry from one adder needs to be forwarded to other adder and that second adder is holding the computation (addition) because carry from first adder has not come yet. So, there is a slight delay for second adder and this is known as carry propagation.

10. 3 bits full adder contains _____
a) 3 combinational inputs
b) 4 combinational inputs
c) 6 combinational inputs
d) 8 combinational inputs

Answer: d
Explanation: Full Adder is a combinational circuit with 3 input bits and 2 output bits CARRY and SUM. Three bits full adder requires 2^3 = 8 combinational circuits.

Multiplexers (Data Selectors) – 1

1. What is a multiplexer?
a) It is a type of decoder which decodes several inputs and gives one output
b) A multiplexer is a device which converts many signals into one
c) It takes one input and results into many output
d) It is a type of encoder which decodes several inputs and gives one output

Answer: b
Explanation: A multiplexer (or MUX) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line, depending on the active select lines.

2. Which combinational circuit is renowned for selecting a single input from multiple inputs & directing the binary information to output line?
a) Data Selector
b) Data distributor
c) Both data selector and data distributor
d) De-Multiplexer

Answer: a
Explanation: Data Selector is another name of Multiplexer. A multiplexer (or MUX) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line, depending on the active select lines.

3. It is possible for an enable or strobe input to undergo an expansion of two or more MUX ICs to the digital multiplexer with the proficiency of large number of _____
a) Inputs
b) Outputs
c) Selection lines
d) Enable lines

Answer: a
Explanation: It is possible for an enable or strobe input to undergo an expansion of two or more MUX ICs to the digital multiplexer with the proficiency of large number of inputs.

4. Which is the major functioning responsibility of the multiplexing combinational circuit?
a) Decoding the binary information
b) Generation of all minterms in an output function with OR-gate
c) Generation of selected path between multiple sources and a single destination
d) Encoding of binary information

Answer: c
Explanation: The major functioning responsibility of the multiplexing combinational circuit is generation of selected path between multiple sources and a single destination because it makes the circuit too flexible. A multiplexer (or MUX) is a device that selects one of several

analog or digital input signals and forwards the selected input into a single line, depending on the active select lines.

5. What is the function of an enable input on a multiplexer chip?
a) To apply Vcc
b) To connect ground
c) To active the entire chip
d) To active one half of the chip

Answer: c
Explanation: Enable input is used to active the chip, when enable is high the chip works (ACTIVE), when enable is low the chip does not work (MEMORY). However, Enable can be Active-High or Active-Low, indicating it is active either when it is connected to VCC or GND respectively.

6. One multiplexer can take the place of _____
a) Several SSI logic gates
b) Combinational logic circuits
c) Several Ex-NOR gates
d) Several SSI logic gates or combinational logic circuits

Answer: d
Explanation: A multiplexer (or MUX) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line, depending on the active select lines. Since many operational behaviour can be performed by using a multiplexer. Whereas, a combinational circuit is a combination of many logic gates which makes the circuit more complex.

7. A digital multiplexer is a combinational circuit that selects _____
a) One digital information from several sources and transmits the selected one
b) Many digital information and convert them into one
c) Many decimal inputs and transmits the selected information
d) Many decimal outputs and accepts the selected information

Answer: a
Explanation: A digital multiplexer is a combinational circuit that selects one digital information from several sources and transmits the selected information on a single output line depending on the status of the select lines. That is why it is also known as a data selector.

8. In a multiplexer, the selection of a particular input line is controlled by _____
a) Data controller
b) Selected lines
c) Logic gates
d) Both data controller and selected lines

Answer: b
Explanation: The selection of a particular input line is controlled by a set of selected lines in a multiplexer, which helps to select a particular input from several sources.

9. If the number of n selected input lines is equal to 2^m then it requires _____ select lines.
a) 2
b) m
c) n
d) 2^n

Answer: b
Explanation: If the number of n selected input lines is equal to 2^m then it requires m select lines to select one of m select lines.

10. How many select lines would be required for an 8-line-to-1-line multiplexer?
a) 2
b) 4
c) 8
d) 3

Answer: d
Explanation: 2^n input lines, n control lines and 1 output line available for MUX. Here, 8 input lines mean 2^3 inputs. So, 3 control lines are possible. Depending on the status of the select lines, the input is selected and fed to the output.

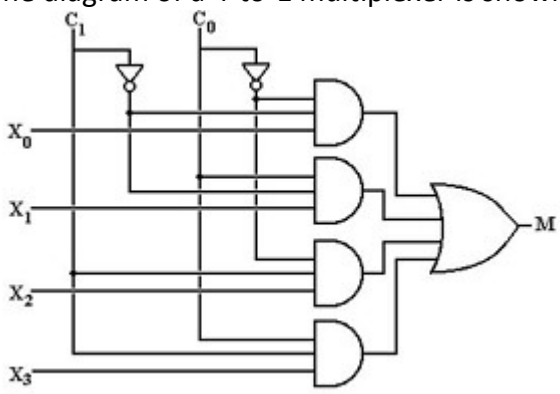
11. A basic multiplexer principle can be demonstrated through the use of a _____
a) Single-pole relay
b) DPDT switch
c) Rotary switch
d) Linear stepper

Answer: c
Explanation: A basic multiplexer principle can be demonstrated through the use of a rotary switch. Since its behaviour is similar to the multiplexer. There are around 10 digits out of which one is selected one at a time and fed to the output.

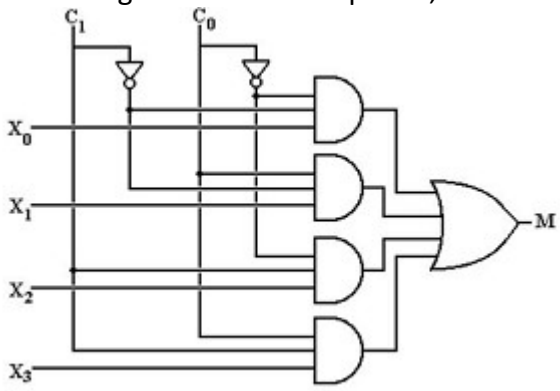
12. How many NOT gates are required for the construction of a 4-to-1 multiplexer?
a) 3
b) 4
c) 2
d) 5

Answer: c
Explanation: There are two NOT gates required for the construction of 4-to-1 multiplexer. x0, x1, x2 and x3 are the inputs and C1 and C0 are the select lines and M is the output.

The diagram of a 4-to-1 multiplexer is shown below:



13. In the given 4-to-1 multiplexer, if c1 = 0 and c0 = 1 then the output M is _____



a) X0
b) X1
c) X2
d) X3

Answer: b
Explanation: The output will be X1, because c1 = 0 and c0 = 1 results into 1 which further results as X1. And rest of the AND gates gives output as 0.

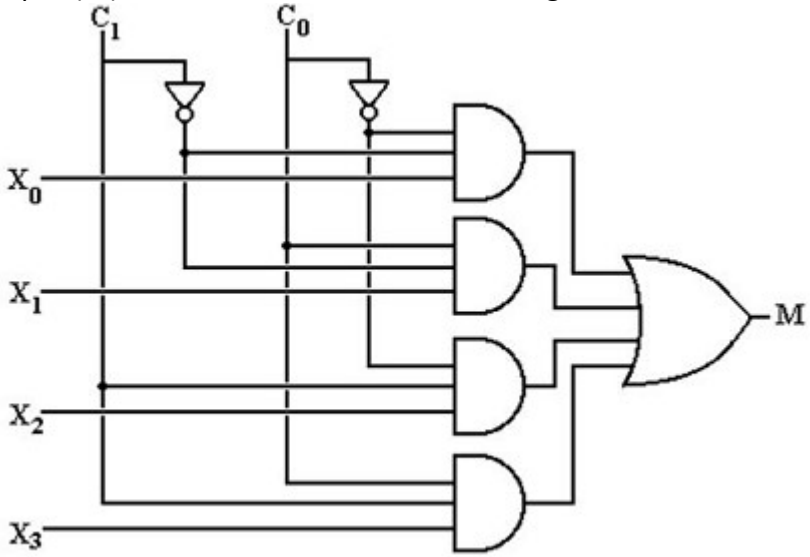
14. The enable input is also known as _____
a) Select input
b) Decoded input
c) Strobe
d) Sink

Answer: c
Explanation: The enable input is also known as strobe which is used to cascade two or more multiplexer ICs to construct a multiplexer with a larger number of inputs. Enable input activates the multiplexer to operate.

Multiplexers (Data Selectors) – 2

1. 4 to 1 MUX would have _____
a) 2 inputs
b) 3 inputs
c) 4 inputs
d) 5 inputs

Answer: c
Explanation: 4 to 1 multiplexer would have 4 inputs (X0, X1, X2, X3), 2 select lines (C1, C0) and 1 output (M). It can be observed from this diagram:



2. The two input MUX would have _____
a) 1 select line
b) 2 select lines
c) 4 select lines
d) 3 select lines

Answer: a
Explanation: The two input multiplexer would have n select lines in 2^n. Thus n =1. Therefore, it has 1 select line.

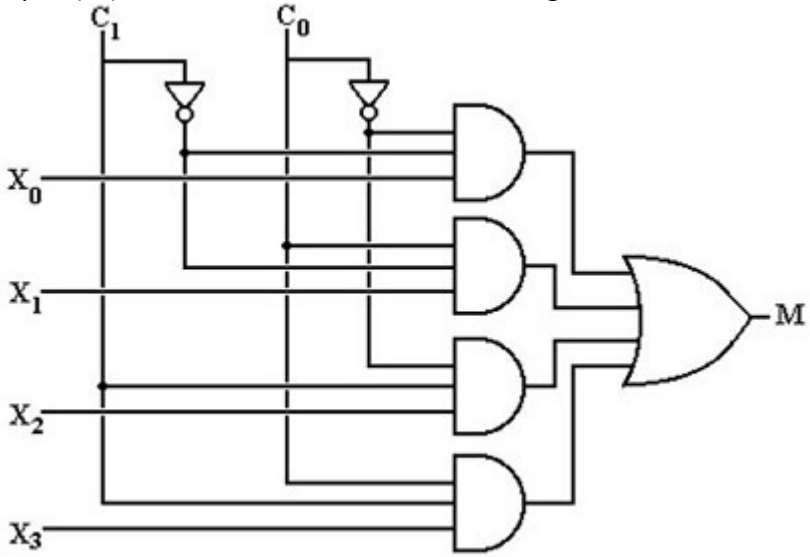
3. A combinational circuit that selects one from many inputs are _____
a) Encoder
b) Decoder
c) Demultiplexer
d) Multiplexer

Answer: d
Explanation: A combinational circuit that selects one from many inputs is known as Multiplexer.

Whereas, a combinational circuit that divides one input into multiple outputs is known as De-multiplexer.

4. 4 to 1 MUX would have _____
a) 1 output
b) 2 outputs
c) 3 outputs
d) 4 outputs

Answer: a
Explanation: 4 to 1 multiplexer would have 4 inputs (X0, X1, X2, X3), 2 select lines (C1, C0) and 1 output (M). It can be observed from this diagram:



5. Which of the following circuit can be used as parallel to serial converter?
a) Multiplexer
b) Demultiplexer
c) Decoder
d) Digital counter

Answer: a
Explanation: A combinational circuit that selects one from many inputs is known as Multiplexer. In multiplexer, different inputs are inserted parallely and then it gives one output which is in serial form.

6. A combinational circuit is one in which the output depends on the _____
a) Input combination at the time
b) Input combination and the previous output
c) Input combination at that time and the previous input combination
d) Present output and the previous output

Answer: a
Explanation: A combinational circuit is one in which the output depends on the input

combination at the time, whereas, a sequential circuit is one in which the output depends on present input as well past outputs.

7. Without any additional circuitry an 8:1 MUX can be used to obtain _____
a) Some but not all Boolean functions of 3 variables
b) All function of 3 variables but none of 4 variables
c) All functions of 3 variables and some but not all of 4 variables
d) All functions of 4 variables

Answer: d
Explanation: A 2^n:1 MUX can implement all logic functions of (n+1) variables without any additional circuitry. Thus 8:1 MUX can implement all logic functions of (3+1) variables, for 4 variables there are 16 possible combinations. So to use 8:1 MUX use 3 inputs as select lines of MUX and the 4th input as input of MUX.

8. A basic multiplexer principle can be demonstrated through the use of a _____
a) Single-pole relay
b) DPDT switch
c) Rotary switch
d) Linear stepper

Answer: c
Explanation: A combinational circuit that selects one from many inputs is known as Multiplexer. A basic multiplexer principle can be demonstrated through the use of a rotary switch. Because rotary switch gives one output corresponding to their inputs.

9. One multiplexer can take the place of _____
a) Several SSI logic gates
b) Combinational logic circuits
c) Several Ex-NOR gates
d) Several SSI logic gates or combinational logic circuits

Answer: d
Explanation: A combinational circuit that selects one from many inputs is known as Multiplexer. One multiplexer can take the place of several SSI logic gates or combinational logic circuits because it has a lot of functions to perform different operations.

10. The inputs/outputs of an analog multiplexer/demultiplexer are _____
a) Bidirectional
b) Unidirectional
c) Even parity
d) Binary-coded decimal

Answer: a
Explanation: One multiplexer can be used as demultiplexer. Hence, it is called bidirectional or two-way transmission.

11. If enable input is high then the multiplexer is _____
a) Enable
b) Disable
c) Saturation
d) High Impedance

Answer: b
Explanation: If enable input is high then the multiplexer is disabled because enable input is in inverted mode always (i.e. E').

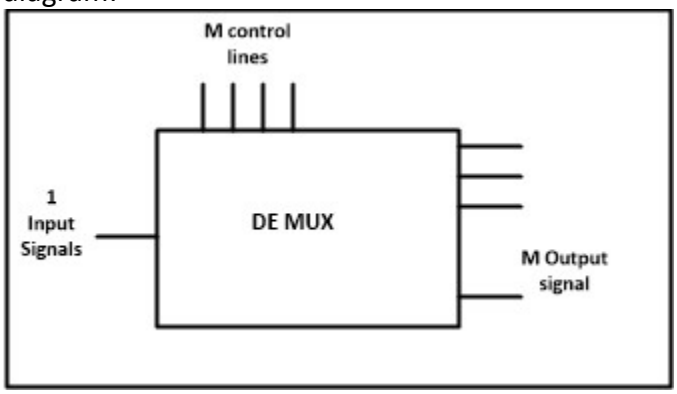
12. What is data routing in a multiplexer?
a) It spreads the information to the control unit
b) It can be used to route data from one of several source to destination
c) It is an application of multiplexer
d) It can be used to route data and it is an application of multiplexer

Answer: d
Explanation: Multiplexing means passing more than one data through the same channel. Data routing is an application of multiplexer and it can be used to route data from one of several source to destination.

Demultiplexers (Data Distributors) – 1

1. The word demultiplex means _____
a) One into many
b) Many into one
c) Distributor
d) One into many as well as Distributor

Answer: d
Explanation: The word demultiplex means “one into many” and distributor. A demultiplexer sends a single input to multiple outputs, depending on the select lines. It is clear from the diagram:



2. Why is a demultiplexer called a data distributor?
a) The input will be distributed to one of the outputs
b) One of the inputs will be selected for the output
c) The output will be distributed to one of the inputs
d) Single input to Single Output

Answer: a
Explanation: A demultiplexer sends a single input to multiple outputs, depending on the select lines. For one input, the demultiplexer gives several outputs. That is why it is called a data distributor.

3. Most demultiplexers facilitate which type of conversion?
a) Decimal-to-hexadecimal
b) Single input, multiple outputs
c) AC to DC
d) Odd parity to even parity

Answer: b
Explanation: A demultiplexer sends a single input to multiple outputs, depending on the select lines. Demultiplexer converts single input into multiple outputs.

4. In 1-to-4 demultiplexer, how many select lines are required?
a) 2
b) 3

c) 4
d) 5

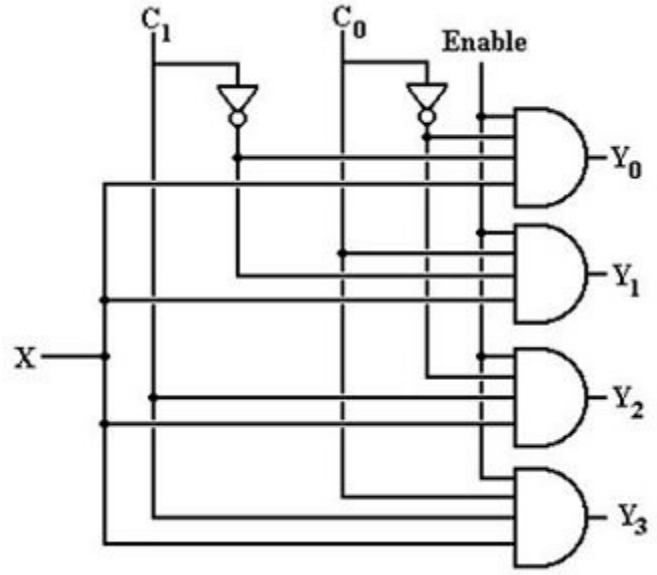
Answer: a
Explanation: The formula for total no. of outputs is given by 2^n, where n is the no. of select lines. Therefore, for 1:4 demultiplexer, 2 select lines are required.

5. In a multiplexer the output depends on its _____
a) Data inputs
b) Select inputs
c) Select outputs
d) Enable pin

Answer: b
Explanation: A demultiplexer sends a single input to multiple outputs, depending on the select lines. As the select input changes, the output of the multiplexer varies according to that input.

6. In 1-to-4 multiplexer, if C1 = 0 & C2 = 1, then the output will be _____
a) Y0
b) Y1
c) Y2
d) Y3

Answer: b
Explanation: It can be calculated from the figure shown below:

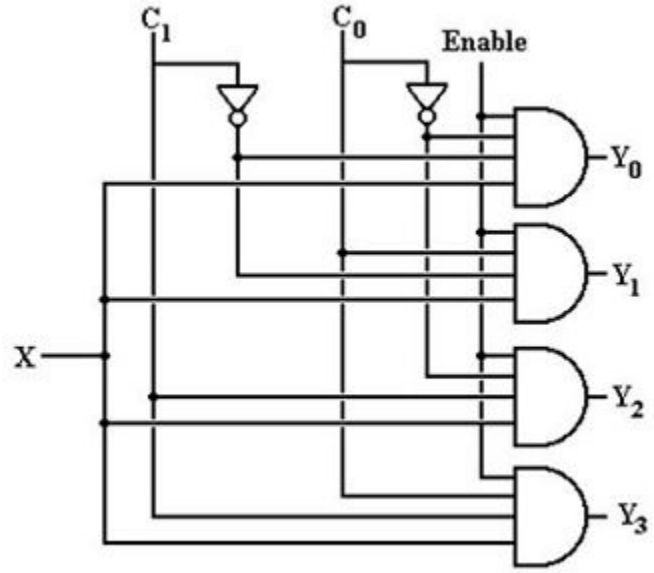


For C0 =1 and C1 =0, Y1 will be the output as 0 and 1 are the bit combinations of 1.

7. In 1-to-4 multiplexer, if C1 = 1 & C2 = 1, then the output will be _____
a) Y0
b) Y1

c) Y2
d) Y3

Answer: d
Explanation: It can be calculated from the figure shown below:



For C0 =1 and C1 =0, Y3 will be the output as 0 and 1 are the bit combinations of 1.

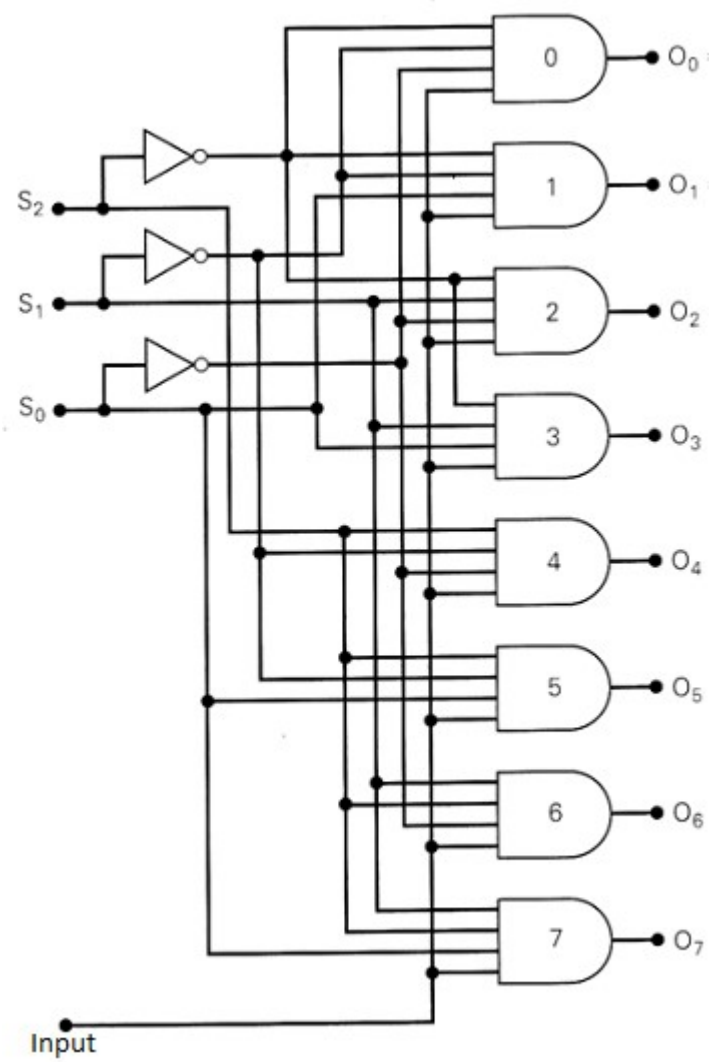
8. How many select lines are required for a 1-to-8 demultiplexer?
a) 2
b) 3
c) 4
d) 5

Answer: b
Explanation: The formula for total no. of outputs is given by 2^n, where n is the no. of select lines. In this case n = 3 since $2^3 = 8$.

9. How many AND gates are required for a 1-to-8 multiplexer?
a) 2
b) 6
c) 8
d) 5

Answer: c
Explanation: The number of AND gates required will be equal to the number of outputs in a demultiplexer, which are 8.

10. The output Q4 of this 1-to-8 demultiplexer is _____



a) Q2.(Q1)'.Q0.I
b) Q2.Q1.(Q0)'.I
c) Q2.(Q1)'.(Q0)'.I
d) Q2.(Q1).Q0.I

Answer: c
Explanation: The output Y4 = Q2.(Q1)'.(Q0)'.I. since the bit combinations of 4 are 100.

11. Which IC is used for the implementation of 1-to-16 DEMUX?
a) IC 74154
b) IC 74155
c) IC 74139
d) IC 74138

Answer: a
Explanation: IC 74154 is used for the implementation of 1-to-16 DEMUX, whose output is inverted input.

Demultiplexers (Data Distributors) – 2

1. Why is a demultiplexer called a data distributor?
a) The input will be distributed to one of the outputs
b) One of the inputs will be selected for the output
c) The output will be distributed to one of the inputs
d) Single input gives single output

Answer: a
Explanation: A demultiplexer sends a single input to multiple outputs, depending on the select lines. For one input, the demultiplexer gives several outputs. That is why it is called a data distributor.

2. Most demultiplexers facilitate which type of conversion?
a) Decimal-to-hexadecimal
b) Single input, multiple outputs
c) AC to DC
d) Odd parity to even parity

Answer: b
Explanation: A demultiplexer sends a single input to multiple outputs, depending on the select lines. Demultiplexer converts single input into multiple outputs.

3. In 1-to-4 demultiplexer, how many select lines are required?
a) 2
b) 3
c) 4
d) 5

Answer: a
Explanation: The formula for total no. of outputs is given by 2^n, where n is the no. of select lines. Therefore, for 1:4 demultiplexer, 2 select lines are required.

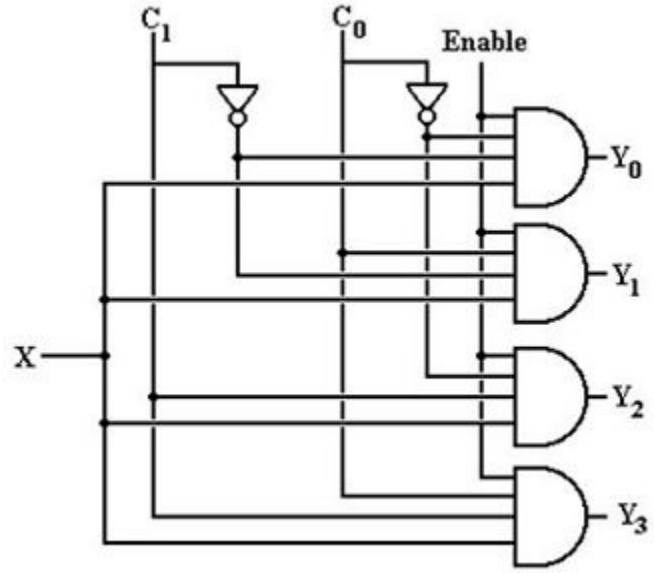
4. In a multiplexer the output depends on its _____
a) Data inputs
b) Select inputs
c) Select outputs
d) Enable pin

Answer: b
Explanation: A demultiplexer sends a single input to multiple outputs, depending on the select lines. As the select input changes, the output of the multiplexer varies according to that input.

5. In 1-to-4 multiplexer, if C1 = 1 & C2 = 1, then the output will be _____
a) Y0
b) Y1

c) Y2
d) Y3

Answer: d
Explanation: It can be calculated from the figure shown below:



For C0 =1 and C1 =1, Y3 will be the output as 0 and 1 are the bit combinations of 1.

6. How many select lines are required for a 1-to-8 demultiplexer?
a) 2
b) 3
c) 4
d) 5

Answer: b
Explanation: The formula for total no. of outputs is given by 2^n, where n is the no. of select lines. In this case n = 3 since $2^3 = 8$.

7. How many AND gates are required for a 1-to-8 multiplexer?
a) 2
b) 6
c) 8
d) 5

Answer: c
Explanation: The number of AND gates required will be equal to the number of outputs in a demultiplexer, which are 8.

8. Which IC is used for the implementation of 1-to-16 DEMUX?
a) IC 74154
b) IC 74155

c) IC 74139
d) IC 74138

Answer: a
Explanation: IC 74154 is used for the implementation of 1-to-16 DEMUX, whose output is inverted input.

Encoders

1. How many inputs will a decimal-to-BCD encoder have?
a) 4
b) 8
c) 10
d) 16

Answer: c
Explanation: An encoder is a combinational circuit encoding the information of 2^n input lines to n output lines, thus producing the binary equivalent of the input. Thus, a Decimal-to-bcd converter has decimal values as inputs which range from 0-9. So, total 10 inputs are there in a decimal-to-BCD encoder.

2. How many outputs will a decimal-to-BCD encoder have?
a) 4
b) 8
c) 12
d) 16

Answer: a
Explanation: An encoder is a combinational circuit encoding the information of 2^n input lines to n output lines, thus producing the binary equivalent of the input. Thus, a decimal to BCD encoder has 4 outputs.

3. How is an encoder different from a decoder?
a) The output of an encoder is a binary code for 1-of-N input
b) The output of a decoder is a binary code for 1-of-N input
c) The output of an encoder is a binary code for N-of-1 output
d) The output of a decoder is a binary code for N-of-1 output

Answer: a
Explanation: An encoder is a combinational circuit encoding the information of 2^n input lines to n output lines, thus producing the binary equivalent of the input. It performs the opposite operation of a decoder which results in 2^n outputs from n inputs. Thus, an encoder different from a decoder because of the output of an encoder is a binary code for 1-of-N input.

4. If we record any music in any recorder, such types of process is called _____
a) Multiplexing
b) Encoding
c) Decoding
d) Demultiplexing

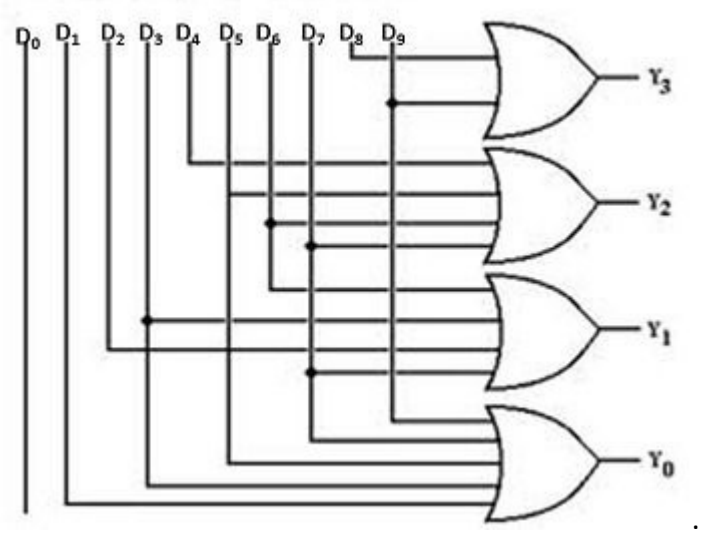
Answer: b
Explanation: If we record any music in any recorder, it means that we are giving data to a recorder. So, such process is called encoding. Getting back the music from the recorded data, is known as decoding.

5. Can an encoder be a transducer?
a) Yes
b) No
c) May or may not be
d) Both are not even related slightly

Answer: a
Explanation: Of course, a transducer is a device which has the capability to emit data as well as to accept. Transducer converts signal from one form of energy to another.

6. How many OR gates are required for a Decimal-to-bcd encoder?
a) 2
b) 10
c) 3
d) 4

Answer: d
Explanation: An encoder is a combinational circuit encoding the information of 2^n input lines to n output lines, thus producing the binary equivalent of the input.
This is clear from the diagram that it requires 4 OR gates:



7. How many OR gates are required for an octal-to-binary encoder?
a) 3
b) 2
c) 8
d) 10

Answer: a
Explanation: An encoder is a combinational circuit encoding the information of 2^n input lines to n output lines, thus producing the binary equivalent of the input. Thus, in octal to binary encoder there are 8 ($=2^3$) inputs, thus 3 output lines.

8. For 8-bit input encoder how many combinations are possible?
a) 8
b) 2^8
c) 4
d) 2^4

Answer: b
Explanation: An encoder is a combinational circuit encoding the information of 2^n input lines to n output lines, thus producing the binary equivalent of the input. There are 2^8 combinations are possible for an 8-bit input encoder but out of which only 8 are used using 3 output lines. It is a disadvantage of encoder.

9. The discrepancy of 0 output due to all inputs being 0 or D0, being 0 is resolved by using additional input known as _____
a) Enable
b) Disable
c) Strobe
d) Clock

Answer: a
Explanation: Such problems are resolved by using enable input, which behaves as active if it gets 0 as input since it is an active-low pin.

10. Can an encoder be called as multiplexer?
a) No
b) Yes
c) Sometimes
d) Never

Answer: b
Explanation: A multiplexer or MUX is a combination circuit that contains more than one input line, one output line and more than one selection line. Whereas, an encoder is also considered a type of multiplexer but without a single output line and without any selection lines.

11. If two inputs are active on a priority encoder, which will be coded on the output?
a) The higher value
b) The lower value
c) Neither of the inputs
d) Both of the inputs

Answer: a
Explanation: An encoder is a combinational circuit encoding the information of 2^n input lines to n output lines, thus producing the binary equivalent of the input. If two inputs are active on a priority encoder, the input of higher value will be coded in the output.

ARITHMETIC CIRCUIT

Half Adder & Full Adder

1. In parts of the processor, adders are used to calculate _____
a) Addresses
b) Table indices
c) Increment and decrement operators
d) All of the Mentioned

Answer: d
Explanation: Adders are used to perform the operation of addition. Thus, in parts of the processor, adders are used to calculate addresses, table indices, increment and decrement operators, and similar operations.

2. Total number of inputs in a half adder is _____
a) 2
b) 3
c) 4
d) 1

Answer: a
Explanation: Total number of inputs in a half adder is two. Since an EXOR gates has 2 inputs and carry is connected with the input of EXOR gates. The output of half-adder is also 2, them being, SUM and CARRY. The output of EXOR gives SUM and that of AND gives carry.

3. In which operation carry is obtained?
a) Subtraction
b) Addition
c) Multiplication
d) Both addition and subtraction

Answer: b
Explanation: In addition, carry is obtained. For example: 1 0 1 + 1 1 1 = 1 0 0; in this example carry is obtained after 1st addition (i.e. 1 + 1 = 1 0). In subtraction, borrow is obtained. Like, 0 – 1 = 1 (borrow 1).

4. If A and B are the inputs of a half adder, the sum is given by _____
a) A AND B
b) A OR B
c) A XOR B
d) A EX-NOR B

Answer: c
Explanation: If A and B are the inputs of a half adder, the sum is given by A XOR B, while the carry is given by A AND B.

5. If A and B are the inputs of a half adder, the carry is given by _____
a) A AND B
b) A OR B
c) A XOR B
d) A EX-NOR B

Answer: a
Explanation: If A and B are the inputs of a half adder, the carry is given by: A(AND)B, while the sum is given by A XOR B.

6. Half-adders have a major limitation in that they cannot _____
a) Accept a carry bit from a present stage
b) Accept a carry bit from a next stage
c) Accept a carry bit from a previous stage
d) Accept a carry bit from the following stages

Answer: c
Explanation: Half-adders have a major limitation in that they cannot accept a carry bit from a previous stage, meaning that they cannot be chained together to add multi-bit numbers. However, the two output bits of a half-adder can also represent the result A+B=3 as sum and carry both being high.

7. The difference between half adder and full adder is _____
a) Half adder has two inputs while full adder has four inputs
b) Half adder has one output while full adder has two outputs
c) Half adder has two inputs while full adder has three inputs
d) All of the Mentioned

Answer: c
Explanation: Half adder has two inputs while full adder has three outputs; this is the difference between them, while both have two outputs SUM and CARRY.

8. If A, B and C are the inputs of a full adder then the sum is given by _____
a) A AND B AND C
b) A OR B AND C
c) A XOR B XOR C
d) A OR B OR C

Answer: c
Explanation: If A, B and C are the inputs of a full adder then the sum is given by A XOR B XOR C.

9. If A, B and C are the inputs of a full adder then the carry is given by _____
a) A AND B OR (A OR B) AND C
b) A OR B OR (A AND B) C
c) (A AND B) OR (A AND B)C
d) A XOR B XOR (A XOR B) AND C

Answer: a
Explanation: If A, B and C are the inputs of a full adder then the carry is given by A AND B OR (A OR B) AND C, which is equivalent to (A AND B) OR (B AND C) OR (C AND A).

10. How many AND, OR and EXOR gates are required for the configuration of full adder?
a) 1, 2, 2
b) 2, 1, 2
c) 3, 1, 2
d) 4, 0, 1

Answer: b
Explanation: There are 2 AND, 1 OR and 2 EXOR gates required for the configuration of full adder, provided using half adder. Otherwise, configuration of full adder would require 3 AND, 2 OR and 2 EXOR.

Design of Combinational Circuits

1. The basic building blocks of the arithmetic unit in a digital computers are _____
a) Subtractors
b) Adders
c) Multiplexer
d) Comparator

Answer: b
Explanation: The basic building blocks of the arithmetic unit in a digital computers are adders. Since, a parallel adder is constructed with a number of full-adder circuits connected in cascade. By controlling the data inputs to the parallel adder, it is possible to obtain different types of arithmetic operations.

2. A digital system consists of _____ types of circuits.
a) 2
b) 3
c) 4
d) 5

Answer: a
Explanation: A digital system consists of two types of circuits and these are combinational and sequential logic circuit. Combinational circuits are the ones which do not depend on previous inputs while Sequential circuits depend on past inputs.

3. In a combinational circuit, the output at any time depends only on the _____ at that time.
a) Voltage
b) Intermediate values
c) Input values
d) Clock pulses

Answer: c
Explanation: In a combinational circuit, the output at any time depends only on the input values at that time and not on past or intermediate values.

4. In a sequential circuit, the output at any time depends only on the input values at that time.
a) Past output values
b) Intermediate values
c) Both past output and present input
d) Present input values

Answer: c
Explanation: In a sequential circuit, the output at any time depends on the present input values as well as past output values. It also depends on clock pulses depending whether it's synchronous or asynchronous sequential circuits.

5. Procedure for the design of combinational circuits are:

A. From the word description of the problem, identify the inputs and outputs and draw a block diagram.

B. Draw the truth table such that it completely describes the operation of the circuit for different combinations

of inputs.

C. Simplify the switching expression(s) for the output(s).

D. Implement the simplified expression using logic gates.

E. Write down the switching expression(s) for the output(s).

a) B, C, D, E, A
b) A, D, E, B, C
c) A, B, E, C, D
d) B, A, E, C, D

Answer: c
Explanation: Combinational circuits are the ones which do not depend on previous inputs and depends only on the present values. The given arrangement in option c is the right sequence for the designing of the combinational circuits.

6. All logic operations can be obtained by means of _____
a) AND and NAND operations
b) OR and NOR operations
c) OR and NOT operations
d) NAND and NOR operations

Answer: d
Explanation: Since, the logic gates NOR and NAND are known as universal logic gates, therefore it can be used to design all the three basic gates AND, OR and NOT. Thus, it means that any operations can be obtained by implementation of these gates.

7. The design of an ALU is based on _____
a) Sequential logic
b) Combinational logic
c) Multiplexing
d) De-Multiplexing

Answer: b
Explanation: The design of an ALU is based on combinational logic. Because the unit has a regular pattern, it can be broken into identical stages connected in cascade through carries.

8. If the two numbers are unsigned, the bit conditions of interest are the _____ carry and a possible _____ result.
a) Input, zero
b) Output, one

c) Input, one
d) Output, zero

Answer: d
Explanation: If the two numbers are unsigned, the bit conditions of interest are the output carry and a possible zero result.

9. If the two numbers include a sign bit in the highest order position, the bit conditions of interest are the sign of the result, a zero indication and _____
a) An underflow condition
b) A neutral condition
c) An overflow condition
d) One indication

Answer: c
Explanation: If the two numbers include a sign bit in the highest order position, the bit conditions of interest are the sign of the result, a zero indication and an overflow condition.

10. The flag bits in an ALU is defined as _____
a) The total number of registers
b) The status bit conditions
c) The total number of control lines
d) All of the Mentioned

Answer: b
Explanation: In an ALU, status bit conditions are sometimes called condition code bits or flag bits. It is so called because they tend to represent the status of the respect flags after any operation.

K-Map Simplification

1. Which statement below best describes a Karnaugh map?
a) It is simply a rearranged truth table
b) The Karnaugh map eliminates the need for using NAND and NOR gates
c) Variable complements can be eliminated by using Karnaugh maps
d) A Karnaugh map can be used to replace Boolean rules

Answer: a
Explanation: K-map is simply a rearranged truth table. It is a pictorial representation of truth table having a specific number of cells or squares, where each cell represents a Maxterm or a Minterm.

2. Which of the examples below expresses the commutative law of multiplication?
a) A + B = B + A
b) A • B = B + A
c) A • (B • C) = (A • B) • C
d) A • B = B • A

Answer: d
Explanation: The commutative law of multiplication is (A * B) = (B * A).
The commutative law of addition is (A + B) = (B + A).

3. The Boolean expression Y = (AB)' is logically equivalent to what single gate?
a) NAND
b) NOR
c) AND
d) OR

Answer: a
Explanation: If A and B are the input for AND gate the output is obtained as AB and after inversion we get (AB)', which is the expression of NAND gate. NAND gate produces high output when any of the input is 0 and produces low output when all inputs are 1.

4. The observation that a bubbled input OR gate is interchangeable with a bubbled output AND gate is referred to as _____
a) A Karnaugh map
b) DeMorgan's second theorem
c) The commutative law of addition
d) The associative law of multiplication

Answer: b
Explanation: DeMorgan's Law: ~(P+Q) <=> (~P).(~Q) Also,
~(P.Q) <=> (~P)+(~Q).

5. The systematic reduction of logic circuits is accomplished by _____
a) Symbolic reduction

b) TTL logic
c) Using Boolean algebra
d) Using a truth table

Answer: c
Explanation: The systematic reduction of logic circuits is accomplished by using boolean algebra.

6. Each “1” entry in a K-map square represents _____
a) A HIGH for each input truth table condition that produces a HIGH output
b) A HIGH output on the truth table for all LOW input combinations
c) A LOW output for all possible HIGH input conditions
d) A DON’T CARE condition for all possible input truth table combinations

Answer: a
Explanation: Each “1” entry in a K-map square represents a HIGH for each input truth table condition that produces a HIGH output. Thus, it represents a minterm.

7. Each “0” entry in a K-map square represents _____
a) A HIGH for each input truth table condition that produces a HIGH output
b) A HIGH output on the truth table for all LOW input combinations
c) A LOW output for all possible HIGH input conditions
d) A DON’T CARE condition for all possible input truth table combinations

Answer: a
Explanation: Each “0” entry in a K-map square represents a LOW output for all possible HIGH input conditions. Thus, it represents Maxterm.

8. Which of the following statements accurately represents the two BEST methods of logic circuit simplification?
a) Actual circuit trial and error evaluation and waveform analysis
b) Karnaugh mapping and circuit waveform analysis
c) Boolean algebra and Karnaugh mapping
d) Boolean algebra and actual circuit trial and error evaluation

Answer: c
Explanation: The two BEST methods of logic circuit simplification are Boolean algebra and Karnaugh mapping. Boolean Algebra uses the Laws of Boolean Algebra for minimization of Boolean expressions while Karnaugh Map is a pictorial representation and reduction of the Boolean expression.

9. Looping on a K-map always results in the elimination of _____
a) Variables within the loop that appear only in their complemented form
b) Variables that remain unchanged within the loop
c) Variables within the loop that appear in both complemented and uncomplemented form
d) Variables within the loop that appear only in their uncomplemented form

Answer: c
Explanation: Looping on a K-map always results in the elimination of variables within the loop that appear in both complemented and uncomplemented form.

10. Which of the following expressions is in the sum-of-products form?
a) (A + B)(C + D)
b) (A * B)(C * D)
c) A* B *(CD)
d) A * B + C * D

Answer: d
Explanation: Sum of product means that it is the sum of all product terms. Thus, the number is multiplied first and then it is added: A * B + C * D.

11. Which of the following is an important feature of the sum-of-products form of expressions?
a) All logic circuits are reduced to nothing more than simple AND and OR operations
b) The delay times are greatly reduced over other forms
c) No signal must pass through more than two gates, not including inverters
d) The maximum number of gates that any signal must pass through is reduced by a factor of two

Answer: a
Explanation: An important feature of the sum-of-products form of expressions in the given option is that all logic circuits are reduced to nothing more than simple AND and OR operations. Sum Of Product means it is the sum of product terms containing variables in complemented as well as uncomplemented forms.

12. Which of the following expressions is in the product-of-sums form?
a) (A + B)(C + D)
b) (AB)(CD)
c) AB(CD)
d) AB + CD

Answer:
Explanation: (A + B)(C + D) represents the product-of-sums form.

CMOS

1. The full form of CMOS is _____
a) Capacitive metal oxide semiconductor
b) Capacitive metallic oxide semiconductor
c) Complementary metal oxide semiconductor
d) Complemented metal oxide semiconductor

Answer: c
Explanation: The full form of CMOS is complementary metal oxide semiconductor. In this type of device, both n-type and p-type transistors are used in a complementary way.

2. The full form of COS-MOS is _____
a) Complementary symmetry metal oxide semiconductor
b) Complementary systematic metal oxide semiconductor
c) Capacitive symmetry metal oxide semiconductor
d) Complemented systematic metal oxide semiconductor

Answer: a
Explanation: The full form of COS-MOS is complementary systematic metal oxide semiconductor. In this type of device, both n-type and p-type transistors are used in a complementary way. Usually, the transistors used are MOSFETs.

3. CMOS is also sometimes referred to as _____
a) Capacitive metal oxide semiconductor
b) Capacitive symmetry metal oxide semiconductor
c) Complementary symmetry metal oxide semiconductor
d) Complemented symmetry metal oxide semiconductor

Answer: c
Explanation: CMOS is also sometimes referred to as complementary systematic metal oxide–semiconductor (COS-MOS). In this type of device, both n-type and p-type transistors are used in a complementary way. Usually, the transistors used are MOSFETs.

4. CMOS technology is used in _____
a) Inverter
b) Microprocessor
c) Digital logic
d) Both microprocessor and digital logic

Answer: d
Explanation: CMOS technology is used in Microprocessor, Microcontroller, static RAM and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors (CMOS sensor), data converters and highly integrated transceivers for many types of communication.

5. Two important characteristics of CMOS devices are _____
a) High noise immunity
b) Low static power consumption
c) High resistivity
d) Both high noise immunity and low static power consumption

Answer: d
Explanation: Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Since one transistor of the pair is always off and the series combination draws significant power only momentarily during switching between on and off states. Also, the performance of CMOS is not altered with the presence of noise and thus it has high noise immunity.

6. CMOS behaves as a/an _____
a) Adder
b) Subtractor
c) Inverter
d) Comparator

Answer: c
Explanation: Since, the outputs of the PMOS and NMOS transistors are complementary such that when the input is low, the output is high and when the input is high, the output is low. Because of this behaviour of input and output, the CMOS circuit's output is the inverse of the input. Whereas, adders and subtractors are combinational circuits.

7. An important characteristic of a CMOS circuit is the _____
a) Noise immunity
b) Duality
c) Symmetricity
d) Noise Margin

Answer: b
Explanation: An important characteristic of a CMOS circuit is the duality that exists between its PMOS transistors and NMOS transistors. Due to the presence of two different types of transistors, the device has the complementary function.

8. CMOS logic dissipates _____ power than NMOS logic circuits.
a) More
b) Less
c) Equal
d) Very High

Answer: b
Explanation: CMOS logic dissipates less power than NMOS logic circuits because CMOS dissipates power only when switching ("dynamic power"). Thus, CMOS has less power consumption and is more efficient.

9. Semiconductors are made of _____
a) Ge and Si
b) Si and Pb
c) Ge and Pb
d) Pb and Au

Answer: a
Explanation: Semiconductors are made of Silicon (Si) and Germanium (Ge). Semiconductors are devices having conductivity between conductors and insulators.

10. Which chip were the first RTC and CMOS RAM chip to be used in early IBM computers, capable of storing a total of 64 bytes?
a) The Samsung 146818
b) The Samsung 146819
c) The Motorola 146818
d) The Motorola 146819

Answer: c
Explanation: The Motorola 146818 was the first RTC and CMOS RAM chip to be used in early IBM computers; capable of storing a total of 64 bytes.

MEMORY

Read Only Memory (ROM) – 1

1. Which of the following has the capability to store the information permanently?
a) RAM
b) ROM
c) Storage cells
d) Both RAM and ROM

Answer: b
Explanation: ROM (Read Only Memory) has the capability to store the information permanently. RAM provides random access to memory. Storage cells are responsible for the transfer of data from and into the memory.

2. ROM has the capability to perform _____
a) Write operation only
b) Read operation only
c) Both write and read operation
d) Erase operation

Answer: b
Explanation: ROM means “Read Only Memory”. Hence, it has the capability to perform read operation only. No write or erase operation could be performed in the ROM.

3. Since, ROM has the capability to read the information only then also it has been designed, why?
a) For controlling purpose
b) For loading purpose
c) For booting purpose
d) For erasing purpose

Answer: c
Explanation: ROM means “Read Only Memory”. Hence, it has capability to perform read operation only. No write or erase operation could be performed in the ROM. It has designed to provide the computer with resident programmes and for booting purpose.

4. The ROM is a _____
a) Sequential circuit
b) Combinational circuit
c) Magnetic circuit
d) Static circuit

Answer: b
Explanation: ROM is a combination of different ICs. So, it is a combinational circuit. It depends on present input and not past states.

5. ROM is made up of _____
a) NAND and OR gates
b) NOR and decoder
c) Decoder and OR gates
d) NAND and decoder

Answer: c
Explanation: ROM (Read Only Memory) has the capability to store the information permanently. ROM is made up of decoder and OR gates within a single IC package.

6. Why are ROMs called non-volatile memory?
a) They lose memory when power is removed
b) They do not lose memory when power is removed
c) They lose memory when power is supplied
d) They do not lose memory when power is supplied

Answer: b
Explanation: Volatile memory stores data as long as it is powered. ROMs are called non-volatile memory because of they do not lose memory when power is removed.

7. In ROM, each bit is a combination of the address variables is called _____
a) Memory unit
b) Storage class
c) Data word
d) Address

Answer: d
Explanation: In ROM, each bit combination that comes out of the output lines is called data word. Usually, a word consists of 16-bits or 2-bytes.

8. Which is not a removable drive?
a) Zip
b) Hard disk
c) Super Disk
d) Jaz

Answer: c
Explanation: Hard disk is present inside a computer. So, it is not a removable drive.

9. In ROM, each bit combination that comes out of the output lines is called _____
a) Memory unit
b) Storage class
c) Data word
d) Address

Answer: c
Explanation: In ROM, each bit combination that comes out of the output lines is called data word. Usually, a word consists of 16-bits or 2-bytes.

10. VLSI chip utilizes _____
a) NMOS
b) CMOS
c) BJT
d) All of the Mentioned

Answer: d
Explanation: Very Large Scale Integration (VLSI) (ranging from 10,000 to 100,000 gates per IC) is a memory chip which is made up of NMOS, CMOS, BJT, and BiCMOS.

Read Only Memory (ROM) – 2

1. The MOS technology based semiconductor ROMs are classified into _____ categories.
a) 2
b) 3
c) 4
d) 5

Answer: b
Explanation: The MOS technology based semiconductor ROMs are classified into three categories: Mask ROM, PROM,& EPROM. PROM stands for Programmable Read Only Memory in which the ROM can be externally programmed by the user. EPROM stands for Erasable Programmable Read Only Memory, where the ROM and be cleared and re-programmed.

2. MOS ROM is constructed using _____
a) FETs
b) Transistors
c) MOSFETs
d) BJTs

Answer: c
Explanation: MOS ROM is made up of MOSFETs. MOSFETs are Metal Oxide Semiconductor Field Effect Transistors.

3. The full form of EEPROM is _____
a) Erasable Electrically Programmable ROMs
b) Electrically Erasable Programmable ROMs
c) Electrically Erasable Programming ROMs
d) Electrically Erasable Programmed ROMs

Answer: b
Explanation: The full form of EEPROM is Electrically Erasable Programmable ROMs. In EPROM (Erasable Programmable ROMs), the ROM is cleared by exposing it to UV radiation and also it's a tedious process. Whereas, in EEPROM, the ROM can be cleared electrically and thus is less time consuming and more efficient.

4. Which of the following best describes EPROMs?
a) EPROMs can be programmed only once
b) EPROMs can be erased by UV
c) EPROMs can be erased by shorting all inputs to the ground
d) EPROMs can be erased electrically

Answer: b
Explanation: EPROM (Erasable Programmable ROMs), the ROM is cleared by exposing it to UV radiation and also it's a tedious process. Whereas, in EEPROM, the ROM can be cleared electrically and thus is less time consuming and more efficient.

5. The Width of a processor's data path is measured in bits. Which of the following are common data paths?
a) 8 bits
b) 12 bits
c) 16 bits
d) 32 bits

Answer: a
Explanation: In generalised form, the data paths are of 8 bits. The data path, also known as data bus, is the channel through which the processor sends and receives data.

6. What type of memory is not directly addressable by the CPU and requires special software called EMS (expanded memory specification)?
a) Extended
b) Expanded
c) Base
d) Conventional

Answer: b
Explanation: Expanded memory is not directly addressable by the CPU. Expanded memory is the additional memory which is incorporated beyond the parent memory limit of the processor.

7. Which bus is used for input and output in case of microprocessor operation?
a) Address bus
b) System bus
c) Control bus
d) Data bus

Answer: c
Explanation: The input and output are used to control the function of a microprocessor. Hence, the control bus is used to transfer the input and output signal from microprocessor to external peripherals and or from external peripherals to microprocessor.

8. What is the major difference between DRAM and SRAM?
a) Dynamic RAMs are always active; static RAMs must reset between data read/write cycles
b) SRAMs can hold data via a static charge, even with power off
c) The only difference is the terminal from which the data is removed—from the FET Drain or Source
d) DRAMs must be periodically refreshed

Answer: d
Explanation: DRAMs must be periodically refreshed so that it can store the new information. DRAMs are slower compared to SRAMs as the access time for SRAM is less than that of DRAM.

9. Which of the following is not a part of Hard disk?
a) Platter
b) Read/Write

c) Valve
d) Spindle

Answer: c
Explanation: A valve is a device that regulates, directs or controls the flow of a fluid (gases, liquids, fluidized solids, or slurries) by opening, closing, or partially obstructing various passageways. So, it is not a part of hard disk.

10. Which ROM can be erased by an electrical signal?
a) ROM
b) Mask ROM
c) EPROM
d) EEPROM

Answer: d
Explanation: In EPROM (Erasable Programmable ROMs), the ROM is cleared by exposing it to UV radiation and also it's a tedious process. Whereas, in EEPROM, the ROM can be cleared electrically and thus is less time consuming and more efficient.

11. In the floppy drive, data is written to and read from the disk via a magnetic _____ head mechanism.
a) Cluster
b) Read/Write
c) Cylinder
d) Recordable

Answer: b
Explanation: A floppy disk is a removable disk used for storing data via magnetic facilities. In the floppy drive, data is written to and read from the disk via a magnetic read/write head mechanism.

12. What does the term "random access" mean in terms of memory?
a) Any address can be accessed in systematic order
b) Any address can be accessed in any order
c) Addresses must be accessed in a specific order
d) Any address can be accessed in reverse order

Answer: b
Explanation: "Random access" mean which can be accessed randomly and in other words any address can be accessed in any order.

13. Which type of ROM has to be custom built by the factory?
a) EEPROM
b) Mask ROM
c) EPROM
d) PROM

Answer: b
Explanation: All types of ROM are programmable and can be programmed as per requirement but the mask ROM is always programmed for specific application and it can't be reprogrammed. PROM stands for Programmable Read Only Memory in which the ROM can be externally programmed by the user. EPROM stands for Erasable Programmable Read Only Memory, where the ROM and be cleared and re-programmed.

14. The computer's main memory is _____
a) Hard drive and RAM
b) CD-ROM and hard drive
c) RAM and ROM
d) CMOS and hard drive

Answer: c
Explanation: The computer's main memory is RAM and ROM because all the storage related operation are performed by the data present in RAM/ROM. RAM stands for Random Access Memory where any address can accessed in any order. ROM stands for Read Only Memory wherefrom data can only be read.

15. A major disadvantage of the mask ROM is that _____
a) It is time consuming to change the stored data when system requirements change
b) It is very expensive to change the stored data when system requirements change
c) It cannot be reprogrammed if stored data needs to be changed
d) It has an extremely short life expectancy and requires frequent replacement

Answer: c
Explanation: A major disadvantage of the mask ROM is that it cannot be reprogrammed if stored data needs to be changed. PROM stands for Programmable Read Only Memory in which the ROM can be externally programmed by the user. EPROM stands for Erasable Programmable Read Only Memory, where the ROM and be cleared and re-programmed.

Read Only Memory (ROM) – 3

1. ROM may be programmed in _____ ways.
a) 2
b) 3
c) 4
d) 5

Answer: a
Explanation: ROM may be programmed in two different ways: (i) Mask Programming & (ii) PROM. Mask Programming is done by the manufacture. Whereas, PROM(Programmable ROM) is programmed by the user.

2. Which programming is done during the manufacturing process?
a) Mask Programming
b) PROM
c) Both PROM and mask programming
d) EPROM

Answer: a
Explanation: Mask ROM is permanently programmed during the manufacturing process. Whereas, PROM(Programmable ROM) is programmed by the user.

3. A photographic negative is called a _____
a) Photo
b) Negative
c) Mask
d) Virtual image

Answer: c
Explanation: A photographic negative is called a mask is used to control the electrical connections on the chip.

4. Mask programming is also known as _____
a) EPROM
b) PROM
c) Custom programming
d) Both PROM and EPROM

Answer: c
Explanation: Mask programming is also known as custom programming. Mask ROM is permanently programmed during the manufacturing process. Whereas, PROM(Programmable ROM) is programmed by the user.

5. The total storage capacity of 16 * 8 ROM is _____
a) 8 bits
b) 16 bits

c) 128 bits
d) 64 bits

Answer: c
Explanation: ROM stands for Read Only Memory in which data is stored permanently and wherefrom data can only be read and rarely modified. The total storage capacity of 16 * 8 ROM is 128 bits (i.e. 16 * 8 = 128).

6. Which IC is a typical MSI/TTL based?
a) IC 74187
b) IC 74189
c) IC 74188
d) IC 74186

Answer: a
Explanation: MSI/TTL stands for Medium Scale Integration of Transistor-Transistor Logic. IC 74187 is a typical MSI/TTL based.

7. IC 74187 is of _____
a) 512 bits
b) 1024 bits
c) 256 bits
d) 68 bits

Answer: b
Explanation: IC 74187 is of 1024 bits because it is organised as 256 * 4. Thus, it has 256 rows and 4 columns.

8. How many rows and columns are present in IC 74187?
a) 128, 3
b) 128, 4
c) 256, 3
d) 256, 4

Answer: d
Explanation: IC 74187 is organised as 256 * 4, hence it has 256 rows and 4 columns.
IC 74187 is of 1024 bits because it is organized as 256 * 4.

9. Which of the following IC is of 256 bit?
a) IC 74187
b) IC 74189
c) IC 74188
d) IC 74186

Answer: c
Explanation: IC 74188 is of 256 bits. Since, it is organised as 32 * 8 = 256. Thus, it has 32 rows and 8 columns.

10. Which IC is known as bipolar ROM?
a) IC 74187
b) IC 74189
c) IC 74188
d) IC 74186

Answer: c
Explanation: IC 74188 is known as bipolar ROM since it is made up of TTL logic.

11. How many address location a bipolar ROM has?
a) 16
b) 32
c) 64
d) 8

Answer: b
Explanation: Bipolar ROM means IC 74188 and it is organized as 32 * 8. Thus, it has 32 rows and 8 columns. So, it has 32 address locations and each of which has 8 bits of storage.

12. Which of the following is known as MOS static ROM?
a) TMS 45276
b) TMS 45278
c) TMS 45279
d) TMS 45275

Answer: a
Explanation: TMS 45276 is known as MOS static ROM and it is made up of MOSFETs.

13. TMS 45276 is of _____
a) 32 KB
b) 56 KB
c) 8 bits
d) 4 bytes

Answer: a
Explanation: TMS 45276 is known as MOS static ROM and it is made up of MOSFETs. In ROM, the data remains even when the power is switched off. TMS 45276 is of 32 KB.

14. Which of the following has the capability to store the highest bits of data?
a) TMS 45276
b) IC 74188
c) IC 74187
d) IC 74185

Answer: a
Explanation: TMS 45276 has the capability to store the highest bits of data because of 32768 * 8 = 12,62,144 organization.

15. What does CS mean in a chip?
a) Storing Capacity
b) Custom Select
c) Chip Select
d) Custom Storage

Answer: c
Explanation: CS means chip select and with the help of CS a chip is activated/deactivated. It is used for enabling or disabling the function of the chip.

16. ROMs are used to _____
a) Store bootstrap program
b) Character generation
c) Code conversion
d) All of the Mentioned

Answer: d
Explanation: ROM stands for Read Only Memory in which data is permanently stored, even when the power is turned off. It is used to store bootstrap program, character generation and code conversion.

Programmable Logic Array

1. What is memory decoding?
a) The process of Memory IC used in a digital system is overloaded with data
b) The process of Memory IC used in a digital system is selected for the range of address assigned
c) The process of Memory IC used in a digital system is selected for the range of data assigned
d) The process of Memory IC used in a digital system is overloaded with data allocated in memory cell

Answer: b
Explanation: The Memory IC used in a digital system is selected or enabled only for the range of addresses assigned to it and this process is called memory decoding. It decodes the memory to be selected for a specific address.

2. The first step in the design of memory decoder is _____
a) Selection of a EPROM
b) Selection of a RAM
c) Address assignment
d) Data insertion

Answer: c
Explanation: Memory decoder decodes the memory to be selected for a specific address. The first step in the design of memory decoder is address assignment in non-overlapped manner.

3. How many address bits are required to select memory location in the Memory decoder?
a) 4 KB
b) 8 KB
c) 12 KB
d) 16 KB

Answer: c
Explanation: Memory decoder decodes the memory to be selected for a specific address. Since the given EPROM and RAM are of 4 KB (4 * 1024 = 4096) capacity, it requires 12 address bit to select one of the 4096 memory locations.

4. How memory expansion is done?
a) By increasing the supply voltage of the Memory ICs
b) By decreasing the supply voltage of the Memory ICs
c) By connecting Memory ICs together
d) By separating Memory ICs

Answer: c
Explanation: Memory ICs can be connected together to expand the number of memory words or the number of bits per word.

5. IC 4116 is organised as _____
a) 512 * 4
b) 16 * 1
c) 32 * 4
d) 64 * 2

Answer: c
Explanation: IC 4116 is organised as 16 * 1 K which has capability to store 16 KB.

6. To construct 16K * 4-bit memory, how many 4116 ICs are required?
a) 1
b) 2
c) 3
d) 4

Answer: d
Explanation: Since, IC 4116 is organised as 16K * 1, which can store about 16KB data. So, four ICs are required for 16K * 4 memory implementation.

7. How many 1024 * 1 RAM chips are required to construct a 1024 * 8 memory system?
a) 4
b) 6
c) 8
d) 12

Answer: c
Explanation: One 1024 * 1 RAM chips is of 1-bit. SO, for construction of 1024 * 8 RAM chip of 8-bits, it will require 8 chips.

8. How many 16K * 4 RAMs are required to achieve a memory with a capacity of 64K and a word length of 8 bits?
a) 2
b) 4
c) 6
d) 8

Answer: d
Explanation: 16K * 4 = 64K RAM is of 64K. Therefore, for a word of length 8-bits,
64 * 8 = 512K RAM required. Thus, number of 16K * 4 RAMs = 512/64 = 8.

9. The full form of PLD is _____
a) Programmable Load Devices
b) Programmable Logic Data
c) Programmable Logic Devices
d) Programmable Loaded Devices

Answer: c
Explanation: The full form of PLD is Programmable Logic Devices. It is a collection of gates, flip-flops and registers on a single chip.

10. PLD contains a large number of _____
a) Flip-flops
b) Gates
c) Registers
d) All of the Mentioned

Answer: d
Explanation: Programmable Logic Devices is a collection of a large number of gates, flip-flops, registers that are interconnected on the chip. Thus, it is used for designing logic circuits.

11. Logic circuits can also be designed using _____
a) RAM
b) ROM
c) PLD
d) PLA

Answer: c
Explanation: Programmable Logic Devices is a collection of large number of gates, flip-flops, registers that are interconnected on the chip. Thus, it is used for designing logic circuits.

12. In PLD, there are provisions to perform interconnections of the gates internally, because of _____
a) High reliability
b) High conductivity
c) The desired logic implementation
d) The desired output

Answer: c
Explanation: Programmable Logic Devices is a collection of a large number of gates, flip-flops, registers that are interconnected on the chip. In PLD, there are provisions to perform interconnections of the gates internally so that the desired logic can be implemented.

13. Why antifuses are implemented in a PLD?
a) To protect from high voltage
b) To increase the memory
c) To implement the programmes
d) As a switching devices

Answer: c
Explanation: Programmable Logic Devices is a collection of a large number of gates, flip-flops, registers that are interconnected on the chip. Programming is accomplished by using antifuses in a PLD and it is fabricated at the cross points of the gates.

14. How many types of PLD is?
a) 2
b) 3
c) 4
d) 5

Answer: a
Explanation: There are two types of PLD, viz., devices with fixed architecture and devices with a flexible architecture. The main categories of PLDs are PROM, PAL and PLA.

15. PLA refers to _____
a) Programmable Loaded Array
b) Programmable Array Logic
c) Programmable Logic Array
d) Programmed Array Logic

Answer: c
Explanation: PLA refers to Programmable Logic Array. It is a type of PLD having programmable AND and OR gates.

Programmable Array Logic

1. The inputs in the PLD is given through _____
a) NAND gates
b) OR gates
c) NOR gates
d) AND gates

Answer: d
Explanation: The inputs in the PLD is given through AND gate followed by inverting & non-inverting buffer. PLDs are Programmable Logic Devices consisting of logic gates, flip-flops and registers connected together on a single chip. Thus, it can be categorised into PROM, PAL and PLA.

2. PAL refers to _____
a) Programmable Array Loaded
b) Programmable Logic Array
c) Programmable Array Logic
d) Programmable AND Logic

Answer: c
Explanation: PAL refers to Programmable Array Logic consisting of programmable AND gates and fixed OR gates.

3. Outputs of the AND gate in PLD is known as _____
a) Input lines
b) Output lines
c) Strobe lines
d) Control lines

Answer: b
Explanation: Outputs of the AND gate in PLD is known as output lines.

4. PLA contains _____
a) AND and OR arrays
b) NAND and OR arrays
c) NOT and AND arrays
d) NOR and OR arrays

Answer: a
Explanation: Programmable Logic Array is a type of fixed architecture logic devices with programmable AND gates followed by programmable OR gates. It is a kind of PLD.

5. PLA is used to implement _____
a) A complex sequential circuit
b) A simple sequential circuit

c) A complex combinational circuit
d) A simple combinational circuit

Answer: c
Explanation: Since, PLA is a combination of programmable AND and OR gates. So, it is used to implement complex combinational circuit.

6. A PLA is similar to a ROM in concept except that _____
a) It hasn't capability to read only
b) It hasn't capability to read or write operation
c) It doesn't provide full decoding to the variables
d) It hasn't capability to write only

Answer: c
Explanation: A PLA is similar to a ROM in concept except that it doesn't provide full decoding to the variables and doesn't generate all the minterms as in the ROM. Programmable Logic Array is a type of fixed architecture logic devices with programmable AND gates followed by programmable OR gates. It is a kind of PLD.

7. For programmable logic functions, which type of PLD should be used?
a) PLA
b) PAL
c) CPLD
d) SLD

Answer: b
Explanation: Since PAL consists of programmable AND gates and fixed OR gates and also circuitry working is less.

8. The complex programmable logic device contains several PLD blocks and _____
a) A language compiler
b) AND/OR arrays
c) Global interconnection matrix
d) Field-programmable switches

Answer: c
Explanation: The complex programmable logic device contains several PLD blocks and a global interconnection matrix by which it communicates through several devices. It is also known as Field-Programmable Gate Arrays (FPGAs).

9. Which type of device FPGA are?
a) SLD
b) SROM
c) EPROM
d) PLD

Answer: d
Explanation: Field-Programmable Gate Arrays (FPGAs) are reprogrammable silicon chips. In

contrast to processors that you find in your PC, programming an FPGA rewires the chip itself to implement your functionality rather than run a software application. Thus, FPGAs are PLD devices.

10. The difference between a PAL & a PLA is _____
a) PALs and PLAs are the same thing
b) The PLA has a programmable OR plane and a programmable AND plane, while the PAL only has a programmable AND plane
c) The PAL has a programmable OR plane and a programmable AND plane, while the PLA only has a programmable AND plane
d) The PAL has more possible product terms than the PLA

Answer: b
Explanation: The main difference between a PAL & PLA is that PLA has a programmable OR plane and a programmable AND plane, while the PAL only has a programmable AND plane and a fixed OR plane.

11. If a PAL has been programmed once _____
a) Its logic capacity is lost
b) Its outputs are only active HIGH
c) Its outputs are only active LOW
d) It cannot be reprogrammed

Answer: d
Explanation: PAL only has a programmable AND plane and a fixed OR plane. Since, PAL is dynamic in nature. So, it can't be reprogrammed.

12. The FPGA refers to _____
a) First programmable Gate Array
b) Field Programmable Gate Array
c) First Program Gate Array
d) Field Program Gate Array

Answer: b
Explanation: The FPGA refers to Field Programmable Gate Array. Field-Programmable Gate Arrays (FPGAs) are reprogrammable silicon chips. In contrast to processors that you find in your PC, programming an FPGA rewires the chip itself to implement your functionality rather than run a software application. Thus, FPGAs are PLD devices.

13. The full form of VLSI is _____
a) Very Long Single Integration
b) Very Least Scale Integration
c) Very Large Scale Integration
d) Very Long Scale Integration

Answer: c
Explanation: The full form of VLSI is Very Large Scale Integration in which FPGA is implemented.

14. In FPGA, vertical and horizontal directions are separated by _____
a) A line
b) A channel
c) A strobe
d) A flip-flop

Answer: b
Explanation: The FPGA refers to Field Programmable Gate Array. Field-Programmable Gate Arrays (FPGAs) are reprogrammable silicon chips. Vertical and horizontal directions is separated by a channel in an FPGA which determines the location of the output.

15. Applications of PLAs are _____
a) Registered PALs
b) Configurable PALs
c) PAL programming
d) All of the Mentioned

Answer: d
Explanation: Applications of PLAs are Registered PALs, Configurable PALs, and PAL programming and these are performed by using an extra flip-flop with PAL.