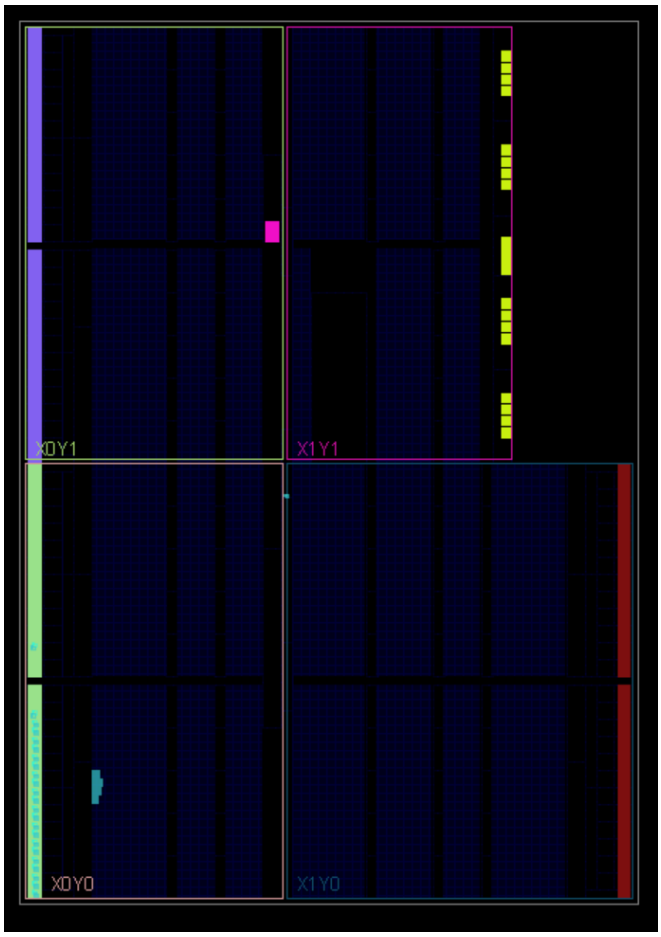
Synthesized and Implemented Design:



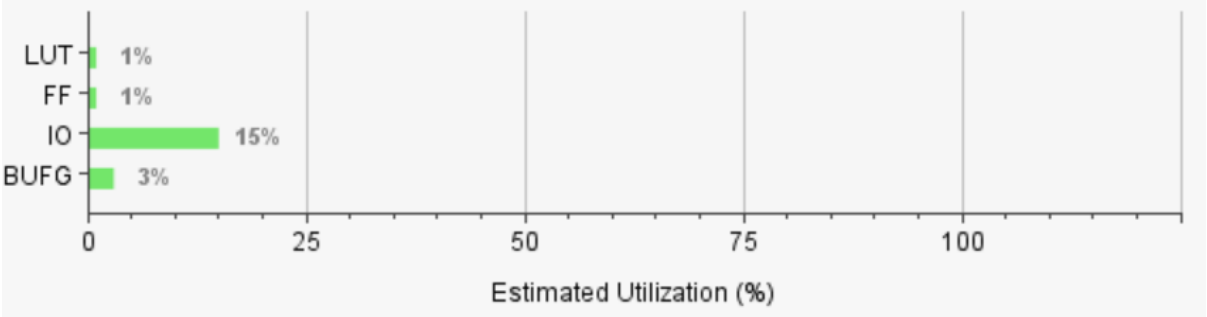
Reports:

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	22	0	8000	0.28
LUT as Logic	22	0	8000	0.28
LUT as Memory	0	0	5000	0.00
Slice Registers	20	0	16000	0.13
Register as Flip Flop	20	0	16000	0.13
Register as Latch	0	0	16000	0.00
F7 Muxes	0	0	7300	0.00
F8 Muxes	0	0	3650	0.00

Ref Name	Used	Functional Category
OBUF	21	IO
FDRE	20	Flop & Latch
LUT6	12	LUT
LUT4	5	LUT
LUT5	4	LUT
LUT3	3	LUT
IBUF	2	IO
LUT2	1	LUT
LUT1	1	LUT
BUFG	1	Clock

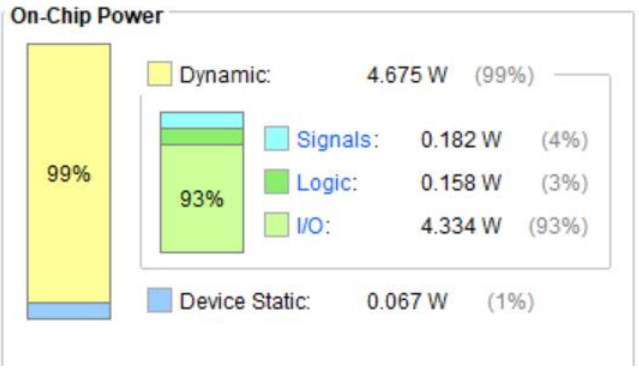
Name	Power (W)
cpu4	4.675
pc_counter	0.299
regs	0.031

Resource	Utilization	Available	Utilization %
LUT	22	8000	0.28
FF	20	16000	0.13
IO	23	150	15.33
BUFG	1	32	3.13



Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**4.741 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**50.0°C**
Thermal Margin:	50.0°C (9.5 W)
Effective ϑJA:	5.3°C/W



On-Chip	Power (W)	Used	Available	Utilization (%)
Slice Logic	0.158	47	---	---
LUT as Logic	0.149	22	8000	0.28
BUFG	0.005	1	32	3.13
Register	0.004	20	16000	0.13
Signals	0.182	46	---	---
I/O	4.334	23	150	15.33
Static Power	0.067			
Total	4.741			