Date: 23-04-2025

DIGITAL LOCK SYSTEM

(i) OBJECTIVE

To design, implement, and simulate a Digital Lock System using Verilog HDL.

(ii) INTRODUCTION

A digital lock system offers an electronic solution for access control, replacing traditional mechanical locks. This design is implemented using a finite state machine (FSM) model that processes a predefined key sequence serially. Only the correct sequence triggers the 'unlock' signal. This approach offers reliability, reprogrammability, and ease of integration into larger systems like smart homes or secured labs.

(iii) SOFTWARE

Tool Name: Synopsys
Components Used:

- Verdi: For waveform analysis and debugging
- Design Compiler: For synthesis and gate-level analysis (if needed)
- ICC: Floor Planning, Power Planning, Placement Planning, Clock-Tree Synthesis and Routing.

(iv) DESCRIPTION

The Digital Lock System is built around a finite state machine that detects a 4-bit key sequence: 1011. The lock starts in a reset state and transitions between states on every clock cycle based on the key input. If the exact sequence is entered, it activates the unlocked output.

Functional Details:

- States: S0 to S4, representing progression in key detection.
- Reset: Brings the FSM to initial state (S0).
- Key Input: 1-bit serial input representing each bit of the key.
- Unlocked Output: Goes high for one cycle when the key 1011 is correctly entered.

(v) DESIGN

The system is designed as a Moore FSM, where the output (unlocked) is determined by the state. The correct input sequence (1011) transitions the FSM through S0 → S1 → S2 → S3 → S4, with S4 being the unlock state.

VERILOG CODE:

```
module digital_lock (

    input wire clk,
    input wire rst, // Active high reset
    input wire key_in, // Serial key input (1 bit at a time)
    output reg unlocked
);

    // State encoding
    parameter S0 = 3'b000,
              S1 = 3'b001,
              S2 = 3'b010,
              S3 = 3'b011,
              S4 = 3'b100;

    reg [2:0] current_state, next_state;

    // Sequential logic: state update
    always @(posedge clk or posedge rst) begin
        if (rst)
            current_state <= S0;
        else
            current_state <= next_state;
    end

    // Combinational logic: next state logic
    always @(*) begin
        case (current_state)
            S0: next_state = (key_in == 1) ? S1 : S0;
            S1: next_state = (key_in == 0) ? S2 : S0;
            S2: next_state = (key_in == 1) ? S3 : S0;
            S3: next_state = (key_in == 1) ? S4 : S0;
            S4: next_state = S0; // Auto-reset after unlocking
            default: next_state = S0;
        endcase
    end
```

```
    // Output logic
    always @(posedge clk or posedge rst) begin
        if (rst)
            unlocked <= 1'b0;
        else if (current_state == S4)
            unlocked <= 1'b1;
        else
            unlocked <= 1'b0;
    end
endmodule
```

TESTBENCH:

```
`timescale 1ns/1ns
`include "digital_lock.v" // Includes the module definition for the digital lock

module testbench;
    reg Clock, Reset, Key_in;
    wire Unlocked;

    // Instantiate the module under test
    digital_lock dut (.clk(Clock), .rst(Reset), .key_in(Key_in), .unlocked(Unlocked));

    // Clock generation: 10ns period
    always #5 Clock = ~Clock;

    // Stimulus
    initial begin
        $fsdbDumpvars(); // Tool-specific command for waveform generation

        // Initialize inputs
        Clock <= 0; Reset <= 1; Key_in <= 0;
        #10 Reset <= 0;

        // Apply test cases
        // Test correct sequence: 1011
        #10 Key_in <= 1;
        #10 Key_in <= 0;
        #10 Key_in <= 1;
        #10 Key_in <= 1;
        #10 $display("Key_in = %b, Unlocked = %b", Key_in, Unlocked);

        // Wait and reset system
        #20 Reset <= 1; #10 Reset <= 0;
```

```
        // Incorrect sequence: 1101
        #10 Key_in <= 1;
        #10 Key_in <= 1;
        #10 Key_in <= 0;
        #10 Key_in <= 1;
        #10 $display("Key_in = %b, Unlocked = %b", Key_in, Unlocked);

        #100 $finish;
    end
endmodule
```

(vi) CIRCUIT DIAGRAM

The FSM diagram showing transitions for key sequence 1011.

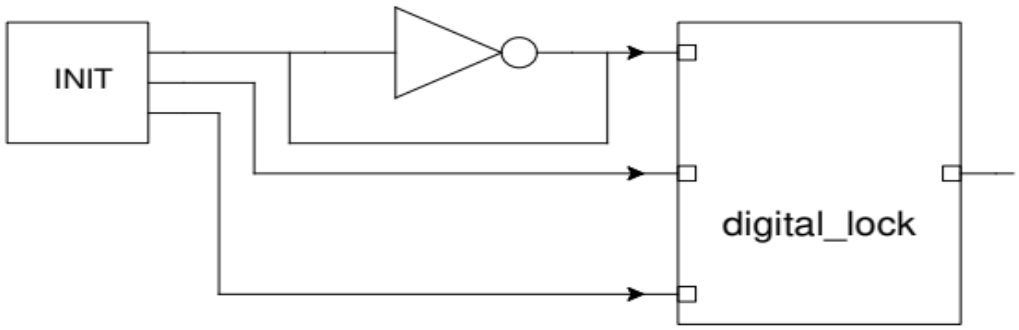


Fig-1 FSM Diagram

- States: Represented as nodes (S0-S4)
- Transitions: Labeled by key_in values (0 or 1)
- Reset: Directs all states back to S0
- Unlock State: Highlight S4 with an unlocked = 1 label

(vii) SIMULATION RESULTS

Using Synopsys VCS:

The simulation included two test sequences:

- Correct input: 1011 → Output: unlocked = 1
- Incorrect input: 1101 → Output: unlocked = 0

(i) Output: Key_in = 1, Unlocked = 1 (for correct sequence)

(ii) Output: Key_in = 1, Unlocked = 0 (for incorrect sequence)

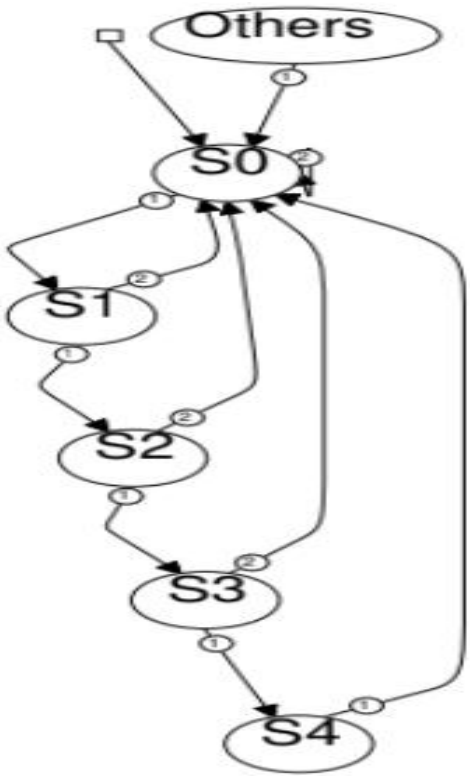


Fig-2 State Diagram

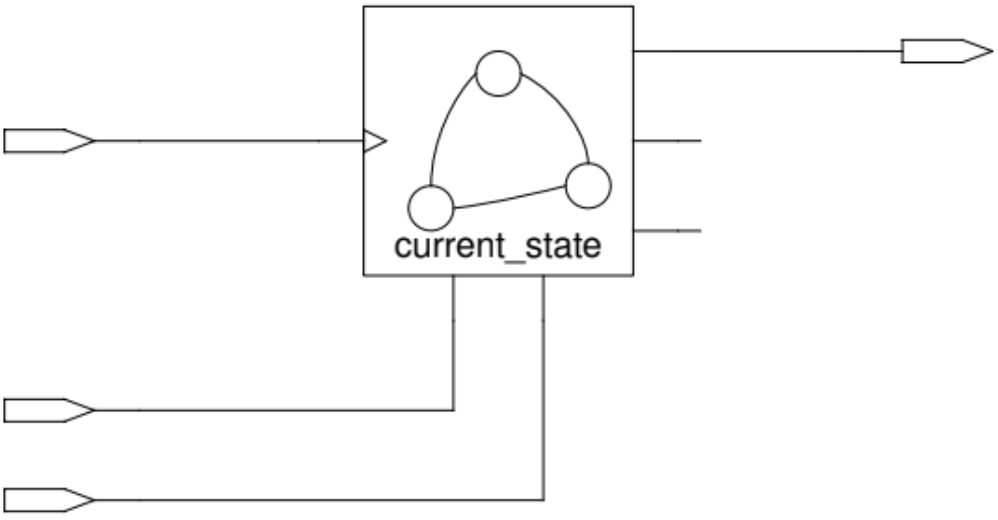


Fig-3 Current State Diagram

Waveform Analysis (Verdi):

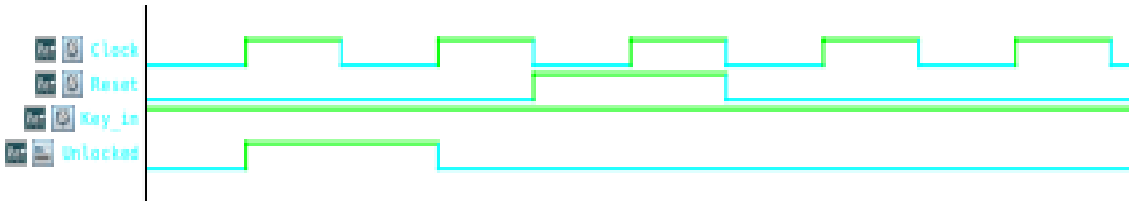


Fig-4 Waveform

- Shows clock, reset, key_in transitions and the corresponding unlocked signal.
- FSM states verified through state transitions on signal inspection.

Design Compiler (DC) Analysis:

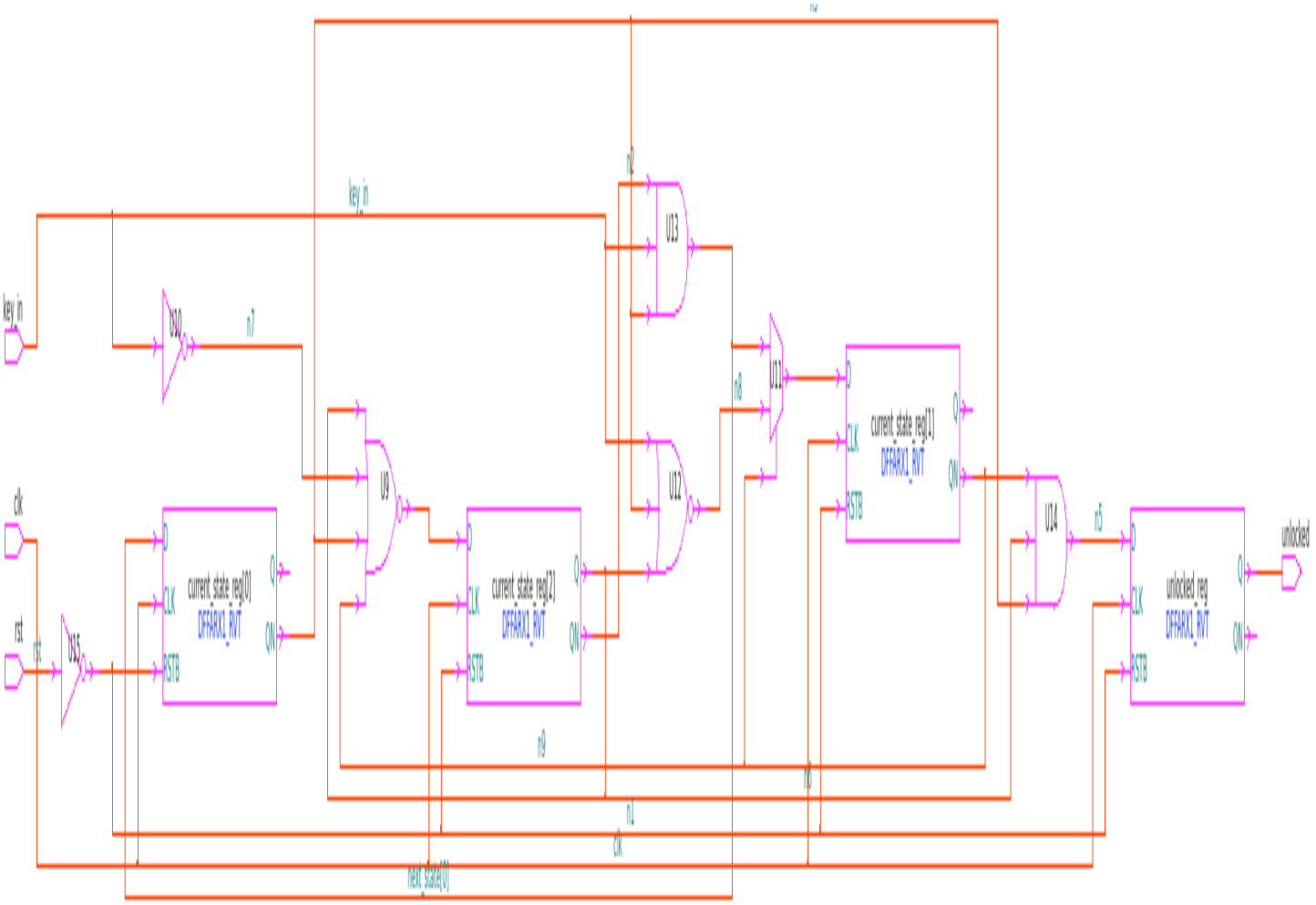


Fig-5 Schematic Diagram

Fig-6 Schematic Diagram

Cell Report:

```
Report : cell
Design : digital_lock
Version: W-2024.09
Date   : Fri Apr 11 14:07:50 2025
****************************************

Attributes:
    b - black box (unknown)
    h - hierarchical
    n - noncombinational
    r - removable
    u - contains unmapped logic

Cell                      Reference       Library              Area  Attributes
-------------------------------------------------------------------------------
U9                        NOR4X0_RVT      saed32rvt_tt0p78vn40c
                                                             3.049728
U10                       INVX0_RVT       saed32rvt_tt0p78vn40c
                                                             1.270720
U11                       MUX21X1_RVT     saed32rvt_tt0p78vn40c
                                                             3.303872
U12                       NOR3X0_RVT      saed32rvt_tt0p78vn40c
                                                             2.795584
U13                       AND3X1_RVT      saed32rvt_tt0p78vn40c
                                                             2.287296
U14                       AND3X1_RVT      saed32rvt_tt0p78vn40c
                                                             2.287296
U15                       INVX0_RVT       saed32rvt_tt0p78vn40c
                                                             1.270720
current_state_reg[0]      DFFARX1_RVT     saed32rvt_tt0p78vn40c
                                                             7.116032  n
current_state_reg[1]      DFFARX1_RVT     saed32rvt_tt0p78vn40c
                                                             7.116032  n
current_state_reg[2]      DFFARX1_RVT     saed32rvt_tt0p78vn40c
                                                             7.116032  n
unlocked_reg              DFFARX1_RVT     saed32rvt_tt0p78vn40c
                                                             7.116032  n
-------------------------------------------------------------------------------
Total 11 cells                                               44.729345
1
```

Timing Report:

```
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : digital_lock
Version: W-2024.09
Date   : Fri Apr 11 14:07:58 2025
****************************************

Operating Conditions: tt0p78vn40c   Library: saed32rvt_tt0p78vn40c
Wire Load Model Mode: enclosed

  Startpoint: unlocked_reg
              (rising edge-triggered flip-flop)
  Endpoint: unlocked (output port)
  Path Group: (none)
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  digital_lock       ForQA                 saed32rvt_tt0p78vn40c

  Point                                    Incr       Path
  -----------------------------------------------------------
  unlocked_reg/CLK (DFFARX1_RVT)           0.00       0.00 r
  unlocked_reg/Q (DFFARX1_RVT)             0.22       0.22 r
  unlocked (out)                           0.00       0.22 r
  data arrival time                                   0.22
  -----------------------------------------------------------
  (Path is unconstrained)


1
```

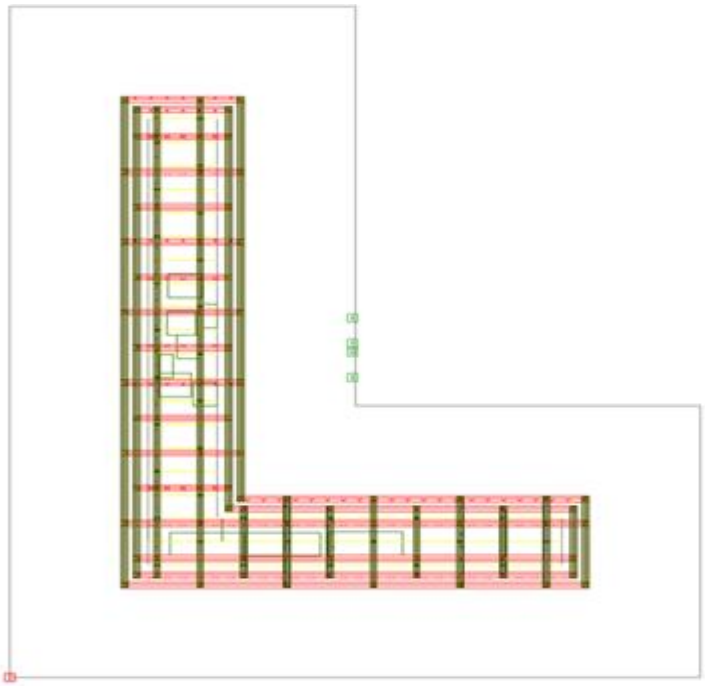
(viii) PERFORMANCE PARAMETERS

Parameter	Value / Observation
Max Frequency	Depends on synthesis result in DC
Area Utilization	Minimal (uses a 3-bit state register only)
Power	Very Low (synchronous, idle when locked)
Timing	Unlock signal is asserted for 1 clock cycle after correct sequence

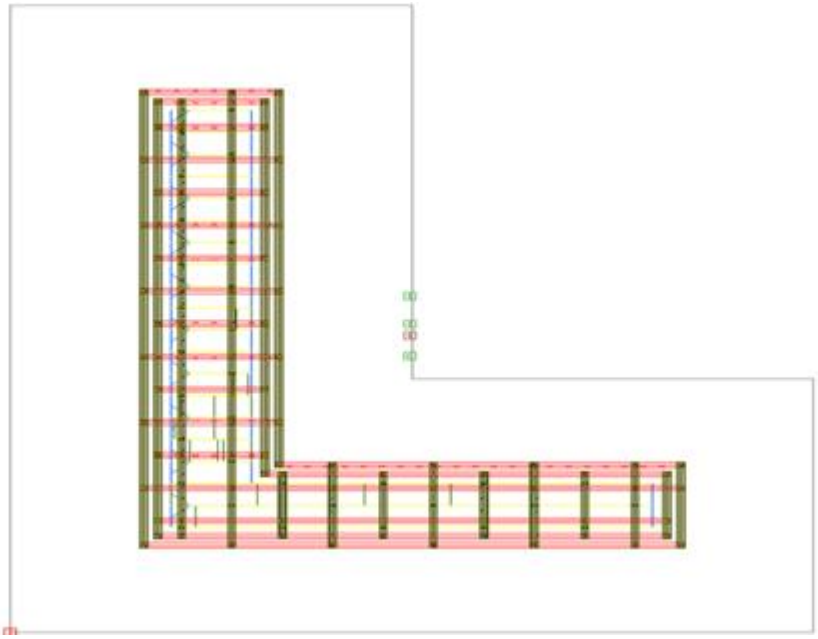
IC Compiler Analysis:

Floor Planning:

Power Planning:



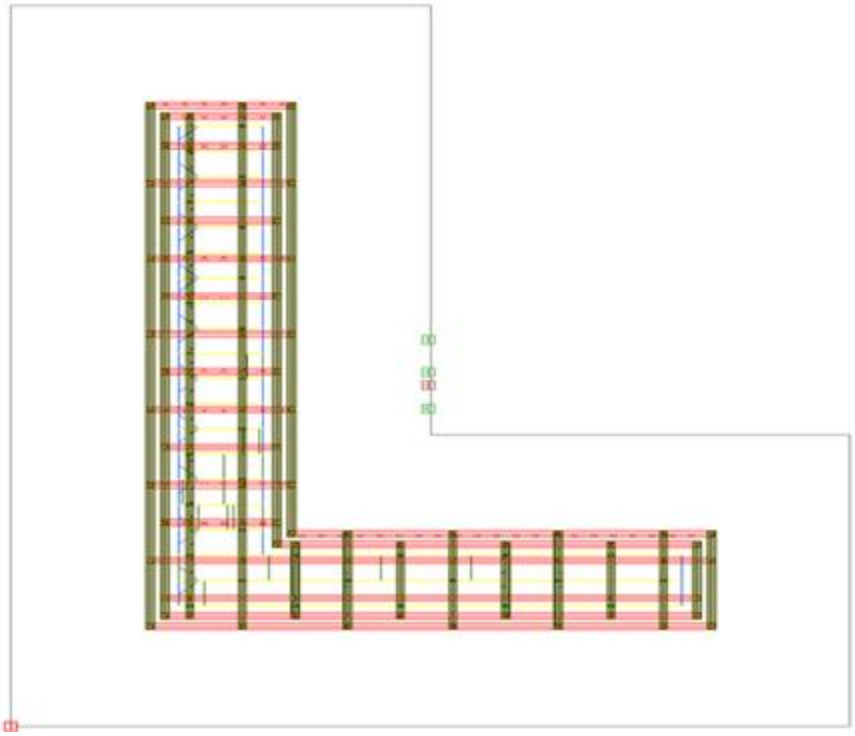
Placement Planning:



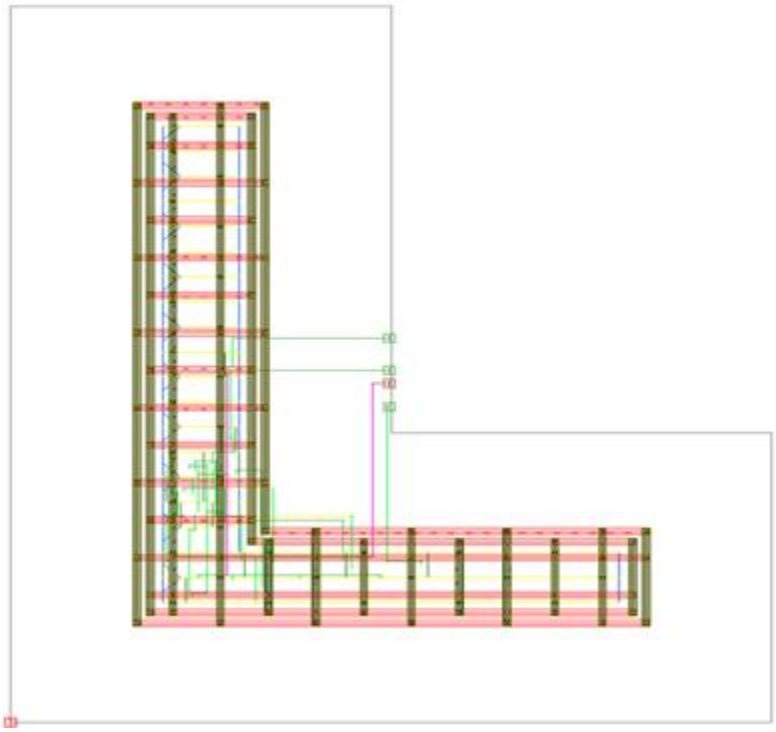
Placement Report:

```
****************************************
Report : report_placement
Design : digital_lock
Version: W-2024.09
Date   : Tue Apr 15 13:47:02 2025
****************************************
  ==================
  Note: Including violations of fixed cells or between fixed pairs of cells.
        To ignore violations of / between fixed cells, enable -ignore_fixed.
  ==================

  Wire length report (all)
  ==================
  wire length in design full_adder: 170.050 microns.
  wire length in design full_adder (see through blk pins): 170.050 microns.

  Physical hierarchy violations report
  ====================================
  Violations in design full_adder:
     0 cells have placement violation.

  Voltage area violations report
  ====================================
  Voltage area placement violations in design full_adder:
     0 cells placed outside the voltage area which they belong to.

Information: Default error view full_adder_dpplace.err is created in GUI error browser. (DPP-054)
1
```

Clock-Tree Synthesis:



Routing:



Track Report:

```
****************************************
Report : report_tracks
Design : digital_lock
Version: W-2024.09
Date   : Tue Apr 15 13:55:52 2025
****************************************
```

Layer	Direction	Start	Tracks	Pitch	Attr
M1	X	0.096	131	0.152	default
M1	X	0.096	262	0.152	default
M1	Y	19.400	187	0.152	default
M1	Y	0.096	127	0.152	default
M2	X	0.096	131	0.152	default
M2	X	0.096	262	0.152	default
M2	Y	19.400	187	0.152	default
M2	Y	0.096	127	0.152	default
M3	X	0.096	66	0.304	default
M3	X	0.096	131	0.304	default
M3	Y	19.552	93	0.304	default
M3	Y	0.096	64	0.304	default
M4	X	0.096	66	0.304	default
M4	X	0.096	131	0.304	default
M4	Y	19.552	93	0.304	default
M4	Y	0.096	64	0.304	default
M5	X	0.096	33	0.608	default
M5	X	0.096	66	0.608	default
M5	Y	19.552	47	0.608	default
M5	Y	0.096	32	0.608	default
M6	X	0.096	33	0.608	default
M6	X	0.096	66	0.608	default
M6	Y	19.552	47	0.608	default
M6	Y	0.096	32	0.608	default
M7	X	0.704	16	1.216	default
M7	X	0.704	33	1.216	default
M7	Y	20.160	23	1.216	default
M7	Y	0.704	16	1.216	default
M8	X	0.704	16	1.216	default
M8	X	0.704	33	1.216	default
M8	Y	20.160	23	1.216	default
M8	Y	0.704	16	1.216	default
M9	X	0.704	8	2.432	default
M9	X	0.704	17	2.432	default
M9	Y	20.160	12	2.432	default
M9	Y	0.704	8	2.432	default
MRDL	X	3.136	4	4.864	default

Date   : Tue Apr 15 13:55:52 2025
****

Layer	Direction	Start	Tracks	Pitch	Attr
M1	X	0.096	131	0.152	default
M1	X	0.096	262	0.152	default
M1	Y	19.400	187	0.152	default
M1	Y	0.096	127	0.152	default
M2	X	0.096	131	0.152	default
M2	X	0.096	262	0.152	default
M2	Y	19.400	187	0.152	default
M2	Y	0.096	127	0.152	default
M3	X	0.096	66	0.304	default
M3	X	0.096	131	0.304	default
M3	Y	19.552	93	0.304	default
M3	Y	0.096	64	0.304	default
M4	X	0.096	66	0.304	default
M4	X	0.096	131	0.304	default
M4	Y	19.552	93	0.304	default
M4	Y	0.096	64	0.304	default
M5	X	0.096	33	0.608	default
M5	X	0.096	66	0.608	default
M5	Y	19.552	47	0.608	default
M5	Y	0.096	32	0.608	default
M6	X	0.096	33	0.608	default
M6	X	0.096	66	0.608	default
M6	Y	19.552	47	0.608	default
M6	Y	0.096	32	0.608	default
M7	X	0.704	16	1.216	default
M7	X	0.704	33	1.216	default
M7	Y	20.160	23	1.216	default
M7	Y	0.704	16	1.216	default
M8	X	0.704	16	1.216	default
M8	X	0.704	33	1.216	default
M8	Y	20.160	23	1.216	default
M8	Y	0.704	16	1.216	default
M9	X	0.704	8	2.432	default
M9	X	0.704	17	2.432	default
M9	Y	20.160	12	2.432	default
M9	Y	0.704	8	2.432	default
MRDL	X	3.136	4	4.864	default
MRDL	X	3.136	8	4.864	default
MRDL	Y	22.592	6	4.864	default
MRDL	Y	3.136	4	4.864	default

1

(ix) CONCLUSIONS

The Digital Lock System was successfully implemented and verified using Verilog in Synopsys tools. The FSM design ensures precise matching of the key sequence to activate the lock. Simulation results confirmed that only the correct sequence triggers unlocking, proving the robustness and correctness of the design.

(x) REFERENCES

1. Synopsys VCS and Verdi User Manuals

2. Verilog HDL by Samir Palnitkar

3. Digital Design by M. Morris Mano

4. Classroom notes and lab material on FSM-based design